300MHz-to-450MHz Low-Power, Crystal-Based ASK Transmitter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +4.0V
All Other Pins to GND .....-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 8.9mW/°C above +70°C).....714mW

Operating Temperature Range .....-40°C to +125°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, output power is referenced to 50Ω, V_{DD} = 2.1V to 3.6V, V_{ENABLE} = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = 2.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE							
Supply Voltage	V_{DD}			2.1		3.6	V
Supply Current	I_{DD}	f_{RF} = 315MHz	V_{ENABLE} = V_{DD} (Note 2)		5.3	9.4	mA
			V_{ENABLE} = V_{DD}, V_{DATA} = V_{DD}		9.1	16.6	
			V_{ENABLE} = V_{DD}, V_{DATA} = 0V		1.5	2.3	
		f_{RF} = 433MHz	V_{ENABLE} = V_{DD} (Note 2)		5.7		
			V_{ENABLE} = V_{DD}, V_{DATA} = V_{DD}		9.6		
			V_{ENABLE} = V_{DD}, V_{DATA} = 0V		1.7	2.7	
Standby Current	I_{STDBY}	V_{ENABLE} < V_{IL}, T_A < +85°C (Note 3)			5	350	nA
		V_{ENABLE} < V_{IL} T_A < +125°C (Note 3)				1.7	µA
Frequency Range	f_{RF}	(Note 1)		300		450	MHz
Data Rate		(Note 3)		0		100	kbps
Modulation Depth		ON to OFF P_{OUT} ratio (Note 4)			90		dB
Output Power	P_{OUT}	T_A = +25°C, V_{DD} = 2.7V (Notes 5, 6)		7.3	10.3	12.8	dBm
		T_A = +125°C, V_{DD} = 2.1V (Notes 5, 6)		3.3	6.0		
		T_A = -40°C, V_{DD} = 3.6V (Notes 5, 6)			13.7	16.2	
Turn-On Time	t_{ON}	To f_{OFFSET} < 50kHz (Note 7)			220		µs
		To f_{OFFSET} < 5kHz (Note 7)			450		
Transmit Efficiency with CW		f_{RF} = 315MHz (Note 8)			43.6		%
		f_{RF} = 433MHz (Note 8)			41.3		
Transmit Efficiency at 50% Duty Cycle		f_{RF} = 315MHz (Note 9)			37.6		%
		f_{RF} = 433MHz (Note 9)			35.1		

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ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, output power is referenced to 50Ω, V_{DD} = 2.1V to 3.6V, V_{ENABLE} = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = 2.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PHASE-LOCKED LOOP PERFORMANCE							
VCO Gain					330		MHz/V
Phase Noise		f_{RF} = 315MHz	f_{OFFSET} = 100kHz		-84		dBc/Hz
			f_{OFFSET} = 1MHz		-91		
		f_{RF} = 433MHz	f_{OFFSET} = 100kHz		-82		
			f_{OFFSET} = 1MHz		-89		
Maximum Carrier Harmonics		f_{RF} = 315MHz			-50		dBc
		f_{RF} = 433MHz			-50		
Reference Spur		f_{RF} = 315MHz			-75		dBc
		f_{RF} = 433MHz			-81		
Loop Bandwidth					1.6		MHz
Crystal Frequency	f_{XTAL}				f_{RF} / 32		MHz
Oscillator Input Capacitance		From each XTAL pin to GND			6.2		pF
Frequency Pushing by V_{DD}					3		ppm/V
DIGITAL INPUTS							
Data Input High	V_{IH}			V_{DD} - 0.25			V
Data Input Low	V_{IL}					0.25	V
Maximum Input Current					2		nA
Pulldown Current					25		µA

Note 1: 100% tested at T_A = +25°C. Guaranteed by design and characterization over temperature.
Note 2: 50% duty cycle at 10kHz data.
Note 3: Guaranteed by design and characterization, not production tested.
Note 4: Generally limited by PC board layout.
Note 5: Output power can be adjusted with external resistor.
Note 6: Guaranteed by design and characterization at f_{RF} = 315MHz.
Note 7: V_{ENABLE} < V_{IL} to V_{ENABLE} > V_{IH}. f_{OFFSET} is defined as the frequency deviation from the desired carrier frequency.
Note 8: V_{ENABLE} > V_{IH}, V_{DATA} > V_{IH}, Efficiency = $P_{OUT}/(V_{DD} \times I_{DD})$.
Note 9: V_{ENABLE} > V_{IH}, DATA toggled from V_{IL} to V_{IH}, 10kHz, 50% duty cycle, Efficiency = $P_{OUT}/(V_{DD} \times I_{DD})$.

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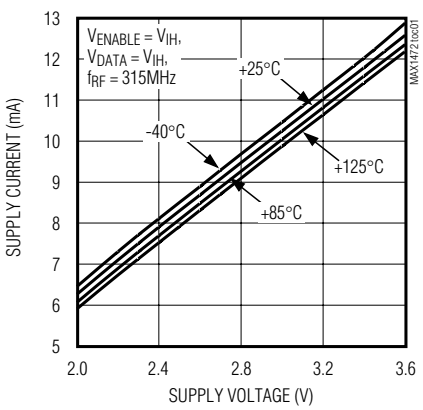
300MHz-to-450MHz Low-Power, Crystal-Based ASK Transmitter

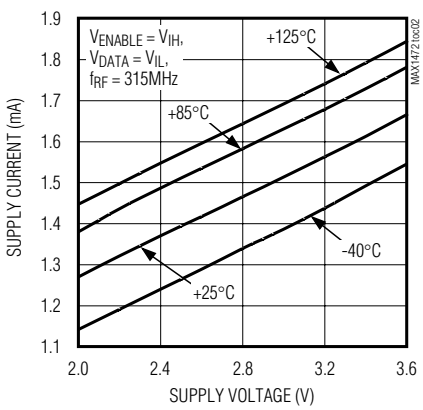
Typical Operating Characteristics

(*Typical Application Circuit*, V_{DD} = 2.7V, T_A = +25°C, unless otherwise noted.)

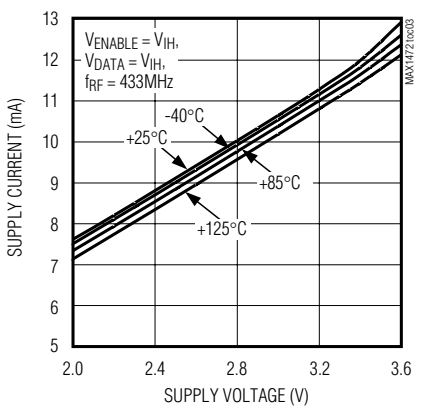
SUPPLY CURRENT vs. SUPPLY VOLTAGE



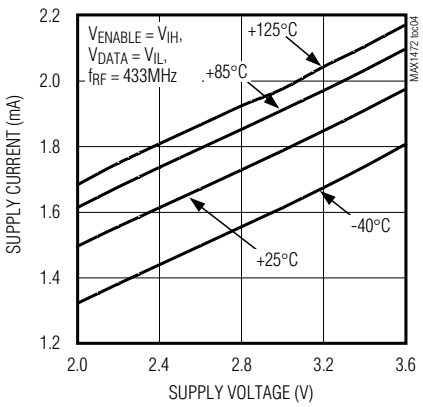
SUPPLY CURRENT vs. SUPPLY VOLTAGE



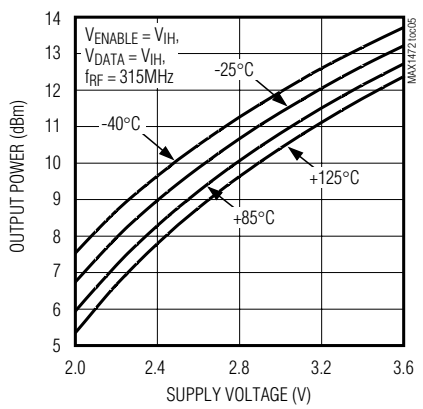
SUPPLY CURRENT vs. SUPPLY VOLTAGE



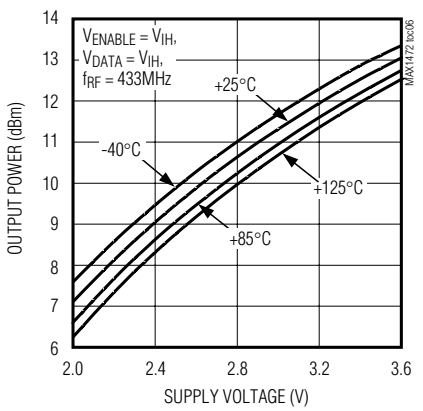
SUPPLY CURRENT vs. SUPPLY VOLTAGE



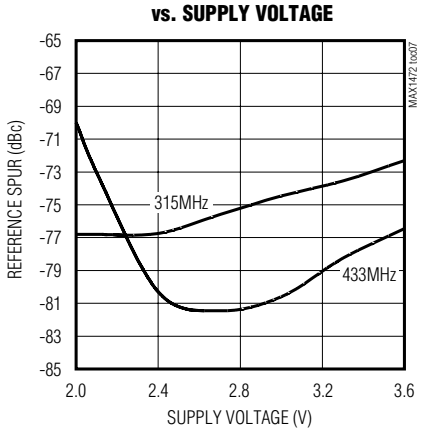
OUTPUT POWER vs. SUPPLY VOLTAGE



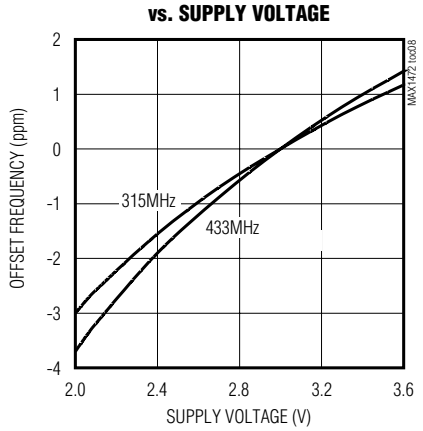
OUTPUT POWER vs. SUPPLY VOLTAGE



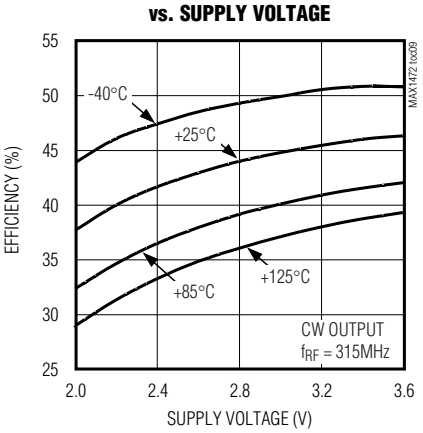
REFERENCE SPUR MAGNITUDE vs. SUPPLY VOLTAGE



FREQUENCY STABILITY vs. SUPPLY VOLTAGE



TRANSMIT POWER EFFICIENCY vs. SUPPLY VOLTAGE



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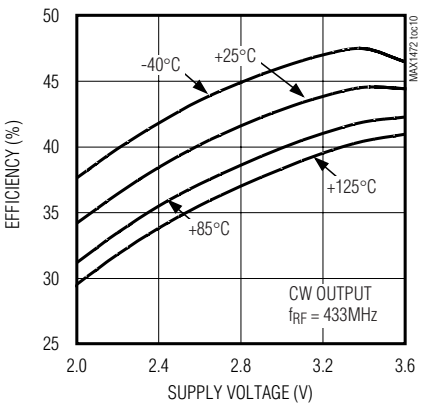
300MHz-to-450MHz Low-Power, Crystal-Based ASK Transmitter

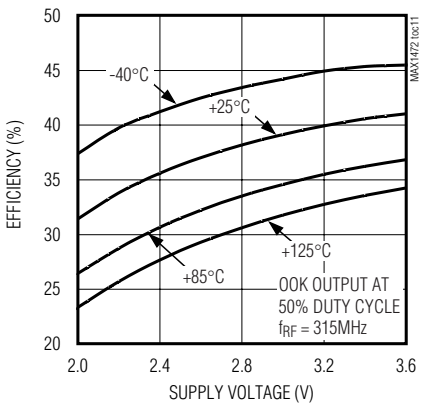
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{DD} = 2.7V, T_A = +25°C, unless otherwise noted.)

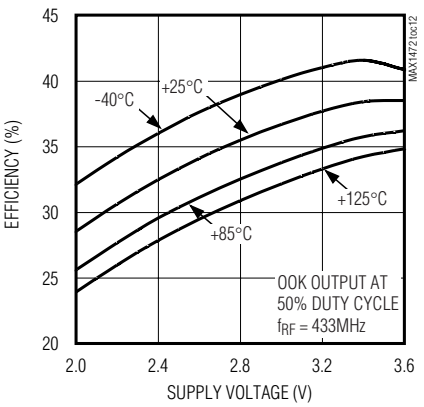
TRANSMIT POWER EFFICIENCY vs. SUPPLY VOLTAGE



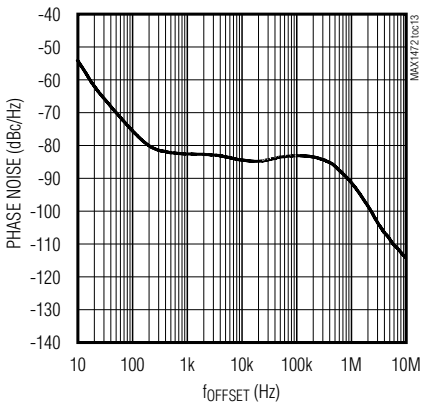
TRANSMIT POWER EFFICIENCY vs. SUPPLY VOLTAGE



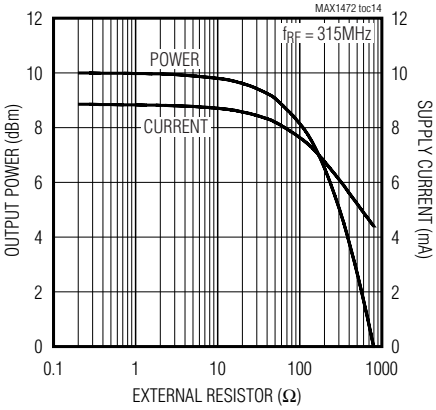
TRANSMIT POWER EFFICIENCY vs. SUPPLY VOLTAGE



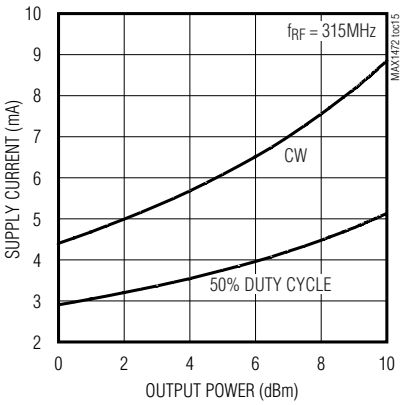
PHASE NOISE vs. OFFSET FREQUENCY



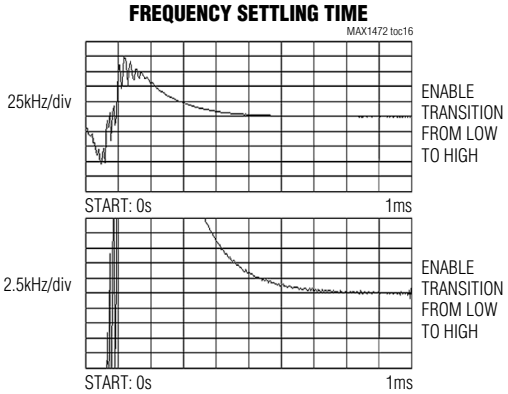
SUPPLY CURRENT AND OUTPUT POWER vs. EXTERNAL RESISTOR



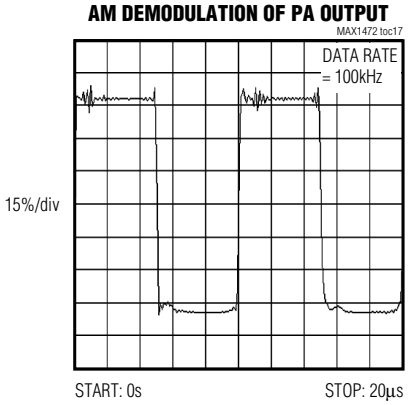
SUPPLY CURRENT vs. OUTPUT POWER



FREQUENCY SETTLING TIME



AM DEMODULATION OF PA OUTPUT



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Pin Description

PIN	NAME	FUNCTION
1	XTAL1	1st Crystal Input. $f_{RF} = 32 \times f_{XTAL}$.
2	GND	Ground. Connect to system ground.
3	PAGND	Ground for the Power Amplifier (PA). Connect to system ground.
4	PAOUT	Power-Amplifier Output. This output requires a pullup inductor to the supply voltage, which may be part of the output-matching network to a 50Ω antenna.
5	ENABLE	Standby/Power-Up Input. A logic low on ENABLE places the device in standby mode.
6	DATA	OOK Data Input. Power amplifier is ON when DATA is high.
7	V_{DD}	Supply Voltage. Bypass to GND with capacitor as close to the pin as possible.
8	XTAL2	2nd Crystal Input. $f_{RF} = 32 \times f_{XTAL}$.

Detailed Description

The MAX1472 is a highly integrated OOK/ASK transmitter operating over the 300MHz to 450MHz frequency range. The IC includes a complete PLL and a highly efficient PA. The device can also be easily placed into a 5nA low-power shutdown mode.

Shutdown Mode

The ENABLE pin is internally pulled down with a 15µA current source. If the pin is left unconnected or pulled low, the MAX1472 goes into shutdown mode, where the supply current drops to less than 5nA. When ENABLE is high, the IC is enabled and is ready for transmission after 220µs (frequency settles to within 50kHz).

The 220µs turn-on time of the MAX1472 is mostly dominated by the crystal oscillator startup time. Once the oscillator is running, the 1.6MHz PLL loop bandwidth allows fast-frequency recovery during power-amplifier toggling.

Phase-Locked Loop

The PLL block contains a phase detector, charge pump, integrated loop filter, VCO, 32X clock divider, and crystal oscillator. This PLL requires no external components, other than a crystal. The relationship between the carrier and crystal frequency is given by:

$$f_{XTAL} = f_{RF} / 32$$

The lock-detect circuit prevents the PA from transmitting until the PLL is locked. In addition, the device shuts down the PA if the reference frequency is lost.

Power Amplifier (PA)

The PA of the MAX1472 is a high-efficiency, open-drain, switch-mode amplifier. With proper output matching network, the PA can drive a wide range of impedances, including the small-loop PC board trace antenna and any 50Ω antenna. The output-matching network for a 50Ω antenna is shown in the *Typical Application Circuit*. The output-matching network suppresses the carrier harmonics and transforms the antenna impedance to an optimal impedance at PAOUT (pin 4), which is between 100Ω and 150Ω for a 2.7V supply.

When the output matching network is properly tuned, the PA transmits power with high efficiency. The *Typical Application Circuit* delivers 10.3dBm at 2.7V supply with 9.1mA of supply current. Thus, the overall efficiency is 44%. The efficiency of the PA itself is more than 52%.

Applications Information

Output Power Adjustment

It is possible to adjust the output power down to -10dBm with the addition of a resistor. The addition of the power-adjust resistor also reduces power consumption. See the Supply Current and Output Power vs. External Resistor and Supply Current vs. Output Power graphs in the *Typical Operating Characteristics* section. It is imperative to add both a low-frequency and a high-frequency decoupling capacitor as shown in the *Typical Application Circuit*.

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Crystal Oscillator

The crystal oscillator in the MAX1472 is designed to present a capacitance of approximately 3.1pF between the XTAL1 and XTAL2 pins. If a crystal designed to oscillate with a different load capacitance is used, the crystal is pulled away from its intended operating frequency, thus introducing an error in the reference frequency. Crystals designed to operate with higher differential load capacitance always pull the reference frequency higher. For example, a 9.84375MHz crystal designed to operate with a 10pF load capacitance oscillates at 9.84688MHz with the MAX1472, causing the transmitter to be transmitting at 315.1MHz rather than 315.0MHz, an error of about 100kHz, or 320ppm.

In actuality, the oscillator pulls every crystal. The crystal's natural frequency is really below its specified frequency, but when loaded with the specified load capacitance, the crystal is pulled and oscillates at its specified frequency. This pulling is already accounted for in the specification of the load capacitance. Additional pulling can be calculated if the electrical parameters of the crystal are known. The frequency pulling is given by:

$$f_p = \frac{C_m}{2}\left(\frac{1}{C_{case}+C_{load}} - \frac{1}{C_{case}+C_{spec}}\right) \times 10^6$$

where:

f_p is the amount the crystal frequency is pulled in ppm.

C_m is the motional capacitance of the crystal.

C_{case} is the case capacitance.

C_{spec} is the specified load capacitance.

C_{load} is the actual load capacitance.

When the crystal is loaded as specified, i.e., $C_{load} = C_{spec}$, the frequency pulling equals zero.

Output Matching to 50Ω

When matched to a 50Ω system, the MAX1472 PA is capable of delivering more than +10dBm of output power at V_{DD} = 2.7V. The output of the PA is an open-drain transistor that requires external impedance matching and pullup inductance for proper biasing. The pullup inductance from PA to V_{DD} serves three main purposes: It resonates the capacitance of the PA output, provides biasing for the PA, and becomes a high-frequency choke to reduce the RF energy coupling into V_{DD}. The recommended output-matching network topology is shown in the *Typical Application Circuit*. The matching network transforms the 50Ω load to a higher impedance at the output of the PA in addition to forming a bandpass filter that provides attenuation for the higher order harmonics.

Output Matching to PC Board Loop Antenna

In most applications, the MAX1472 PA output has to be impedance matched to a small-loop antenna. The antenna is usually fabricated out of a copper trace on a PC board in a rectangular, circular, or square pattern. The antenna has an impedance that consists of a lossy component and a radiative component. To achieve high radiating efficiency, the radiative component should be as high as possible, while minimizing the lossy component. In addition, the loop antenna has an inherent loop inductance associated with it (assuming the antenna is terminated to ground). For example, in a typical application, the radiative impedance is less than 0.5Ω, the lossy impedance is less than 0.7Ω, and the inductance is approximately 50nH to 100nH.

The objective of the matching network is to match the PA output to the small loop antenna. The matching components thus transform the low radiative and resistive parts of the antenna into the much higher value of the PA output, which gives higher efficiency. The low radiative and lossy components of the small loop antenna result in a higher Q matching network than the 50Ω network; thus, the harmonics are lower.

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Layout Considerations

A properly designed PC board is an essential part of any RF/microwave circuit. On the PA output, use controlled-impedance lines and keep them as short as possible to minimize losses and radiation. At high frequencies, trace lengths that are on the order of λ/10 or longer can act as antennas.

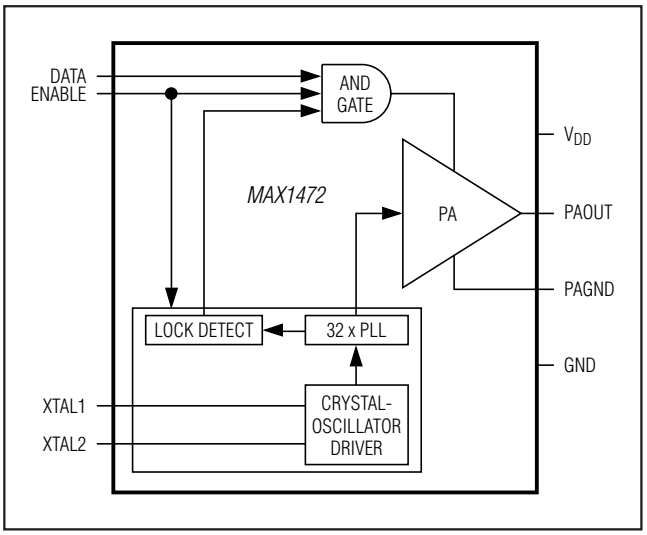
Keeping the traces short also reduces parasitic inductance. Generally, 1in of PC board trace adds about 20nH of parasitic inductance. The parasitic inductance can have a dramatic effect on the effective inductance. For example, a 0.5in trace connecting a 100nH inductor adds an extra 10nH of inductance, or 10%.

To reduce the parasitic inductance, use wider traces and a solid ground or power plane below the signal traces. Using a solid ground plane can reduce the parasitic inductance from approximately 20nH/in to 7nH/in. Also, use low-inductance connections to ground on all GND pins, and place decoupling capacitors close to all V_{DD} connections.

Chip Information

PROCESS: CMOS

Functional Diagram



Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SOT23	K8SN+1	21-0078	90-0176

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1	4/05	—	—
2	6/09	Updated EC table Max supply currents, added lead-free note, and corrected *Electrical Characteristics* notes	1, 2, 3, 6, 8
3	10/10	Removed *Maximum Crystal Inductance* spec from *Electrical Characteristics* table	3
4	6/12	Updated *Electrical Characteristics*, updated Power Amplifier (PA) section	3, 6

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