Absolute Maximum Ratings

All voltages referenced to GND.
V_{CC}, TDP, TDM, CB0, CB1, DP, DM, $\overline{CEN}$, CEN -0.3V to +6.0V
Continuous Current into Any Terminal.....±30mA
Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 11.9mW/°C above +70°C).....953.5mW

Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....84°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....37°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{CC} = 3.0V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5.0V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Range	V_{CC}	V_{CB0} > V_{IH} (Note 6)	3.0		5.5	V
		V_{CB0} = 0V (Note 3)	4.75		5.25	
Supply Current	I_{CC}	V_{CB0} = V_{CB1} = V_{CC} = 5.25V, CM mode		50	100	µA
		V_{CB0} = V_{CC} = 5.25V, V_{CB1} = 0V, PM mode		4	20	
		V_{CB0} = 0V, V_{CB1} = V_{CC} = 5.25V, FM mode		10	50	
		V_{CB0} = 0V, V_{CB1} = V_{CC} = 5.25V (MAX14618)		130	200	
		V_{CB0} = V_{CB1} = 0V, AM mode		130	200	
ANALOG SWITCH						
Analog-Signal Range	V_{DP}, V_{DM}		0		V_{CC}	V
On-Resistance TDP/TDM Switch	R_{ON}	V_{TDP} = V_{TDM} = 0V to V_{CC}, I_{TDP} = I_{TDM} = 10mA		3.5	6.5	Ω
On-Resistance Match Between Channels TDP/TDM Switch	ΔR_{ON}	V_{CC} = 5.0V, V_{DP} = V_{DM} = 400mV, I_{DP} = I_{DM} = 10mA		0.1		Ω
On-Resistance Flatness TDP/TDM Switch	R_{FLAT}	V_{CC} = 5.0V, V_{DP} = V_{DM} = 0 to V_{CC}, I_{DP} = I_{DM} = 10mA		0.1		Ω
On-Resistance of DP/DM Short	R_{SHORT}	V_{CB0} = 0V, V_{CB1} = V_{CC}, V_{DP} = 1V, R_{DM} = 20kΩ		70	120	Ω
Off-Leakage Current	I_{TDPOFF}, I_{TDMOFF}	V_{CC} = 3.6V, V_{DP} = V_{DM} = 0.3V to 3.3V, V_{TDP} = V_{TDM} = 3.3V to 0.3V	-250		+250	nA
On-Leakage Current	I_{DPON}, I_{DMON}	V_{CC} = 3.6V, V_{DP} = V_{DM} = 3.3V to 0.3V, $V_{CB\_}$ = V_{CC}	-250		+250	nA
DYNAMIC PERFORMANCE (Note 4)						
Turn-On Time	t_{ON}	V_{TDP} or V_{TDM} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IH} = V_{CC}, V_{IL} = 0V, Figure 1		300	800	µs

Electrical Characteristics (continued)

(V_{CC} = 3.0V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5.0V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Turn-Off Time	t_{OFF}	V_{TDP} or V_{TDM} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IH} = V_{CC}, V_{IL} = 0V, Figure 1 (Note 5)		1	5	µs
TDP, TDM Switch Propagation Delay	t_{PLH}, t_{PHL}	R_L = R_S = 50Ω		60		ps
Output Skew	t_{SK}	Skew between DP and DM when connected to TDP and TDM, R_L = R_S = 50Ω, Figure 2		40		ps
TDP, TDM Off-Capacitance	C_{OFF}	f_{SW} = 1MHz, V_{BIAS} = 0V, V_{IN} = 500mV_{P-P}		2.0		pF
DP, DM On-Capacitance (Connected to TDP, TDM)	C_{ON}	f_{SW} = 240MHz, V_{BIAS} = 0V, V_{IN} = 500mV_{P-P}		4.0	5.5	pF
-3dB Bandwidth	BW	R_L = R_S = 50Ω		1000		MHz
Off-Isolation	V_{ISO}	V_{TDP} or V_{DP} = 0dBm, R_L = R_S = 50Ω, f_{SW} = 250MHz, Figure 3		-20		dB
Crosstalk	V_{CT}	V_{TDP} or V_{DP} = 0dBm, R_L = R_S = 50Ω, f_{SW} = 250MHz, Figure 3		-25		dB
DPC INTERNAL RESISTORS						
DP/DM Short Pulldown	R_{PD}		320	500	730	kΩ
RP1/RP2 Ratio	RT_{RP}		1.4	1.5	1.55	—
RP1 + RP2 Resistance	R_{RP}		85	125	170	kΩ
RM1/RM2 Ratio	RT_{RM}		0.85	0.86	0.87	—
RM1 + RM2 Resistance	R_{RM}		60	93	125	kΩ
DPC COMPARATORS (Note 4)						
DM1 Comparator Threshold	V_{DM1F}	DM falling	40	41	42	%V_{CC}
DM1 Comparator Hysteresis				1		%
DM2 Comparator Threshold	V_{DM2F}	DM falling	6.31	7	7.6	%V_{CC}
DM2 Comparator Hysteresis				1		%
DP Comparator Threshold	V_{DPR}	DP rising	45	46	47	%V_{CC}
DP Comparator Hysteresis				1		%
CDP INTERNAL RESISTORS						
DP Pulldown Resistor	R_{DP_DWN}			14.25	24.8	kΩ
DM Pulldown Resistor	R_{DM_DWN}			14.25	24.8	kΩ
CDP LOW-SPEED COMPARATORS						
V_{DM_SRC} Voltage	V_{DM_SRC}	I_{LOAD} = 0 to 200µA	0.5		0.7	V
V_{DAT_REF} Voltage	V_{DAT_REF}		0.25		0.4	V
V_{LGC} Voltage	V_{LGC}		0.8		2.0	V
I_{DP_SINK} Current	I_{DP_SINK}	V_{DP} = 0.15V to 3.6V	50		150	µA

Electrical Characteristics (continued)

(V_{CC} = 3.0V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5.0V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS (CB0, CB1)						
CB0/CB1 Input Logic-High	V_{IH}		1.4			V
CB0/CB1 Input Logic-Low	V_{IL}				0.4	V
CB0/CB1 Input Leakage Current	I_{IN}	V_{CC} = 5.5V, 0V ≤ V_{IN} ≤ V_{IL} or V_{IH} ≤ V_{IN} ≤ V_{CC}	-1		+1	µA
$\overline{CEN}$/CEN OUTPUTS						
V_{BUS} Toggle Time	t_{VBT}	CB0 = V_{IL} to V_{IH} or V_{IH} to V_{IL}	1	2	3	s
$\overline{CEN}$ Output Logic-High Voltage		CB0 = V_{IL} to V_{IH}, I_{SOURCE} = 2mA	V_{CC} - 0.4			V
$\overline{CEN}$ Output Leakage Current		V_{CC} = 5.5V, $V_{\overline{CEN}}$ = 0V, $\overline{CEN}$ deasserted			1	µA
CEN Output Logic-Low Voltage		CB0 = V_{IL} to V_{IH}, I_{SINK} = 2mA			0.4	V
CEN Output Leakage Current		V_{CC} = V_{CEN} = 5.5V, CEN deasserted			1	µA
ESD PROTECTION						
ESD Protection Level	V_{ESD}	HBM		±2		kV

Note 2: All units are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 3: The device is operational from 3.0V to 5.5V. However, to have the valid Apple resistor-divider network, the V_{CC} supply must stay within 4.75V to 5.25V.
Note 4: Guaranteed by design.
Note 5: Does not include the delay by the state machine.
Note 6: For BC1.2 CDP compliance, $V_{CC,MIN}$ = 4.75V, $V_{CC,MAX}$ = 5.25V.

Test Circuits/Timing Diagrams

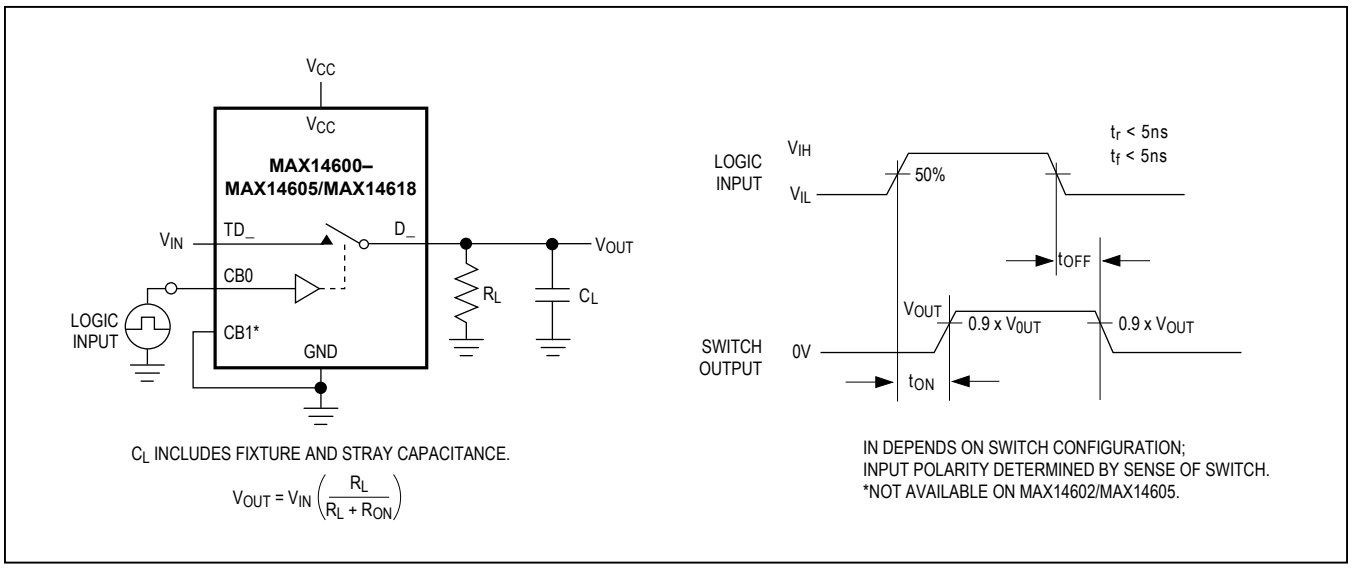


Figure 1. Switching Time

Test Circuits/Timing Diagrams (continued)

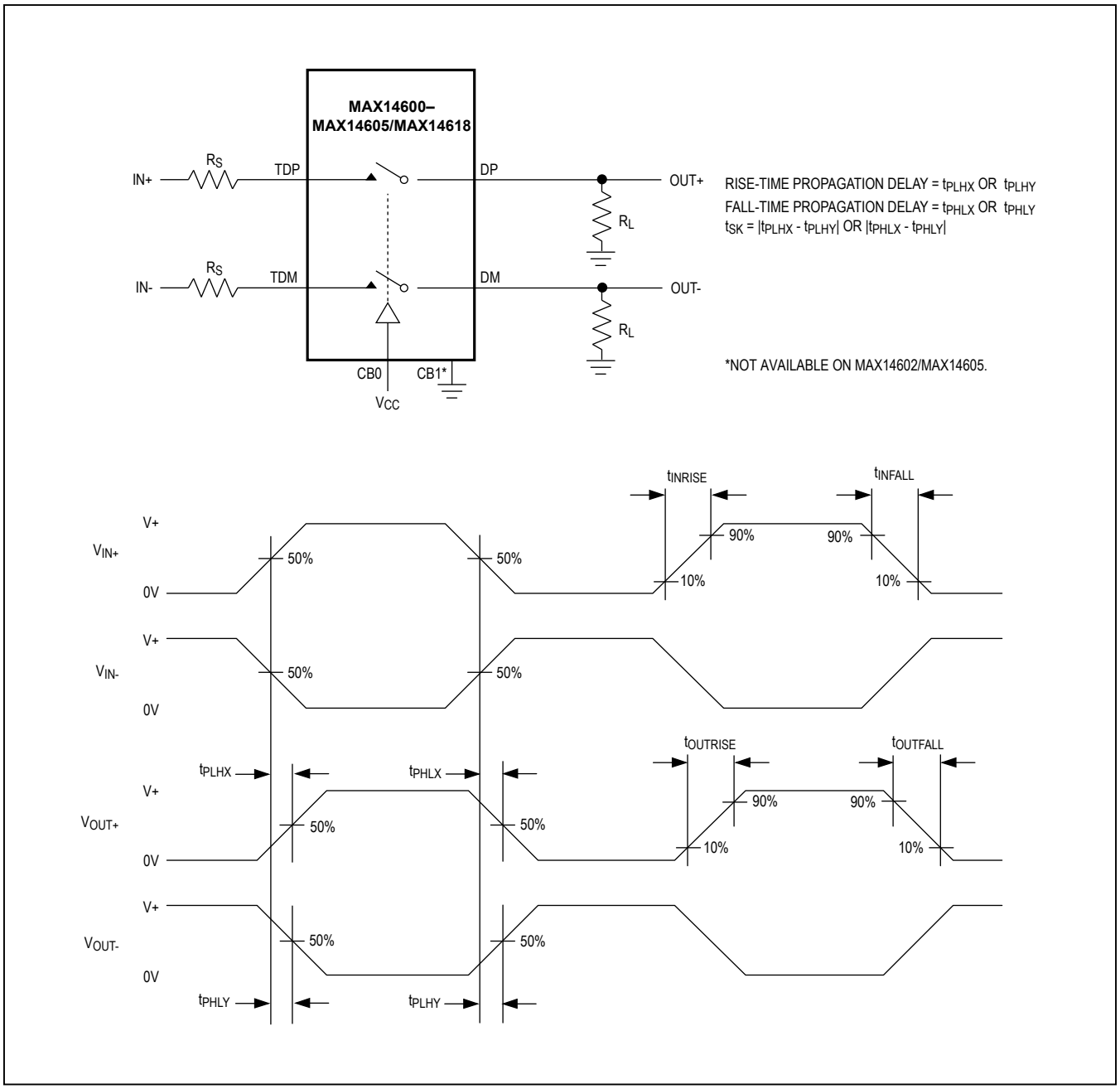


Figure 2. Output Signal Skew

Test Circuits/Timing Diagrams (continued)

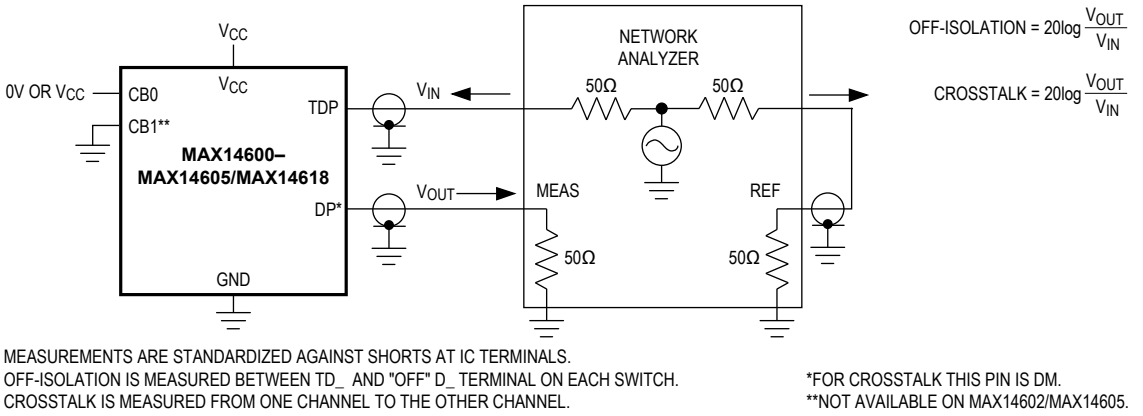
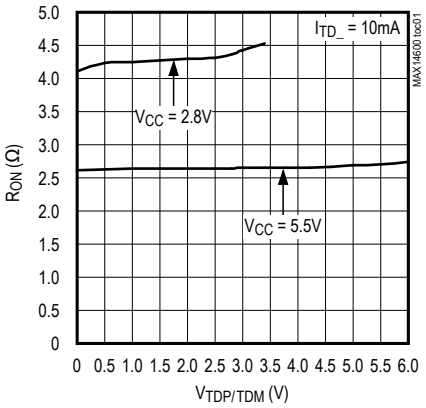


Figure 3. Off-Isolation and Crosstalk

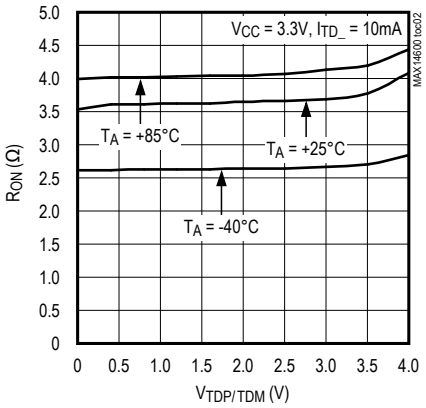
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

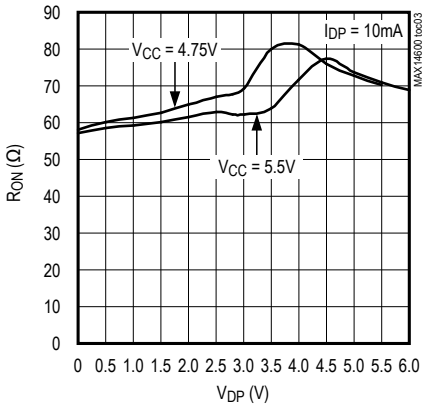
TDP/TDM ON-RESISTANCE vs. SUPPLY VOLTAGE



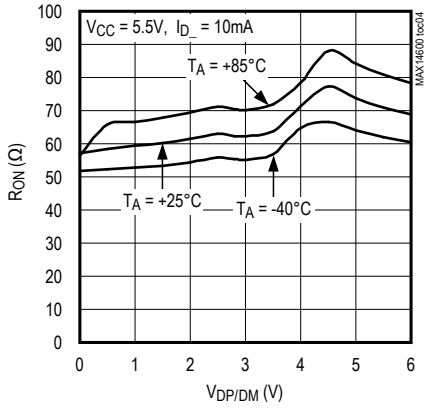
ON-RESISTANCE vs. VTDP/TDM



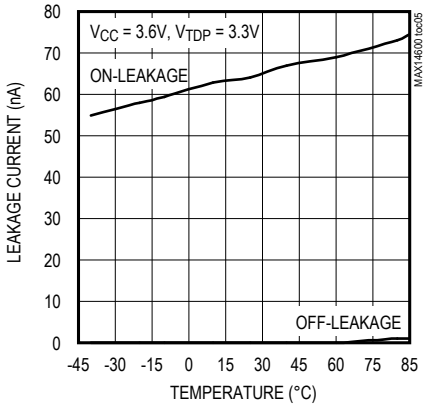
DP/DM SHORT ON-RESISTANCE vs. VDP



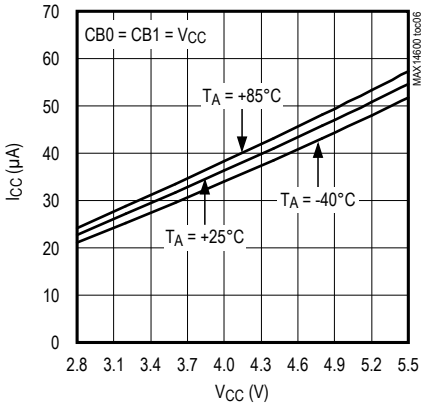
DP/DM SHORT ON-RESISTANCE vs. TEMPERATURE



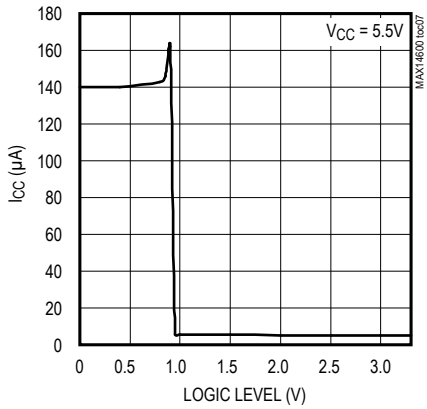
TDP/DP LEAKAGE CURRENT vs. TEMPERATURE



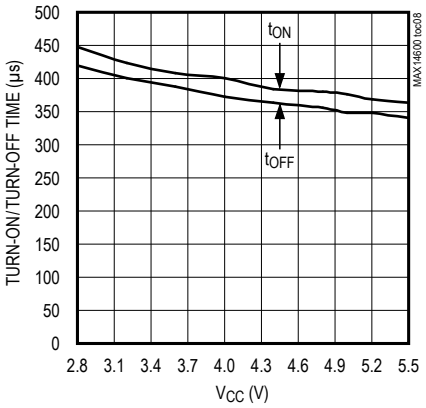
SUPPLY CURRENT vs. SUPPLY VOLTAGE



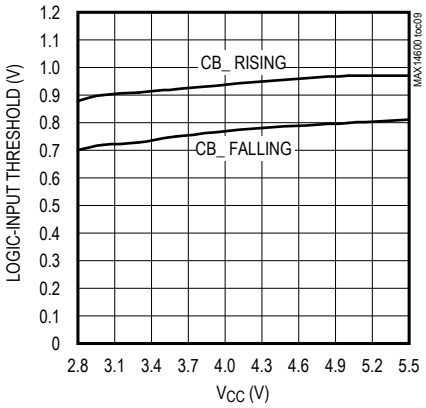
SUPPLY CURRENT vs. LOGIC LEVEL



TURN-ON/TURN-OFF TIME vs. SUPPLY VOLTAGE



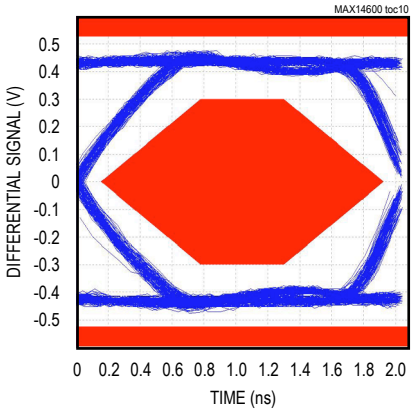
LOGIC-INPUT THRESHOLD vs. SUPPLY VOLTAGE



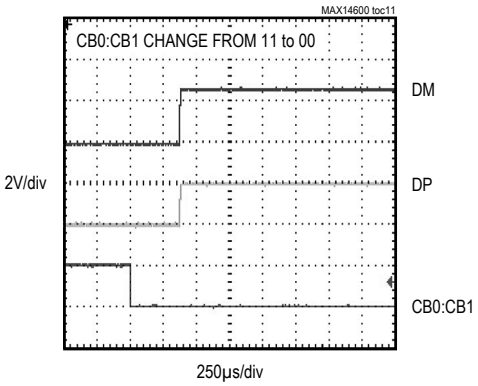
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

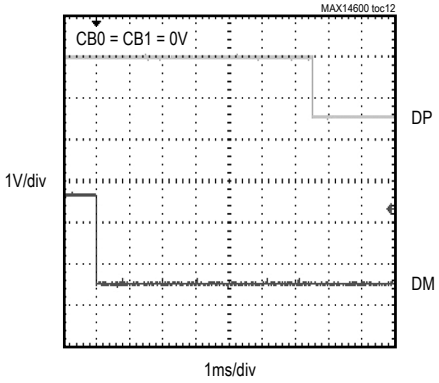
EYE DIAGRAM



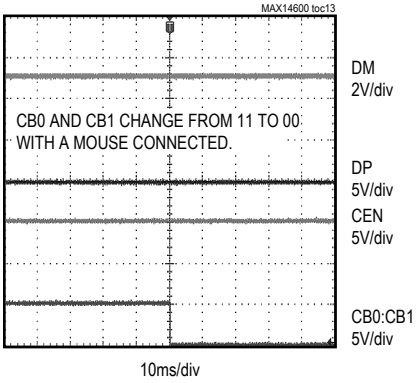
AUTODETECTION MODE



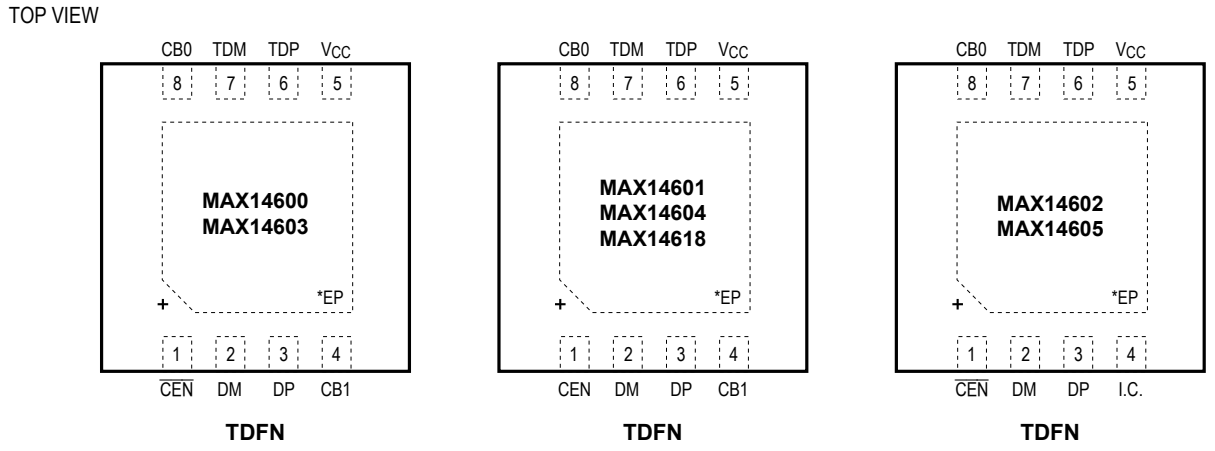
AUTODETECTION MODE



REMOTE WAKE-UP SUPPORT



Pin Configurations

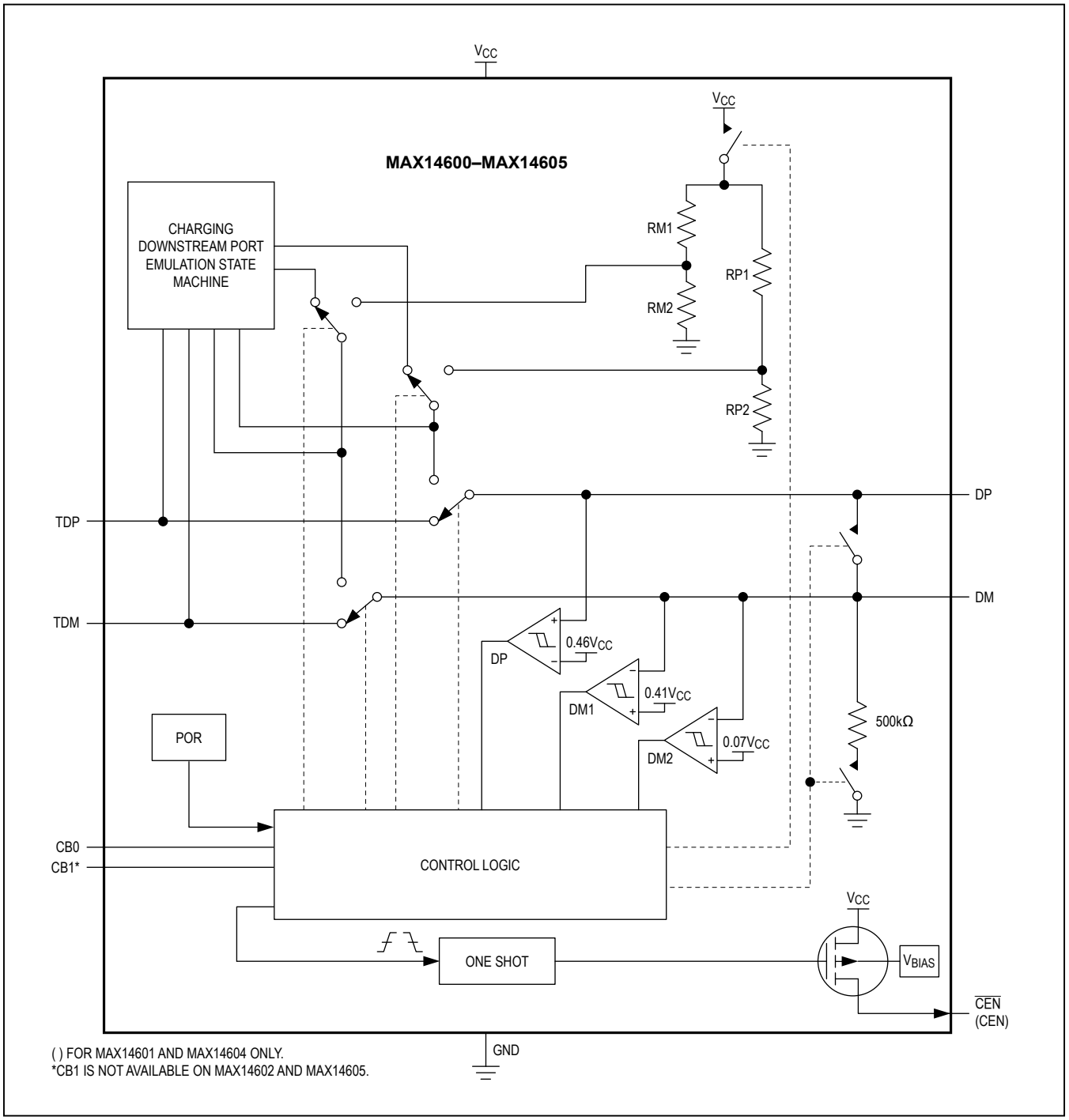


*CONNECT EP TO GND.

Pin Descriptions

PIN			NAME	FUNCTION
MAX14600/ MAX14603	MAX14601/ MAX14604/ MAX14618	MAX14602/ MAX14605		
1	—	1	$\overline{CEN}$	Active-Low pMOSFET Open-Drain Output, Current-Limit Switch (CLS) Control Output. When CB0 changes from V_{IL} to V_{IH} or V_{IH} to V_{IL}, $\overline{CEN}$ is high.
—	1	—	CEN	nMOSFET Open-Drain Output, CLS Control Output. When CB0 changes from V_{IL} to V_{IH} or from V_{IH} to V_{IL}, CEN is low.
2	2	2	DM	USB Connector D- Connection
3	3	3	DP	USB Connector D+ Connection
4	4	—	CB1	Switch Control Bit. See Table 1.
—	—	4	I.C.	Internally Connected. Do not externally connect.
5	5	5	V_{CC}	Power Supply. Connect a 0.1µF capacitor between V_{CC} and ground as close as possible to the device.
6	6	6	TDP	Host USB Transceiver D+ Connection
7	7	7	TDM	Host USB Transceiver D- Connection
8	8	8	CB0	Switch Control Bit. See Table 1.
—	—	—	EP	Exposed Pad. Connect EP to ground. For enhanced thermal dissipation, connect EP to a copper area as large as possible.

Functional Diagram



Detailed Description

The MAX14600–MAX14605 and MAX14618 adapter emulator family has Hi-Speed USB analog switches that support USB hosts to identify the USB port as a charger port when the USB host is in a low-power mode and cannot enumerate USB devices. These Hi-Speed USB switches feature low 4pF (typ) on-capacitance and low 3.5Ω (typ) on-resistance. DP and DM can handle signals between 0V and 6V with any supply voltage.

Resistor-Dividers

The MAX14600–MAX14605/MAX14618 family features an internal resistor-divider for biasing data lines to provide support for Apple-compliant devices. When the MAX14600–MAX14605/MAX14618 family is not operated with the resistor-divider, the device disconnects the resistor-dividers from the supply voltage to minimize supply current requirements. The resistor-dividers are not connected in pass-through mode.

Switch Control

The MAX14600–MAX14605/MAX14618 family features dual digital inputs, CB0 and CB1, for mode selection.

For the MAX14600/MAX14601/MAX14603/MAX14604, connect CB0 and CB1 to a logic-level low voltage for autodetection charger mode (AM). Change only CB1 to a logic-level high for forced dedicated charger mode (FM). Change only CB1 to a logic-level low for normal high-speed pass-through mode (PM). Connect CB0 and CB1 to a logic-level high for high-speed pass-through mode with CDP emulation (CM). See Table 1.

For the MAX14618, connect CB0 to a logic-level low voltage for autodetection charger mode (AM). Change CB0 to a logic-level high voltage and CB1 to a logic-level low voltage to place the MAX14618 in normal high-speed pass-through charger mode (PM). Connect CB0 and CB1 to a logic-level high for high-speed pass-through mode with CDP emuation (CM). See Table 2.

Table 1. Digital Input State for MAX14600/MAX14601/MAX14603/MAX14604

CB0	CB1	CHARGER/USB	MODE	STATUS
0	0	Charger	AM	Autodetection Charger Mode
0	1	Charger	FM	Force Dedicated Charger Mode: DP/DM shorted.
1	0	USB	PM	USB Pass-Through Mode: DP/DM connected to TDP/TDM.
1	1	USB	CM	USB Pass-Through Mode with CDP Emulation: Auto connects DP/DM to TDP/TDM depending on CDP status.

Table 2. Digital Input State for MAX14618

CB0	CB1	CHARGER/USB	MODE	STATUS
0	X	Charger	AM	Auto detection Charger Mode with Remote Wake-Up
1	0	USB	PM	USB Pass-Through Mode: DP/DM connected to TDP/TDM.
1	1	USB	CM	USB Pass-Through Mode with CDP Emulation: Auto connects DP/DM to TDP/TDM depending on CDP status.

Table 3. Digital Input State for MAX14602/MAX14605

CB0	CHARGER/USB	MODE	STATUS
0	Charger	AM	Autodetection Charger Mode
1	USB	CM	USB Pass-Through Mode with CDP Emulation: Auto connects DP/DM to TDP/TDM depending on CDP status.

In CDP emulation mode, the peripheral device with CDP detection capability draws the charging current up to 1.5A immediately without USB enumeration. The MAX14602/ MAX14605 have CB0 digital input control only (Table 3). The MAX14602/MAX14605 are pin-to-pin compatible with the MAX14566E, and CB0 and CB1 are connected together internally, which makes these devices easy upgrades for CDP emulation.

Autodetection

The MAX14600–MAX14605/MAX14618 family features autodetection charger mode for dedicated chargers and USB masters. Both CB0 and CB1 must be set low to activate autodetection charger mode.

In autodetection charger mode, the device monitors the voltages at DM and DP to determine the type of device attached. If the voltage at DM is 2.05V (typ) or higher and the voltage at DP is 2.3V (typ) or lower, the voltage stays unchanged. If the voltage at DM is forced below the 2.05V (typ) threshold, the internal switch disconnects DM and DP from the resistor-divider and DP and DM are shorted together for dedicated charging mode.

Also, if the voltage at DP is forced higher than the 2.3V (typ) threshold, the internal switch disconnects DM and DP from the resistor-divider and DP and DM are shorted together for dedicated charging mode.

Once the charging voltage is removed, the short between DP and DM is disconnected for normal operation.

Auto-Peripheral Reset

The MAX14600–MAX14605/MAX14618 family features an auto current-limit switch-control output. This feature resets the peripheral connected to V_{BUS} in the event the USB host switches to or from standby mode. $\overline{CEN}$ or CEN provide a 2s (typ) pulse on the rising or falling-edge of CB0 (Figure 4 and Figure 5.) With the MAX14603/ MAX14604/MAX14605/MAX14618, the auto-peripheral reset is suspended in case of CB0 and CB1 transition from 11 to 00 as long as the peripheral remains connected. See the *Remote Wake-Up Support* section for more information.

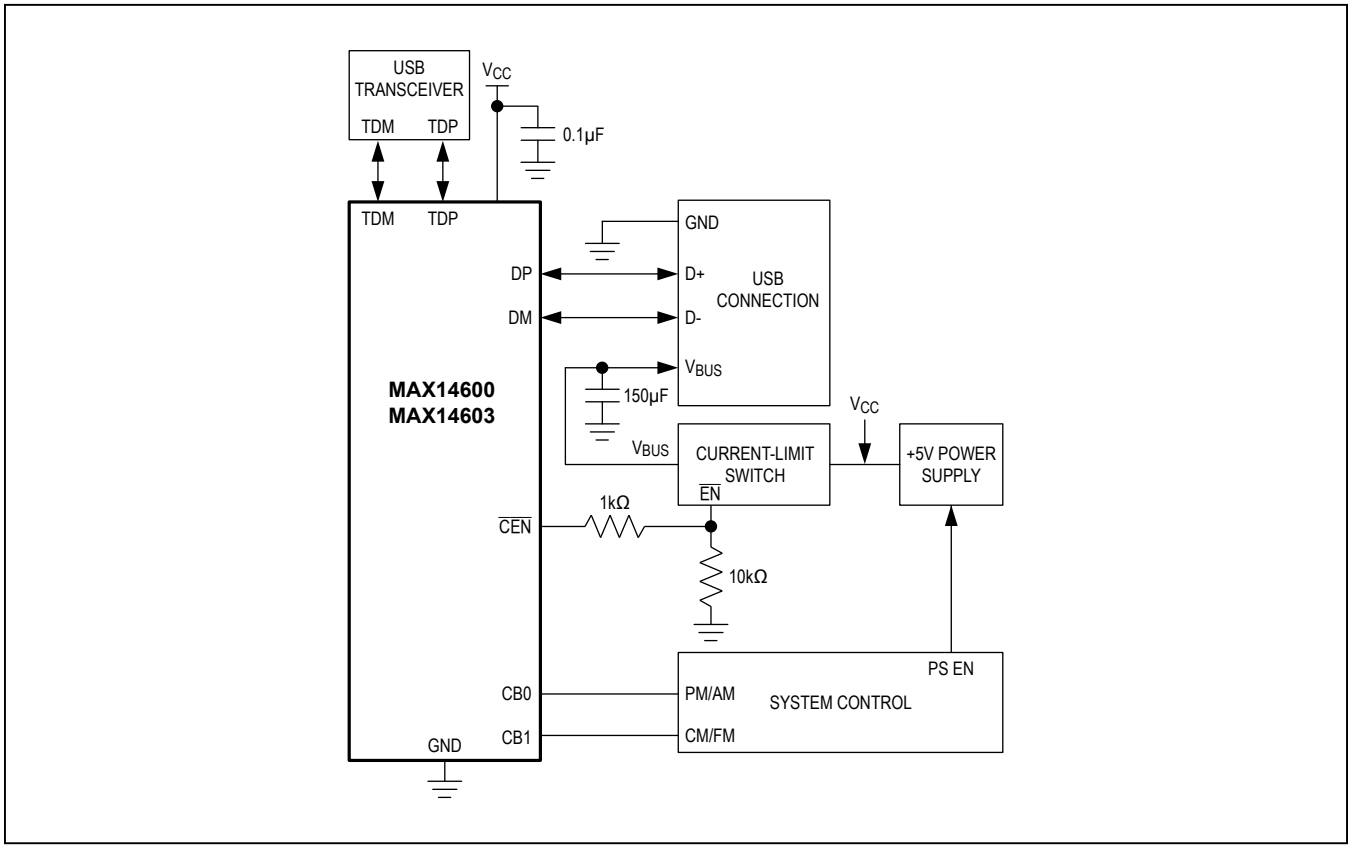


Figure 4. MAX14600/MAX14603 Peripheral Reset Applications Diagram

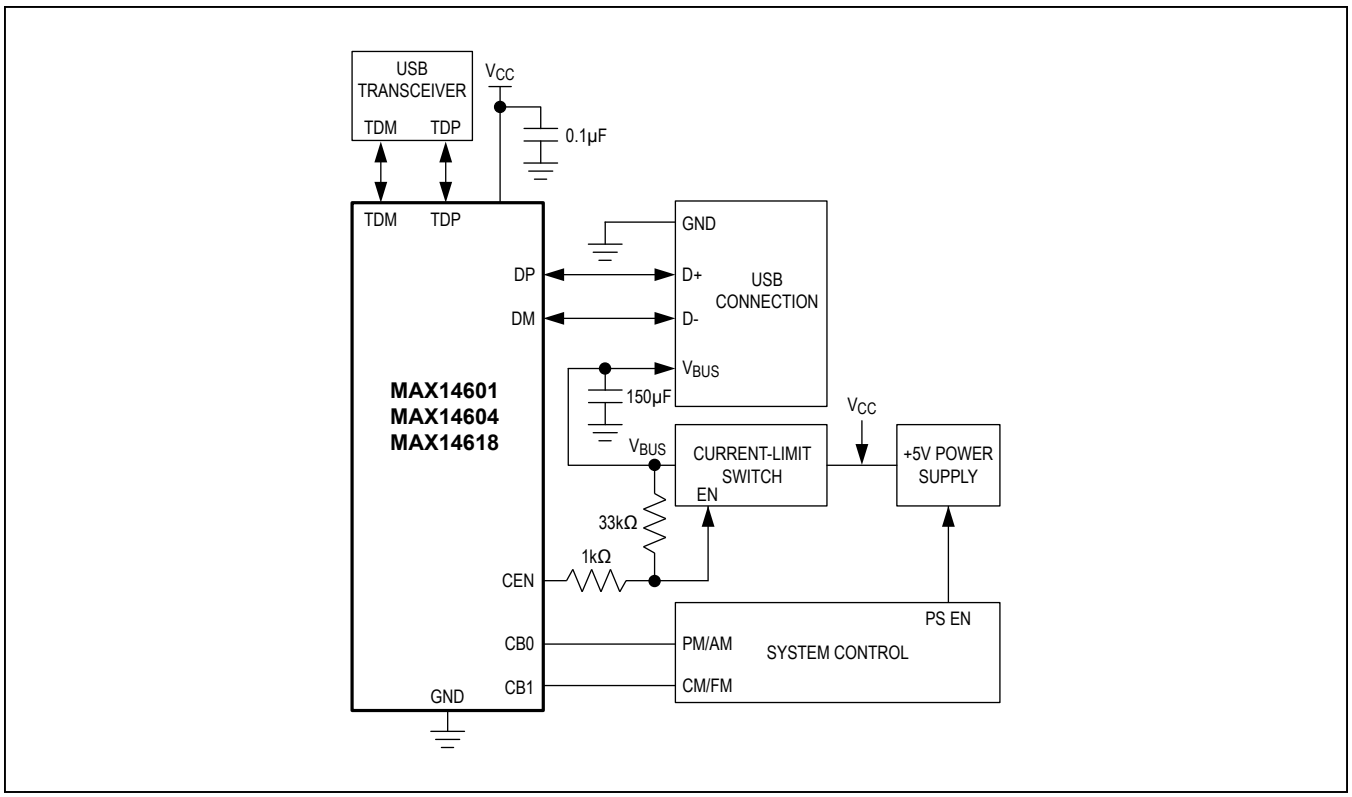


Figure 5. MAX14601/MAX14604/MAX14618 Peripheral Reset Applications Diagram

Table 4. Different Power States

STATE	DESCRIPTION
S0	System on.
S1	Power to the CPU(s) and RAM is maintained; devices that do not indicate they must remain on can be powered down.
S2	CPU is powered off.
S3	Standby (suspend to RAM). System memory context is maintained, and all other system context is lost.
S4	Hibernate. Platform context is maintained.
S5	Soft off.

USB Pass-Through Mode with CDP Emulation

The MAX14600–MAX14605/MAX14618 family features a pass-through mode with CDP emulation. This is to support the higher charging current capability during the pass-through mode in normal USB operation (S0 state). The peripheral device equipped with CDP detection capability could draw a charging current as defined in USB Battery Charger Specification 1.2 when the charging host supports the CDP mode. This is a useful feature since most host USB transceivers do not have the CDP function. Table 4 shows the different power states of S0–S5.

Bus Voltage Discharge

The MAX14601/MAX14604/MAX14618 auto current-limit switch-control output can be used to discharge the V_{BUS} during V_{BUS} reset. When the system controls the current limit switch for V_{BUS} toggle, the output capacitor can be discharged slowly depending upon the load. If fast discharge of the V_{BUS} is desired, the CEN output can be used to discharge the V_{BUS} (Figure 6.)

Data Contact Detect Support

The MAX14600–MAX14605/MAX14618 family support USB devices that require detecting the USB data lines prior to charging. When a USB Revision 1.2-compliant device is attached, the USB data lines DP and DM are shorted together. The short remains until it is detected by the USB device. This feature guarantees appropriate charger detection if a USB Revision 1.2-compliant device is attached. The autodetection charger mode is activated after the data contact detect is established. CB0 and CB1 must be set low to activate data contact detect support.

Remote Wake-Up Support

The MAX14603/MAX14604/MAX14605/MAX14618 feature remote wake-up if pass-through mode with CDP emulation is used prior to transitioning to auto mode in standby state (S3). If the peripheral device is connected and remains in the USB port during S0 state, the MAX14603/MAX14604/MAX14605/MAX14618 maintain the pass-through mode until it is removed. If this feature is not needed, such as in battery-powered mode, the embedded control could cancel the remote wake-up by toggling the V_{BUS} as it moves into the standby state.

Backward Compatibility

The MAX14602/MAX14605 offer easy backward-compatible CDP emulation upgrade to the MAX14566E.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test methodology and results.

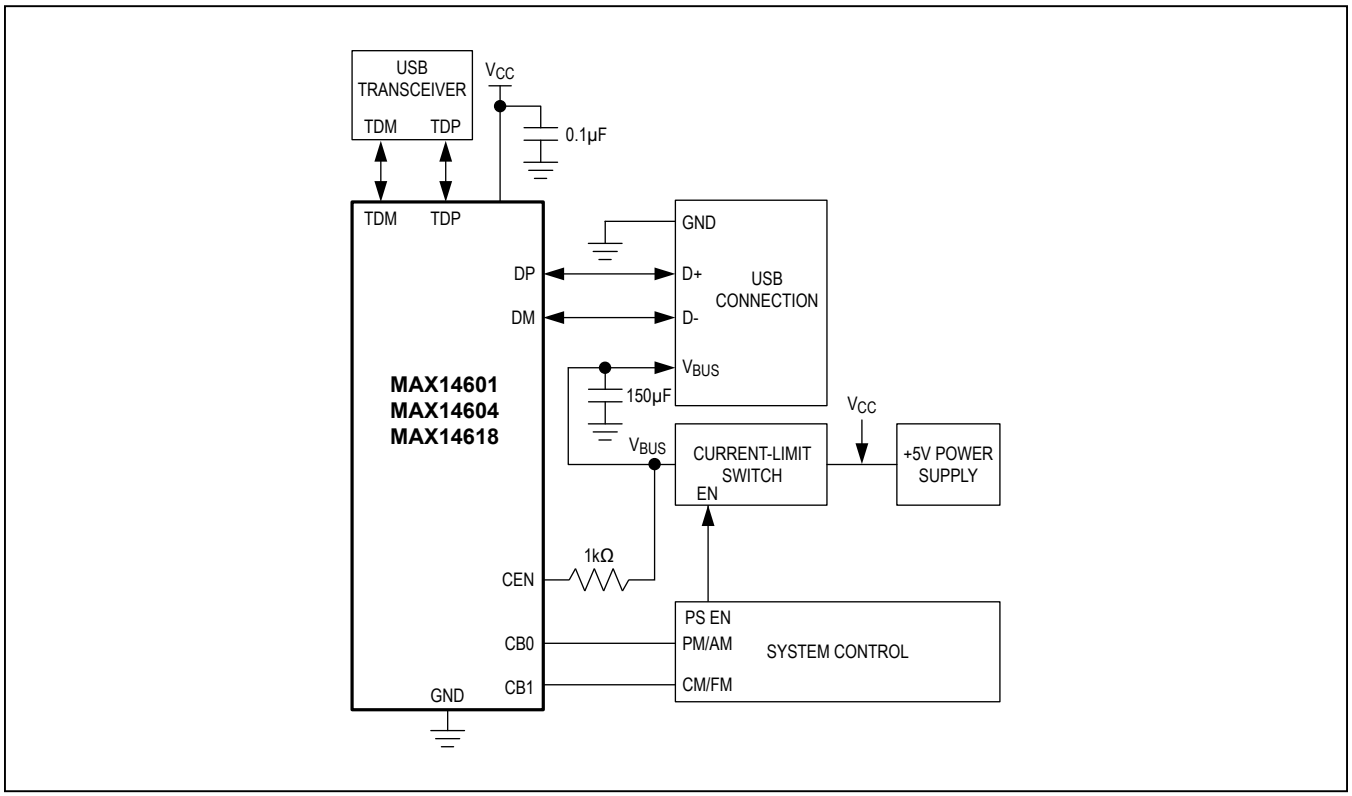


Figure 6. MAX14601/MAX14604/MAX14618 V_{BUS} Discharge Circuit

Extended ESD Protection (Human Body Model)

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV (Human Body Model) encountered during handling and assembly. The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the device continues to function without latchup (Figure 7a and Figure 7b).

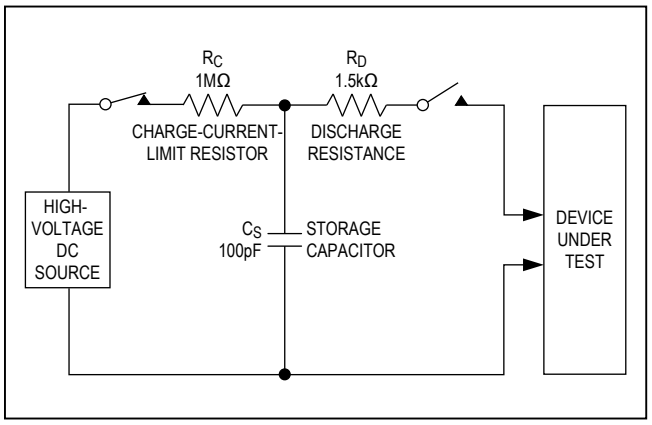


Figure 7a. Human Body ESD Test Model

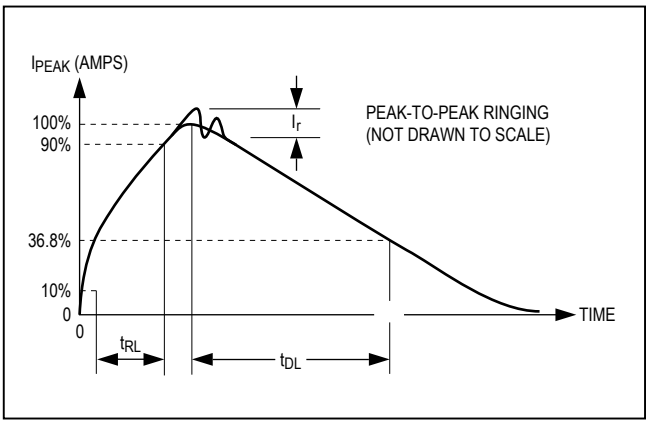


Figure 7b. Human Body Current Waveform

Ordering Information/Selector Guide

PART	TEMP RANGE	MODE CONTROL	CLS CONTROL	REMOTE WAKE-UP	PIN-PACKAGE
MAX14600ETA+T	-40°C to +85°C	CB0, CB1	$\overline{\text{CEN}}$	No	8 TDFN-EP*
MAX14601ETA+T**	-40°C to +85°C	CB0, CB1	CEN	No	8 TDFN-EP*
MAX14602ETA+T	-40°C to +85°C	CB0	$\overline{\text{CEN}}$	No	8 TDFN-EP*
MAX14603ETA+T**	-40°C to +85°C	CB0, CB1	$\overline{\text{CEN}}$	Yes	8 TDFN-EP*
MAX14604ETA+T	-40°C to +85°C	CB0, CB1	CEN	Yes	8 TDFN-EP*
MAX14605ETA+T**	-40°C to +85°C	CB0	$\overline{\text{CEN}}$	Yes	8 TDFN-EP*
MAX14618ETA+T†	-40°C to +85°C	CB0, CB1	CEN	Yes	8 TDFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

***Future product—contact factory for availability.*

†Refer to Table 2 for differences in digital input.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 TDFN-EP	T822+2	**21-0168**	**90-0065**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—
1	9/11	Added MAX14618 to data sheet; corrected Conditions on V_{DM_SRC} Voltage in the *Electrical Characteristics*; corrected x-scale labels on TOC5 in the *Typical Operating Characteristics*	1–7, 9, 11–15
2	10/11	Corrected package code and land pattern number in the *Package Information*	15
3	5/12	Relabeled TOC 10	9
4	2/16	Added Note 6 to *Electrical Characteristics* table	2, 3