2.7V to 3.6V and 4.5V to 5.5V, Low-Power, 4-/8-/12-Channel 2-Wire Serial 8-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
AIN0–AIN11, REF to GND .....-0.3V to the lower of (V_{DD} + 0.3V) and +6V
SDA, SCL to GND.....-0.3V to +6V
Maximum Current into Any Pin .....±50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 7.1mW/°C above +70°C).....567mW
16-Pin QSOP (derate 8.3mW/°C above +70°C).....666.7mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 3.6V (MAX11601/MAX11603/MAX11605), V_{DD} = 4.5V to 5.5V (MAX11600/MAX11602/MAX11604). External reference, V_{REF} = 2.048V (MAX11601/MAX11603/MAX11605), V_{REF} = 4.096V (MAX11600/MAX11602/MAX11604). External clock, f_{SCL} = 1.7MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			8			Bits
Relative Accuracy	INL	(Note 2)			±1	LSB
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error					±1.5	LSB
Offset-Error Temperature Coefficient				3		ppm/°C
Gain Error		(Note 3)			±1	LSB
Gain Temperature Coefficient				±1		ppm/°C
Total Unadjusted Error	TUE	MAX11600/MAX11601		±0.5	±2	LSB
		MAX11602/MAX11603		±0.5	±1	
		MAX11604/MAX11605		±0.5	±1	
Channel-to-Channel Offset Matching				±0.1		LSB
Channel-to-Channel Gain Matching				±0.5		LSB
Input Common-Mode Rejection Ratio	CMRR	Pseudo-differential input mode		75		dB
DYNAMIC PERFORMANCE (f_{IN}(sine wave) = 25kHz, V_{IN} = $V_{REF(P-P)}$, f_{SAMPLE} = 188ksps, R_{IN} = 100Ω)						
Signal-to-Noise Plus Distortion	SINAD			49		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-69		dB
Spurious-Free Dynamic Range	SFDR			69		dB
Channel-to-Channel Crosstalk		(Note 4)		75		dB
Full-Power Bandwidth		-3dB point		2.0		MHz
Full-Linear Bandwidth		SINAD > 49dB		200		kHz
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock			6.1	µs
		External clock	4.7			

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 3.6V (MAX11601/MAX11603/MAX11605), V_{DD} = 4.5V to 5.5V (MAX11600/MAX11602/MAX11604). External reference, V_{REF} = 2.048V (MAX11601/MAX11603/MAX11605), V_{REF} = 4.096V (MAX11600/MAX11602/MAX11604). External clock, f_{SCL} = 1.7MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Throughput Rate	f_{SAMPLE}	Internal clock, SCAN[1:0] = 01 (MAX11600/MAX11601)				76	ksps
		SCAN[1:0] = 00 CS[3:0] = 0111 (MAX11602/MAX11603)				76	
		Internal clock, SCAN[1:0] = 00 CS[3:0] = 1011 (MAX11604/MAX11605)				77	
		External clock				188	
Track/Hold Acquisition Time				588			ns
Internal Clock Frequency					2.25		MHz
Aperture Delay	t_{AD}	External clock, fast mode			45		ns
		External clock, high-speed mode			30		
ANALOG INPUT (AIN0–AIN11)							
Input Voltage Range, Single Ended and Differential (Note 6)		Unipolar		0		V_{REF}	V
		Bipolar				$\pm V_{REF}/2$	
Input Multiplexer Leakage Current		On/off-leakage current, $V_{AIN\_}$ = 0 or V_{DD}, no clock, f_{SCL} = 0			±0.01	±1	µA
Input Capacitance	C_{IN}				18		pF
INTERNAL REFERENCE (Note 7)							
Reference Voltage	V_{REF}	T_A = +25°C	MAX11601/MAX11603/MAX11605	1.925	2.048	2.171	V
			MAX11600/MAX11602/MAX11604	3.850	4.096	4.342	
Reference Temperature Coefficient	TC_{REF}				120		ppm/°C
Reference Short-Circuit Current						10	mA
Reference Source Impedance		(Note 8)			675		Ω
EXTERNAL REFERENCE							
Reference Input Voltage Range	V_{REF}	(Note 9)		1.0		V_{DD}	V
REF Input Current	I_{REF}	f_{SAMPLE} = 188ksps			14	30	µA
DIGITAL INPUTS/OUTPUTS (SCL, SDA)							
Input High Voltage	V_{IH}			0.7 x V_{DD}			V
Input Low Voltage	V_{IL}					0.3 x V_{DD}	V
Input Hysteresis	V_{HYST}			0.1 x V_{DD}			V
Input Current	I_{IN}	V_{IN} = 0 to V_{DD}				±10	µA
Input Capacitance	C_{IN}				15		pF
Output Low Voltage	V_{OL}	I_{SINK} = 3mA				0.4	V

2.7V to 3.6V and 4.5V to 5.5V, Low-Power, 4-/8-/12-Channel 2-Wire Serial 8-Bit ADCs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 3.6V (MAX11601/MAX11603/MAX11605), V_{DD} = 4.5V to 5.5V (MAX11600/MAX11602/MAX11604). External reference, V_{REF} = 2.048V (MAX11601/MAX11603/MAX11605), V_{REF} = 4.096V (MAX11600/MAX11602/MAX11604). External clock, f_{SCL} = 1.7MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Voltage (Note 10)	V_{DD}	MAX11601/MAX11603/MAX11605		2.7		3.6	V
		MAX11600/MAX11602/MAX11604		4.5		5.5	
Supply Current	I_{DD}	f_{SAMPLE} = 188ksps	Internal REF, external clock		350	650	µA
			External REF, external clock		250		
		f_{SAMPLE} = 75ksps	External REF, external clock		110		
			External REF, internal clock		150		
		f_{SAMPLE} = 10ksps	External REF, external clock		8		
			External REF, internal clock		10		
		f_{SAMPLE} = 1ksps	External REF, external clock		2		
			External REF, internal clock		2.5		
		Power-down			1	10	
Power-Supply Rejection Ratio	PSRR	(Note 11)			±0.25	±1	LSB/V
TIMING CHARACTERISTICS FOR 2-WIRE FAST MODE (Figures 1a and 2)							
Serial-Clock Frequency	f_{SCL}					400	kHz
Bus Free Time Between a STOP (P) and a START (S) Condition	t_{BUF}			1.3			µs
Hold Time for START Condition	$t_{HD.STA}$			0.6			µs
Low Period of the SCL Clock	t_{LOW}			1.3			µs
High Period of the SCL Clock	t_{HIGH}			0.6			µs
Setup Time for a Repeated START Condition (Sr)	$t_{SU.STA}$			0.6			µs
Data Hold Time	$t_{HD.DAT}$	(Note 12)		0		150	ns
Data Setup Time	$t_{SU.DAT}$			100			ns
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Note 13)		$20 + 0.1C_B$		300	ns
Fall Time of SDA Transmitting	t_F	(Note 13)		$20 + 0.1C_B$		300	ns
Setup Time for STOP Condition	$t_{SU.STO}$			0.6			µs
Capacitive Load for Each Bus Line	C_B					400	pF
Pulse Width of Spike Suppressed	t_{SP}					50	ns
TIMING CHARACTERISTICS FOR 2-WIRE HIGH-SPEED MODE (Figures 1b and 2)							
Serial-Clock Frequency	f_{SCLH}	(Note 14)				1.7	MHz
Hold Time (Repeated) START Condition	$t_{HD.STA}$			160			ns
Low Period of the SCL Clock	t_{LOW}			320			ns
High Period of the SCL Clock	t_{HIGH}			120			ns
Setup Time for a Repeated START Condition (Sr)	$t_{SU.STA}$			160			ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 3.6V (MAX11601/MAX11603/MAX11605), V_{DD} = 4.5V to 5.5V (MAX11600/MAX11602/MAX11604). External reference, V_{REF} = 2.048V (MAX11601/MAX11603/MAX11605), V_{REF} = 4.096V (MAX11600/MAX11602/MAX11604). External clock, f_{SCL} = 1.7MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Hold Time	$t_{HD·DAT}$	(Note 12)	0		150	ns
Data Setup Time	$t_{SU·DAT}$		10			ns
Rise Time of SCL Signal (Current Source Enabled)	t_{RCL}	(Note 13)	20		80	ns
Rise Time of SCL Signal After Acknowledge Bit	t_{RCL1}	(Note 13)	20		160	ns
Fall Time of SCL Signal	t_{FCL}	(Note 13)	20		80	ns
Rise Time of SDA Signal	t_{RDA}	(Note 13)	20		160	ns
Fall Time of SDA Signal	t_{FDA}	(Note 13)	20		160	ns
Setup Time for STOP Condition	$t_{SU, STO}$		160			ns
Capacitive Load for Each Bus Line	C_B				400	pF
Pulse Width of Spike Suppressed	t_{SP}		0		10	ns

Note 1: The MAX11600/MAX11602/MAX11604 are tested at V_{DD} = 5V and the MAX11601/MAX11603/MAX11605 are tested at V_{DD} = 3V. All devices are configured for unipolar, single-ended inputs.

Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range and offsets have been calibrated.

Note 3: Offset nulled.

Note 4: Ground on channel; sine wave applied to all off channels.

Note 5: Conversion time is defined as the number of clock cycles (eight) multiplied by the clock period. Conversion time does not include acquisition time. SCL is the conversion clock in the external clock mode.

Note 6: The absolute voltage range for the analog inputs (AIN0–AIN11) is from GND to V_{DD}.

Note 7: When AIN_/REF (MAX11600/MAX11601/MAX11604/MAX11605) or REF (MAX11602/MAX11603) is configured to be an internal reference (SEL[2:1] = 11), decouple AIN_/REF or REF to GND with a 0.01µF capacitor.

Note 8: The switch connecting the reference buffer to AIN_/REF or REF has a typical on-resistance of 675Ω.

Note 9: ADC performance is limited by the converter's noise floor, typically 1.4mV_{P-P}.

Note 10: Electrical characteristics are guaranteed from $V_{DD(MIN)}$ to $V_{DD(MAX)}$. For operation beyond this range, see the *Typical Operating Characteristics*.

Note 11: Power-supply rejection ratio is measured as:

$$\frac{\left[V_{FS}(3.3V) - V_{FS}(2.7V)\right] \times \frac{2^N}{V_{REF}}}{3.3V - 2.7V},$$

for the MAX11601/MAX11603/MAX11605, where N is the number of bits.
Power-supply rejection ratio is measured as:

$$\frac{\left[V_{FS}(5.5V) - V_{FS}(4.5V)\right] \times \frac{2^N}{V_{REF}}}{5.5V - 4.5V},$$

for the MAX11600/MAX11602/MAX11604, where N is the number of bits.

Note 12: A master device must provide a data hold time for SDA (referred to V_{IL} of SCL) to bridge the undefined region of SCL's falling edge (Figure 1).

Note 13: C_B = total capacitance of one bus line in pF. t_R, t_{FDA}, and t_F measured between 0.3V_{DD} and 0.7V_{DD}. The minimum value is specified at T_A = +25°C with C_B = 400pF.

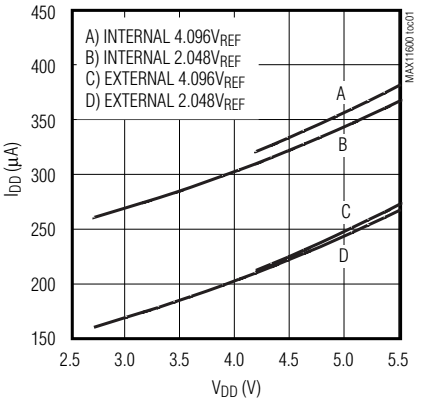
Note 14: f_{SCLH} must meet the minimum clock low time plus the rise/fall times.

2.7V to 3.6V and 4.5V to 5.5V, Low-Power, 4-/8-/12-Channel 2-Wire Serial 8-Bit ADCs

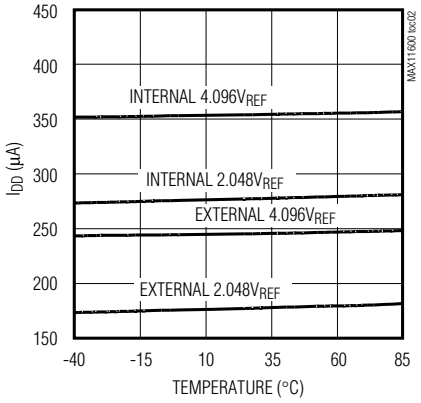
Typical Operating Characteristics

(V_{DD} = 3.3V (MAX11601/MAX11603/MAX11605), V_{DD} = 5V (MAX11600/MAX11602/MAX11604), f_{SCL} = 1.7MHz, external clock (33% duty cycle), f_{SAMPLE} = 188ksps, single ended, unipolar, T_A = +25°C, unless otherwise noted.)

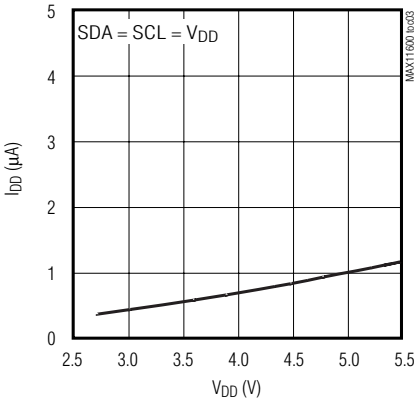
SUPPLY CURRENT vs. VOLTAGE



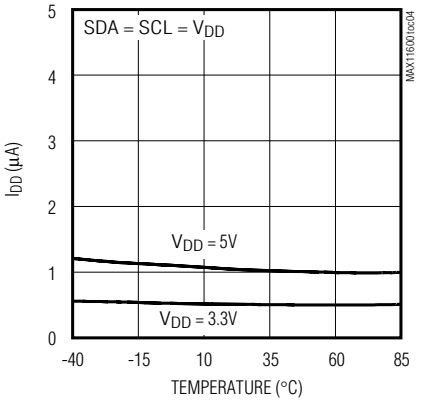
SUPPLY CURRENT vs. TEMPERATURE



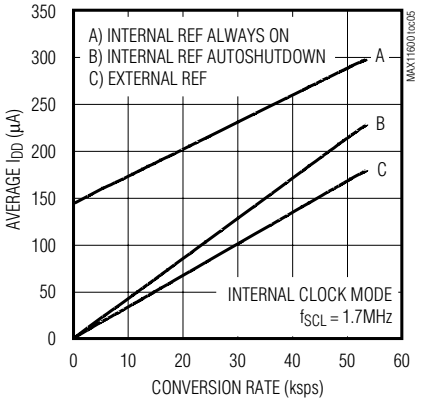
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



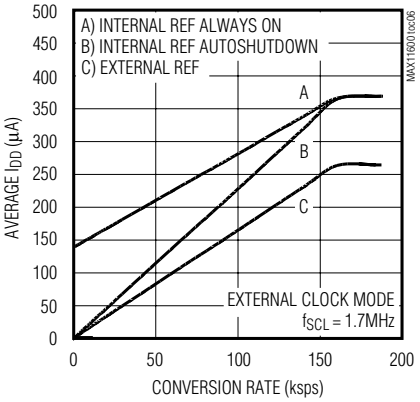
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



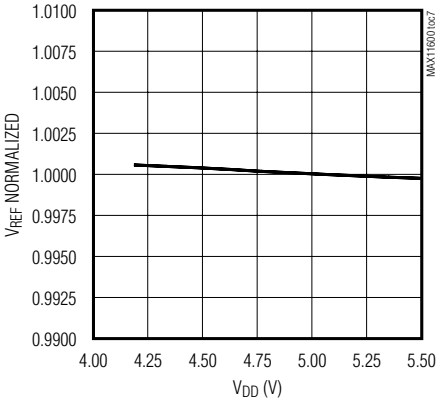
AVERAGE SUPPLY CURRENT vs. CONVERSION RATE (INTERNAL CLOCK)



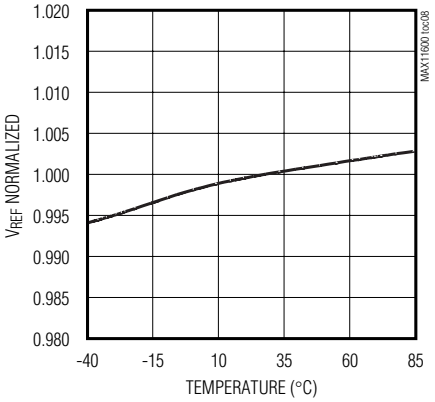
AVERAGE SUPPLY CURRENT vs. CONVERSION RATE (EXTERNAL CLOCK)



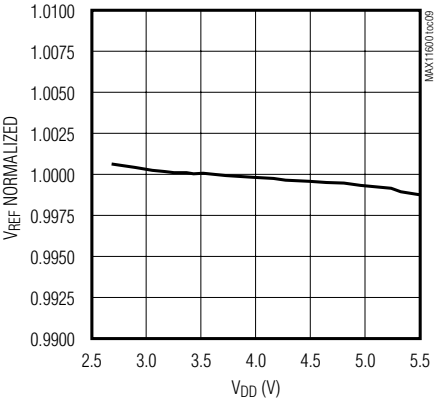
NORMALIZED 4.096V REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



INTERNAL 4.096V REFERENCE VOLTAGE vs. TEMPERATURE



INTERNAL 2.048V REFERENCE VOLTAGE vs. SUPPLY VOLTAGE

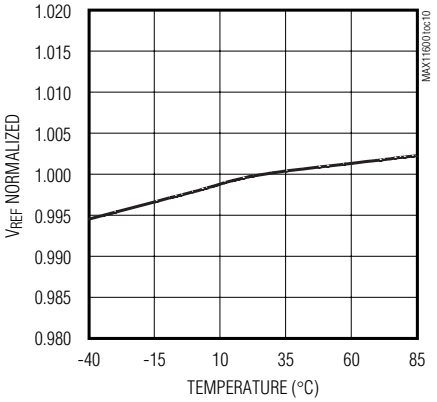


2.7V to 3.6V and 4.5V to 5.5V, Low-Power, 4-/8-/12-Channel 2-Wire Serial 8-Bit ADCs

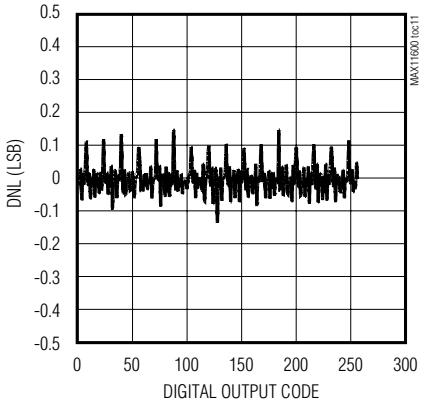
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V (MAX11601/MAX11603/MAX11605), V_{DD} = 5V (MAX11600/MAX11602/MAX11604), f_{SCL} = 1.7MHz, external clock (33% duty cycle), f_{SAMPLE} = 188ksps, single ended, unipolar, T_A = +25°C, unless otherwise noted.)

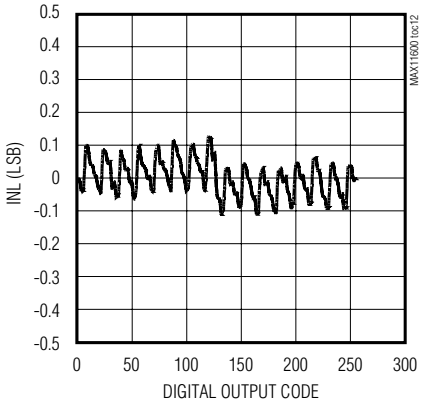
INTERNAL 2.048V REFERENCE VOLTAGE vs. TEMPERATURE



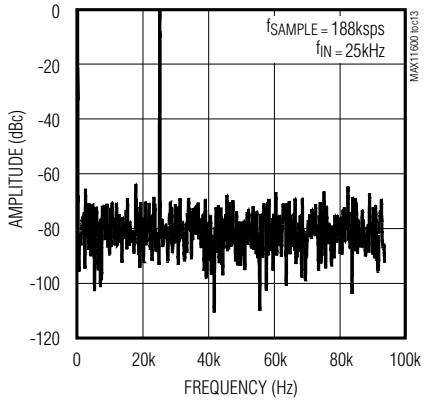
DIFFERENTIAL NONLINEARITY vs. DIGITAL CODE



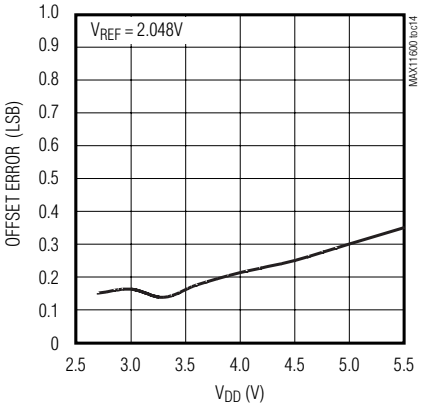
INTEGRAL NONLINEARITY vs. DIGITAL CODE



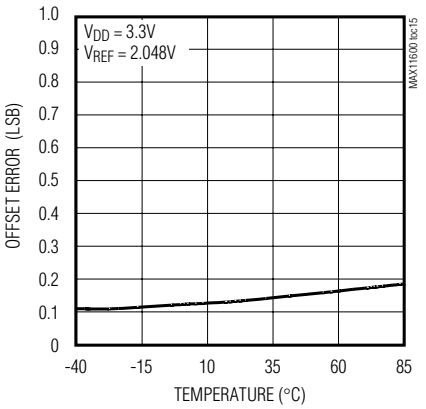
FFT PLOT



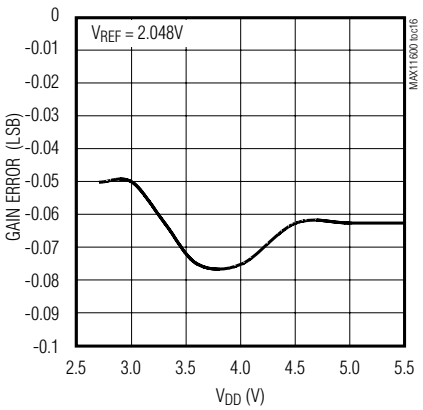
OFFSET ERROR vs. SUPPLY VOLTAGE



OFFSET ERROR vs. TEMPERATURE



GAIN ERROR vs. SUPPLY VOLTAGE



2.7V to 3.6V and 4.5V to 5.5V, Low-Power, 4-/8-/12-Channel 2-Wire Serial 8-Bit ADCs

Pin Description

PIN			NAME	FUNCTION
MAX11600 MAX11601	MAX11602 MAX11603	MAX11604 MAX11605		
1, 2, 3	12, 11, 10	12, 11, 10	AIN0, AIN1, AIN2	Analog Inputs
—	9–5	9–5	AIN3–AIN7	
—	—	4, 3, 2	AIN8–AIN10	
4	—	—	AIN3/REF	Analog Input 3/Reference Input/Output. Selected in the setup register (see Tables 1 and 6).
—	1	—	REF	Reference Input/Output. Selected in the setup register (see Tables 1 and 6).
—	—	1	AIN11/REF	Analog Input 11/Reference Input/Output. Selected in the setup register (see Tables 1 and 6).
5	13	13	SCL	Clock Input
6	14	14	SDA	Data Input/Output
7	15	15	GND	Ground
8	16	16	V_{DD}	Positive Supply. Bypass to GND with a 0.1µF capacitor.
—	2, 3, 4	—	N.C.	No Connection

Detailed Description

The MAX11600–MAX11605 ADCs use successive-approximation conversion techniques and input T/H circuitry to capture and convert an analog signal to a serial 8-bit digital output. The MAX11600/MAX11601 are 4-channel ADCs, the MAX11602/MAX11603 are 8-channel ADCs and the MAX11604/MAX11605 are 12-channel ADCs. These devices feature a high-speed 2-wire serial interface supporting data rates up to 1.7MHz. Figure 3 shows the simplified functional diagram for the MAX11604/MAX11605.

Power Supply

The MAX11600–MAX11605 operate from a single supply and consume 350µA at sampling rates up to 188ksps. The MAX11601/MAX11603/MAX11605 feature a 2.048V internal reference and the MAX11600/MAX11602/MAX11604 feature a 4.096V internal reference. All devices can be configured for use with an external reference from 1V to V_{DD}.

Analog Input and Track/Hold

The MAX11600–MAX11605 analog input architecture contains an analog input multiplexer (MUX), a T/H capacitor, T/H switches, a comparator, and a switched capacitor digital-to-analog converter (DAC) (Figure 4).

In single-ended mode, the analog input multiplexer connects $C_{T/H}$ to the analog input selected by CS[3:0] (see the *Configuration/Setup Bytes (Write Cycle)* section). The charge on $C_{T/H}$ is referenced to GND when converted. In pseudo-differential mode, the analog input multiplexer connects $C_{T/H}$ to the positive analog input selected by CS[3:0]. The charge on $C_{T/H}$ is referenced to the negative analog input when converted.

The MAX11600–MAX11605 input configuration is pseudo-differential in that only the signal at the positive analog input is sampled with the T/H circuitry. The negative analog input signal must remain stable within ±0.5 LSB (±0.1 LSB for best results) with respect to GND during a conversion. To accomplish this, connect a 0.1µF capacitor from the negative analog input to GND. See the *Single-Ended/Pseudo-Differential Input* section.

During the acquisition interval, the T/H switches are in the track position and $C_{T/H}$ charges to the analog input signal. At the end of the acquisition interval, the T/H switches move to the hold position retaining the charge on $C_{T/H}$ as a sample of the input signal.

During the conversion interval, the switched capacitive DAC adjusts to restore the comparator input voltage to zero within the limits of 8-bit resolution. This action requires eight conversion clock cycles and is equivalent to transferring a charge of 18pF × (V_{IN}+ - V_{IN}-) from $C_{T/H}$ to the binary weighted capacitive DAC, forming a digital representation of the analog input signal.

Sufficiently low source impedance is required to ensure an accurate sample. A source impedance below 1.5kΩ does not significantly degrade sampling accuracy. To

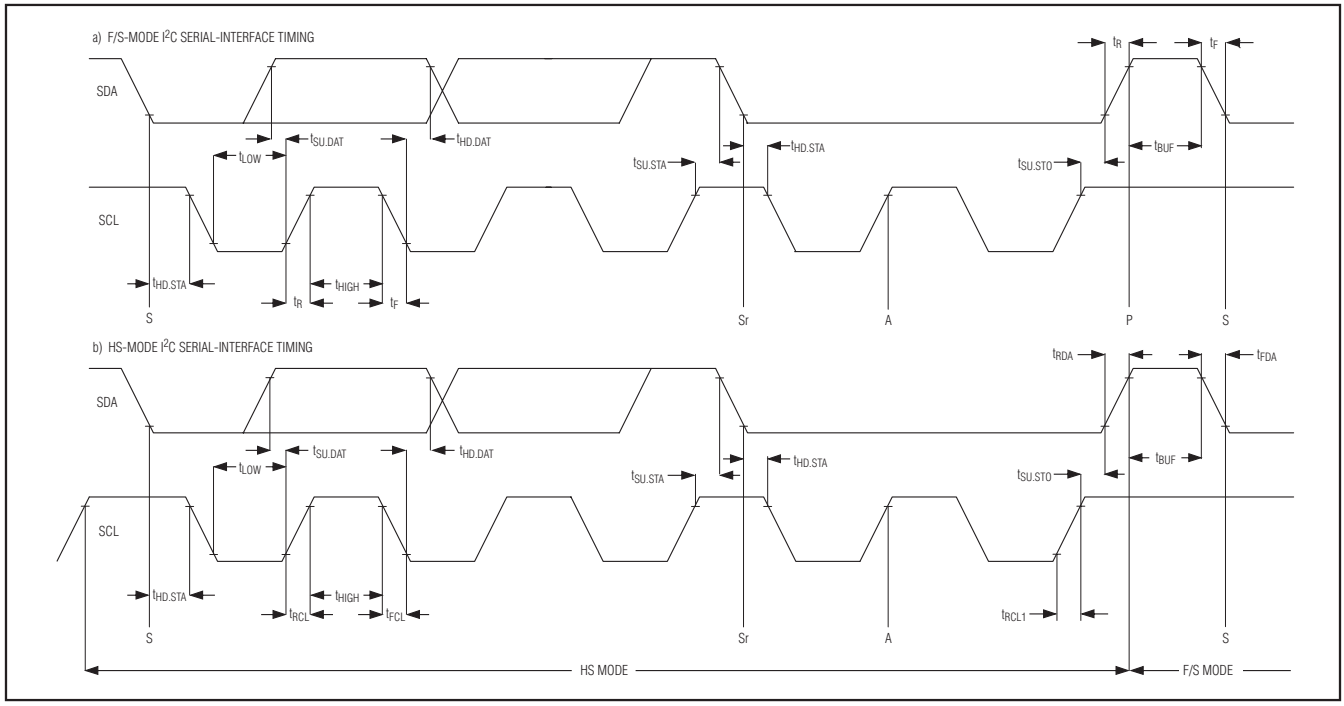


Figure 1. I²C Serial-Interface Timing

minimize sampling errors with higher source impedances, connect a 100pF capacitor from the analog input to GND. This input capacitor forms an RC filter with the source impedance limiting the analog input bandwidth. For larger source impedances, use a buffer amplifier to maintain analog input signal integrity.

When operating in internal clock mode, the T/H circuitry enters its tracking mode on the ninth falling clock edge of the address byte (see the *Slave Address* section). The T/H circuitry enters hold mode two internal clock cycles later. A conversion or a series of conversions is then internally clocked (eight clock cycles per conversion) and the MAX11600–MAX11605 hold SCL low. When operating in external clock mode, the T/H circuitry enters track mode on the seventh falling edge of a valid slave address byte. Hold mode is then entered on the falling edge of the eighth clock cycle. The conversion is performed during the next eight clock cycles.

The time required for the T/H circuitry to acquire an input signal is a function of input capacitance. If the analog input source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. The acquisition time (t_{ACQ}) is the minimum time needed for the signal to be acquired. It is calculated by:

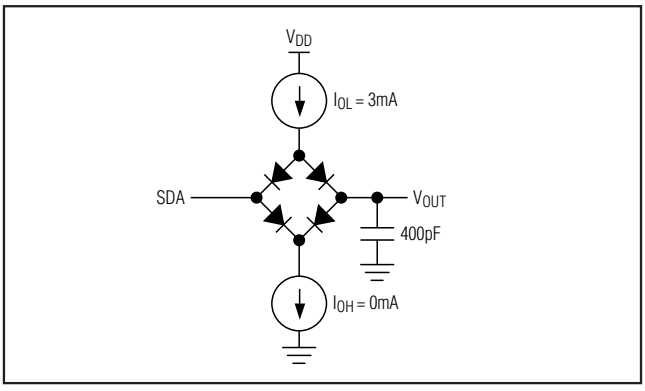


Figure 2. Load Circuit

$$t_{ACQ} \geq 6.25 \times (R_{SOURCE} + R_{IN}) \times C_{IN}$$

where R_{SOURCE} is the analog input source impedance, R_{IN} = 2.5kΩ, and C_{IN} = 18pF. t_{ACQ} is $1/f_{SCL}$ for external clock mode. For internal clock mode, the acquisition time is two internal clock cycles. To select R_{SOURCE}, allow 625ns for t_{ACQ} in internal clock mode to account for clock frequency variations.

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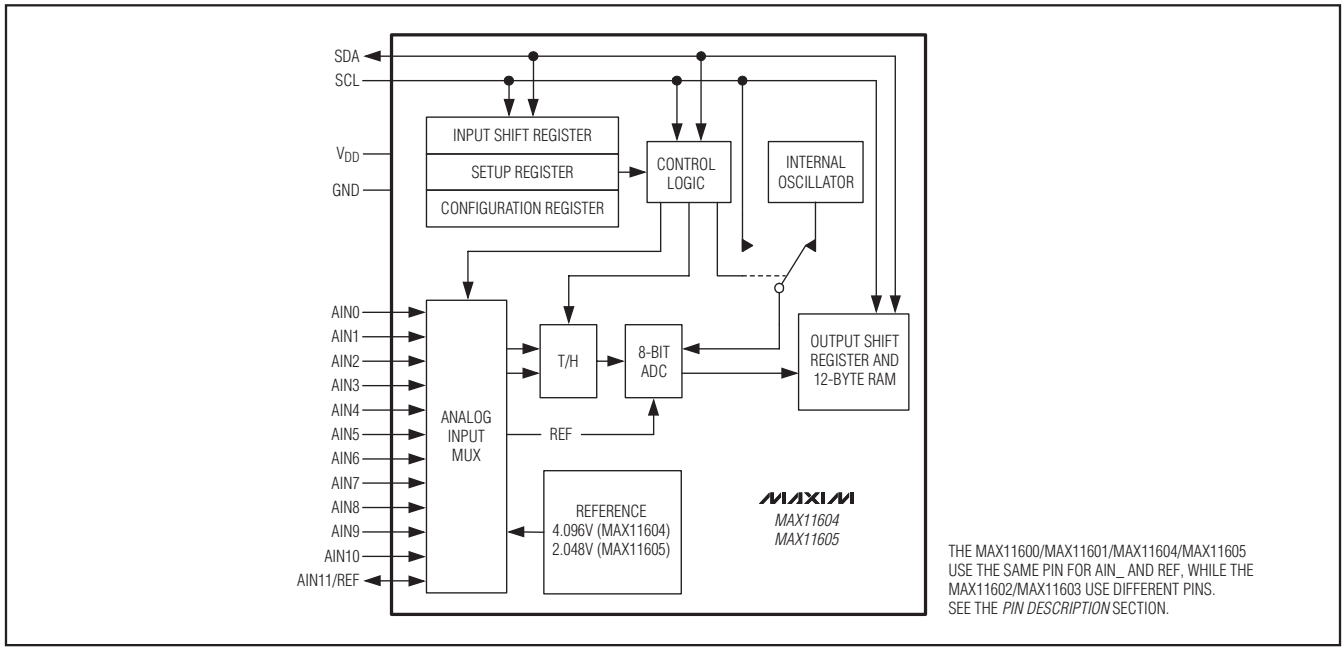

Figure 3. MAX11604/MAX11605 Simplified Functional Diagram

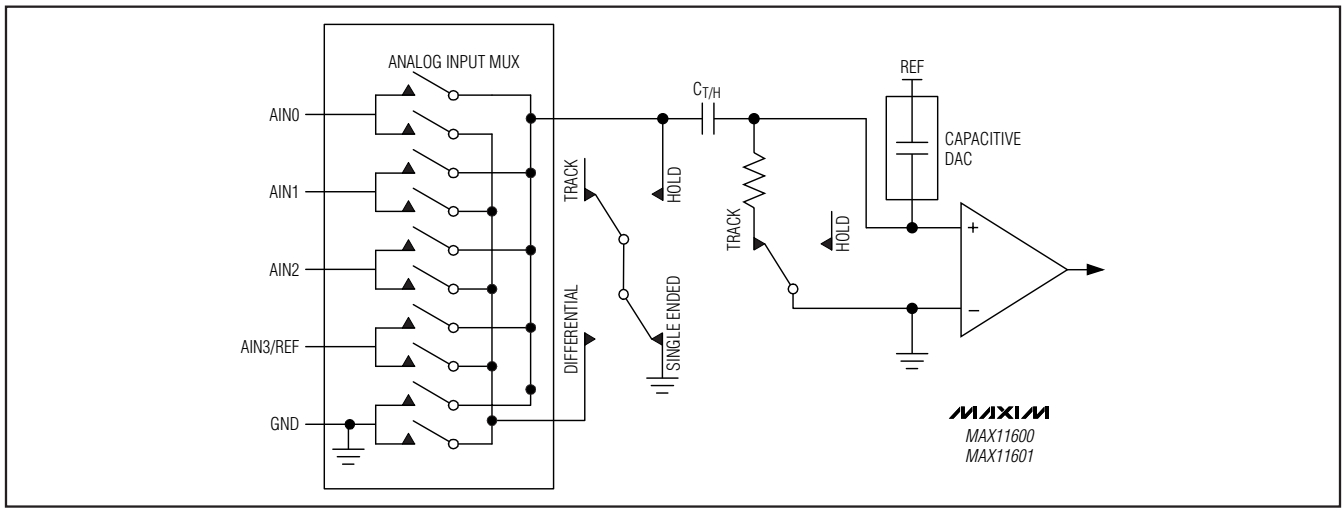

Figure 4. Equivalent Input Circuit

Analog Input Bandwidth

The MAX11600–MAX11605 feature input tracking circuitry with a 2MHz small signal bandwidth. The 2MHz input bandwidth makes it possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Range and Protection

Internal protection diodes clamp the analog input to V_{DD} and GND. These diodes allow the analog inputs to swing from (GND - 0.3V) to (V_{DD} + 0.3V) without causing damage to the device. For accurate conversions, the inputs must not go more than 50mV below GND or above V_{DD}. If the analog input exceeds V_{DD} by more than 50mV, the input current should be limited to 2mA.

Table 1. Setup Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
REG	SEL2	SEL1	SEL0	CLK	BIP/$\overline{\text{UNI}}$	$\overline{\text{RST}}$	X

BIT	NAME	DESCRIPTION
7	REG	Register bit. 1 = setup byte, 0 = configuration byte (Table 2).
6	SEL2	Three bits select the reference voltage and the state of AIN_/REF (MAX11600/MAX11601/MAX11604/MAX11605) or REF (MAX11602/MAX11603) (Table 6). Default to 000 at power-up.
5	SEL1	
4	SEL0	
3	CLK	1 = external clock, 0 = internal clock. Defaulted to zero at power-up.
2	BIP/$\overline{\text{UNI}}$	1 = bipolar, 0 = unipolar. Defaulted to zero at power-up (see the *Unipolar/Bipolar* section).
1	$\overline{\text{RST}}$	1 = no action, 0 = resets the configuration register to default. Setup register remains unchanged.
0	X	Don't care; can be set to 1 or 0.

Single-Ended/Pseudo-Differential Input

The SGL/$\overline{\text{DIF}}$ bit of the configuration byte configures the MAX11600–MAX11605 analog input circuitry for single-ended or pseudo-differential inputs (Table 2). In single-ended mode (SGL/$\overline{\text{DIF}}$ = 1), the digital conversion results are the difference between the analog input selected by CS[3:0] and GND (Table 3). In pseudo-differential mode (SGL/$\overline{\text{DIF}}$ = 0), the digital conversion results are the difference between the positive and the negative analog inputs selected by CS[3:0] (Table 4). The negative analog input signal must remain stable within ±0.5 LSB (±0.1 LSB for best results) with respect to GND during a conversion.

Unipolar/Bipolar

When operating in pseudo-differential mode, the BIP/$\overline{\text{UNI}}$ bit of the setup byte (Table 1) selects unipolar or bipolar operation. Unipolar mode sets the differential analog input range from zero to V_{REF}. A negative differential analog input in unipolar mode causes the digital output code to be zero. Selecting bipolar mode sets the differential input range to ±V_{REF}/2, with respect to the negative input. The digital output code is binary in unipolar mode and two's complement binary in bipolar mode (see the *Transfer Functions* section).

In single-ended mode, the MAX11600–MAX11605 always operate in unipolar mode regardless of the BIP/$\overline{\text{UNI}}$ setting, and the analog inputs are internally referenced to GND with a full-scale input range from zero to V_{REF}.

Digital Interface

The MAX11600–MAX11605 feature a 2-wire interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX11600–MAX11605 and the master at rates up to 1.7MHz. The MAX11600–MAX11605 are slaves that transmit and receive data. The master (typically a microcontroller) initiates data transfer on the bus and generates SCL to permit that transfer.

SDA and SCL must be pulled high. This is typically done with pullup resistors (500Ω or greater) (see *Typical Operating Circuit*). Series resistors (R_S) are optional. They protect the input architecture of the MAX11600–MAX11605 from high-voltage spikes on the bus lines and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL clock cycle. Nine clock cycles are required to transfer the data in or out of the MAX11600–MAX11605. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). Both SDA and SCL idle high when the bus is not busy.

START and STOP Conditions

The master initiates a transmission with a START condition (S), a high-to-low transition on SDA with SCL high. The master terminates a transmission with a STOP condition (P), a low-to-high transition on SDA, while

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SCL is high (Figure 5). A repeated START condition (Sr) can be used in place of a STOP condition to leave the bus active and in its current timing mode (see the *HS Mode* section).

Acknowledge Bits

Successful data transfers are acknowledged with an acknowledge bit (A) or a not-acknowledge bit ($\overline{A}$). Both the master and the MAX11600–MAX11605 (slave) generate acknowledge bits. To generate an acknowledge bit, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse (Figure 6). To generate a not acknowledge bit, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by a slave address. When idle, the MAX11600–MAX11605 continuously wait for a START condition followed by their slave address. When the MAX11600–MAX11605 recognize their slave address, they are ready to accept or send data. The slave address has been factory programmed and is always 1100100 for the MAX11600/MAX11601, 1101101 for MAX11602/MAX11603, and 1100101 for MAX11604/MAX11605 (Figure 7). The least significant bit (LSB) of the address byte (R/$\overline{W}$) determines whether the master is writing to or reading from the MAX11600–MAX11605 (R/$\overline{W}$ = zero selects a write condition. R/$\overline{W}$ = 1 selects a read condition). After receiving the address, the MAX11600–MAX11605 (slave) issue an acknowledge by pulling SDA low for one clock cycle.

Bus Timing

At power-up, the MAX11600–MAX11605 bus timing defaults to fast mode (F/S mode), allowing conversion rates up to 44ksps. The MAX11600–MAX11605 must operate in high-speed mode (HS mode) to achieve conversion rates up to 188ksps. Figure 1 shows the bus timing for the MAX11600–MAX11605 2-wire interface.

HS Mode

At power-up, the MAX11600–MAX11605 bus timing is set for F/S mode. The master selects HS mode by addressing all devices on the bus with the HS mode master code 0000 1XXX (X = don't care). After successfully receiving the HS-mode master code, the MAX11600–MAX11605 issues a not acknowledge, allowing SDA to be pulled high for one clock cycle (Figure 8). After the not acknowledge, the MAX11600–MAX11605 are in HS mode. The master must then send a repeated START followed by a slave address to initiate HS mode communication. If the master generates a STOP condition, the MAX11600–MAX11605 return to F/S mode.

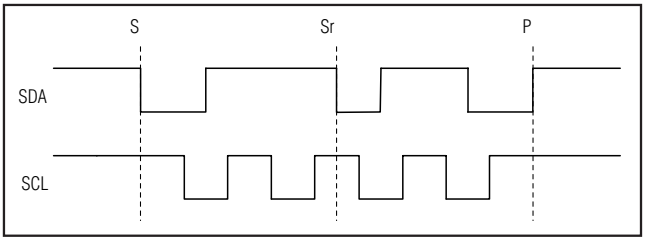

Figure 5. START and STOP Conditions

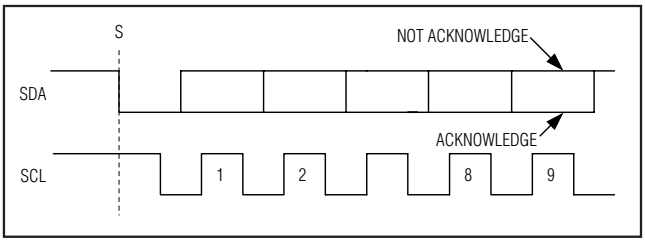

Figure 6. Acknowledge Bits

Configuration/Setup Bytes (Write Cycle)

Write cycles begin with the master issuing a START condition followed by 7 address bits (Figure 7) and 1 write bit (R/$\overline{W}$ = zero). If the address byte is successfully received, the MAX11600–MAX11605 (slave) issue an acknowledge. The master then writes to the slave. The slave recognizes the received byte as the setup byte (Table 1) if the most significant bit (MSB) is 1. If the MSB is zero, the slave recognizes that byte as the configuration byte (Table 2). The master can write either 1 or 2 bytes to the slave in any order (setup byte then configuration byte; configuration byte then setup byte; setup byte only; configuration byte only; Figure 9). If the slave receives bytes successfully, it issues an acknowledge. The master ends the write cycle by issuing a STOP condition or a repeated START condition. When operating in HS mode, a STOP condition returns the bus to F/S mode (see the *HS Mode* section).

DEVICE	SLAVE ADDRESS
MAX11600/MAX11601	1100100
MAX11602/MAX11603	1101101
MAX11604/MAX11605	1100101

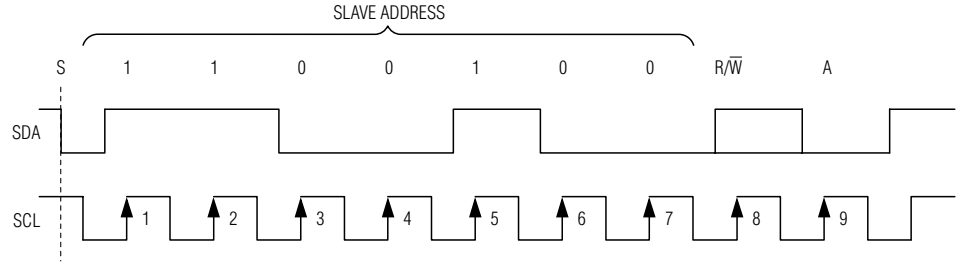

Figure 7. Slave Address Byte

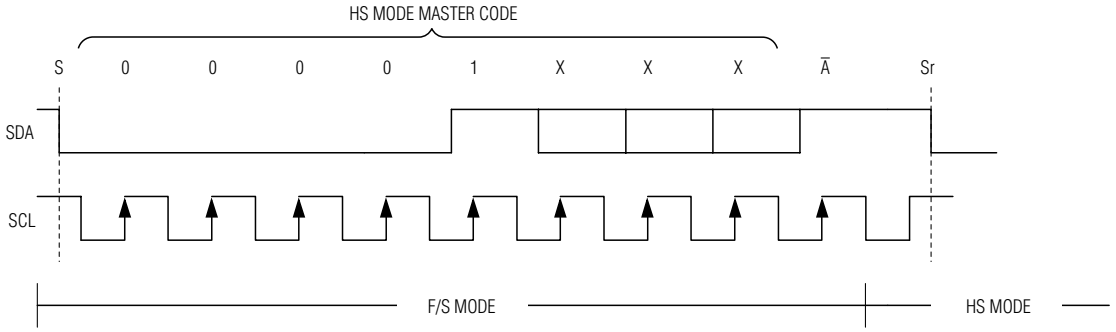

Figure 8. F/S Mode to HS Mode Transfer

Data Byte (Read Cycle)

A read cycle must be initiated to obtain conversion results. Read cycles begin with the bus master issuing a START condition followed by 7 address bits and a read bit (R/$\overline{W}$ = 1). If the address byte is successfully received, the MAX11600–MAX11605 (slave) issue an acknowledge. The master then reads from the slave. After the master has received the results, it can issue an acknowledge if it wants to continue reading or a not acknowledge if it no longer wishes to read. If the MAX11600–MAX11605 receive a not acknowledge, they release SDA, allowing the master to generate a STOP or repeated START. See the *Clock Mode* and *Scan Mode* sections for detailed information on how data is obtained and converted.

Clock Mode

The clock mode determines the conversion clock, the acquisition time, and the conversion time. The clock mode also affects the scan mode. The state of the setup byte's CLK bit determines the clock mode (Table 1). At power-up, the MAX11600–MAX11605 default to internal clock mode (CLK = zero).

Internal Clock

When configured for internal clock mode (CLK = zero), the MAX11600–MAX11605 use their internal oscillator as the conversion clock. In internal clock mode, the MAX11600–MAX11605 begin tracking analog input on the ninth falling clock edge of a valid slave address byte. Two internal clock cycles later, the analog signal is acquired and the conversion begins. While tracking and converting the analog input signal, the MAX11600–MAX11605 hold SCL low (clock stretching). After the conversion completes, the results are stored in

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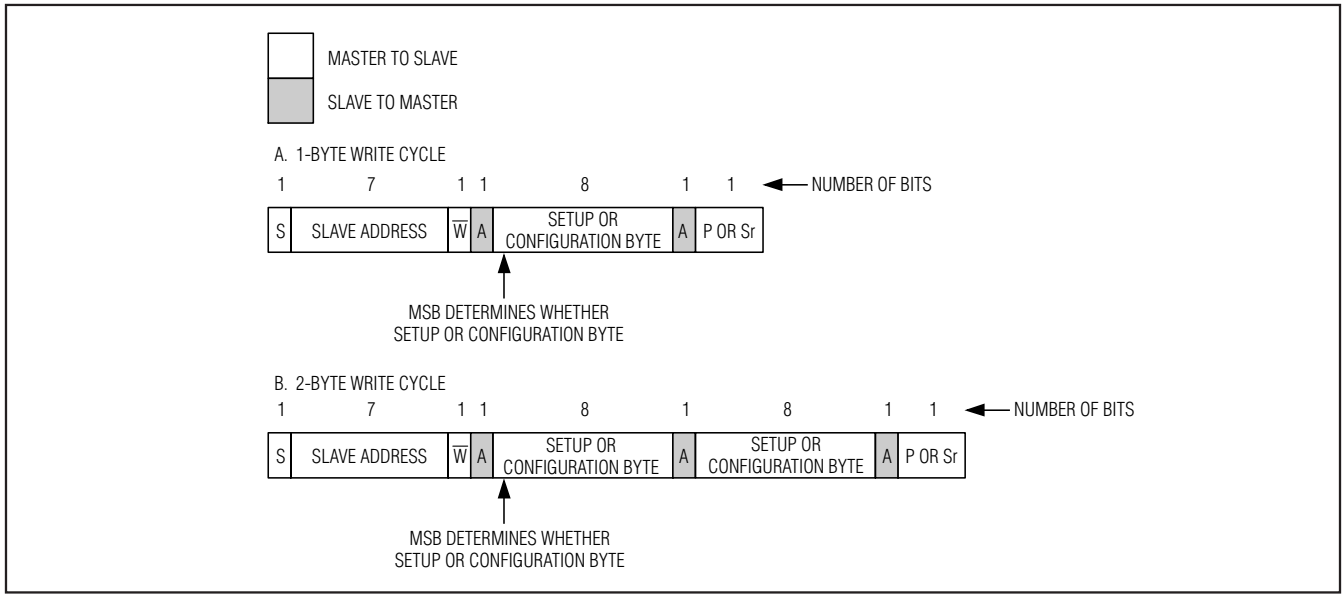

Figure 9. Write Cycle

random access memory (RAM). If the scan mode is set for multiple conversions, they all happen in succession with each additional result being stored in RAM. The MAX11600/MAX11601 contain 8 bytes of RAM, the MAX11602/MAX11603 contain 8 bytes of RAM, and the MAX11604/MAX11605 contain 12 bytes of RAM. Once all conversions are complete, the MAX11600–MAX11605 release SCL, allowing it to be pulled high. The master can now clock the results out of the output shift register at a clock rate of up to 1.7MHz. SCL is stretched for a maximum acquisition and conversion time of 7.6µs per channel (Figure 10).

The device RAM contains all of the conversion results when the MAX11600–MAX11605 release SCL. The converted results are read back in a first-in-first-out (FIFO) sequence. If AIN_/REF is set to be a reference input or output (SEL1 = 1, Table 6), AIN_/REF is excluded from a multichannel scan. This does not apply to the MAX11602/MAX11603 as each provides separate pins for AIN7 and REF. RAM contents can be read continuously. If reading continues past the last result stored in RAM, the pointer wraps around and points to the first result. Note that only the current conversion results are read from memory. The device must be addressed with a read command to obtain new conversion results.

The internal clock mode's clock stretching quiets the SCL bus signal, reducing the system noise during conversion. Using the internal clock also frees the master (typically a microcontroller) from the burden of running the conversion clock.

External Clock

When configured for external clock mode (CLK = 1), the MAX11600–MAX11605 use SCL as the conversion clock. In external clock mode, the MAX11600–MAX11605 begin tracking the analog input on the seventh falling clock edge of a valid slave address byte. One SCL clock cycle later, the analog signal is acquired and the conversion begins. Unlike internal clock mode, converted data is available immediately after the slave-address acknowledge bit. The device continuously converts input channels dictated by the scan mode until given a not acknowledge. There is no need to re-address the device with a read command to obtain new conversion results (Figure 11).

The conversion must complete in 9ms or droop on the T/H capacitor degrades conversion results. Use internal clock mode if the SCL clock period exceeds 1ms.

The MAX11600–MAX11605 must operate in external clock mode for conversion rates up to 188ksps.

Scan Mode

SCAN0 and SCAN1 of the configuration byte set the scan-mode configuration. Table 5 shows the scanning configurations. If AIN_/REF is set to be a reference input or output (SEL1 = 1, Table 6), AIN_/REF is excluded from a multichannel scan. This does not apply to the MAX11602/MAX11603 as each provides separate pins for AIN7 and REF.

Table 2. Configuration Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
REG	SCAN1	SCAN0	CS3	CS2	CS1	CS0	SGL/$\overline{DIF}$

BIT	NAME	DESCRIPTION
7	REG	Register bit. 1 = setup byte (Table 1), 0 = configuration byte.
6	SCAN1	Scan select bits. Two bits select the scanning configuration (Table 5). Default to 00 at power-up.
5	SCAN0	
4	CS3	Channel select bits. Four bits select which analog input channels are to be used for conversion (Tables 3 and 4). Default to 0000 at power-up. For the MAX11600/MAX11601, CS3 and CS2 are internally set to 0. For the MAX11602/MAX11603, CS3 is internally set to zero.
3	CS2	
2	CS1	
1	CS0	
0	SGL/$\overline{DIF}$	1 = single-ended, 0 = pseudo-differential (Tables 3 and 4). Default to 1 at power-up (see the *Single-Ended/Pseudo-Differential Input* section).

Applications Information

Power-On Reset

The configuration and setup registers (Tables 1 and 2) default to a single-ended, unipolar, single-channel conversion on AIN0 using the internal clock with V_{DD} as the reference and AIN_/REF (MAX11600/MAX11601/MAX11604/MAX11605) configured as an analog input. For the MAX11602/MAX11603, the REF pin is floating after power-up. The RAM contents are unknown after power-up.

Automatic Shutdown

SEL[2:0] of the setup byte (Tables 1 and 6) controls the state of the reference and AIN_/REF (MAX11600/MAX11601/MAX11604/MAX11605) or REF (MAX11602/MAX11603). If automatic shutdown is selected (SEL[2:0] = 100), shutdown occurs between conversions when the MAX11600–MAX11605 are idle. When operating in external clock mode, a STOP condition must be issued to place the devices in idle mode and benefit from automatic shutdown. A STOP condition is not necessary in internal clock mode to benefit from automatic shutdown because power-down occurs once all contents are written to memory (Figure 10). All analog circuitry is inactive in shutdown and supply current is less than 1µA. The digital conversion results are maintained in RAM during shutdown and are available for access through the serial interface at any time prior to a STOP or repeated START condition.

When idle, the MAX11600–MAX11605 wait for a START condition followed by their slave address (see the *Slave Address* section). Upon reading a valid address byte, the MAX11600–MAX11605 power up. The analog circuits do not require any wakeup time from shutdown, whether using external or internal reference.

Automatic shutdown results in dramatic power savings, particularly at slow conversion rates. For example, at a conversion rate of 10ksps, the average supply current for the MAX1036 is 8µA and drops to 2µA at 1ksps. At 0.1ksps the average supply current is just 1µA (see Average Supply Current vs. Conversion Rate in the *Typical Operating Characteristics* section).

Reference Voltage

SEL[2:0] of the setup byte (Table 1) controls the reference and the AIN_/REF (MAX11600/MAX11601/MAX11604/MAX11605) or REF (MAX11602/MAX11603) configuration (Table 6). When AIN_/REF (MAX11600/MAX11601/MAX11604/MAX11605) is configured to be a reference input or reference output (SEL1 = 1), conversions on AIN_/REF appear as if AIN_/REF is connected to GND (see note 2 of Tables 3 and 4).

Internal Reference

The internal reference is 4.096V for the MAX11600/MAX11602/MAX11604 and 2.048V for the MAX11601/MAX11603/MAX11605. SEL1 of the setup byte controls whether AIN_/REF (MAX11600/MAX11601/MAX11604/MAX11605) is used for an analog input or a reference (Table 6). When AIN_/REF (MAX11600/MAX11601/MAX11604/MAX11605) or REF (MAX11602/MAX11603) is configured to be an internal reference output (SEL[2:1] = 11), decouple AIN_/REF (MAX11600/MAX11601/MAX11604/MAX11605) or REF (MAX11602/MAX11603) to GND with a 0.01µF capacitor. Due to the decoupling capacitor and the 675Ω reference source impedance, allow 80µs for the reference to stabilize during initial power-up. Once powered up, the reference always remains on until reconfigured. The reference should not be used to supply current for external circuitry. When the MAX11602/MAX11603 is in shutdown, the internal reference output is in a high-impedance state.

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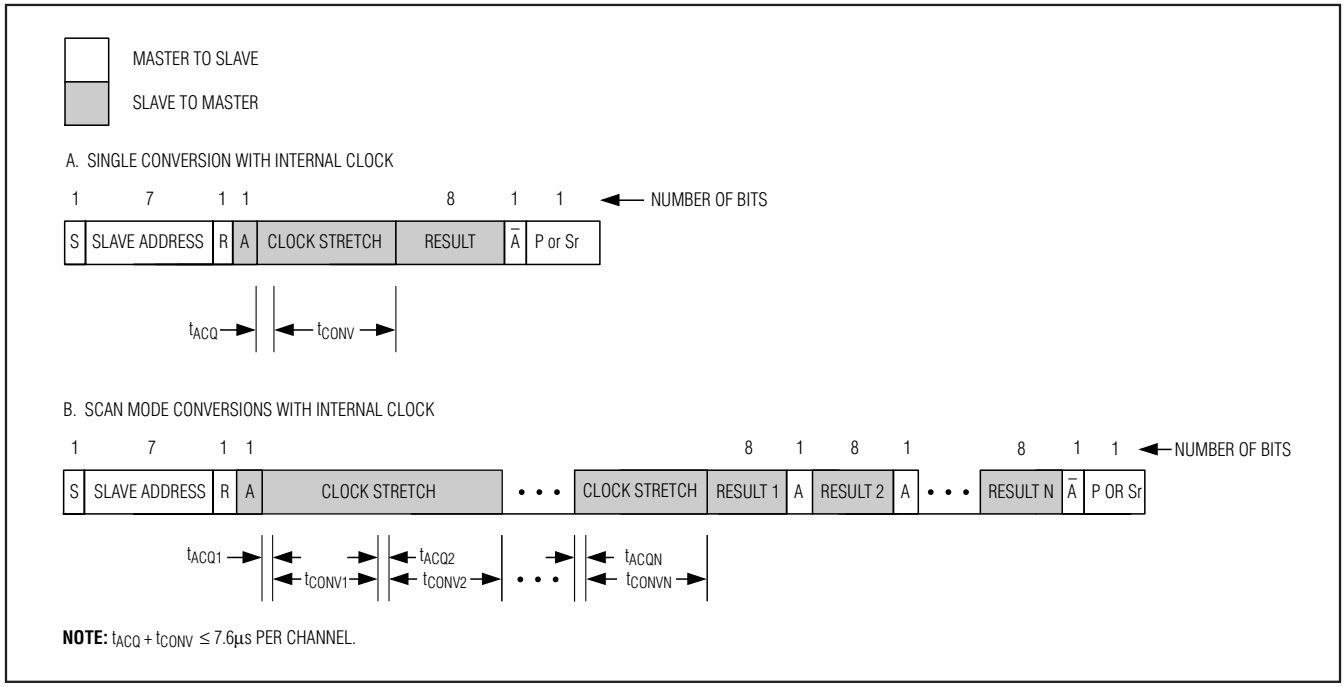

Figure 10. Internal Clock Mode Read Cycles

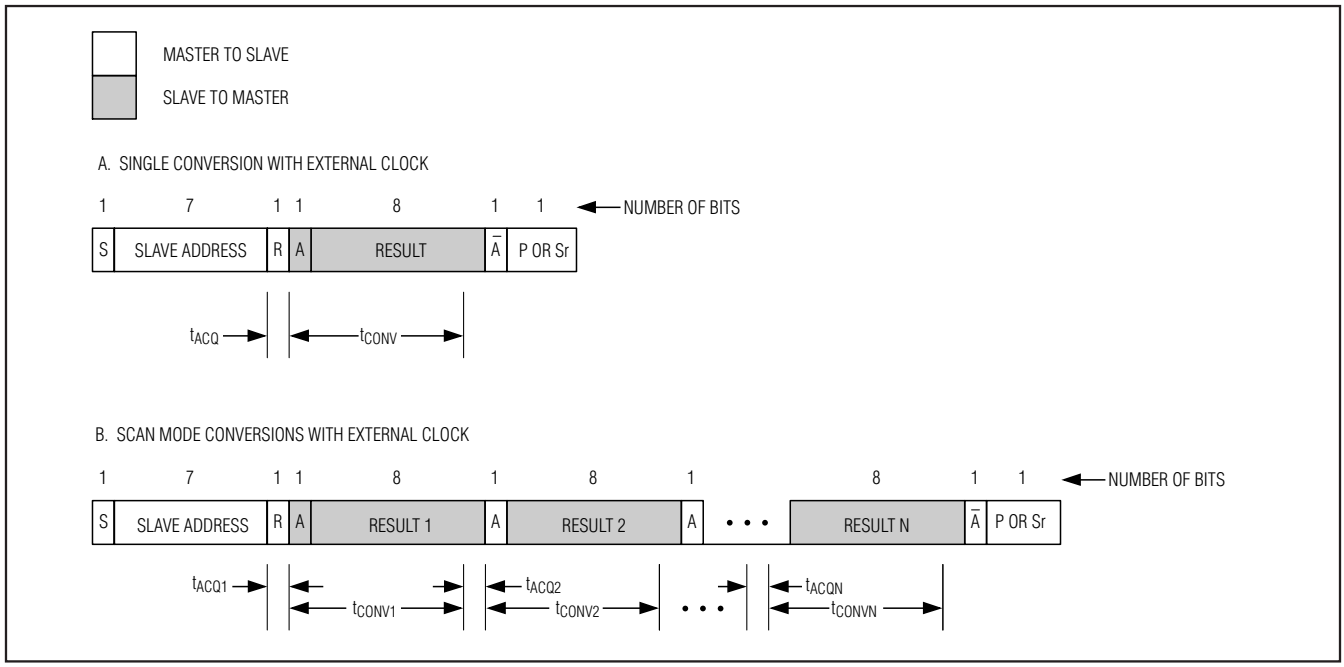

Figure 11. External Clock Mode Read Cycles

Table 3. Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

CS3[1]	CS2[1]	CS1	CS0	AIN0	AIN1	AIN2	AIN3[2]	AIN4	AIN5	AIN6	AIN7	AIN8	AIN9	AIN10	AIN11[2]	GND
0	0	0	0	+												-
0	0	0	1		+											-
0	0	1	0			+										-
0	0	1	1				+									-
0	1	0	0					+								-
0	1	0	1						+							-
0	1	1	0							+						-
0	1	1	1								+					-
1	0	0	0									+				-
1	0	0	1										+			-
1	0	1	0											+		-
1	0	1	1												+	-
1	1	0	0	Reserved												
1	1	0	1	Reserved												
1	1	1	0	Reserved												
1	1	1	1	Reserved												

[1] *For the MAX11600/MAX11601, CS3 and CS2 are internally set to zero. For the MAX11602/MAX11603, CS3 is internally set to zero.*

[2] *When SEL1 = 1, a single-ended read of AIN3/REF (MAX11600/MAX11601) or AIN11/REF (MAX11604/MAX11605) returns GND. This does not apply to the MAX11602/MAX11603 as each provides separate pins for AIN7 and REF.*

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Table 4. Channel Selection in Pseudo-Differential Mode (SGL/$\overline{DIF}$ = 0)[1]

CS3[2]	CS2[2]	CS1	CS0	AIN0	AIN1	AIN2	AIN3[2]	AIN4	AIN5	AIN6	AIN7	AIN8	AIN9	AIN10	AIN11[3]
0	0	0	0	+	-										
0	0	0	1	-	+										
0	0	1	0			+	-								
0	0	1	1			-	+								
0	1	0	0					+	-						
0	1	0	1					-	+						
0	1	1	0							+	-				
0	1	1	1							-	+				
1	0	0	0									+	-		
1	0	0	1									-	+		
1	0	1	0											+	-
1	0	1	1											-	+
1	1	0	0	Reserved											
1	1	0	1	Reserved											
1	1	1	0	Reserved											
1	1	1	1	Reserved											

[1] *When scanning multiple channels (SCAN0 = 0), CS0 = 0 causes the even-numbered channel-select bits to be scanned, while CS0 = 1 causes the odd-numbered channel-select bits to be scanned. For example, if the MAX11604/MAX11605 SCAN[1:0] = 00 and CS[3:0] = 1010, a pseudo-differential read returns AIN0–AIN1, AIN2–AIN3, AIN4–AIN5, AIN6–AIN7, AIN8–AIN9, and AIN10–AIN11. If the MAX11604/MAX11605 SCAN[1:0] = 00 and CS[3:0] = 1011, a pseudo-differential read returns AIN1–AIN0, AIN3–AIN2, AIN5–AIN4, AIN7–AIN6, AIN9–AIN8, and AIN11–AIN10.*

[2] *For the MAX11600/MAX11601, CS3 and CS2 are internally set to zero. For the MAX11602/MAX11603, CS3 is internally set to zero.*

[3] *When SEL1 = 1, a pseudo-differential read between AIN2 and AIN3/REF (MAX11600/MAX11601) or AIN10 and AIN11/REF (MAX11604/MAX11605) returns the difference between GND and AIN2 or AIN10, respectively. For example, a pseudo-differential read of 1011 returns the negative difference between AIN10 and GND. This does not apply to the MAX11602/MAX11603 as each provides separate pins for AIN7 and REF.*

Table 5. Scanning Configuration

SCAN1	SCAN0	SCANNING CONFIGURATION
0	0	Scans up from AIN0 to the input selected by CS3–CS0 (default setting).
0	1	Converts the input selected by CS3–CS0 eight times.*
1	0	**MAX11600/MAX11601: Scans upper half of channels.** Scans up from AIN2 to the input selected by CS1 and CS0. When CS1 and CS0 are set for AIN0, AIN1, and AIN2, the scanning stops at AIN2 (MAX11600/MAX11601).
		MAX11602/MAX11603: Scans upper quartile of channels. Scans up from AIN6 to the input selected by CS3–CS0. When CS3–CS0 is set for AIN0–AIN6, the scanning stops at AIN6 (MAX11602/MAX11603).
		MAX11604/MAX11605: Scans upper half of channels. Scans up from AIN6 to the input selected by CS3–CS0. When CS3–CS0 is set for AIN0–AIN6, the scanning stops at AIN6 (MAX11604/MAX11605).
1	1	Converts the channel selected by CS3–CS0.*

**When operating in external clock mode, there is no difference between SCAN[1:0] = 01 and SCAN[1:0] = 11 and converting continues until a not acknowledge occurs.*

Table 6. Reference Voltage, AIN_/REF, and REF Format

SEL2	SEL1	SEL0	REFERENCE VOLTAGE	AIN_/REF (MAX11600/ MAX11601/ MAX11604/ MAX11605)	REF (MAX11602/ MAX11603)	INTERNAL REFERENCE STATE
0	0	X	V_{DD}	Analog input	Not connected	Always off
0	1	X	External reference	Reference input	Reference input	Always off
1	0	0	Internal reference	Analog input	Not connected	AutoShutdown
1	0	1	Internal reference	Analog input	Not connected	Always on
1	1	X	Internal reference	Reference output	Reference output	Always on

X = Don't care.

External Reference

The external reference can range from 1.0V to V_{DD}. For maximum conversion accuracy, the reference must be able to deliver up to 30µA and have an output impedance of 1kΩ or less. If the reference has a higher output impedance or is noisy, bypass it to GND as close as possible to AIN_/REF (MAX11600/MAX11601/MAX11604/MAX11605) or REF (MAX11602/MAX11603) with a 0.1µF capacitor.

Transfer Functions

Output data coding for the MAX11600–MAX11605 is binary in unipolar mode and two's complement binary in bipolar mode with 1 LSB = $V_{REF}/2^N$ where N is the number of bits (8). Code transitions occur halfway between successive-integer LSB values. Figures 12 and 13 show the input/output (I/O) transfer functions for unipolar and bipolar operations, respectively.

2.7V to 3.6V and 4.5V to 5.5V, Low-Power, 4-/8-/12-Channel 2-Wire Serial 8-Bit ADCs

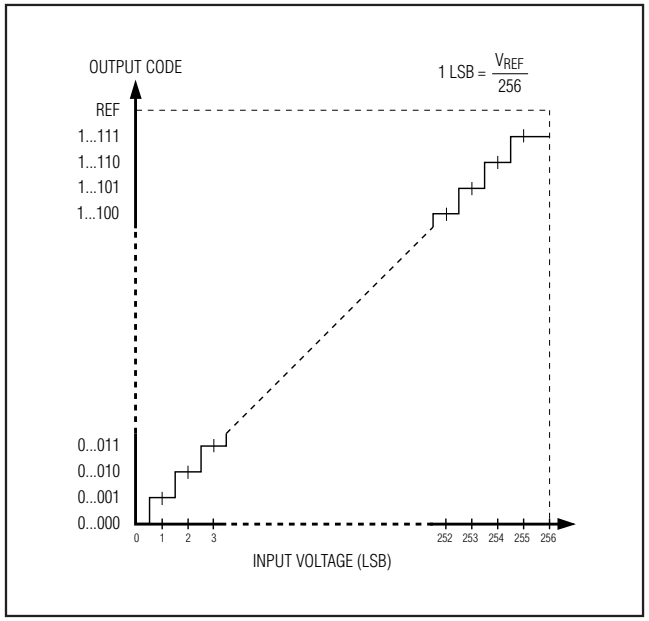


Figure 12. Unipolar Transfer Function

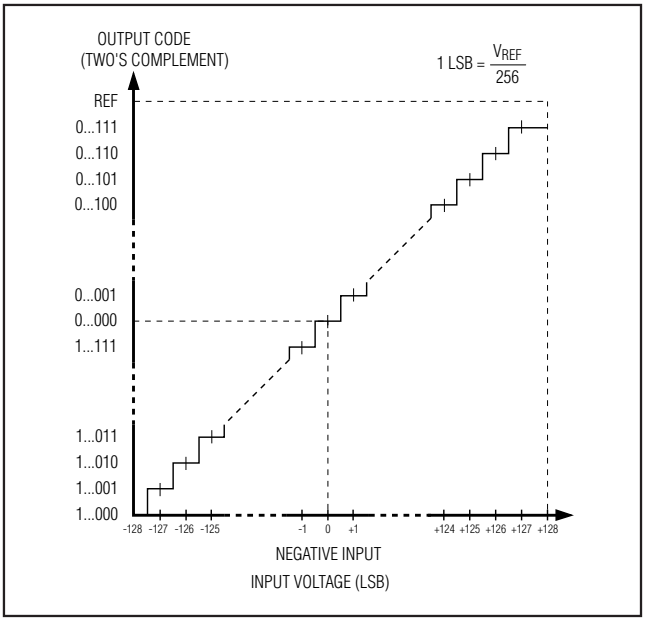


Figure 13. Bipolar Transfer Function

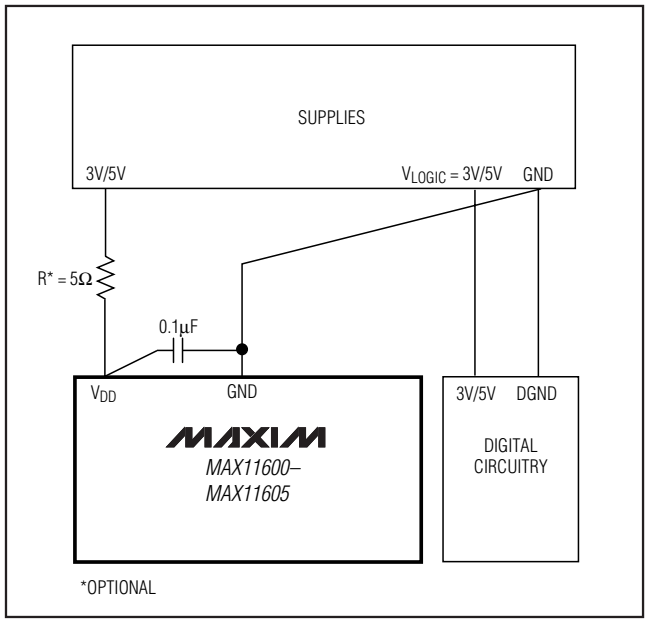


Figure 14. Power-Supply and Grounding Connections

Layout, Grounding, and Bypassing

For best performance, use PC boards. Wire-wrap configurations are not recommended since the layout should ensure proper separation of analog and digital traces. Do not run analog and digital lines parallel to each other, and do not lay out digital signal paths underneath the ADC package. Use separate analog and digital PCB ground sections with only one star point (Figure 14) connecting the two ground systems (analog and digital). For lowest noise operation, ensure the ground return to the star ground's power supply is low impedance and as short as possible. Route digital signals far away from sensitive analog and reference inputs.

High-frequency noise in the power supply (V_{DD}) could influence the proper operation of the ADC's fast comparator. Bypass V_{DD} to the star ground with a 0.1µF capacitor located as close as possible to the MAX11600–MAX11605 power-supply pin. Minimize capacitor lead length for best supply-noise rejection, and add an attenuation resistor (5Ω) if the power supply is extremely noisy.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The INL is measured using the end point method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples.

Aperture Delay

Aperture delay (t_{AD}) is the time between the rising edge of the sampling clock and the instant when an actual sample is taken.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise, including thermal noise, reference noise, clock jitter, etc. Therefore, SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to RMS equivalent of all other ADC output signals.

$$SINAD\ (dB) = 20 \times \log\ (Signal_{RMS}/Noise_{RMS})$$

Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the ADC's full-scale range, calculate the ENOB as follows:

$$ENOB = (SINAD - 1.76)/6.02$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the input signal's first five harmonics to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left(\sqrt{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2\right)}/V_1\right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

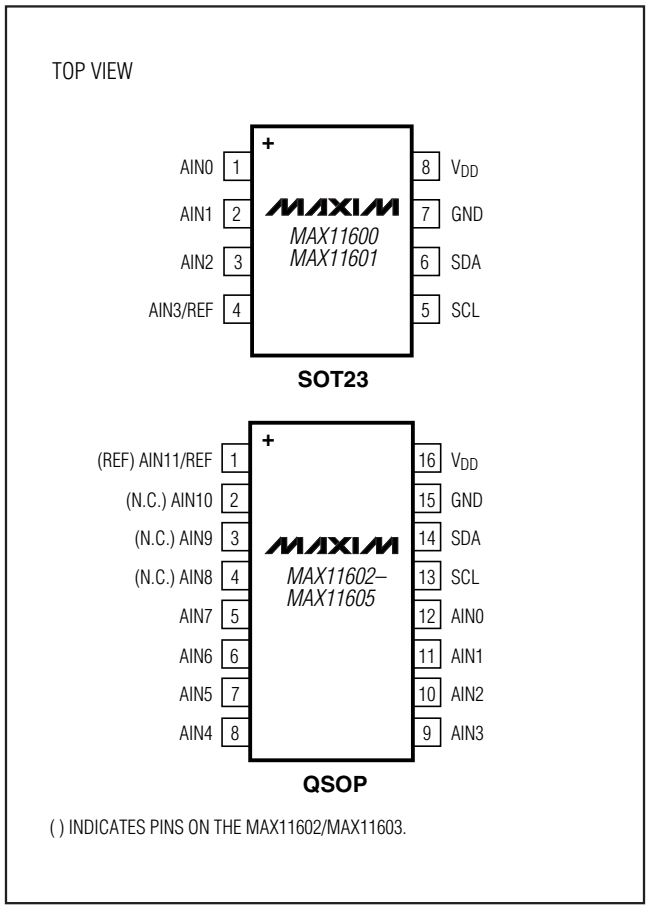
Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest distortion component.

Chip Information

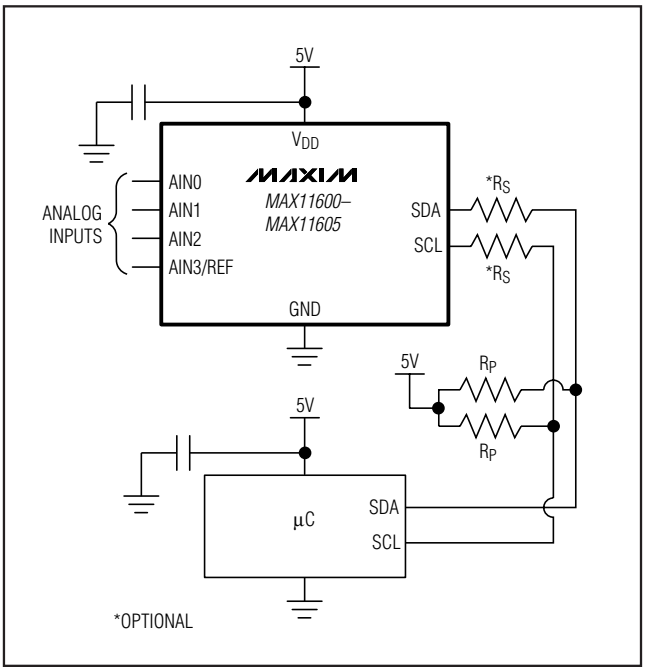
PROCESS: BiCMOS

2.7V to 3.6V and 4.5V to 5.5V, Low-Power, 4-/8-/12-Channel 2-Wire Serial 8-Bit ADCs

Pin Configurations



Typical Operating Circuit



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 SOT23	K8CN+2	**21-0078**
16 QSOP	E16+4	**21-0055**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/09	Introduction of the MAX11600/MAX11601/MAX11603	—
1	7/09	Introduction of the MAX11602/MAX11604/MAX11605	1
2	3/10	Changed top mark on the MAX11600/MAX11601	1