

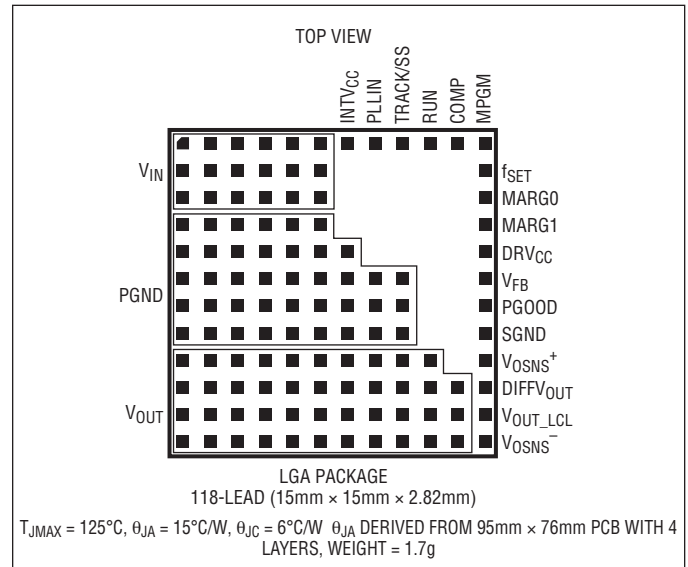
LTM4603HV

ABSOLUTE MAXIMUM RATINGS

(Note 1)

INTV_{CC}, DRV_{CC}, V_{OUT_LCL}, V_{OUT} (V_{OUT} ≤ 3.3V with Remote Sense Amp)..... -0.3V to 6V
PLLIN, TRACK/SS, MPGM, MARG0, MARG1, PGOOD, f_{SET} -0.3V to INTV_{CC} + 0.3V
RUN -0.3V to 5V
V_{FB}, COMP -0.3V to 2.7V
V_{IN} -0.3V to 28V
V_{OSNS}⁺, V_{OSNS}⁻ -0.3V to INTV_{CC} + 0.3V
Operating Temperature Range (Note 2).... -40°C to 85°C
Junction Temperature 125°C
Storage Temperature Range -55°C to 125°C

PIN CONFIGURATION



ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4603HVEV#PBF	Au (RoHS)	LTM4603HV	e4	LGA	3	-40°C to 85°C
LTM4603HVIV#PBF						

- Consult Marketing for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures: www.linear.com/module/pcbassembly
- Terminal Finish Part Marking: www.linear.com/leadfree
- LGA and BGA Package and Tray Drawings: www.linear.com/packaging

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range (Note 2), otherwise specifications are at T_A = 25°C, V_{IN} = 12V, per typical application (front page) configuration, R_{SET} = 40.2k.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V _{IN(DC)}	Input DC Voltage		●	4.5		28	V
V _{OUT(DC)}	Output Voltage	C _{IN} = 10μF ×2, C _{OUT} = 2× 100μF X5R Ceramic V _{IN} = 5V, V _{OUT} = 1.5V, I _{OUT} = 0A V _{IN} = 12V, V _{OUT} = 1.5V, I _{OUT} = 0A	● ●	1.478 1.478	1.5 1.5	1.522 1.522	V V

Input Specifications

V _{IN(UVLO)}	Undervoltage Lockout Threshold	I _{OUT} = 0A		3.2	4	V
I _{INRUSH(VIN)}	Input Inrush Current at Startup	I _{OUT} = 0A. V _{OUT} = 1.5V V _{IN} = 5V V _{IN} = 12V		0.6 0.7		A A

4603hvf

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range (Note 2), otherwise specifications are at $T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, per typical application (front page) configuration, $R_{SET} = 40.2\text{k}$.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$I_{Q(VIN, NOLOAD)}$	Input Supply Bias Current	$V_{IN} = 12\text{V}$, No Switching $V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$, Switching Continuous $V_{IN} = 5\text{V}$, No Switching $V_{IN} = 5\text{V}$, $V_{OUT} = 1.5\text{V}$, Switching Continuous Shutdown, RUN = 0, $V_{IN} = 12\text{V}$		3.8 25 2.5 43 22		mA mA mA mA μA
$I_S(VIN)$	Input Supply Current	$V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$, $I_{OUT} = 6\text{A}$ $V_{IN} = 12\text{V}$, $V_{OUT} = 3.3\text{V}$, $I_{OUT} = 6\text{A}$ $V_{IN} = 5\text{V}$, $V_{OUT} = 1.5\text{V}$, $I_{OUT} = 6\text{A}$		0.92 1.83 2.12		A A A
$INTV_{CC}$	$V_{IN} = 12\text{V}$, RUN > 2V	No Load	4.7	5	5.3	V

Output Specifications

I_{OUTDC}	Output Continuous Current Range	$V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$ (Note 5)		0	6	A
$\frac{\Delta V_{OUT(LINE)}}{V_{OUT}}$	Line Regulation Accuracy	$V_{OUT} = 1.5\text{V}$, $I_{OUT} = 0\text{A}$, $V_{IN} = 4.5\text{V}$ to 28V	●		0.3	%
$\frac{\Delta V_{OUT(LOAD)}}{V_{OUT}}$	Load Regulation Accuracy	$V_{OUT} = 1.5\text{V}$, $I_{OUT} = 0\text{A}$ to 6A, $V_{IN} = 12\text{V}$ with Remote Sense Amp (Note 5)	●		0.25	%
$V_{OUT(AC)}$	Output Ripple Voltage	$I_{OUT} = 0\text{A}$, $C_{OUT} = 2 \times 100\mu\text{F}$ X5R Ceramic $V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$ $V_{IN} = 5\text{V}$, $V_{OUT} = 1.5\text{V}$		10 10		mV _{P-P} mV _{P-P}
f_s	Output Ripple Voltage Frequency	$I_{OUT} = 3\text{A}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$		1000		kHz
$\Delta V_{OUT(START)}$	Turn-On Overshoot	$C_{OUT} = 200\mu\text{F}$ $V_{OUT} = 1.5\text{V}$, $I_{OUT} = 0\text{A}$, TRACK/SS = 10nF $V_{IN} = 12\text{V}$ $V_{IN} = 5\text{V}$		20 20		mV mV
t_{START}	Turn-On Time	$C_{OUT} = 200\mu\text{F}$, TRACK/SS = Open $V_{OUT} = 1.5\text{V}$, $I_{OUT} = 1\text{A}$ Resistive Load $V_{IN} = 12\text{V}$ $V_{IN} = 5\text{V}$		0.5 0.5		ms ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, $C_{OUT} = 2 \times 22\mu\text{F}$ Ceramic, 470 μF 4V Sanyo POSCAP $V_{IN} = 12\text{V}$ $V_{IN} = 5\text{V}$		35 35		mV mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 10% of Full Load $V_{IN} = 12\text{V}$		25		μs
I_{OUTPK}	Output Current Limit	$C_{OUT} = 2 \times 100\mu\text{F}$ X5R Ceramic $V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$ $V_{IN} = 5\text{V}$, $V_{OUT} = 1.5\text{V}$		8 8		A A

Remote Sense Amp (Note 3)

V_{OSNS}^+ , V_{OSNS}^- CM Range	Common Mode Input Voltage Range	$V_{IN} = 12\text{V}$, RUN > 2V		0	$INTV_{CC} - 1$	V
$DIFFV_{OUT}$ Range	Output Voltage Range	$V_{IN} = 12\text{V}$, $DIFFV_{OUT}$ Load = 100k		0	$INTV_{CC} - 1$	V
V_{OS}	Input Offset Voltage Magnitude				1.25	mV
AV	Differential Gain				1	V/V
GBP	Gain Bandwidth Product				3	MHz
SR	Slew Rate				2	V/ μs
R_{IN}	Input Resistance	V_{OSNS}^+ to GND			20	k Ω
CMRR	Common Mode Rejection Ratio				100	dB

LTM4603HV

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range (Note 2), otherwise specifications are at $T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, per typical application (front page) configuration, $R_{SET} = 40.2\text{k}$.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Control Stage							
V_{FB}	Error Amplifier Input Voltage Accuracy	$I_{OUT} = 0\text{A}$, $V_{OUT} = 1.5\text{V}$	●	0.594	0.6	0.606	V
V_{RUN}	RUN Pin On/Off Threshold			1	1.5	1.9	V
$I_{TRACK/SS}$	Soft-Start Charging Current	$V_{TRACK/SS} = 0\text{V}$		-1	-1.5	-2	μA
$t_{ON(MIN)}$	Minimum On Time	(Note 4)			50	100	ns
$t_{OFF(MIN)}$	Minimum Off Time	(Note 4)			250	400	ns
R_{PLLIN}	PLLIN Input Resistance				50		$\text{k}\Omega$
I_{DRVCC}	Current into DRV_{CC} Pin	$V_{OUT} = 1.5\text{V}$, $I_{OUT} = 1\text{A}$, $DRV_{CC} = 5\text{V}$			18	25	mA
R_{FBHI}	Resistor Between V_{OUT_LCL} and V_{FB}			60.098	60.4	60.702	$\text{k}\Omega$
V_{MPGM}	Margin Reference Voltage				1.18		V
V_{MARG0} , V_{MARG1}	MARG0, MARG1 Voltage Thresholds				1.4		V
PGOOD Output							
ΔV_{FBH}	PGOOD Upper Threshold	V_{FB} Rising		7	10	13	%
ΔV_{FBL}	PGOOD Lower Threshold	V_{FB} Falling		-7	-10	-13	%
$\Delta V_{FB(HYS)}$	PGOOD Hysteresis	V_{FB} Returning (Note 4)			1.5	3	%
V_{PGL}	PGOOD Low Voltage	$I_{PGOOD} = 5\text{mA}$			0.15	0.4	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4603HV is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4603HVEV is guaranteed to meet performance specifications from 0°C to 85°C . Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4603HVIV is guaranteed over the -40°C to 85°C operating temperature range.

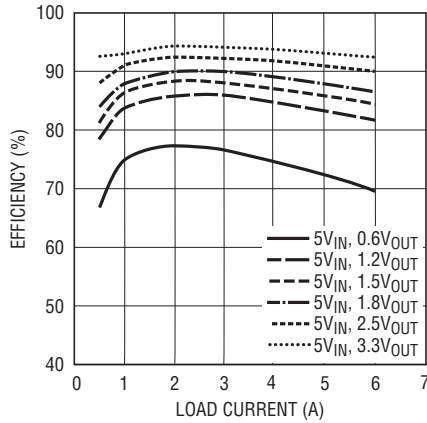
Note 3: Remote sense amplifier recommended for $\leq 3.3\text{V}$ output.

Note 4: 100% tested at die level only.

Note 5: See output current derating curves for different V_{IN} , V_{OUT} and T_A .

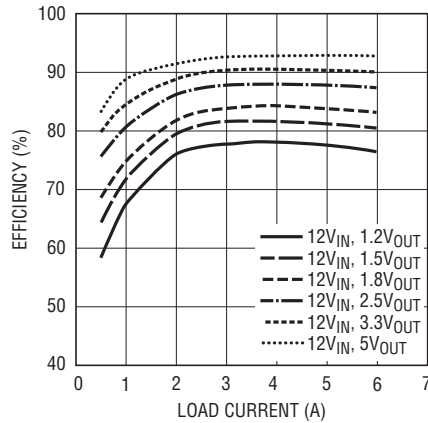
TYPICAL PERFORMANCE CHARACTERISTICS (See Figure 20 for all curves)

Efficiency vs Load Current with 5V_{IN}



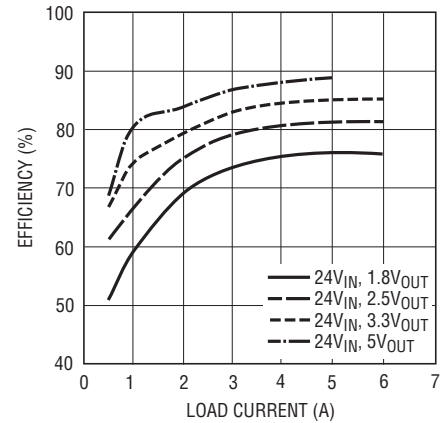
4603HV G01

Efficiency vs Load Current with 12V_{IN}



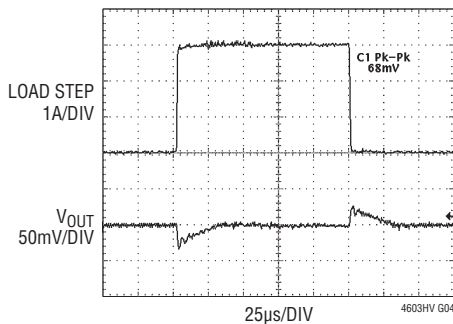
4603HV G02

Efficiency vs Load Current with 24V_{IN}



4603HV G03

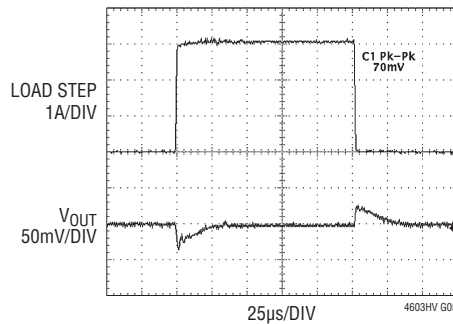
1.2V Transient Response



4603HV G04

1.2V AT 3A/μs LOAD STEP
C_{OUT}: 1x 22μF, 6.3V CERAMIC
1x 330μF, 4V SANYO POSCAP

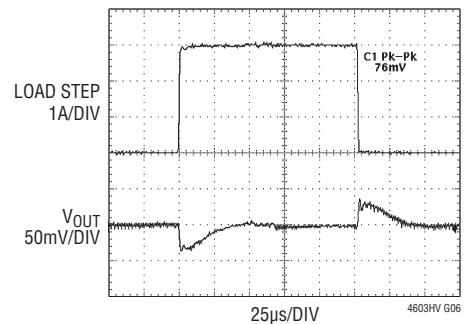
1.5V Transient Response



4603HV G05

1.5V AT 3A/μs LOAD STEP
C_{OUT}: 1x 22μF, 6.3V CERAMIC
1x 330μF, 4V SANYO POSCAP

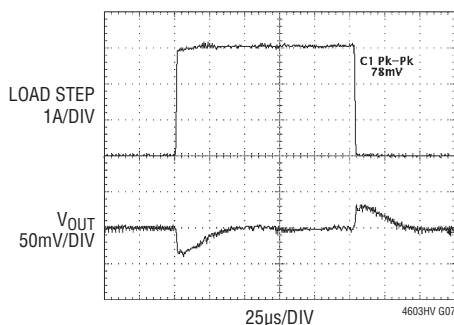
1.8V Transient Response



4603HV G06

1.8V AT 3A/μs LOAD STEP
C_{OUT}: 1x 22μF, 6.3V CERAMIC
1x 330μF, 4V SANYO POSCAP

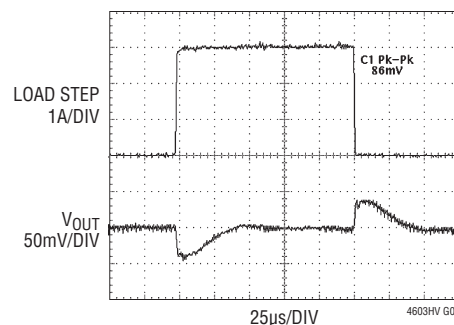
2.5V Transient Response



4603HV G07

2.5V AT 3A/μs LOAD STEP
C_{OUT}: 1x 22μF, 6.3V CERAMIC
1x 330μF, 4V SANYO POSCAP

3.3V Transient Response

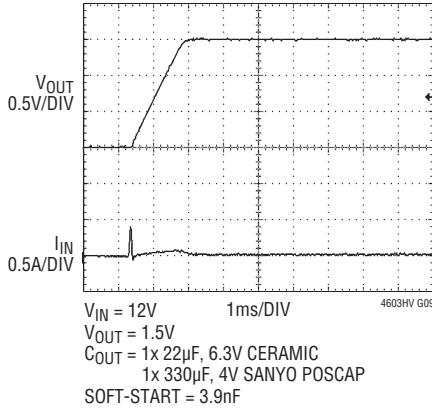


4603HV G08

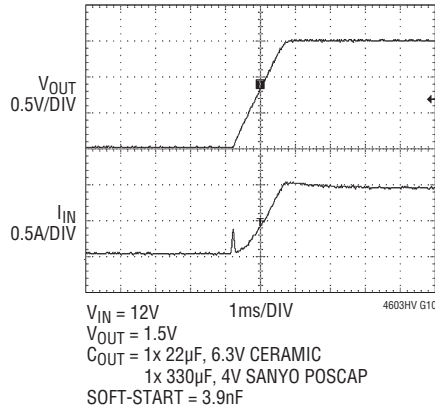
3.3V AT 3A/μs LOAD STEP
C_{OUT}: 1x 22μF, 6.3V CERAMIC
1x 330μF, 4V SANYO POSCAP

TYPICAL PERFORMANCE CHARACTERISTICS (See Figure 20 for all curves)

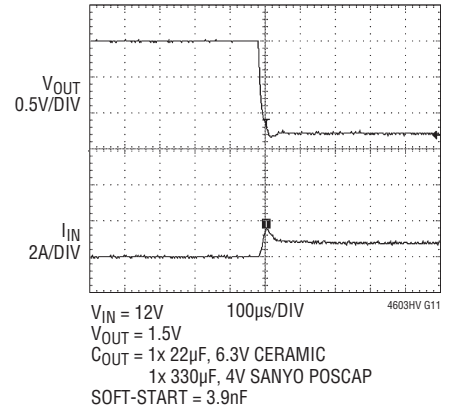
Start-Up, $I_{OUT} = 0A$



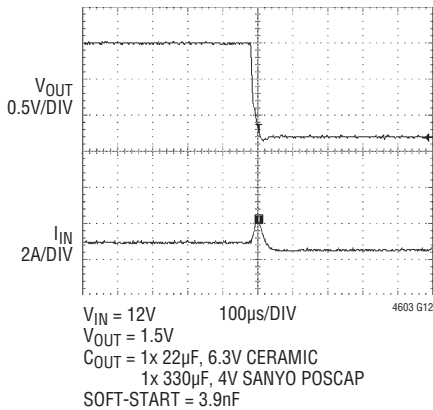
**Start-Up, $I_{OUT} = 6A$
(Resistive Load)**



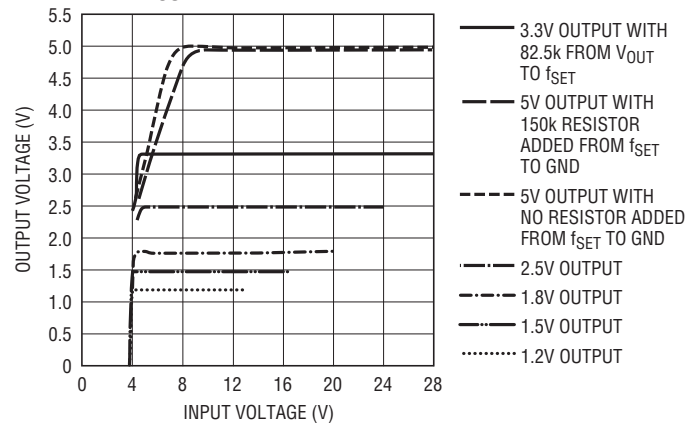
**Short-Circuit Protection,
 $I_{OUT} = 0A$**



**Short-Circuit Protection,
 $I_{OUT} = 6A$**



V_{IN} to V_{OUT} Step-Down Ratio



4603HV G13

PIN FUNCTIONS (See Package Description for Pin Assignment)

V_{IN} (Bank 1): Power Input Pins. Apply input voltage between these pins and PGND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and PGND pins.

V_{OUT} (Bank 3): Power Output Pins. Apply output load between these pins and PGND pins. Recommend placing output decoupling capacitance directly between these pins and PGND pins. See Figure 17.

PGND (Bank 2): Power ground pins for both input and output returns.

V_{OSNS}⁻ (Pin M12): (-) Input to the Remote Sense Amplifier. This pin connects to the ground remote sense point. The remote sense amplifier is used for V_{OUT} ≤ 3.3V. Tie to INTV_{CC} if not used.

V_{OSNS}⁺ (Pin J12): (+) Input to the Remote Sense Amplifier. This pin connects to the output remote sense point. The remote sense amplifier is used for V_{OUT} ≤ 3.3V. Tie to ground if not used.

DIFFV_{OUT} (Pin K12): Output of the Remote Sense Amplifier. This pin connects to the V_{OUT_LCL} pin. Leave floating if remote sense amplifier is not used.

DRV_{CC} (Pin E12): This pin normally connects to INTV_{CC} for powering the internal MOSFET drivers. This pin can be biased up to 6V from an external supply with about 50mA capability, or an external circuit shown in Figure 18. This improves efficiency at the higher input voltages by reducing power dissipation in the module.

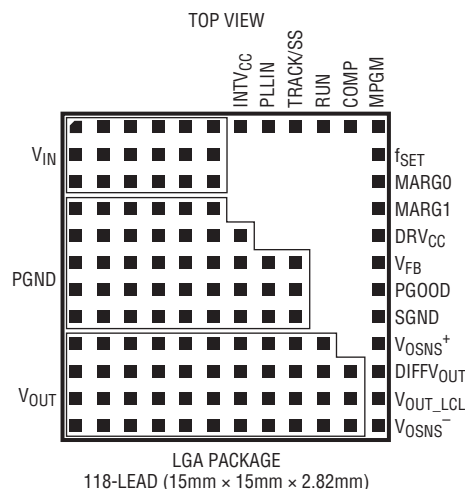
INTV_{CC} (Pin A7): This pin is for additional decoupling of the 5V internal regulator.

PLLIN (Pin A8): External Clock Synchronization Input to the Phase Detector. This pin is internally terminated to SGND with a 50k resistor. Apply a clock with a high level above 2V and below INTV_{CC}. See the Applications Information section.

TRACK/SS (Pin A9): Output Voltage Tracking and Soft-Start Pin. When the module is configured as a master output, then a soft-start capacitor is placed on this pin to ground to control the master ramp rate. A soft-start capacitor can be used for soft-start turn on as a stand alone regulator. Slave operation is performed by putting a resistor divider from the master output to ground, and connecting the center point of the divider to this pin. See the Applications Information section.

MPGM (Pin A12): Programmable Margining Input. A resistor from this pin to ground sets a current that is equal to 1.18V/R. This current multiplied by 10kΩ will equal a value in millivolts that is a percentage of the 0.6V reference voltage. See the Applications Information section. To parallel LTM4603HVs, each requires an individual MPGM resistor. Do not tie MPGM pins together.

f_{SET} (Pin B12): Frequency Set Internally to 1MHz. An external resistor can be placed from this pin to ground to increase frequency. See the Applications Information section for frequency adjustment.



PIN FUNCTIONS (See Package Description for Pin Assignment)

V_{FB} (Pin F12): The Negative Input of the Error Amplifier. Internally, this pin is connected to V_{OUT_LCL} with a 60.4k precision resistor. Different output voltages can be programmed with an additional resistor between V_{FB} and SGND pins. See the Applications Information section.

MARG0 (Pin C12): This pin is the LSB logic input for the margining function. Together with the MARG1 pin will determine if margin high, margin low or no margin state is applied. The pin has an internal pull-down resistor of 50k. See the Applications Information section.

MARG1 (Pin D12): This pin is the MSB logic input for the margining function. Together with the MARG0 pin will determine if margin high, margin low or no margin state is applied. The pin has an internal pull-down resistor of 50k. See the Applications Information section.

SGND (Pin H12): Signal Ground. This pin connects to PGND at output capacitor point.

COMP (Pin A11): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V with 0.7V corresponding to zero sense voltage (zero current).

PGOOD (Pin G12): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is not within $\pm 10\%$ of the regulation point, after a 25 μ s power bad mask timer expires.

RUN (Pin A10): Run Control Pin. A voltage above 1.9V will turn on the module, and when below 1V, will turn off the module. A programmable UVLO function can be accomplished by connecting to a resistor divider from V_{IN} to ground. See Figure 1. This pin has a 5.1V Zener to ground. Maximum pin voltage is 5V. Limit current into the RUN pin to less than 1mA.

V_{OUT_LCL} (Pin L12): V_{OUT} connects directly to this pin to bypass the remote sense amplifier, or DIFFV_{OUT} connects to this pin when remote sense amplifier is used.

OPERATION

Power Module Description

The LTM4603HV is a standalone nonisolated switching mode DC/DC power supply. It can deliver up to 6A of DC output current with few external input and output capacitors. This module provides precisely regulated output voltage programmable via one external resistor from $0.6V_{DC}$ to $5.0V_{DC}$ over a 4.5V to 28V wide input voltage. The typical application schematic is shown in Figure 20.

The LTM4603HV has an integrated constant on-time current mode regulator, ultralow $R_{DS(ON)}$ FETs with fast switching speed and integrated Schottky diodes. The typical switching frequency is 1MHz at full load. With current mode control and internal feedback loop compensation, the LTM4603HV module has sufficient stability margins and good transient performance under a wide range of operating conditions and with a wide range of output capacitors, even all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit. Besides, foldback current limiting is provided in an overcurrent condition while V_{FB} drops. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a $\pm 10\%$ window around the regulation point. Furthermore,

in an overvoltage condition, internal top FET Q1 is turned off and bottom FET Q2 is turned on and held on until the overvoltage condition clears.

Pulling the RUN pin below 1V forces the controller into its shutdown state, turning off both Q1 and Q2. At low load current, the module works in continuous current mode by default to achieve minimum output voltage ripple.

When DRV_{CC} pin is connected to $INTV_{CC}$ an integrated 5V linear regulator powers the internal gate drivers. If a 5V external bias supply is applied on the DRV_{CC} pin, then an efficiency improvement will occur due to the reduced power loss in the internal linear regulator. This is especially true at the higher input voltage range.

The LTM4603HV has a very accurate differential remote sense amplifier with very low offset. This provides for very accurate output voltage sensing at the load. The MPGM pin, MARG0 pin and MARG1 pin are used to support voltage margining, where the percentage of margin is programmed by the MPGM pin, and the MARG0 and MARG1 select margining.

The PLLIN pin provides frequency synchronization of the device to an external clock. The TRACK/SS pin is used for power supply tracking and soft-start programming.

APPLICATIONS INFORMATION

The typical LTM4603HV application circuit is shown in Figure 20. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 2 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} step down ratio that can be achieved for a given input voltage. These constraints are shown in the Typical Performance Characteristics curves labeled V_{IN} to V_{OUT} Step-Down Ratio. Note that additional thermal derating may apply. See the Thermal Considerations and Output Current Derating section of this data sheet.

Output Voltage Programming and Margining

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 1M and a 60.4k 0.5% internal feedback resistor connects V_{OUT} and V_{FB} pins together. The V_{OUT_LCL} pin is connected between the 1M and the 60.4k resistor. The 1M resistor is used to protect against an output overvoltage condition if the V_{OUT_LCL} pin is not connected to the output, or if the remote sense amplifier output is not connected to V_{OUT_LCL} . The output voltage will default to 0.6V. Adding a resistor R_{SET} from the V_{FB} pin to SGND pin programs the output voltage:

$$V_{OUT} = 0.6V \frac{60.4k + R_{SET}}{R_{SET}}$$

Table 1. R_{SET} Standard 1% Resistor Values vs V_{OUT}

R_{SET} (k Ω)	Open	60.4	40.2	30.1	25.5	19.1	13.3	8.25
V_{OUT} (V)	0.6	1.2	1.5	1.8	2	2.5	3.3	5

The MPGM pin programs a current that when multiplied by an internal 10k resistor sets up the 0.6V reference $\pm$ offset for margining. A 1.18V reference divided by the R_{PGM} resistor on the MPGM pin programs the current. Calculate $V_{OUT(MARGIN)}$:

$$V_{OUT(MARGIN)} = \frac{\%V_{OUT}}{100} \cdot V_{OUT}$$

where $\%V_{OUT}$ is the percentage of V_{OUT} you want to margin, and $V_{OUT(MARGIN)}$ is the margin quantity in volts:

$$R_{PGM} = \frac{V_{OUT}}{0.6V} \cdot \frac{1.18V}{V_{OUT(MARGIN)}} \cdot 10k$$

where R_{PGM} is the resistor value to place on the MPGM pin to ground.

The margining voltage, $V_{OUT(MARGIN)}$, will be added or subtracted from the nominal output voltage as determined by the state of the MARG0 and MARG1 pins. See the truth table below:

MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

Input Capacitors

LTM4603HV module should be connected to a low AC impedance DC source. Input capacitors are required to be placed adjacent to the module. In Figure 20, the 10 μ F ceramic input capacitors are selected for their ability to handle the large RMS current into the converter. An input bulk capacitor of 100 μ F is optional. This 100 μ F capacitor is only needed if the input source impedance is compromised by long inductive leads or traces.

For a buck converter, the switching duty-cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor ripple current, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \cdot \sqrt{D \cdot (1-D)}$$

In the above equation, $\eta\%$ is the estimated efficiency of the power module. C_{IN} can be a switcher-rated electrolytic aluminum capacitor, OS-CON capacitor or high value ceramic capacitor. Note the capacitor ripple current ratings

APPLICATIONS INFORMATION

are often based on temperature and hours of life. This makes it advisable to properly derate the input capacitor, or choose a capacitor rated at a higher temperature than required. Always contact the capacitor manufacturer for derating requirements.

In Figure 20, the 10 μ F ceramic capacitors are together used as a high frequency input decoupling capacitor. In a typical 6A output application, two very low ESR, X5R or X7R, 10 μ F ceramic capacitors are recommended. These decoupling capacitors should be placed directly adjacent to the module input pins in the PCB layout to minimize the trace inductance and high frequency AC noise. Each 10 μ F ceramic is typically good for 2A to 3A of RMS ripple current. Refer to your ceramics capacitor catalog for the RMS current ratings.

Multiphase operation with multiple LTM4603HV devices in parallel will lower the effective input RMS ripple current due to the interleaving operation of the regulators. Application Note 77 provides a detailed explanation. Refer to Figure 2 for the input capacitor ripple current requirement as a function of the number of phases. The figure provides a ratio of RMS ripple current to DC load current as a function of duty cycle and the number of paralleled phases. Pick the corresponding duty cycle and the number of phases to arrive at the correct ripple current value. For example, the 2-phase parallel LTM4603HV design provides 10A at 2.5V output from a 12V input. The duty cycle is $DC = 2.5V/12V = 0.21$. The 2-phase curve has a ratio of ~ 0.25 for a duty cycle of 0.21. This 0.25 ratio of RMS ripple current to a

DC load current of 10A equals $\sim 2.5A$ of input RMS ripple current for the external input capacitors.

Output Capacitors

The LTM4603HV is designed for low output ripple voltage. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output ripple voltage and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor or a ceramic capacitor. The typical capacitance is 200 μ F if all ceramic output capacitors are used. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spikes is required. Table 2 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 3A/ μ s transient. The table optimizes total equivalent ESR and total bulk capacitance to maximize transient performance.

Multiphase operation with multiple LTM4603HV devices in parallel will lower the effective output ripple current due to the interleaving operation of the regulators. For example, each LTM4603HV's inductor current in a 12V to 2.5V multiphase design can be read from the Inductor Ripple Current vs Duty Cycle graph (Figure 3). The large ripple current at low duty cycle and high output voltage can be reduced by adding an external resistor from f_{SET} to ground which increases the frequency. If we choose the duty cycle of $DC = 2.5V/12V = 0.21$, the inductor ripple current for 2.5V output at 21% duty cycle is $\sim 2A$ in Figure 3.

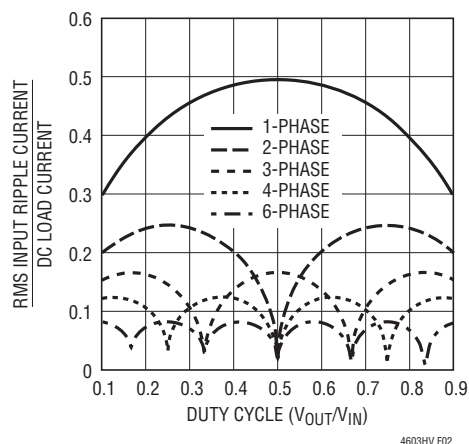


Figure 2. Normalized Input RMS Ripple Current vs Duty Cycle for One to Six Modules (Phases)

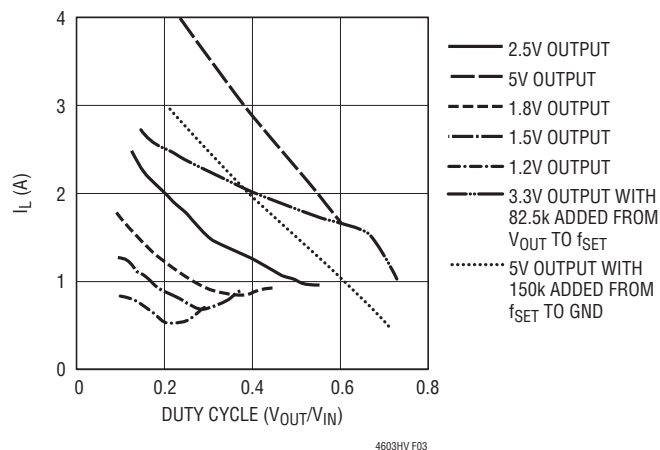


Figure 3. Inductor Ripple Current vs Duty Cycle

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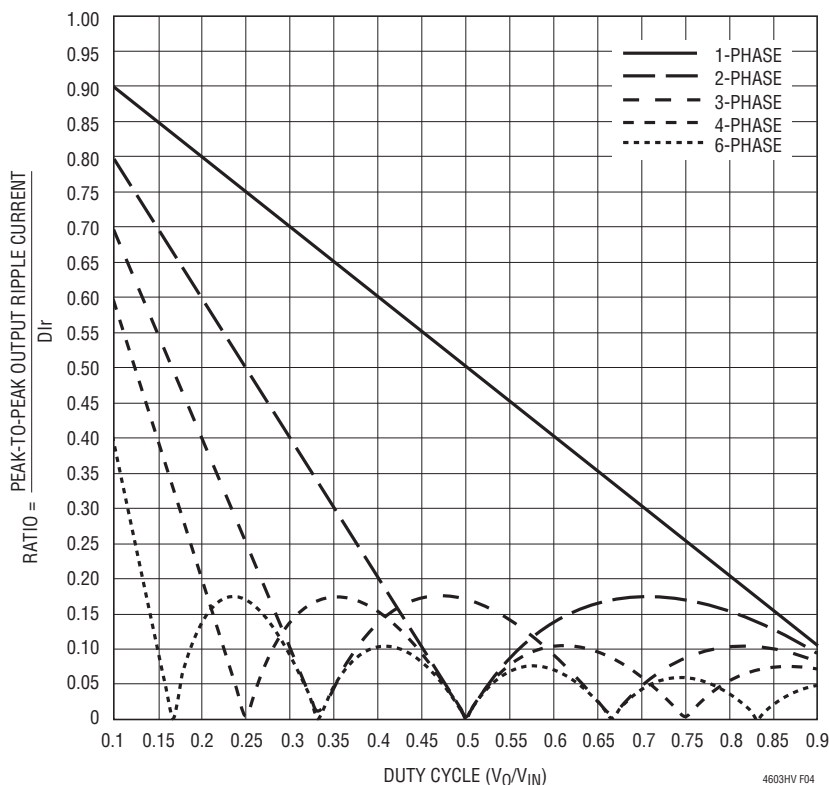


Figure 4. Normalized Output Ripple Current vs Duty Cycle, $D_{lr} = V_O T/L_I$

Figure 4 provides a ratio of peak-to-peak output ripple current to the inductor current as a function of duty cycle and the number of paralleled phases. Pick the corresponding duty cycle and the number of phases to arrive at the correct output ripple current ratio value. If a 2-phase operation is chosen at a duty cycle of 21%, then 0.6 is the ratio. This 0.6 ratio of output ripple current to inductor ripple of 2A equals 1.2A of effective output ripple current. Refer to Application Note 77 for a detailed explanation of output ripple current reduction as a function of paralleled phases.

The output ripple voltage has two components that are related to the amount of bulk capacitance and effective series resistance (ESR) of the output bulk capacitance. Therefore, the output ripple voltage can be calculated with the known effective output ripple current. The equation: $\Delta V_{OUT(P-P)} \approx (\Delta I_L / (8 \cdot f \cdot m \cdot C_{OUT}) + ESR \cdot \Delta I_L)$, where f is frequency and m is the number of parallel phases. This calculation process can be easily accomplished by using LTpowerCAD™.

Fault Conditions: Current Limit and Overcurrent Foldback

The LTM4603HV has a current mode controller, which inherently limits the cycle-by-cycle inductor current not only in steady-state operation, but also in response to transients.

To further limit current in the event of an overload condition, the LTM4603HV provides foldback current limiting. If the output voltage falls by more than 50%, then the maximum output current is progressively lowered to about one sixth of its full current limit value.

Soft-Start and Tracking

The TRACK/SS pin provides a means to either soft-start the regulator or track it to a different power supply. A capacitor on this pin will program the ramp rate of the output voltage. A 1.5μA current source will charge up the external soft-start capacitor to 80% of the 0.6V internal

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voltage reference minus any margin delta. This will control the ramp of the internal reference and the output voltage. The total soft-start time can be calculated as:

$$t_{\text{SOFTSTART}} = 0.8 \cdot (0.6V \pm V_{\text{OUT(MARGIN)}}) \cdot \frac{C_{\text{SS}}}{1.5\mu\text{A}}$$

When the RUN pin falls below 1.5V, then the TRACK/SS pin is reset to allow for proper soft-start control when the regulator is enabled again. Current foldback and forced continuous mode are disabled during the soft-start process. The soft-start function can also be used to control the output ramp up time, so that another regulator can be easily tracked to it.

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider. Figure 5 shows an example of coincident tracking. Ratiometric modes of tracking can be achieved by selecting different resistor values to change the output tracking ratio. The master output must be greater than the slave output for the tracking to work. Figure 6 shows the coincident output tracking characteristics.

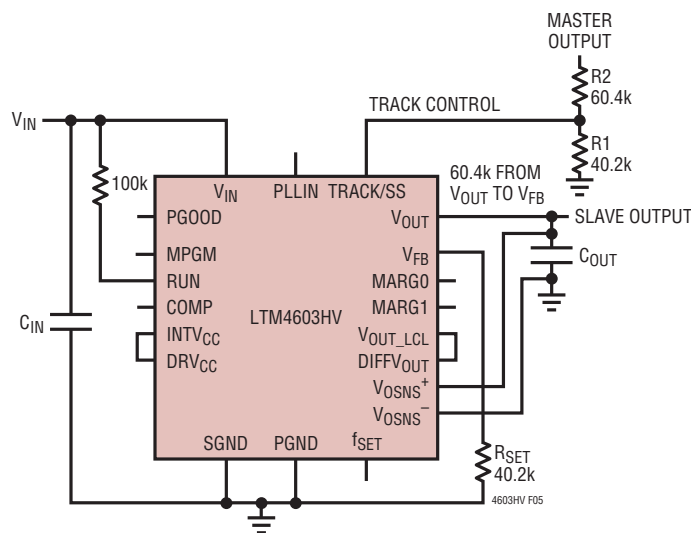


Figure 5. Coincident Tracking Schematic

Run Enable

The RUN pin is used to enable the power module. The pin has an internal 5.1V Zener to ground. The pin can be driven with a logic input not to exceed 5V.

The RUN pin can also be used as an undervoltage lock out (UVLO) function by connecting a resistor divider from the input supply to the RUN pin:

$$V_{\text{UVLO}} = \frac{R1+R2}{R2} \cdot 1.5V$$

See the Simplified Block Diagram (Figure 1).

Power Good

The PGOOD pin is an open-drain pin that can be used to monitor valid output voltage regulation. This pin monitors a $\pm 10\%$ window around the regulation point and tracks with margining.

COMP Pin

This pin is the external compensation pin. The module has already been internally compensated for most output voltages. Table 2 is provided for most application requirements. LTpowerCAD is available for control loop optimization.

PLLIN

The power module has a phase-locked loop comprised of an internal voltage controlled oscillator and a phase detector. This allows the internal top MOSFET turn-on

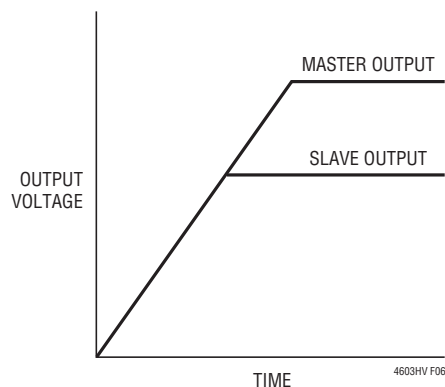


Figure 6. Coincident Output Tracking Characteristics

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to be locked to the rising edge of the external clock. The frequency range is $\pm 30\%$ around the operating frequency of 1MHz. A pulse detection circuit is used to detect a clock on the PLLIN pin to turn on the phase-locked loop. The pulse width of the clock has to be at least 400ns and the amplitude at least 2V. The PLLIN pin must be driven from a low impedance source such as a logic gate located close to the pin. During start-up of the regulator, the phase-locked loop function is disabled.

INTV_{CC} and DRV_{CC} Connection

An internal low dropout regulator produces an internal 5V supply that powers the control circuitry and DRV_{CC} for driving the internal power MOSFETs. Therefore, if the system does not have a 5V power rail, the LTM4603HV can be directly powered by V_{IN}. The gate driver current through the LDO is about 20mA. The internal LDO power dissipation can be calculated as:

$$P_{LDO_LOSS} = 20\text{mA} \cdot (V_{IN} - 5\text{V})$$

The LTM4603HV also provides the external gate driver voltage pin DRV_{CC}. If there is a 5V rail in the system, it is recommended to connect DRV_{CC} pin to the external 5V rail. This is especially true for higher input voltages. Do not apply more than 6V to the DRV_{CC} pin. A 5V output can be used to power the DRV_{CC} pin with an external circuit as shown in Figure 18.

Parallel Operation of the Module

The LTM4603HV device is an inherently current mode controlled device. Parallel modules will have very good current sharing. This will balance the thermals on the design. The voltage feedback equation changes with the variable n as modules are paralleled:

$$V_{OUT} = 0.6\text{V} \frac{\frac{60.4\text{k}}{n} + R_{SET}}{R_{SET}}$$

n is the number of paralleled modules.

Thermal Considerations and Output Current Derating

The power loss curves in Figures 7 and 8 can be used in coordination with the load current derating curves in Figures 9 to 12, and Figures 13 to 16 for calculating an approximate θ_{JA} for the module with various heat sinking methods. Thermal models are derived from several temperature measurements at the bench and thermal modeling analysis. Thermal Application Note 103 provides a detailed explanation of the analysis for the thermal models and the derating curves. Tables 3 and 4 provide a summary of the equivalent θ_{JA} for the noted conditions. These equivalent θ_{JA} parameters are correlated to the measured values, and are improved with air flow. The case temperature is maintained at 100°C or below for the derating curves.

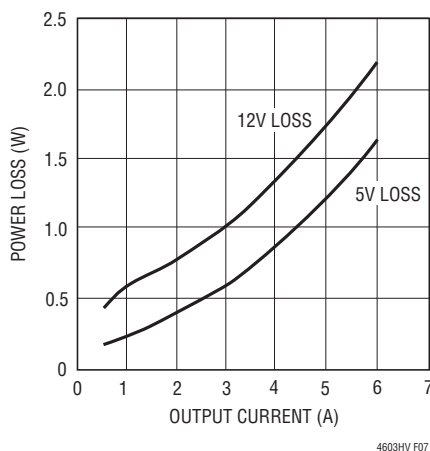


Figure 7. 1.5V Power Loss

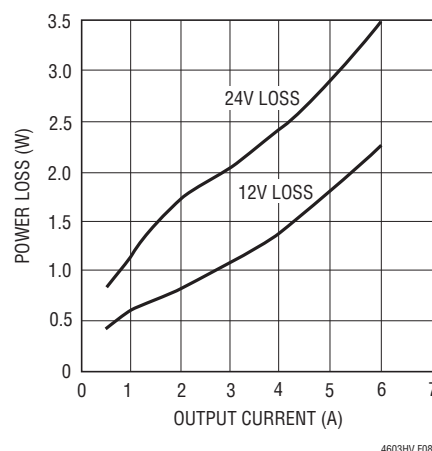


Figure 8. 3.3V Power Loss

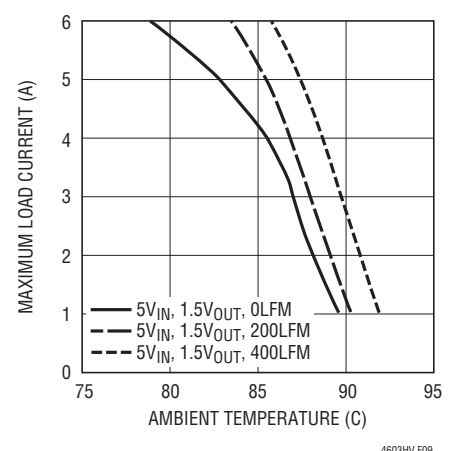


Figure 9. No Heat Sink

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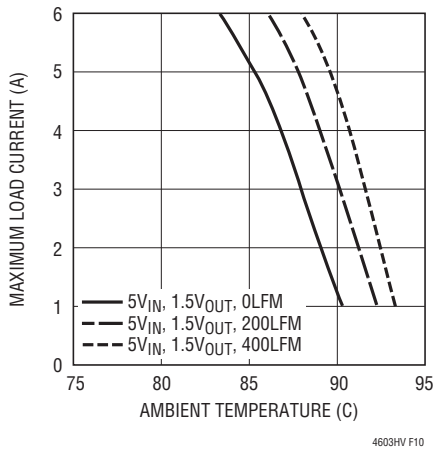


Figure 10. BGA Heat Sink

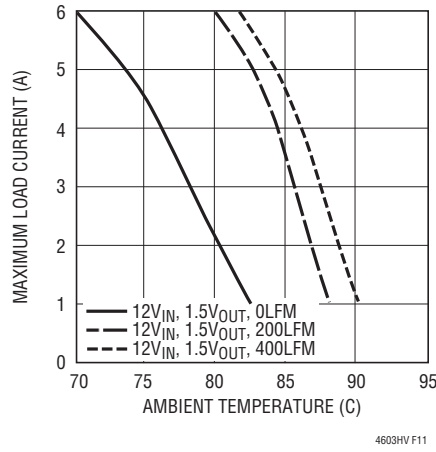


Figure 11. No Heat Sink

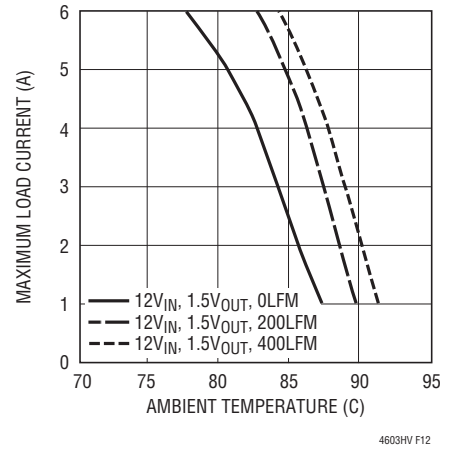


Figure 12. BGA Heat Sink

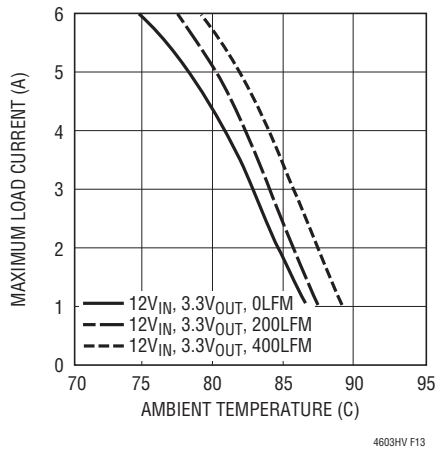


Figure 13. No Heat Sink

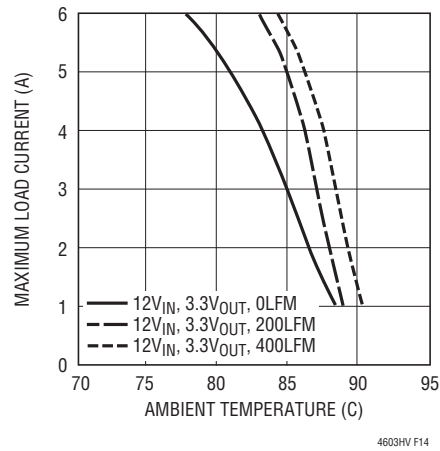


Figure 14. BGA Heat Sink

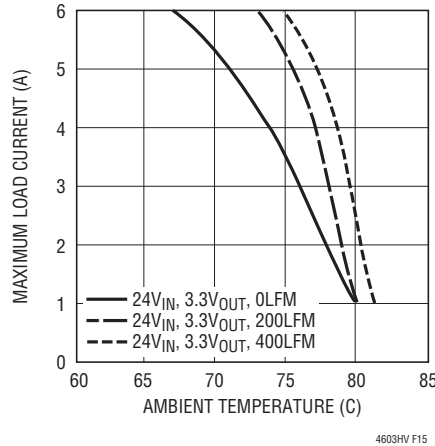


Figure 15. No Heat Sink

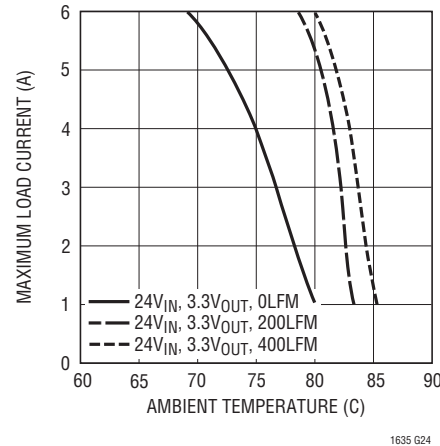


Figure 16. BGA Heat Sink

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Table 2. Output Voltage Response Versus Component Matrix (Refer to Figure 20)

TYPICAL MEASURED VALUES

C _{OUT1} VENDORS	PART NUMBER	C _{OUT2} VENDORS	PART NUMBER
TAIYO YUDEN	JMK316BJ226ML-T501 (22μF, 6.3V)	SANYO POSCAP	6TPE220MIL (220μF, 6.3V)
TAIYO YUDEN	JMK325BJ476MM-T (47μF, 6.3V)	SANYO POSCAP	2R5TPE330M9 (330μF, 2.5V)
TDK	C3225X5R0J476M (47μF, 6.3V)	SANYO POSCAP	4TPE330MCL (330μF, 4V)

V _{OUT} (V)	C _{IN} (CERAMIC)	C _{IN} (BULK)	C _{OUT1} (CERAMIC)	C _{OUT2} (BULK)	V _{IN} (V)	DROOP (mV)	PEAK TO PEAK (mV)	RECOVERY TIME (μs)	LOAD STEP (A/μs)	R _{SET} (kΩ)
1.2	2 × 10μF 35V	150μF 35V	1 × 22μF 6.3V	330μF 4V	5	34	68	30	3	60.4
1.2	2 × 10μF 35V	150μF 35V	1 × 47μF 6.3V	330μF 2.5V	5	22	40	26	3	60.4
1.2	2 × 10μF 35V	150μF 35V	2 × 47μF 6.3V	220μF 6.3V	5	20	40	24	3	60.4
1.2	2 × 10μF 35V	150μF 35V	4 × 47μF 6.3V	NONE	5	32	60	18	3	60.4
1.2	2 × 10μF 35V	150μF 35V	1 × 22μF 6.3V	330μF 4V	12	34	68	30	3	60.4
1.2	2 × 10μF 35V	150μF 35V	1 × 47μF 6.3V	330μF 2.5V	12	22	40	26	3	60.4
1.2	2 × 10μF 35V	150μF 35V	2 × 47μF 6.3V	220μF 6.3V	12	20	39	24	3	60.4
1.2	2 × 10μF 35V	150μF 35V	4 × 47μF 6.3V	NONE	12	29.5	55	18	3	60.4
1.5	2 × 10μF 35V	150μF 35V	1 × 22μF 6.3V	330μF 4V	5	35	70	30	3	40.2
1.5	2 × 10μF 35V	150μF 35V	1 × 47μF 6.3V	330μF 2.5V	5	25	48	30	3	40.2
1.5	2 × 10μF 35V	150μF 35V	2 × 47μF 6.3V	220μF 6.3V	5	24	47.5	26	3	40.2
1.5	2 × 10μF 35V	150μF 35V	4 × 47μF 6.3V	NONE	5	36	68	26	3	40.2
1.5	2 × 10μF 35V	150μF 35V	1 × 22μF 6.3V	330μF 4V	12	35	70	30	3	40.2
1.5	2 × 10μF 35V	150μF 35V	1 × 47μF 6.3V	330μF 2.5V	12	25	48	30	3	40.2
1.5	2 × 10μF 35V	150μF 35V	2 × 47μF 6.3V	220μF 6.3V	12	24	45	26	3	40.2
1.5	2 × 10μF 35V	150μF 35V	4 × 47μF 6.3V	NONE	12	32.6	61.9	26	3	40.2
1.8	2 × 10μF 35V	150μF 35V	1 × 22μF 6.3V	330μF 4V	5	38	76	37	3	30.1
1.8	2 × 10μF 35V	150μF 35V	1 × 47μF 6.3V	330μF 2.5V	5	29.5	57.5	30	3	30.1
1.8	2 × 10μF 35V	150μF 35V	2 × 47μF 6.3V	220μF 6.3V	5	28	55	26	3	30.1
1.8	2 × 10μF 35V	150μF 35V	4 × 47μF 6.3V	NONE	5	43	80	26	3	30.1
1.8	2 × 10μF 35V	150μF 35V	1 × 22μF 6.3V	330μF 4V	12	38	76	37	3	30.1
1.8	2 × 10μF 35V	150μF 35V	1 × 47μF 6.3V	330μF 2.5V	12	28	55	30	3	30.1
1.8	2 × 10μF 35V	150μF 35V	2 × 47μF 6.3V	220μF 6.3V	12	27	52	26	3	30.1
1.8	2 × 10μF 35V	150μF 35V	4 × 47μF 6.3V	NONE	12	36.4	70	26	3	30.1
2.5	2 × 10μF 35V	150μF 35V	1 × 22μF 6.3V	330μF 4V	5	38	78	40	3	19.1
2.5	2 × 10μF 35V	150μF 35V	1 × 47μF 6.3V	330μF 4V	5	37.6	74	34	3	19.1
2.5	2 × 10μF 35V	150μF 35V	2 × 47μF 6.3V	220μF 6.3V	5	39.5	78.1	28	3	19.1
2.5	2 × 10μF 35V	150μF 35V	4 × 47μF 6.3V	NONE	5	66	119	12	3	19.1
2.5	2 × 10μF 35V	150μF 35V	1 × 22μF 6.3V	330μF 4V	12	38	78	40	3	19.1
2.5	2 × 10μF 35V	150μF 35V	1 × 47μF 6.3V	330μF 4V	12	34.5	66.3	34	3	19.1
2.5	2 × 10μF 35V	150μF 35V	2 × 47μF 6.3V	220μF 6.3V	12	35.8	68.8	28	3	19.1
2.5	2 × 10μF 35V	150μF 35V	4 × 47μF 6.3V	NONE	12	50	98	18	3	19.1
3.3	2 × 10μF 35V	150μF 35V	1 × 22μF 6.3V	330μF 4V	7	42	86	40	3	13.3
3.3	2 × 10μF 35V	150μF 35V	1 × 47μF 6.3V	330μF 4V	7	47	89	32	3	13.3
3.3	2 × 10μF 35V	150μF 35V	2 × 47μF 6.3V	220μF 6.3V	7	50	94	28	3	13.3
3.3	2 × 10μF 35V	150μF 35V	4 × 47μF 6.3V	NONE	7	75	141	14	3	13.3
3.3	2 × 10μF 35V	150μF 35V	1 × 22μF 6.3V	330μF 4V	12	42	86	40	3	13.3
3.3	2 × 10μF 35V	150μF 35V	1 × 47μF 6.3V	330μF 4V	12	47	88	32	3	13.3
3.3	2 × 10μF 35V	150μF 35V	2 × 47μF 6.3V	220μF 6.3V	12	50	94	28	3	13.3
3.3	2 × 10μF 35V	150μF 35V	4 × 47μF 6.3V	NONE	12	69	131	22	3	13.3
5	2 × 10μF 35V	150μF 35V	4 × 47μF 6.3V	NONE	15	110	215	20	3	8.25
5	2 × 10μF 35V	150μF 35V	4 × 47μF 6.3V	NONE	20	110	217	20	3	8.25

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Table 3. 1.5V Output

DERATING CURVE	V _{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ _{JA} (°C/W)
Figures 9, 11	5, 12	Figure 7	0	None	15.2
Figures 9, 11	5, 12	Figure 7	200	None	14
Figures 9, 11	5, 12	Figure 7	400	None	12
Figures 10, 12	5, 12, 20	Figure 7	0	BGA Heat Sink	13.9
Figures 10, 12	5, 12, 20	Figure 7	200	BGA Heat Sink	11.3
Figures 10, 12	5, 12, 20	Figure 7	400	BGA Heat Sink	10.25

Table 4. 3.3V Output

DERATING CURVE	V _{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ _{JA} (°C/W)
Figures 13, 15	12, 24	Figure 8	0	None	15.2
Figures 13, 15	12, 24	Figure 8	200	None	14.6
Figures 13, 15	12, 24	Figure 8	400	None	13.4
Figures 14, 16	12, 24	Figure 8	0	BGA Heat Sink	13.9
Figures 14, 16	12, 24	Figure 8	200	BGA Heat Sink	11.1
Figures 14, 16	12, 24	Figure 8	400	BGA Heat Sink	10.5

Heat Sink Manufacturer

Aavid Thermalloy	Part No: 375424B00034G	Phone: 603-224-9988
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This allows for 4W maximum power dissipation in the total module with top and bottom heat sinking, and 2W power dissipation through the top of the module with an approximate θ_{JC} between 6°C/W to 9°C/W. This equates to a total of 124°C at the junction of the device.

Safety Considerations

The LTM4603HV modules do not provide galvanic isolation from V_{IN} to V_{OUT} . There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

Layout Checklist/Example

The high integration of LTM4603HV makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current path, including V_{IN} , PGND and V_{OUT} . It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN} , PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.

- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads.
- If vias are placed onto the pads, the the vias must be capped.
- Interstitial via placement can also be used if necessary.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to PGND underneath the unit.

Figure 17 gives a good example of the recommended layout.

Frequency Adjustment

The LTM4603HV is designed to typically operate at 1MHz across most input conditions. The f_{SET} pin is typically left open. The switching frequency has been optimized for maintaining constant output ripple noise over most operating ranges. The 1MHz switching frequency and the 400ns minimum off-time can limit operation at higher duty cycles like 5V_{IN} to 3.3V_{OUT}, and produce excessive inductor ripple currents for lower duty cycle applications like 28V_{IN} to 5V_{OUT}. The 5V_{OUT} and 3.3V_{OUT} drop out curves are modified by adding an external resistor on the f_{SET} pin to allow for wider input voltage operation.

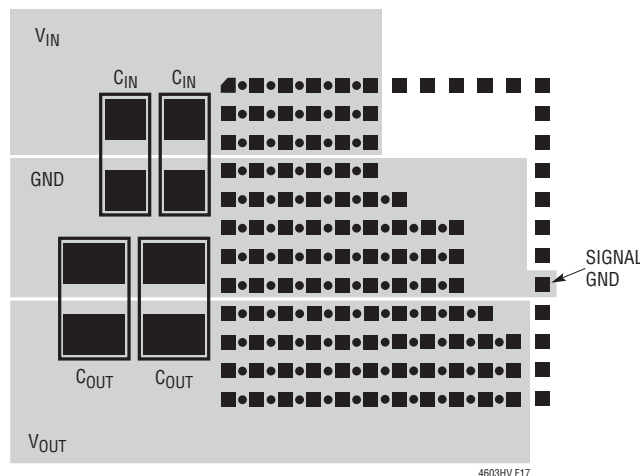


Figure 17. Recommended Layout

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Example for 5V Output

LTM4603HV minimum on-time = 100ns
 $t_{ON} = ((V_{OUT} \cdot 10\text{pF})/I_{fSET})$, for $V_{OUT} > 4.8\text{V}$ use 4.8V

LTM4603HV minimum off-time = 400ns
 $t_{OFF} = t - t_{ON}$, where $t = 1/\text{Frequency}$

Duty Cycle = t_{ON}/t or V_{OUT}/V_{IN}

Equations for setting frequency:

$I_{fSET} = (V_{IN}/(3 \cdot R_{fSET}))$, for 28V input operation, $I_{fSET} = 281\mu\text{A}$, $t_{ON} = ((4.8\text{V} \cdot 10\text{pF})/I_{fSET})$, $t_{ON} = 171\text{ns}$, where the internal R_{fSET} is 33.2k. Frequency = $(V_{OUT}/(V_{IN} \cdot t_{ON})) = (5\text{V}/(28\text{V} \cdot 171\text{ns})) \sim 1\text{MHz}$. The inductor ripple current begins to get high at the higher input voltages due to a larger voltage across the inductor. This is shown in the Inductor Ripple Current vs Duty Cycle graph as over 4A at 18% duty cycle. The inductor ripple current can be lowered at the higher input voltages by adding an external resistor from f_{SET} to ground to increase the switching frequency. A 3A ripple current is chosen, and the total peak current is equal to 1/2 of the 3A ripple current plus the output current. The 5V output current is limited to 5A, so total peak current is less than 6.5A. This is below the 8A peak specified value. A 150k resistor is placed from f_{SET} to ground, and the parallel combination of 150k and 33.2k equates to 27.2k. The I_{fSET} calculation with 27.2k and 28V input voltage equals $343\mu\text{A}$. This equates to a t_{ON} of 140ns. This will increase the switching frequency from 1MHz to $\sim 1.28\text{MHz}$ for the 28V to 5V conversion. The minimum on time is above 100ns at 28V input. Since the switching frequency is approximately constant over input and output conditions, then the lower input voltage range is limited to 10V for the 1.28MHz operation due to the 400ns minimum off-time. Equation: $t_{ON} = (V_{OUT}/V_{IN}) \cdot (1/\text{Frequency})$ equates to a 382ns on time, and a 400ns off-time. The V_{IN} to V_{OUT} Step-Down Ratio curve reflects an operating range of 10V to 28V for 1.28MHz operation with a 150k resistor to ground (shown in Figure 18), and an 8V to 16V operating range for f_{SET} floating. These modifications are made to provide wider input voltage ranges for the 5V output designs while limiting the inductor ripple current, and maintaining the 400ns minimum off-time.

Example for 3.3V Output

LTM4603HV minimum on-time = 100ns
 $t_{ON} = ((3.3\text{V} \cdot 10\text{pF})/I_{fSET})$

LTM4603HV minimum off-time = 400ns
 $t_{OFF} = t - t_{ON}$, where $t = 1/\text{Frequency}$

Duty Cycle (DC) = t_{ON}/t or V_{OUT}/V_{IN}

Equations for setting frequency:

$I_{fSET} = (V_{IN}/(3 \cdot R_{fSET}))$, for 28V input operation, $I_{fSET} = 281\mu\text{A}$, $t_{ON} = ((3.3\text{V} \cdot 10\text{pF})/I_{fSET})$, $t_{ON} = 117\text{ns}$, where the internal R_{fSET} is 33.2k. Frequency = $(V_{OUT}/(V_{IN} \cdot t_{ON})) = (3.3\text{V}/(28\text{V} \cdot 117\text{ns})) \sim 1\text{MHz}$. The minimum on-time and minimum off-time are within specification at 117ns and 883ns. But the 4.5V minimum input for converting 3.3V output will not meet the minimum off-time specification of 400ns. $t_{ON} = 733\text{ns}$, Frequency = 1MHz, $t_{OFF} = 267\text{ns}$.

Solution

Lower the switching frequency at lower input voltages to allow for higher duty cycles, and meet the 400ns minimum off-time at 4.5V input voltage. The off-time should be about 500ns with 100ns guard band included. The duty cycle for $(3.3\text{V}/4.5\text{V}) = \sim 73\%$. Frequency = $(1 - \text{DC})/t_{OFF}$ or $(1 - 0.73)/500\text{ns} = 540\text{kHz}$. The switching frequency needs to be lowered to 540kHz at 4.5V input. $t_{ON} = \text{DC}/\text{frequency}$, or $1.35\mu\text{s}$. The f_{SET} pin voltage compliance is 1/3 of V_{IN} , and the I_{fSET} current equates to $45\mu\text{A}$ with the internal 33.2k. The I_{fSET} current needs to be $24\mu\text{A}$ for 540kHz operation. A resistor can be placed from V_{OUT} to f_{SET} to lower the effective I_{fSET} current out of the f_{SET} pin to $24\mu\text{A}$. The f_{SET} pin is $4.5\text{V}/3 = 1.5\text{V}$ and $V_{OUT} = 3.3\text{V}$, therefore an 82.5k resistor will source $21\mu\text{A}$ into the f_{SET} node and lower the I_{fSET} current to $24\mu\text{A}$. This enables the 540kHz operation and the 4.5V to 28V input operation for down converting to 3.3V output as shown in Figure 19. The frequency will scale from 540kHz to 1.27MHz over this input range. This provides for an effective output current of 5A over the input range.

TYPICAL APPLICATIONS

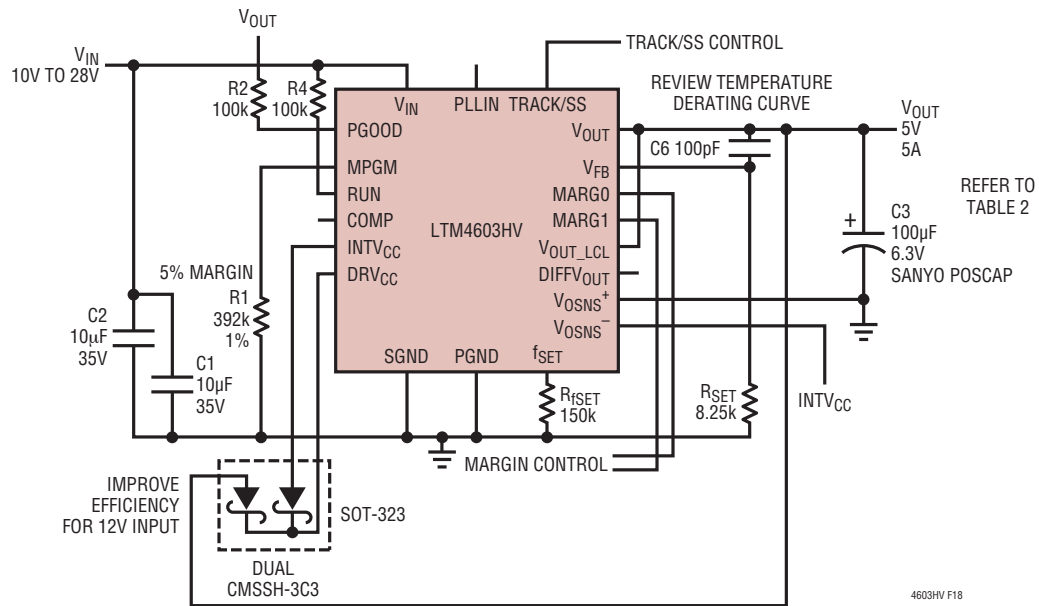


Figure 18. 5V at 5A Design

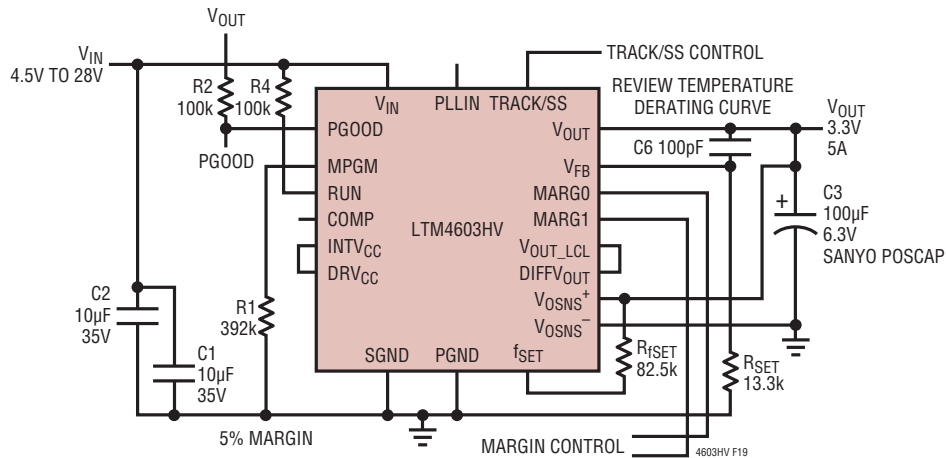


Figure 19. 3.3V at 5A Design

TYPICAL APPLICATIONS

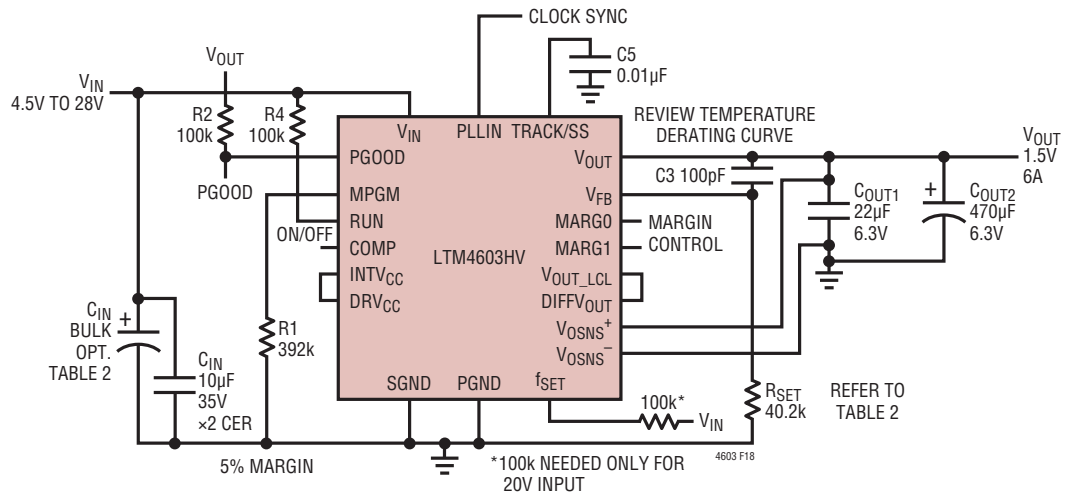


Figure 20. Typical 4.5V-28VIN, 1.5V at 6A Design

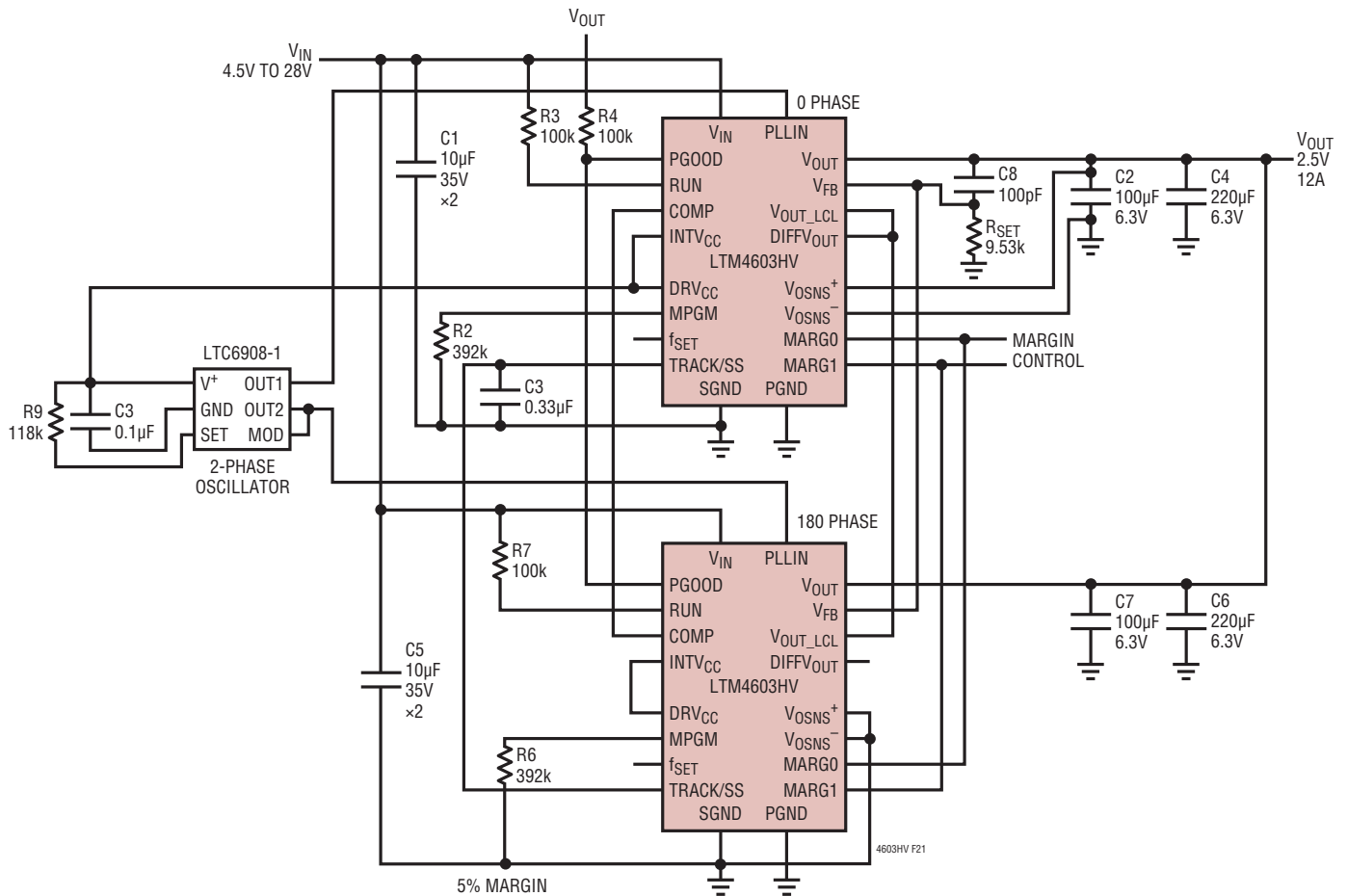


Figure 21. 2-Phase, Parallel 2.5V at 12A Design

TYPICAL APPLICATIONS

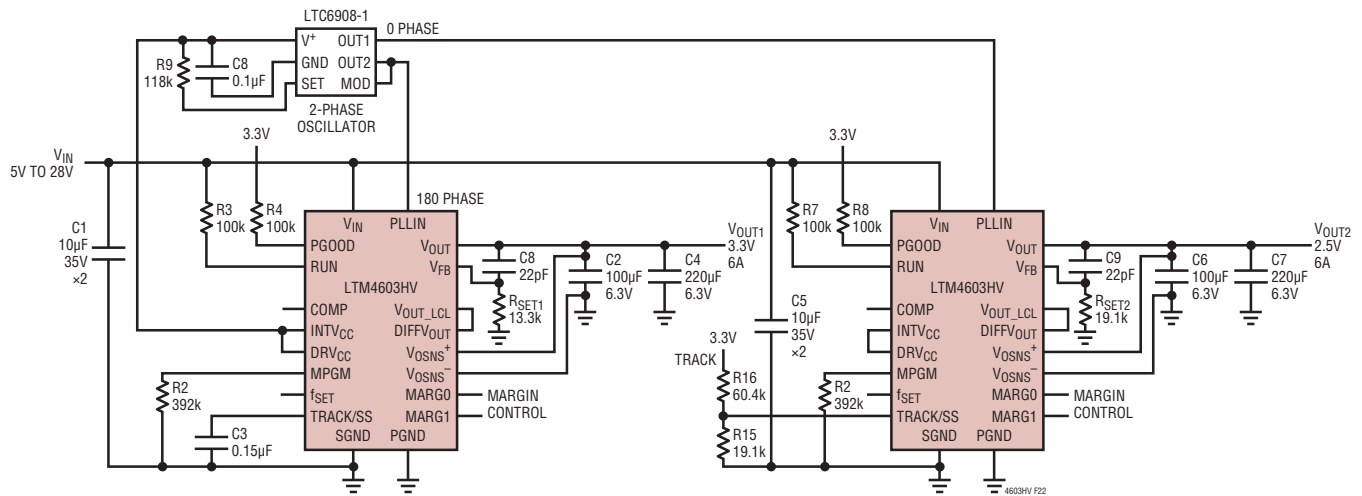


Figure 22. 2-Phase, 3.3V and 2.5V at 6A with Tracking

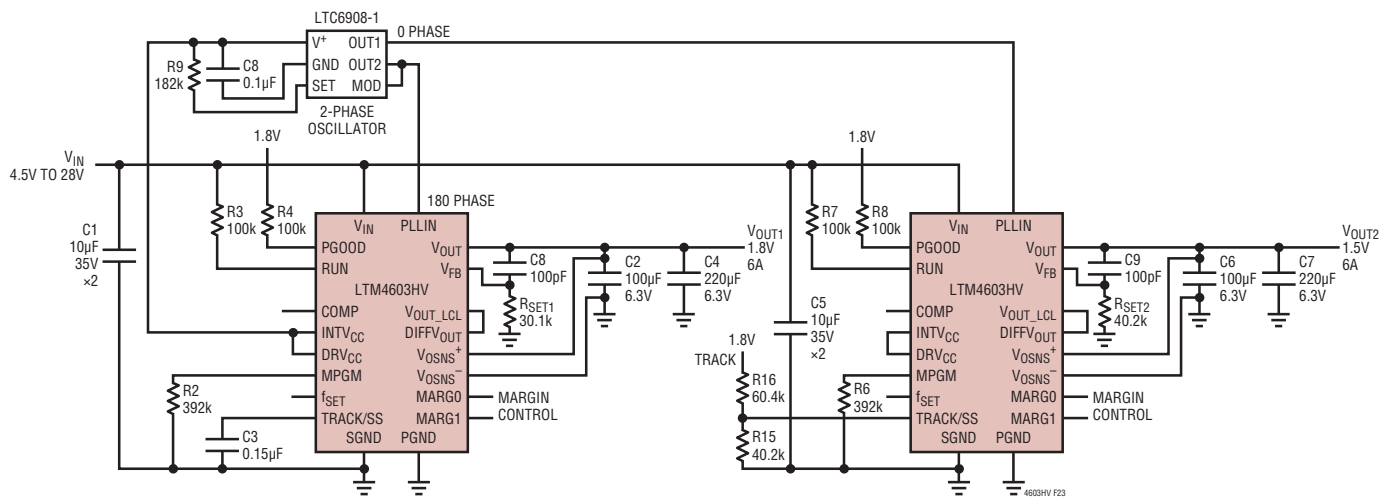


Figure 23. 2-Phase, 1.8V and 1.5V at 6A with Tracking

For more information www.linear.com/LTM4603HV



4603hvfa



REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	6/14	Updated Absolute Maximum Ratings.	2
		Updated the Order Information table.	2
		Updated the Electrical Characteristics table.	2-4
		Updated the Pin Functions information.	7-8
		Updated the Output Voltage Programming and Margining section.	11
		Updated the PLLIN section.	15
		Updated the Applications Information section.	20
		Updated Figure 18.	21

LTM4603HV

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2900	Quad Supply Monitor with Adjustable Reset Timer	Monitors Four Supplies; Adjustable Reset Timer
LTC2923	Power Supply Tracking Controller	Tracks Both Up and Down; Power Supply Sequencing
LT3825/LT3837	Synchronous Isolated Flyback Controllers	No Opto-Coupler Required; 3.3V, 12A Output; Simple Design
LTM4600	10A DC/DC μ Module	Fast Transient Response
LTM4601	12A DC/DC μ Module	with PLL, Output Tracking and Margining, LTM4603HV Pin Compatible
LTM4602	6A DC/DC μ Module	Pin Compatible with the LTM4600
LTM4603	6A DC/DC μ Module with Tracking PLL/Margining	Pin Compatible with the LTM4601