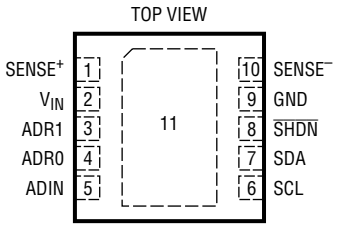
ABSOLUTE MAXIMUM RATINGS (Notes 1, 3)

V_{IN} Voltage ..... –0.3V to 90V
SENSE+, SENSE– Voltages ..... V_{IN} – 10V or –0.3V to V_{IN} + 0.3V
ADR1, ADR0 Voltages ..... –0.3V to 90V
ADIN, $\overline{SHDN}$, $\overline{SDAO}$, SDAO Voltages ..... –0.3V to 6V
SCL, SDA, SDAI Voltages (Note 2) ..... –0.3V to 5.5V
SCL, SDA, SDAI Clamp Current 5mA

Operating Temperature Range
LTC4151C/LTC4151C-1/LTC4151C-2 ..... 0°C to 70°C
LTC4151I/LTC4151I-1/LTC4151I-2 ..... –40°C to 85°C
LTC4151H ..... –40°C to 125°C
Storage Temperature Range
MSOP, SO ..... –65°C to 150°C
DFN ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
MSOP, SO ..... 300°C

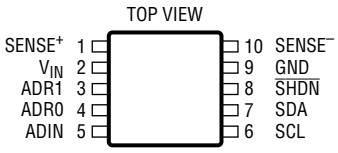
PIN CONFIGURATION

LTC4151



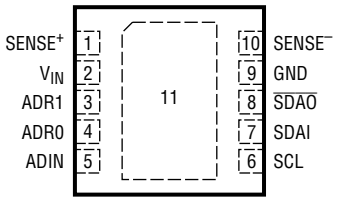
DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 45°C/W
EXPOSED PAD (PIN 11) PCB GND CONNECTION OPTIONAL

LTC4151



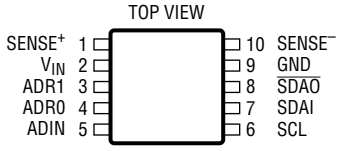
MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 85°C/W

LTC4151-1



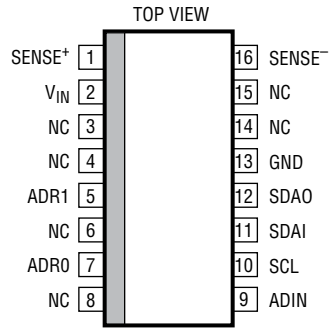
DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 45°C/W
EXPOSED PAD (PIN 11) PCB GND CONNECTION OPTIONAL

LTC4151-1



MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 85°C/W

LTC4151-2



S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4151CDD#PBF	LTC4151CDD#TRPBF	LCWZ	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4151IDD#PBF	LTC4151IDD#TRPBF	LCWZ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4151HDD#PBF	LTC4151HDD#TRPBF	LCWZ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4151CDD-1#PBF	LTC4151CDD-1#TRPBF	LCXC	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4151IDD-1#PBF	LTC4151IDD-1#TRPBF	LCXC	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4151CMS#PBF	LTC4151CMS#TRPBF	LTCWY	10-Lead Plastic MSOP	0°C to 70°C
LTC4151IMS#PBF	LTC4151IMS#TRPBF	LTCWY	10-Lead Plastic MSOP	–40°C to 85°C
LTC4151HMS#PBF	LTC4151HMS#TRPBF	LTCWY	10-Lead Plastic MSOP	–40°C to 125°C
LTC4151CMS-1#PBF	LTC4151CMS-1#TRPBF	LTCXB	10-Lead Plastic MSOP	0°C to 70°C
LTC4151IMS-1#PBF	LTC4151IMS-1#TRPBF	LTCXB	10-Lead Plastic MSOP	–40°C to 85°C
LTC4151CS-2#PBF	LTC4151CS-2#TRPBF	LTC4151S-2	16-Lead Plastic SO	0°C to 70°C
LTC4151IS-2#PBF	LTC4151IS-2#TRPBF	LTC4151S-2	16-Lead Plastic SO	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} is from 7V to 80V, unless noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
General							
V_{IN}	Supply Voltage		●	7		80	V
I_{IN}	Supply Current	V_{IN} = 48V, Normal Operation Mode V_{IN} = 12V, Shutdown Mode	● ●		1.2 120	1.7 300	mA µA
I_{SENSE^+}	SENSE+ Input Current	V_{IN}, SENSE+, SENSE– = 48V	●		5	9	µA
I_{SENSE^-}	SENSE– Input Current	V_{IN}, SENSE+, SENSE– = 48V	●		0.1	1	µA
$V_{\overline{SHDN}(TH)}$	$\overline{SHDN}$ Input Threshold		●	1	1.5	2	V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Input Current	$\overline{SHDN}$ = 0V	●	–3	–5	–8	µA
ADC							
RES	Resolution (No Missing Codes)	(Note 4)	●	12			Bits
V_{FS}	Full-Scale Voltage	(SENSE+ – SENSE–) V_{IN} ADIN			81.92 102.4 2.048		mV V V
LSB	LSB Step Size	(SENSE+ – SENSE–) V_{IN} ADIN			20 25 0.5		µV mV mV
TUE	Total Unadjusted Error	(SENSE+ – SENSE–) V_{IN} (Note 5) ADIN, C-Grade ADIN, I-, H-Grade	● ● ● ●			±1.25 ±1 ±0.75 ±1	% % % %
V_{OS}	Offset Error	(SENSE+ – SENSE–) V_{IN} (Note 6) ADIN	● ● ●			±5 ±6 ±8	LSB LSB LSB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} is from 7V to 80V, unless noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
INL	Integral Nonlinearity	(SENSE⁺ – SENSE⁻) V_{IN} (Note 5) ADIN	● ● ●		±1 ±1 ±0.5	±3 ±3 ±2	LSB LSB LSB
σ_T	Transition Noise	(SENSE⁺ – SENSE⁻) V_{IN} ADIN			1.2 0.3 22		μV_{RMS} mV_{RMS} μV_{RMS}
f_{CONV}	Conversion Rate (Continuous Mode)		●	6	7.5	9	Hz
t_{CONV}	Conversion Time (Snapshot Mode)	(SENSE⁺ – SENSE⁻) ADIN, V_{IN}	● ●	53 26	67 33	85 42	ms ms
R_{ADIN}	ADIN Pin Input Resistance	ADIN = 3V	●	2	10		MΩ
I_{ADIN}	ADIN Pin Input Current	ADIN = 3V	●			±2	µA
I²C Interface							
$V_{ADR(H)}$	ADR0, ADR1 Input High Threshold		●	2.3	2.65	3.0	V
$V_{ADR(L)}$	ADR0, ADRI Input Low Threshold		●	0.2	0.6	0.9	V
$I_{ADR(IN)}$	ADR0, ADRI Input Current	ADR0, ADR1 = 0V or 3V ADR0, ADR1 = 0.8V or 2.2V	● ●	 ±8		±70	µA µA
$V_{SDA(OL)}$	SDA, SDAO, $\overline{SDAO}$ Output Low Voltage	I_{SDA}, I_{SDAO}, $I_{\overline{SDAO}}$ = 8mA	●		0.15	0.4	V
$I_{SDA,SCL(IN)}$	SDA, SDAI, SDAO, $\overline{SDAO}$, SCL Input Current	SDA, SDAI, SDAO, $\overline{SDAO}$, SCL = 5V	●		0	±2	µA
$V_{SDA,SCL(TH)}$	SDA, SDAI, SCL Input Threshold		●	1.6	1.8	2	V
$V_{SDA,SCL(CL)}$	SDA, SDAI, SCL Clamp Voltage	I_{SDA}, I_{SDAI}, I_{SCL} = 3mA	●	5.5	6.1	6.6	V
I²C Interface Timing (Note 4)							
$f_{SCL(MAX)}$	Maximum SCL Clock Frequency			400			kHz
t_{LOW}	Minimum SCL Low Period				0.65	1.3	µs
t_{HIGH}	Minimum SCL High Period				50	600	ns
$t_{BUF(MIN)}$	Minimum Bus Free Time Between Stop/Start Condition				0.12	1.3	µs
$t_{HD,STA(MIN)}$	Minimum Hold Time After (Repeated) Start Condition				140	600	ns
$t_{SU,STA(MIN)}$	Minimum Repeated Start Condition Set-Up Time				30	600	ns
$t_{SU,STO(MIN)}$	Minimum Stop Condition Set-Up Time				30	600	ns
$t_{HD,DATI(MIN)}$	Minimum Data Hold Time Input				–100	0	ns
$t_{HD,DATO(MIN)}$	Minimum Data Hold Time Output			300	600	900	ns
$t_{SU,DAT(MIN)}$	Minimum Data Set-Up Time Input				30	100	ns
$t_{SP(MAX)}$	Maximum Suppressed Spike Pulse Width			50	110	250	ns
t_{RST}	Stuck-Bus Reset Time	SCL or SDA/SDAI Held Low		20	33		ms
C_X	SCL, SDA Input Capacitance				5	10	pF

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Internal clamps limit the SCL, SDA (LTC4151) and SDAI (LTC4151-1/LTC4151-2) pins to a minimum of 5.5V. Driving these pins to voltages beyond the clamp may damage the part. The pins can be safely tied to higher voltages through a resistor that limits the current below 5mA.

Note 3: All currents into pins are positive. All voltages are referenced to GND, unless otherwise noted.

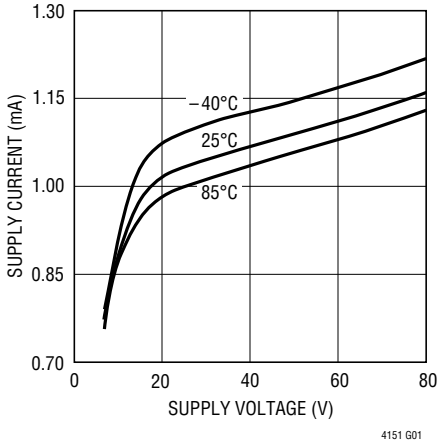
Note 4: Guaranteed by design and not subject to test.

Note 5: Integral nonlinearity and total unadjusted error of V_{IN} are tested between 7V and 80V.

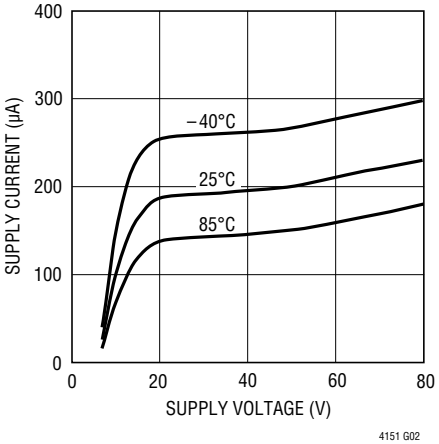
Note 6: Offset error of V_{IN} is defined by extrapolating the straight line measured between 7V and 80V.

TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 12V, T_A = 25°C, unless noted.

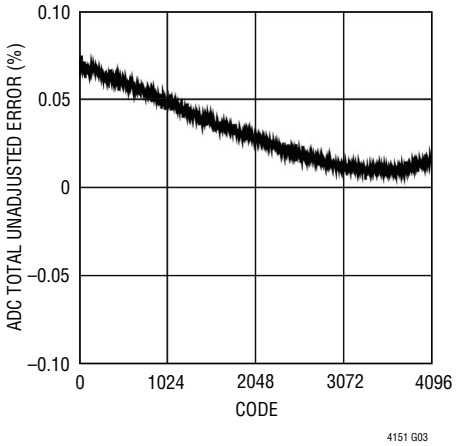
Supply Current vs Supply Voltage (Normal Mode)



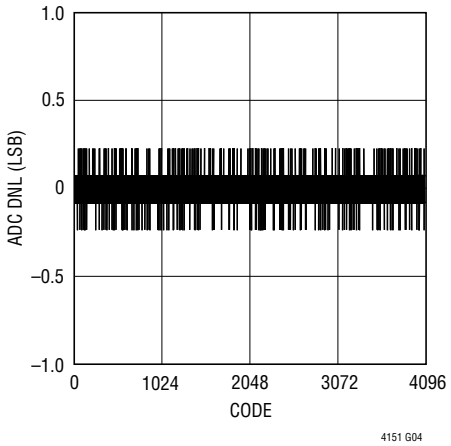
Supply Current vs Supply Voltage (Shutdown Mode)



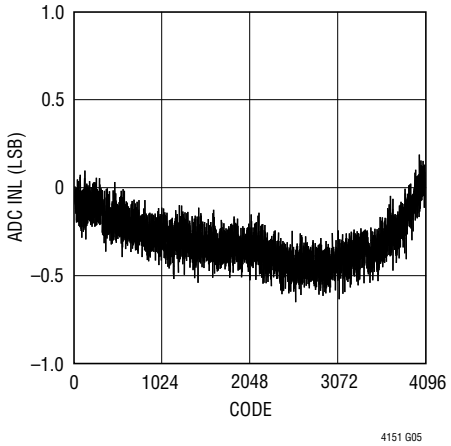
ADC Total Unadjusted Error vs Code (ADIN Voltage)



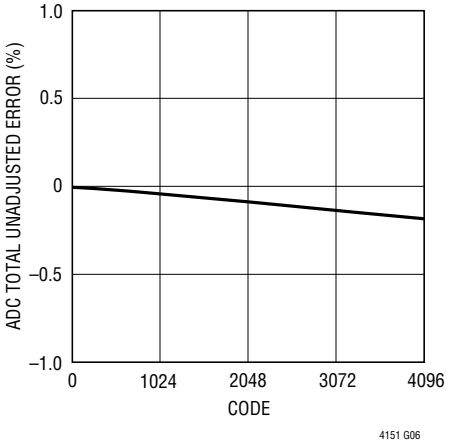
ADC DNL vs Code (ADIN Voltage)



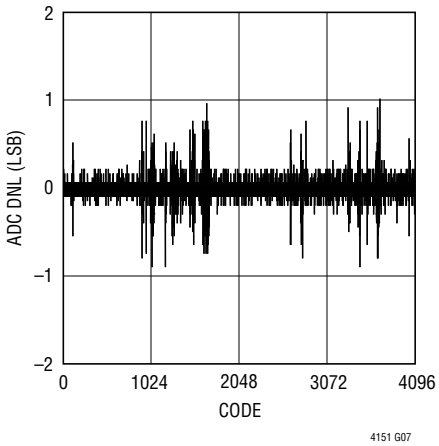
ADC INL vs Code (ADIN Voltage)



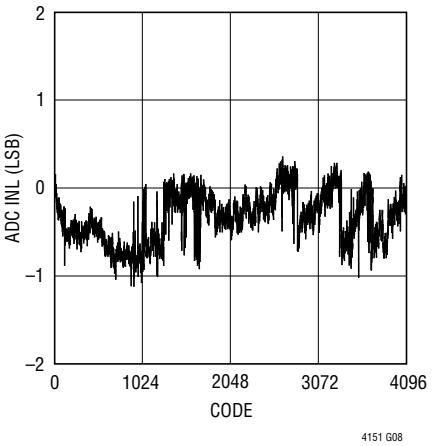
ADC Total Unadjusted Error vs Code (SENSE Voltage)



ADC DNL vs Code (SENSE Voltage)

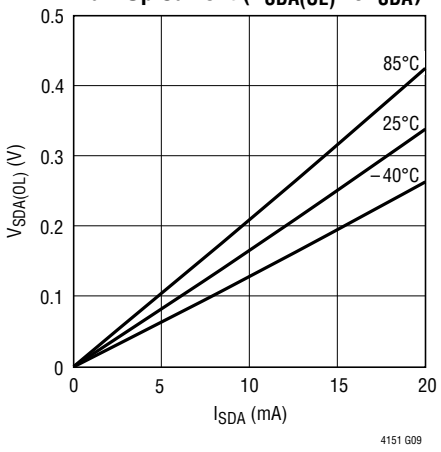


ADC INL vs Code (SENSE Voltage)

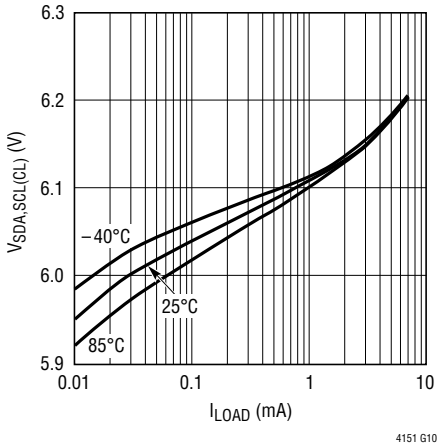


TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 12V, T_A = 25°C, unless noted.

SDA, SDAO, $\overline{SDAO}$ Output Low vs Pull-Up Current ($V_{SDA(OL)}$ vs I_{SDA})



SDA, SDAI, SCL Clamp Voltage vs Load Current



PIN FUNCTIONS

ADIN: ADC Input. The onboard ADC measures voltage range between 0V and 2.048V. Tie to GND if unused.

ADR1, ADR0: I²C Device Address Inputs. Connecting ADR1 and ADR0 to V_{IN}, GND or leaving the pins open configures one of nine possible addresses. See Table 1 in the Applications Information section for details.

Exposed Pad (DD Package Only): Exposed pad may be left open or connected to device ground (GND).

GND: Device Ground.

SCL: I²C Bus Clock Input. Data is shifted in and out at the SDA pin on rising edges of SCL. This pin is driven by an open-collector output from a master controller. An external pull-up resistor or current source is required and can be placed between SCL and V_{IN}. The voltage at SCL is internally clamped to 6V (5.5V minimum).

SDA (LTC4151 Only): I²C Bus Data Input/Output. Used for shifting in address, command or data bits and sending out data. An external pull-up resistor or current source is required and can be placed between SDA and V_{IN}. The voltage at SDA is internally clamped to 6V (5.5V minimum).

SDAI (LTC4151-1/LTC4151-2 Only): I²C Bus Data Input. Used for shifting in address, command, data, and SDAO acknowledge bits. This pin is driven by an open-collector output from a master controller. An external pull-up resistor or current source is required and can be placed between SDAI and V_{IN}. If the master separates SDAI and SDAO, data read at SDAO needs to be echoed back to SDAI for proper I²C communication. The voltage at SDAI is internally clamped to 6V (5.5V minimum).

SDAO (LTC4151-2 Only): Serial Bus Data Output. Open-drain output used for sending data back to the master controller or acknowledging a write operation. Normally tied to SDAI to form the SDA line. An external pull-up resistor or current source is required.

$\overline{SDAO}$ (LTC4151-1 Only): Inverted Serial Bus Data Output. Open-drain output used for sending data back to the master controller or acknowledging a write operation. Data is inverted for convenience of opto-isolation. An external pull-up resistor or current source is required.

$SENSE^+$: Kelvin Sense of the V_{IN} Pin. See Figure 10 for recommended Kelvin connection.

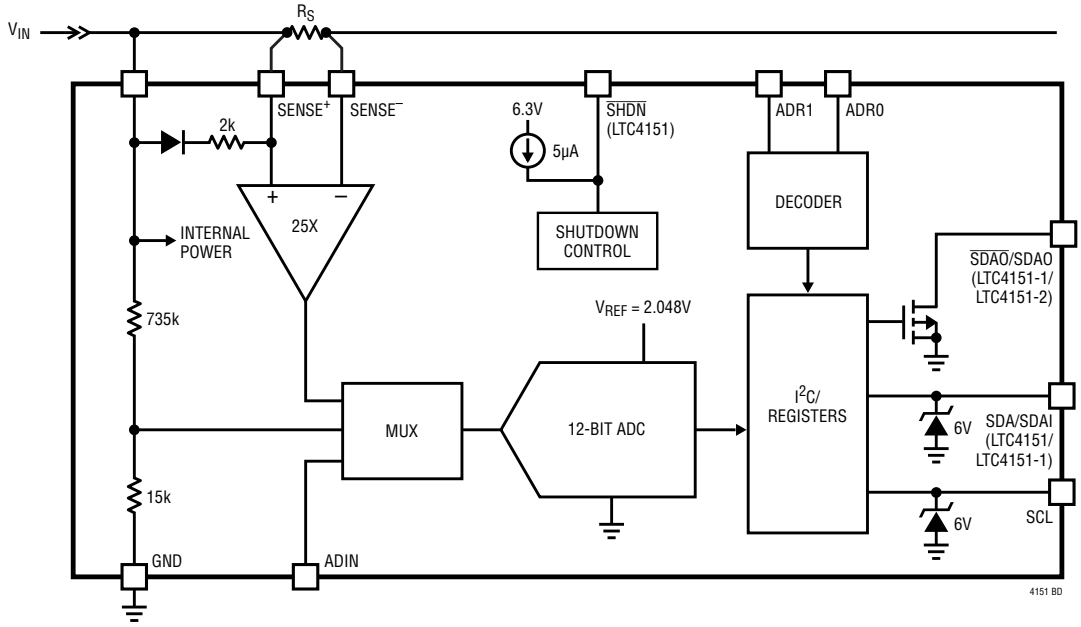
$SENSE^-$: High Side Current Sense Input. Connect an external sense resistor between $SENSE^+$ and $SENSE^-$. The differential voltage between $SENSE^+$ and $SENSE^-$ is monitored by the onboard ADC with a full-scale sense voltage of 81.92mV.

PIN FUNCTIONS

$\overline{SHDN}$ (LTC4151 Only): Shutdown Input. Internally pulled up to 6.3V. Pull this pin below 1V to force the LTC4151 into shutdown mode. Leave this pin open if unused.

V_{IN}: Supply Voltage Input. Accepts 7V to 80V. The voltage at this pin is monitored by the onboard ADC with a full-scale input range of 102.4V. $SENSE^+$ must be connected to V_{IN} for proper ADC readout.

BLOCK DIAGRAM



OPERATION

The LTC4151 accurately monitors high side current and voltages. This device accepts a wide range of input voltages from as low as 7V up to 80V and consumes less than 1.7mA quiescent current in normal operation. A shutdown mode is available with the LTC4151 to reduce the quiescent current to less than 300µA by pulling the $\overline{SHDN}$ pin below 1V.

In default continuous scan mode after power-up, the onboard 12-bit analog-to-digital converter (ADC) continuously and sequentially measures the high side differential voltage between $SENSE^+$ (Kelvin sense of V_{IN}) and $SENSE^-$ (full-scale 81.92mV) through an internal sense amplifier, the input voltage V_{IN} (full-scale 102.4V) through an internal voltage divider, and the voltage applied to the ADIN pin (full-scale 2.048V). The reference voltage of the ADC is internally set to 2.048V. The digital data obtained by the ADC is stored in the onboard registers.

In snapshot mode, the LTC4151 can perform on-demand measurement of a selected voltage without the need of continuous polling by a master controller. The snapshot mode is enabled by programming the control register through the I^2C interface. A status bit in the data register monitors the ADC's conversion. When the conversion is completed, the 12-bit digital code of the measured voltage is held in the corresponding data registers.

The LTC4151 provides an I^2C interface to read the ADC data from the data registers and to program the control register. Two three-state pins, ADR0 and ADR1, are used to decode nine device addresses (see Table 1). The LTC4151 features a single SDA pin to handle both input data and output data, while the LTC4151-1/LTC4151-2 provide separate data in (SDAI) and data out ($\overline{SDAO}$ on the LTC4151-1 and SDAO on the LTC4151-2) pins to facilitate opto-isolation.

APPLICATIONS INFORMATION

The LTC4151 offers a compact complete solution for high side power monitoring. With a wide operating voltage range from 7V to 80V, this device is ideal for a variety of applications including consumer, automotive, industrial and telecom infrastructure. The simple application circuit as shown in Figure 1 provides monitoring of high side current with a 0.02Ω resistor (4.096A in full scale), input voltage (102.4V in full scale) and an external voltage (2.048V in full scale), all with an internal 12-bit resolution ADC.

Data Converter

The LTC4151 features an onboard, 12-bit ΔΣ A/D converter (ADC) that continuously monitors three voltages in the sequence of (V_{SENSE+} – $V_{SENSE–}$) first, V_{IN} second and V_{ADIN} third. The ΔΣ architecture inherently averages signal noise during the measurement period. The differential voltage between $SENSE^+$ and $SENSE^–$ is monitored with an 81.92mV full scale and 20μV resolution that allows accurate measurement of the high side input current. $SENSE^+$ is a Kelvin sense pin for the V_{IN} pin and must be connected to V_{IN} (see Figure 10) for proper ADC readout. The supply voltage at V_{IN} is directly measured with a 102.4V full scale and 25mV resolution. The voltage at the uncommitted ADIN pin is measured with a 2.048V full scale and 0.5mV resolution that allows monitoring of any external voltage. The 12-bit digital code of each measured voltage is stored in two adjacent registers out of the six total data registers A through F, with the eight MSBs in the first register and the four LSBs in the second (Table 2).

The data in registers A through F is refreshed at a frequency of 7.5Hz in continuous scan mode. Setting control register bit G4 (Table 6) invokes a test mode that halts updating of these registers so that they can be written to and read from for software testing.

The data converter features a snapshot mode allowing users to make one-time measurements of a selected voltage (either the SENSE voltage, V_{IN} voltage, or ADIN voltage). To enable snapshot mode, set control register bit G7 and write the 2-bit code of the desired ADC channel to G6 and G5 (Table 6) using a Write Byte command. When the Write Byte command is completed, the ADC measures the selected voltage and a Busy Bit in the LSB data register is set to indicate that the data is not ready. After completing the conversion, the ADC is halted and the Busy Bit is reset to indicate that the data is ready. To make another measurement of the same voltage or to measure another voltage, first disable the snapshot mode for the previous measurement by clearing control bit G7, then re-enable the snapshot mode and write the code of the desired voltage according to the procedure described above. The Busy Bit remains reset in the continuous scan mode.

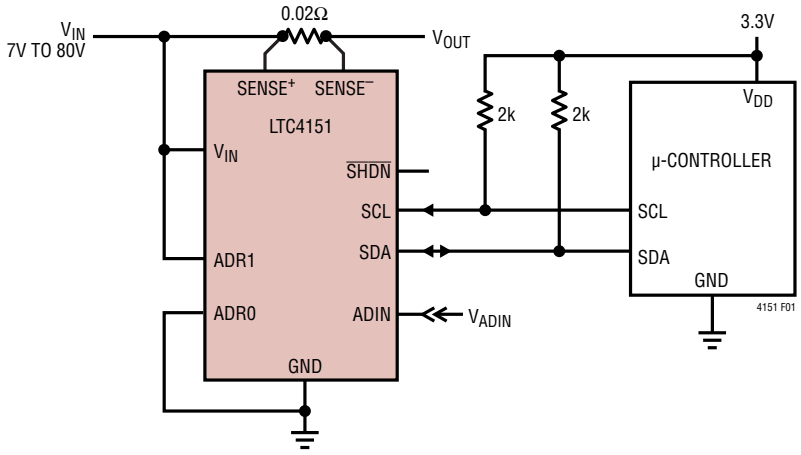


Figure 1. Monitoring High Side Current and Voltages Using the LTC4151

APPLICATIONS INFORMATION

I²C Interface

The LTC4151 features an I²C-compatible interface to provide access to six ADC data registers and a control register for monitoring the measured voltages. Figure 2 shows a general data transfer format using the I²C. The LTC4151is a read-write slave device and supports SMBus Read Byte, Write Byte, Read Word and Write Word commands. The device also supports Read Page and Write Page commands that allow one to read or write more than two bytes of data. When using the Read Page and Write Page commands, the host need only to issue an initial register address and the internal register address pointer automatically increments by 1 after each byte of data is read or written. After the register address reaches 06h, it will be reset to 00h and continue the increment. Upon a Stop condition, the register address is reset to 00h. If desired, the Read Page and Write Page support can be disabled by clearing control register bit G3. The data formats for the above commands are shown in Figures 3 to 8.

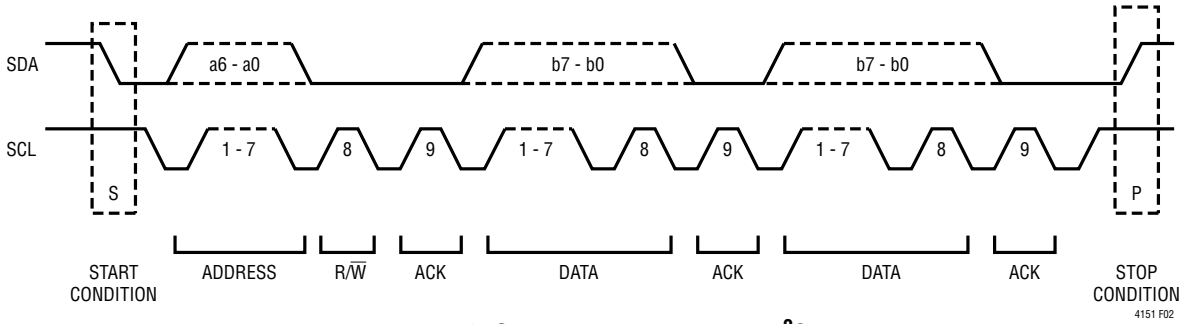


Figure 2. General Data Transfer over I²C

S	ADDRESS	W	A	COMMAND	A	DATA	A	P
	1 1 0 a3:a0	0	0	X X X X X b2:b0	0	b7:b0	0	

4151 F03

FROM MASTER TO SLAVE
FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)
$\overline{A}$: NOT ACKNOWLEDGE (HIGH)
R: READ BIT (HIGH)

$\overline{W}$: WRITE BIT (LOW)
S: START CONDITION
P: STOP CONDITION

Figure 3. LTC4151 Serial Bus SDA Write Byte Protocol

S	ADDRESS	W	A	COMMAND	A	DATA	A	DATA	A	P
	1 1 0 a3:a0	0	0	X X X X X b2:b0	0	b7:b0	0	b7:b0	0	

4151 F04

Figure 4. LTC4151 Serial Bus SDA Write Word Protocol

S	ADDRESS	W	A	COMMAND	A	DATA	A	DATA	A	...	DATA	A	P
	1 1 0 a3:a0	0	0	X X X X X b2:b0	0	b7:b0	0	b7:b0	0	...	b7:b0	0	

4151 F05

Figure 5. LTC4151 Serial Bus SDA Write Page Protocol

S	ADDRESS	W	A	COMMAND	A	S	ADDRESS	R	A	DATA	A	DATA	A	P
	1 1 0 a3:a0	0	0	X X X X X b2:b0	0		1 1 0 a3:a0	1	0	b7:b0	1			

4151 F06

Figure 6. LTC4151 Serial Bus SDA Read Byte Protocol

S	ADDRESS	W	A	COMMAND	A	S	ADDRESS	R	A	DATA	A	DATA	A	P
	1 1 0 a3:a0	0	0	X X X X X b2:b0	0		1 1 0 a3:a0	1	0	b7:b0	0	b7:b0	1	

4151 F07

Figure 7. LTC4151 Serial Bus SDA Read Word Protocol

S	ADDRESS	W	A	COMMAND	A	S	ADDRESS	R	A	DATA	A	DATA	...	DATA	A	P
	1 1 0 a3:a0	0	0	X X X X X b2:b0	0		1 1 0 a3:a0	1	0	b7:b0	0	b7:b0	...	b7:b0	1	

4151 F08

Figure 8. LTC4151 Serial Bus SDA Read Page Protocol

APPLICATIONS INFORMATION

Using Opto-Isolators with LTC4151-1 and LTC4151-2

The LTC4151-1/LTC4151-2 split the SDA line into SDAI (input) and $\overline{\text{SDAO}}$ (LTC4151-1 inverted output) or SDAO (LTC4151-2 output) for convenience of opto-coupling with a host controller that sits at a different ground level.

When using opto-isolators with the LTC4151-1, connect the SDAI to the output of the incoming opto-coupler and connect the $\overline{\text{SDAO}}$ to the anode of the outgoing opto-coupler (see Figure 9). With the outgoing opto-coupler clamping $\overline{\text{SDAO}}$ and internal 6V (5.5V minimum) clamps on SDAI and SCL, the pull-up resistors on these three pins can be directly connected to V_{IN}. In this way (with $\overline{\text{SDAO}}$ rather than conventional SDAO), the need for a separate low voltage supply for pull-ups is eliminated.

Figure 11 shows the LTC4151-2 with high speed opto-couplers for faster bus speeds. The LTC4151-2 has a non-inverter SDAO output. Powered from V_{IN}, the high voltage LT3010-5 low dropout regulator provides the supply for the opto-couplers as well as the bus lines pull-up. If the SDAI and SDAO on the master controller are not tied together, the ACK bit of the SDAO must be returned back to SDAI.

Start and Stop Conditions

When the I²C bus is idle, both SCL and SDA must remain in the high state. A bus master signals the beginning of a transmission with a Start condition by transitioning SDA from high to low while SCL stays high. When the master has finished communicating with the slave, it issues a Stop condition by transitioning SDA from low to high while SCL stays high. The bus is then free for another transmission.

Stuck-Bus Reset

The LTC4151 I²C interface features a stuck-bus reset timer. The low conditions of the SCL and the SDA/SDAI pins are OR'ed to start the timer. The timer is reset when both SCL and SDA/SDAI are pulled high. If the SCL pin or the SDA/SDAI pin is held low for over 33ms, the stuck-bus timer will expire and the internal I²C state machine will be reset to allow normal communication after the stuck-bus condition is cleared. The stuck-bus timer can be disabled by clearing control register bit G2.

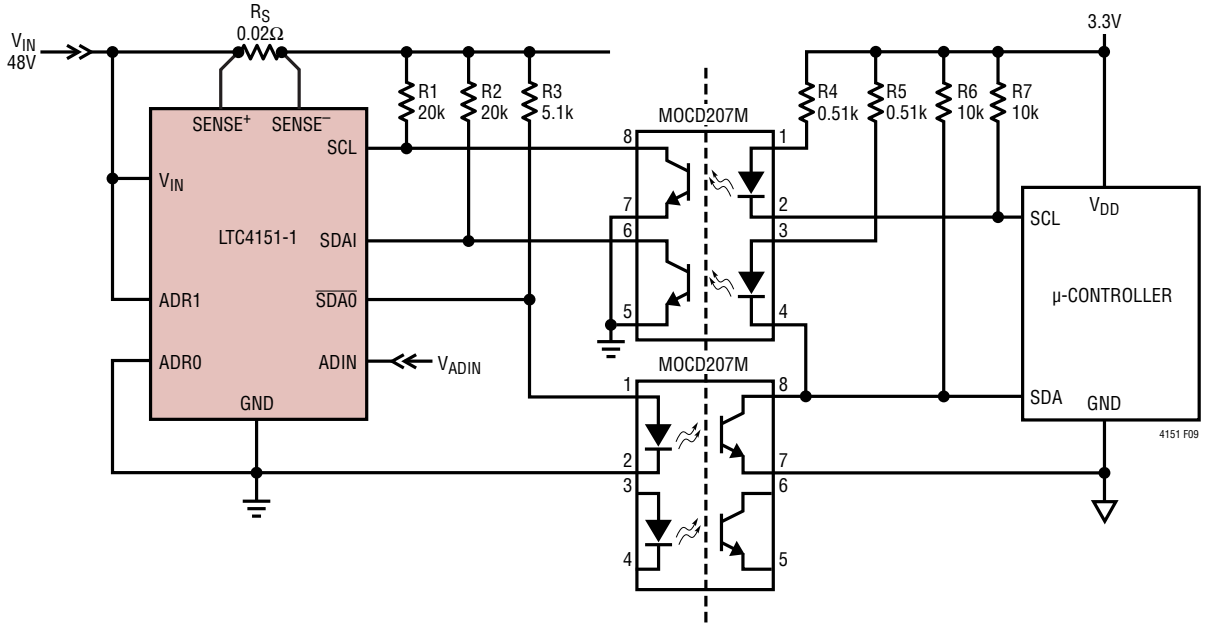


Figure 9. Opto-Isolation of the I²C Interface Between LTC4151-1 and a Microcontroller (1.5kHz Data Rate of I²C is Limited by Slew Rate of Opto-Isolators)

APPLICATIONS INFORMATION

I²C Device Addressing

Nine distinct I²C bus addresses are configurable using the three-state pins ADR0 and ADR1, as shown in Table 1. Address bits a6, a5 and a4 are configured to (110) and the least significant bit is the R/$\overline{W}$ bit. In addition, the LTC4151 will respond to a mass write address (1100 110) b for writing to all LTC4151s, regardless of their individual address settings.

Acknowledge

The acknowledge signal is used for handshaking between the transmitter and the receiver to indicate that the last byte of data was received. The transmitter always releases the SDA line during the acknowledge clock pulse. The LTC4151 pulls the SDA line low on the 9th clock cycle to acknowledge receipt of the data. If the slave fails to acknowledge by leaving SDA high, then the master can abort the transmission by generating a Stop condition. When the master is receiving data from the slave, the master must pull down the SDA line during the clock pulse to indicate receipt of a data byte, and that another byte is to be read. After the last byte has been received the master will leave the SDA line high (not acknowledge) and issue a Stop condition to terminate the transmission.

Write Protocol

The master begins a write operation with a Start condition followed by the seven bit slave address and the R/$\overline{W}$ bit set to zero. After the addressed LTC4151 acknowledges the address byte, the master then sends a command byte which indicates which internal register the master wishes to write. The LTC4151 acknowledges this and then latches the lower three bits of the command byte into its internal register address pointer. The master then delivers the data byte and the LTC4151 acknowledges once more and latches the data into its internal register. If the master continues sending a second byte or more data bytes, as in a Write Word or Write Page command, the second byte or more data bytes will be acknowledged by the LTC4151, the internal register address pointer will increment automatically, and each byte of data will be latched into an internal register corresponding to the address pointer. The write operation terminates and the register address pointer resets to 00h when the master sends a Stop condition.

Read Protocol

The master begins a read operation with a Start condition followed by the seven bit slave address and the R/$\overline{W}$ bit set to zero. After the addressed LTC4151 acknowledges the address byte, the master then sends a command byte that indicates which internal register the master wishes to read. The LTC4151 acknowledges this and then latches the lower three bits of the command byte into its internal register address pointer. The master then sends a repeated Start condition followed by the same seven bit

Table 1. LTC4151 Device Addressing*

DESCRIPTION	HEX DEVICE ADDRESS	BINARY DEVICE ADDRESS								LTC4151 ADDRESS PINS	
	h	a6	a5	a4	a3	a2	a1	a0	R/$\overline{W}$	ADR1	ADR0
Mass Write	CC	1	1	0	0	1	1	0	0	X	X
0	CE	1	1	0	0	1	1	1	X	H	L
1	D0	1	1	0	1	0	0	0	X	NC	H
2	D2	1	1	0	1	0	0	1	X	H	H
3	D4	1	1	0	1	0	1	0	X	NC	NC
4	D6	1	1	0	1	0	1	1	X	NC	L
5	D8	1	1	0	1	1	0	0	X	L	H
6	DA	1	1	0	1	1	0	1	X	H	NC
7	DC	1	1	0	1	1	1	0	X	L	NC
8	DE	1	1	0	1	1	1	1	X	L	L

*H = Tie High; L = Tie to GND; NC = Open; X = Don't Care

APPLICATIONS INFORMATION

Table 2. LTC4151 Register Address and Contents

REGISTER ADDRESS*	REGISTER NAME	READ/WRITE	DESCRIPTION
00h	SENSE (A)	R/W**	ADC Current Sense Voltage Data (8 MSBs)
01h	SENSE (B)	R/W**	ADC Current Sense Voltage Data (4 LSBs)
02h	V_{IN} (C)	R/W**	ADC V_{IN} Voltage Data (8 MSBs)
03h	V_{IN} (D)	R/W**	ADC V_{IN} Voltage Data (4 LSBs)
04h	ADIN (E)	R/W**	ADC ADIN Voltage Data (8 MSBs)
05h	ADIN (F)	R/W**	ADC ADIN Voltage Data (4 LSBs)
06h	CONTROL (G)	R/W	Controls ADC Operation Mode and Test Mode
07h	Reserved		

*Register address MSBs b7-b3 are ignored. **Writable if bit G4 is set.

Table 3. SENSE Registers A (00h) and B (01h)—Read/Write

BIT	NAME	OPERATION
A7:0, B7:4	SENSE Voltage Data	12-Bit Data of Current Sense Voltage with 20µV LSB and 81.92mV Full-Scale
B3	ADC Busy in Snapshot Mode	1 = SENSE Being Converted; 0 = SENSE Conversion Completed. Not Writable
B2:0	Reserved	Always Returns 0. Not Writable

Table 4. V_{IN} Registers C (02h) and D (03h)—Read/Write

BIT	NAME	OPERATION
C7:0, D7:4	V_{IN} Voltage Data	12-Bit Data of V_{IN} Voltage with 25mV LSB and 102.4V Full-Scale
D3	ADC Busy in Snapshot Mode	1 = V_{IN} Being Converted; 0 = V_{IN} Conversion Completed. Not Writable
D2:0	Reserved	Always Returns 0, Not Writable

Table 5. ADIN Registers E (04h) and F (05h)—Read/Write

BIT	NAME	OPERATION
E7:0, F7:4	ADIN Voltage Data	12-Bit Data of Current Sense Voltage with 500µV LSB and 2.048V Full-Scale
F3	ADC Busy in Snapshot Mode	1 = ADIN Being Converted; 0 = ADIN Conversion Completed. Not Writable
F2:0	Reserved	Always Returns 0, Not Writable

Table 6. CONTROL Register G (06h)—Read/Write

<table>
<tr><th>BIT</th><th>NAME</th><th>OPERATION</th></tr>
<tr><td>G7</td><td>ADC Snapshot Mode Enable</td><td>Enables ADC Snapshot Mode; 1 = Snapshot Mode Enabled. Only the channel selected by G6 and G5 is measured by the ADC. After the conversion, the channel busy bit is reset and the ADC is halted.
0 = Snapshot Mode Disabled (ADC free running, Default).</td></tr>
<tr><td>G6</td><td>ADC Channel Label for Snapshot Mode</td><td rowspan="2">ADC Channel Label for Snapshot Mode
<table><tr><th>G6</th><th>G5</th><th>ADC CHANNEL</th></tr><tr><td>0</td><td>0</td><td>SENSE (Default)</td></tr><tr><td>0</td><td>1</td><td>V_{IN}</td></tr><tr><td>1</td><td>0</td><td>ADIN</td></tr></table></td></tr>
<tr><td>G5</td><td>ADC Channel Label for Snapshot Mode</td></tr>
<tr><td>G4</td><td>Test Mode Enable</td><td>Test Mode Halts ADC Operation and Enables Writes to ADC Registers; 1 = Enable Test Mode,
0 = Disable Test Mode (Default)</td></tr>
<tr><td>G3</td><td>Page Read/Write Enable</td><td>Enables Page Read/Write; 1 = Enable I^2C Page Read/Write (Default), 0 = Disable I^2C Page Read/Write</td></tr>
<tr><td>G2</td><td>Stuck-Bus Timer Enable</td><td>Enables I^2C Stuck-Bus Reset Timer; 1 = Enable Stuck-Bus Timer (Default), 0 = Disable Stuck-Bus Timer</td></tr>
<tr><td>G1:0</td><td>Reserved</td><td>Always Returns 0, Not Writable</td></tr>
</table>

APPLICATIONS INFORMATION

address with the R/$\overline{W}$ bit now set to one. The LTC4151 acknowledges and sends the contents of the requested register. The transmission terminates when the master sends a Stop condition. If the master acknowledges the transmitted data byte, as in a Read Word command, the LTC4151 will send the contents of the next register. If the master acknowledges the second data byte and each of the following (if more) data bytes, as in a Read Page command, the LTC4151 will keep sending out each data byte in the register that corresponds to the incrementing register pointer. The read operation terminates and the register address pointer resets to 00h when the master sends a Stop condition.

Layout Considerations

A Kelvin connection between the sense resistor R_S and the LTC4151 is recommended to achieve accurate current sensing (Figure 10). The minimum trace width for 1oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. Using 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 530µΩ per square.

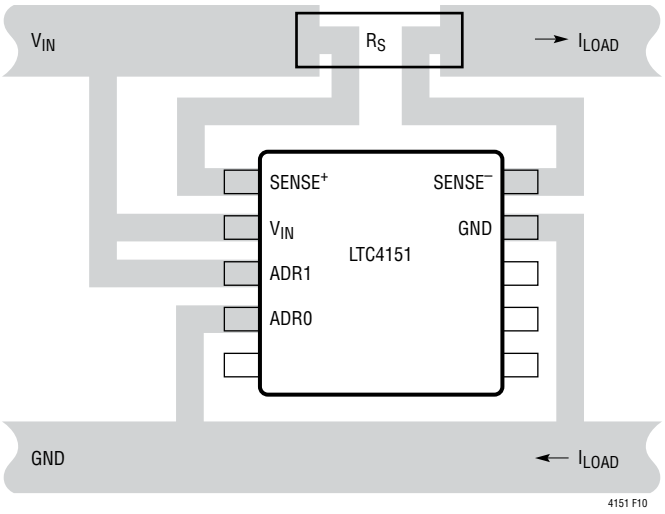


Figure 10. Recommended Layout for Kelvin Connection

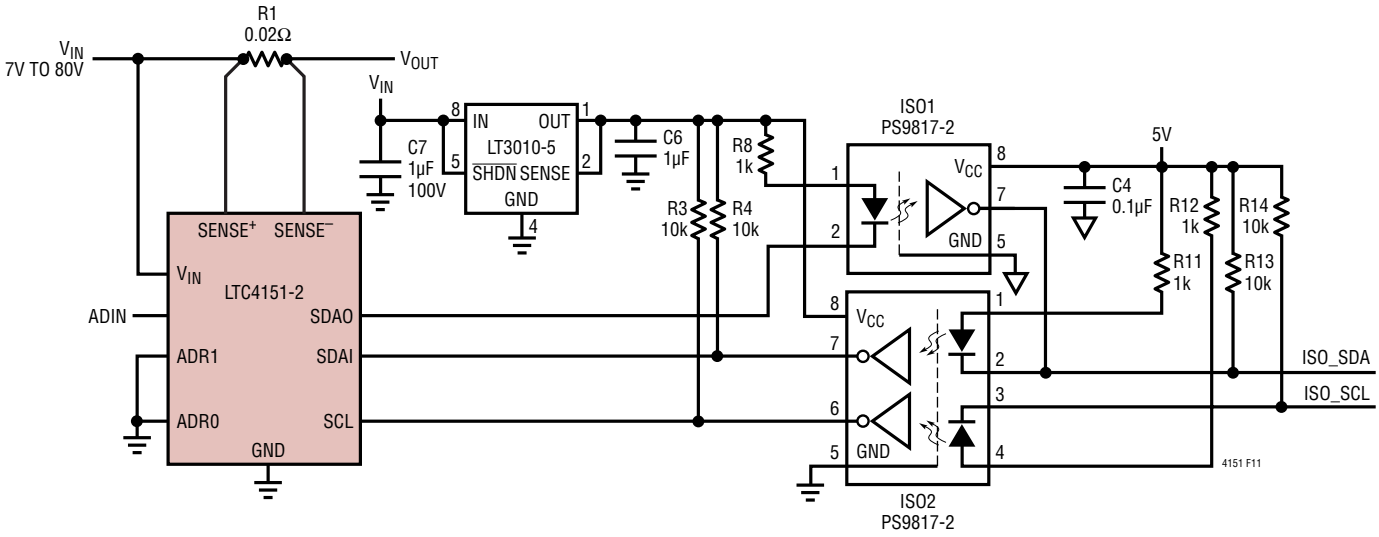
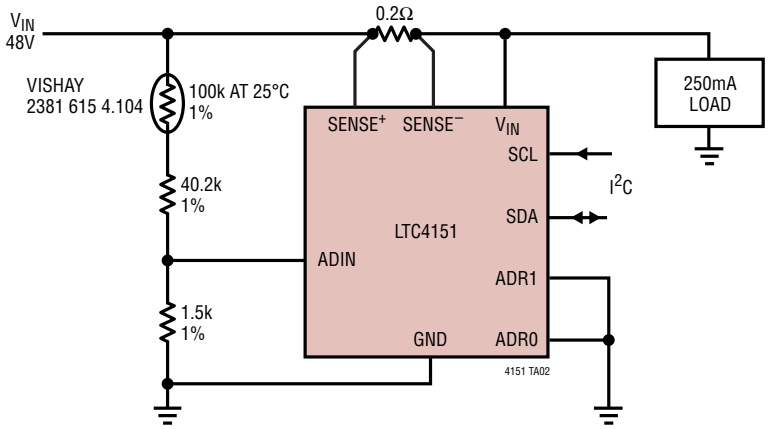


Figure 11. LTC4151-2 I²C Opto-Isolation Interface with High Speed Opto-Couplers

TYPICAL APPLICATION

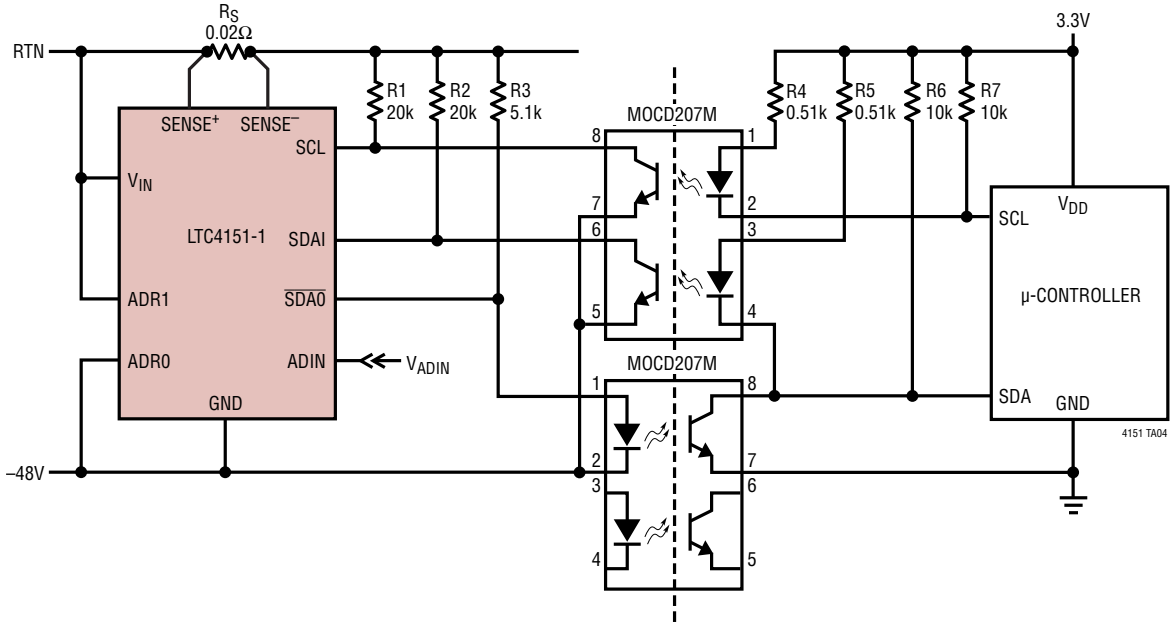
Temperature Monitoring with an NTC Thermistor While Measuring Load Current and LTC4151 Supply Current



$T(°C) = 58.82 \bullet (N_{ADIN}/N_{VIN} - 0.1066)$, 20°C < T < 60°C.

N_{ADIN} AND N_{VIN} ARE DIGITAL CODES MEASURED BY THE ADC AT THE ADIN AND V_{IN} PINS, RESPECTIVELY.

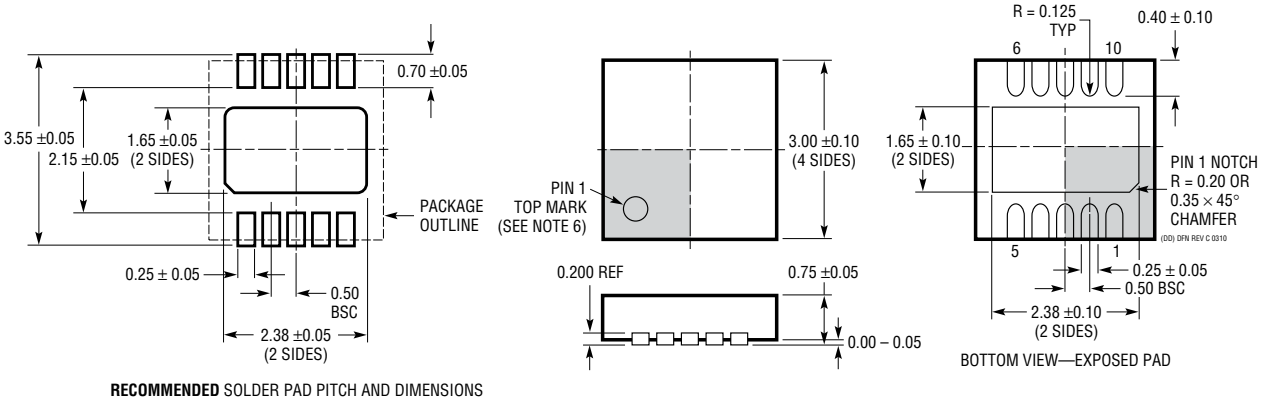
LTC4151-1 Monitors Current and Input Voltage of a –48V System and Interfaces with a Microcontroller (1.5kHz Data Rate of I²C is Limited by Slew Rate of Opto-Isolators)



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

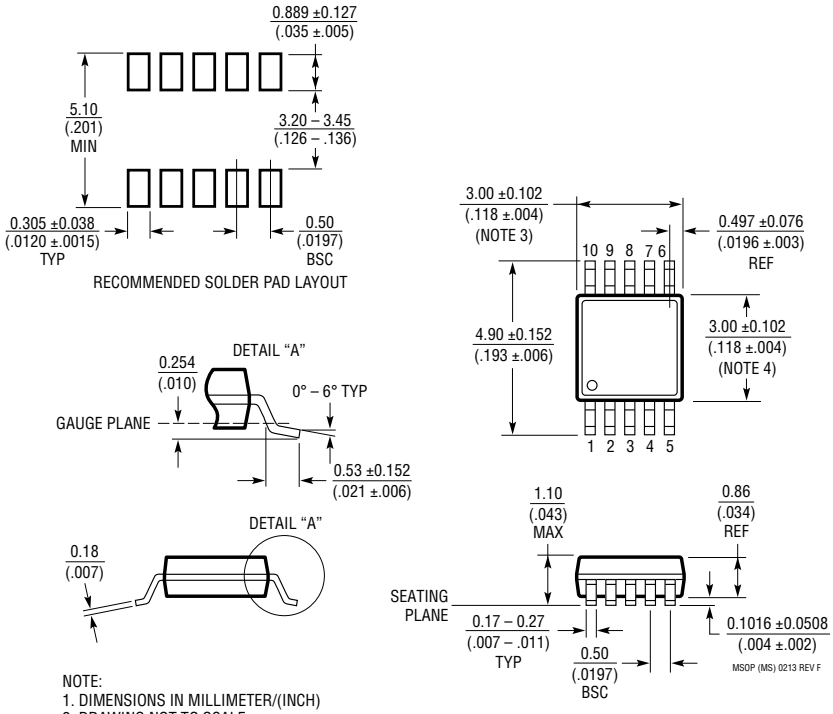
DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661 Rev F)

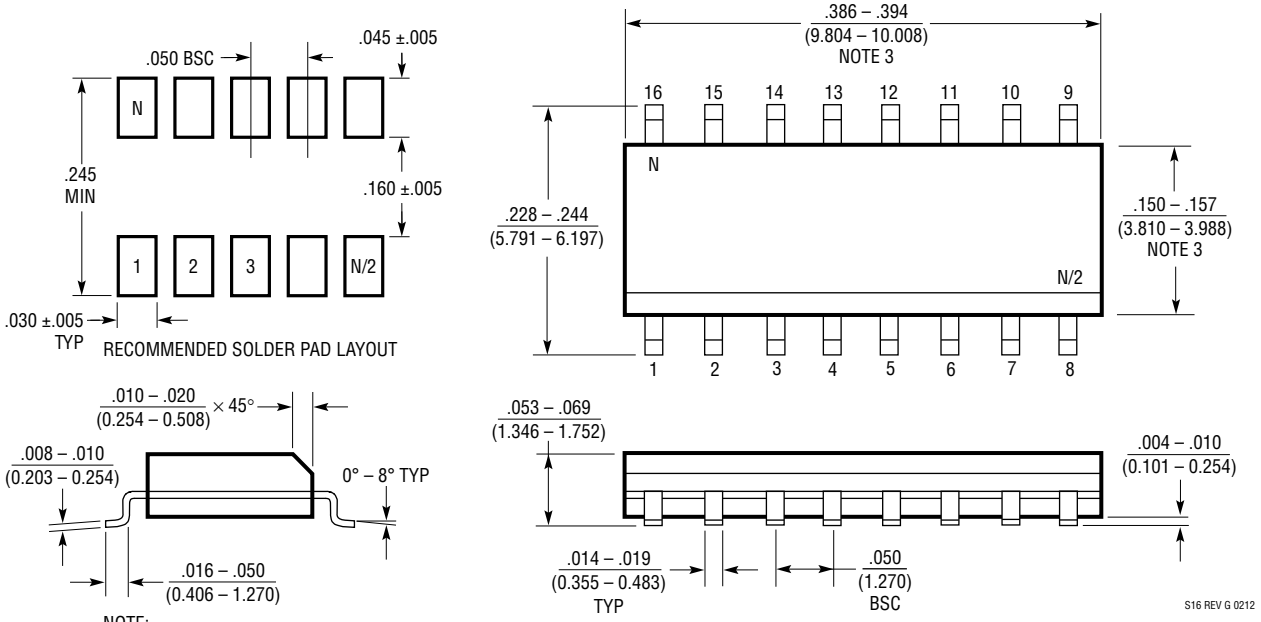


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S Package
16-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



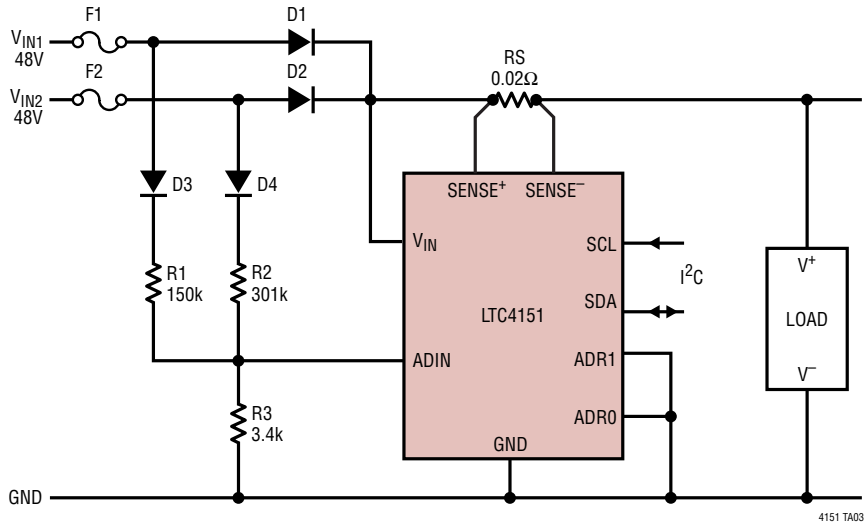
NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	11/10	Added H-grade information	2, 3
		Revised order of Pin Functions section and added information to SDAI pin description	6
		Added diode and 2k resistor to Block Diagram	7
		Added information to Application Information section	10
D	7/12	Changed part number in Pin Configuration section from LT4151 to LTC4151	2
E	11/12	Added –48V application schematic	14
F	3/14	Increased $V_{ADR(H)}$ MAX limit and decreased $V_{ADR(L)}$ MIN limit	4

TYPICAL APPLICATION

High Side Current, Input Voltage and Open Fuse Monitoring with a Single LTC4151



CONDITION	RESULT
$N_{ADIN} \geq 1.375 \bullet N_{VIN}$	Normal Operation
$0.835 \bullet N_{VIN} \leq N_{ADIN} < 1.375 \bullet N_{VIN}$	F2 is Open
$0.285 \bullet N_{VIN} \leq N_{ADIN} < 0.835 \bullet N_{VIN}$	F1 is Open
(Not Responding)	Both F1 and F2 are Open

V_{IN1} AND V_{IN2} ARE WITHIN 20% APART. N_{ADIN} AND N_{VIN} ARE DIGITAL CODES MEASURED BY THE ADC AT THE ADIN AND V_{IN} PINS, RESPECTIVELY.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT2940	Power and Current Monitor	Four-Quadrant Multiplication, ±5% Power Accuracy, 4V to 80V Operation
LTC2945	Wide Range I²C Power Monitor	0V to 80V Input Range, 2.7V to 80V Supply Range, Shunt Regulator, 12-Bit ADC with ±0.75% TUE
LTC2451	16-Bit I²C Ultra Tiny Delta Sigma ADC	Single-Ended Input, 0 to V_{CC} Input Range, 60Hz Output Rate, 3mm × 2mm DFN-8 Package
LTC2453	16-Bit I²C Ultra Tiny Delta Sigma ADC	Differential Input, $\pm V_{CC}$ Input Range, 60Hz Output Rate, 3mm × 2mm DFN-8 Package
LTC2970	Power Supply Monitor and Margining Controller	14-Bit ADC Monitoring Current and Voltages, Supplies from 8V to 15V
LTC4215	Positive Hot Swap™ Controller with ADC and I²C	8-Bit ADC Monitoring Current and Voltages, Supplies from 2.9V to 15V
LTC4260	Positive High Voltage Hot Swap Controller with ADC and I²C	8-Bit ADC Monitoring Current and Voltages, Supplies from 8.5V to 80V
LTC4261/ LTC4261-2	Negative High Voltage Hot Swap Controller with ADC and I²C	10-Bit ADC Monitoring Current and Voltages, Supplies from –12V
LTC6101/ LTC6101HV	High Voltage, High Side Current Sense Amplifier in SOT-23 Package	Supplies from 4V to 60V (LTC6101) and 5V to 100V (LTC6101HV)

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LTC4151
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