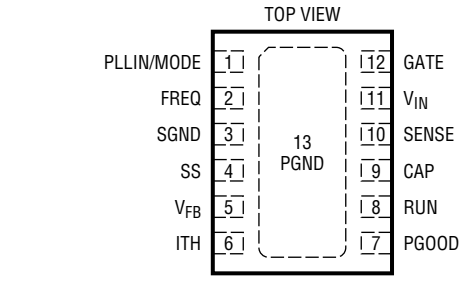
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3V to 65V
V_{IN}-V_{SENSE} Voltage ..... –0.3V to 6V
V_{IN}-V_{CAP} Voltage ..... –0.3V to 10V
RUN Voltage ..... –0.3V to 65V
PGOOD, PLLIN/MODE Voltages ..... –0.3V to 6V
SS, ITH, FREQ, V_{FB} Voltages ..... –0.3V to 5V

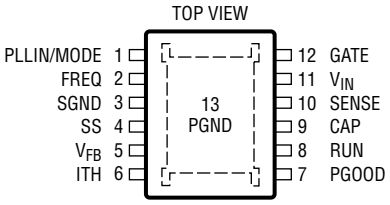
Operating Junction Temperature Range (Notes 2, 3, 4)
LTC3864E,I ..... –40°C to 125°C
LTC3864H ..... –40°C to 150°C
LTC3864MP ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP Package ..... 300°C

PIN CONFIGURATION



DE PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 5.5°C/W
EXPOSED PAD (PIN 13) IS PGND, MUST BE SOLDERED TO PCB FOR OPTIMAL THERMAL PERFORMANCE



MSE PACKAGE
12-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 13) IS PGND, MUST BE SOLDERED TO PCB FOR OPTIMAL THERMAL PERFORMANCE

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3864EMSE#PBF	LTC3864EMSE#TRPBF	3864	12-Lead Plastic MSOP	–40°C to 125°C
LTC3864IMSE#PBF	LTC3864IMSE#TRPBF	3864	12-Lead Plastic MSOP	–40°C to 125°C
LTC3864HMSE#PBF	LTC3864HMSE#TRPBF	3864	12-Lead Plastic MSOP	–40°C to 150°C
LTC3864MPMSE#PBF	LTC3864MPMSE#TRPBF	3864	12-Lead Plastic MSOP	–55°C to 150°C
LTC3864EDE#PBF	LTC3864EDE#TRPBF	3864	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3864IDE#PBF	LTC3864IDE#TRPBF	3864	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3864HDE#PBF	LTC3864HDE#TRPBF	3864	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 150°C
LTC3864MPDE#PBF	LTC3864MPDE#TRPBF	3864	12-Lead (4mm × 3mm) Plastic DFN	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4) V_{IN} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply							
V_{IN}	Input Voltage Operating Range			3.5		60	V
V_{UVLO}	Undervoltage Lockout	(V_{IN}-V_{CAP}) Ramping Up Threshold (V_{IN}-V_{CAP}) Ramping Down Threshold Hysteresis	● ●	3.25 3.00	3.50 3.25 0.25	3.8 3.50	V V V
I_Q	Input DC Supply Current						
	Pulse-Skipping Mode	PLLIN/MODE = 0V, FREQ = 0V, V_{FB} = 0.83V (No Load)			0.77	1.2	mA
	Burst Mode Operation	PLLIN/MODE = Open, FREQ = 0V, V_{FB} = 0.83V (No Load)			40	60	µA
	Shutdown Supply Current	RUN = 0V			7	12	µA
Output Sensing							
V_{REG}	Regulated Feedback Voltage	V_{ITH} = 1.2V (Note 5)	●	0.792	0.800	0.809	V
$\frac{\Delta V_{REG}}{\Delta V_{IN}}$	Feedback Voltage Line Regulation	V_{IN} = 3.8V to 60V (Note 5)		–0.005		0.005	%/V
$\frac{\Delta V_{REG}}{\Delta V_{ITH}}$	Feedback Voltage Load Regulation	V_{ITH} = 0.6V to 1.8V (Note 5)		–0.1	–0.015	0.1	%
$g_{m(EA)}$	Error Amplifier Transconductance	V_{ITH} = 1.2V, ΔI_{ITH} = ±5µA (Note 5)			1.8		mS
I_{FB}	Feedback Input Bias Current			–50	–10	50	nA
Current Sensing							
V_{ILIM}	Current Limit Threshold (V_{IN}-V_{SENSE})	V_{FB} = 0.77V	●	85	95	103	mV
I_{SENSE}	SENSE Pin Input Current	V_{SENSE} = V_{IN}			0.1	2	µA
Start-Up and Shutdown							
V_{RUN}	RUN Pin Enable Threshold	V_{RUN} Rising	●	1.22	1.26	1.32	V
V_{RUNHYS}	RUN Pin Hysteresis				150		mV
I_{SS}	Soft-Start Pin Charging Current	V_{SS} = 0V			10		µA
Switching Frequency and Clock Synchronization							
f	Programmable Switching Frequency	R_{FREQ} = 24.9kΩ R_{FREQ} = 64.9kΩ R_{FREQ} = 105kΩ		375	105 440 810	505	kHz kHz kHz
f_{LO}	Low Switching Frequency	FREQ = 0V		320	350	380	kHz
f_{HI}	High Switching Frequency	FREQ = Open		485	535	585	kHz
f_{SYNC}	Synchronization Frequency		●	75		750	kHz
$V_{CLK(IH)}$	Clock Input High Level into PLLIN/MODE		●	2			V
$V_{CLK(LO)}$	Clock Input Low Level into PLLIN/MODE		●			0.5	V
f_{FOLD}	Foldback Frequency as Percentage of Programmable Frequency	V_{FB} = 0V, FREQ = 0V			18		%
$t_{ON(MIN)}$	Minimum On-Time				220		ns
Gate Driver							
V_{CAP}	Gate Bias LDO Output Voltage (V_{IN}-V_{CAP})	I_{GATE} = 0mA	●	7.6	8.0	8.5	V
$V_{CAPDROP}$	Gate Bias LDO Dropout Voltage	V_{IN} = 5V, I_{GATE} = 15mA			0.2	0.5	V
$\Delta V_{CAP(LINE)}$	Gate Bias LDO Line Regulation	9V ≤ V_{IN} ≤ 60V, I_{GATE} = 0mA			0.002	0.03	%/V
$\Delta V_{CAP(LOAD)}$	Gate Bias LDO Load Regulation	Load = 0mA to 20mA		–3.5			%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4) V_{IN} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
R_{UP}	Gate Pull-Up Resistance	Gate High			2		Ω
R_{DN}	Gate Pull-Down Resistance	Gate Low			0.9		Ω
PGOOD and Overvoltage							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.2	0.4	V
I_{PG}	PGOOD Leakage Current	V_{PGOOD} = 5V				1	µA
%PGD	PGOOD Trip Level	V_{FB} Ramping Negative with Respect to V_{REG} Hysteresis		–13	–10 2.5	–7	% %
		V_{FB} Ramping Positive with Respect to V_{REG} Hysteresis		7	10 2.5	13	% %
t_{PGDLY}	PGOOD Delay	PGOOD Going High to Low PGOOD Going Low to High			100 100		µs µs
V_{FBOV}	V_{FB} Overvoltage Lockout Threshold	GATE Going High without Delay, $V_{FB(OV)}$-$V_{FB(NOM)}$ in Percent			10		%

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Continuous operation above the specified maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 3: The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) as follows:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

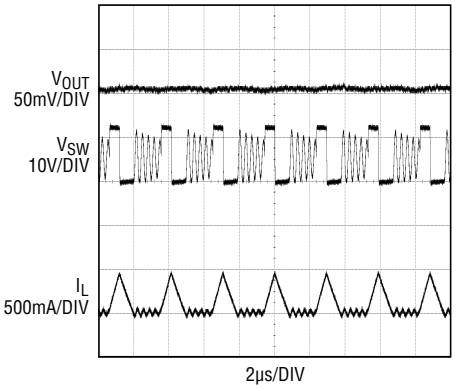
where θ_{JA} (in °C/W) is the package thermal impedance provided in the Pin Configuration section for the corresponding package.

Note 4: The LTC3864 is tested under pulsed loading conditions such that $T_J \approx T_A$. The LTC3864E is guaranteed to meet performance specifications from 0°C to 85°C operating junction temperature range. The LTC3864E specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3864I is guaranteed to meet performance specifications over the –40°C to 125°C operating junction temperature range, the LTC3864H is guaranteed over the –40°C to 150°C operating junction temperature range, and the LTC3864MP is guaranteed and tested over the full –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 5: The LTC3864 is tested in a feedback loop that adjust V_{FB} to achieve a specified error amplifier output voltage (on ITH pin).

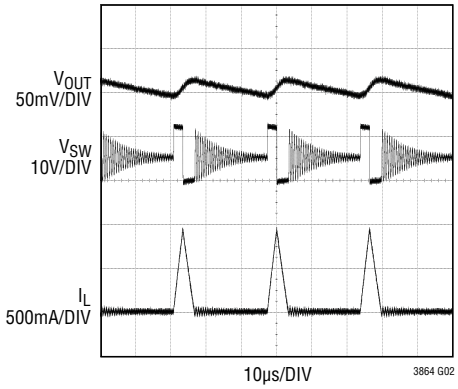
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Pulse-Skipping Mode Operation Waveforms



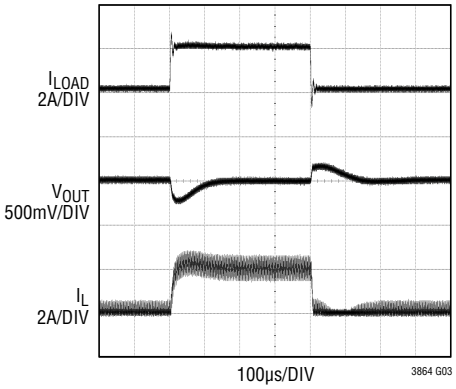
V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 100mA
FIGURE 8 CIRCUIT

Burst Mode Operation Waveforms



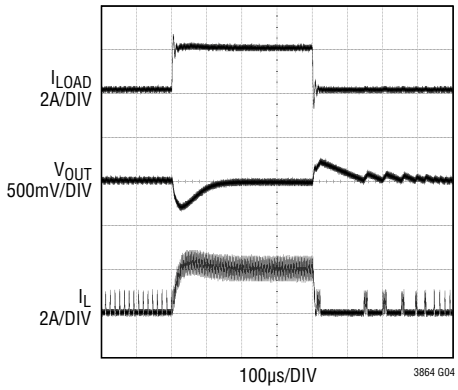
V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 100mA
FIGURE 8 CIRCUIT

Transient Response: Pulse-Skipping Mode Operation



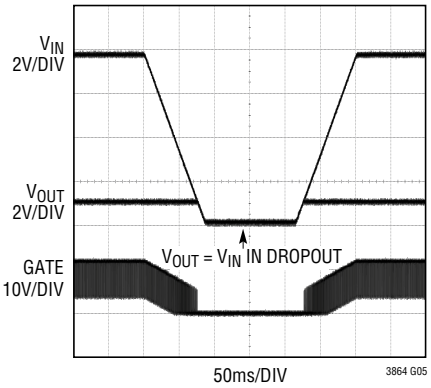
V_{IN} = 12V
V_{OUT} = 5V
TRANSIENT = 100mA TO 2A
FIGURE 8 CIRCUIT

Transient Response: Burst Mode Operation



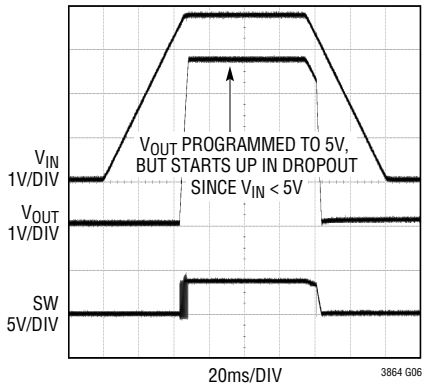
V_{IN} = 12V
V_{OUT} = 5V
TRANSIENT = 100mA TO 2A
FIGURE 8 CIRCUIT

Dropout Behavior (100% Duty Cycle)



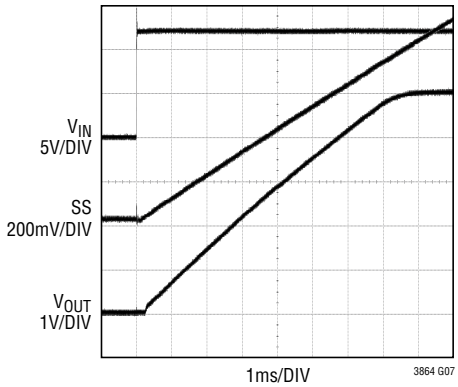
V_{IN} TRANSIENT: 12V TO 4V
AND BACK TO 12V
V_{OUT} = 5V, I_{LOAD} = 100mA, FIGURE 8 CIRCUIT

Low V_{IN} Operation



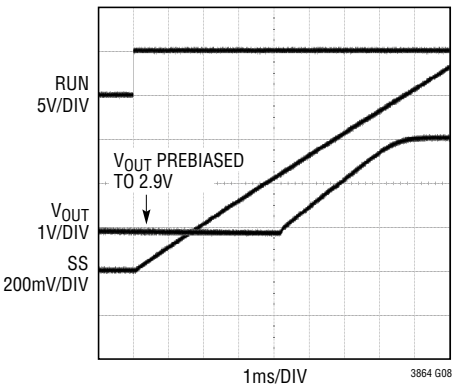
V_{IN} = 0V TO 3.8V
THEN BACK TO 0V
I_{LOAD} = 100mA
FIGURE 8 CIRCUIT

Normal Soft Start-Up



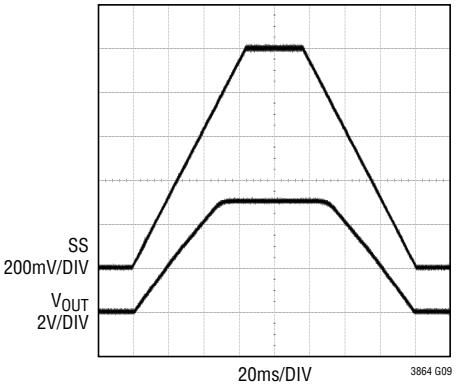
V_{IN} = 12V, V_{OUT} = 5V
FIGURE 8 CIRCUIT

Soft Start-Up into a Prebiased Output



V_{IN} = 12V, V_{OUT} = 5V
I_{LOAD} = 0.5mA
FIGURE 8 CIRCUIT

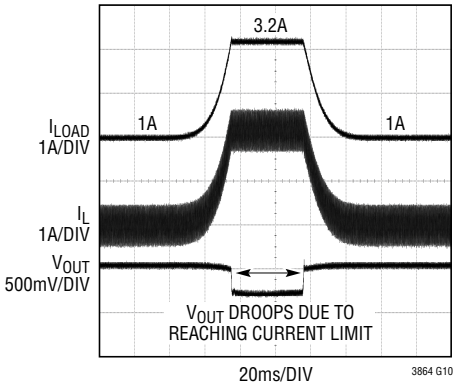
Output Tracking



V_{IN} = 12V, V_{OUT} = 5V
I_{LOAD} = 100mA
FIGURE 8 CIRCUIT

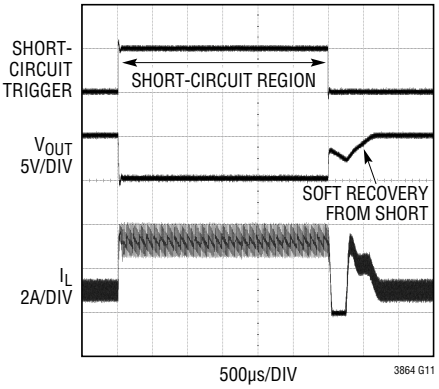
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Overcurrent Protection



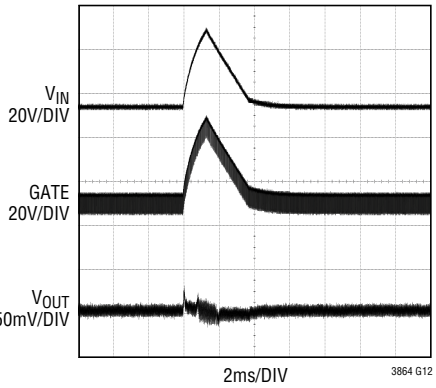
V_{IN} = 12V, V_{OUT} = 5V
FIGURE 8 CIRCUIT

Short-Ciruit Protection



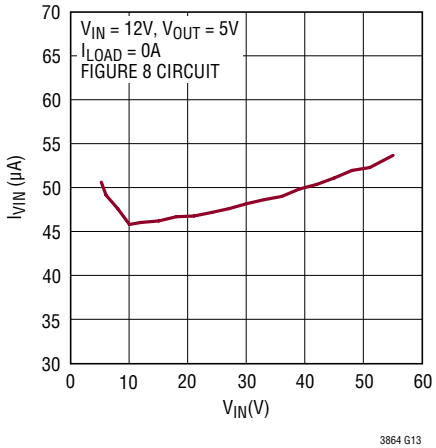
V_{IN} = 12V, V_{OUT} = 5V
FIGURE 8 CIRCUIT

V_{IN} Line Transient Behavior

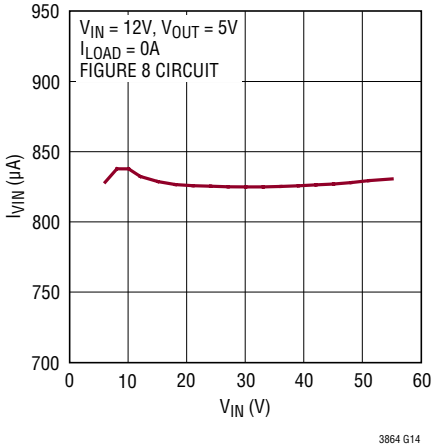


V_{IN} = 12V, SURGE TO 48V
V_{OUT} = 5V
I_{LOAD} = 200mA, FIGURE 8 CIRCUIT

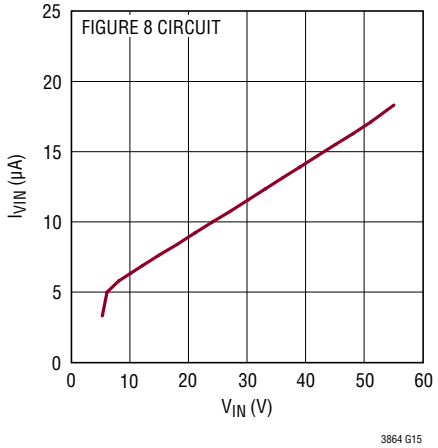
Burst Mode Input Current Over Input Voltage (No Load)



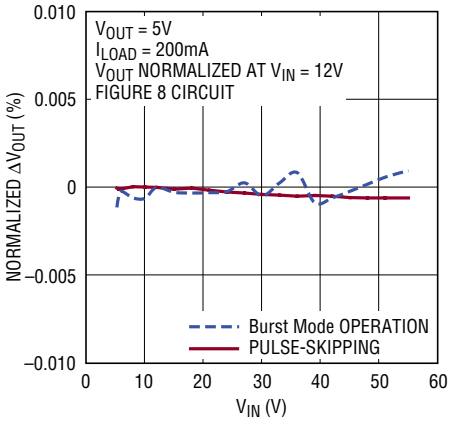
Pulse-Skipping Mode Input Current Over Input Voltage (No Load)



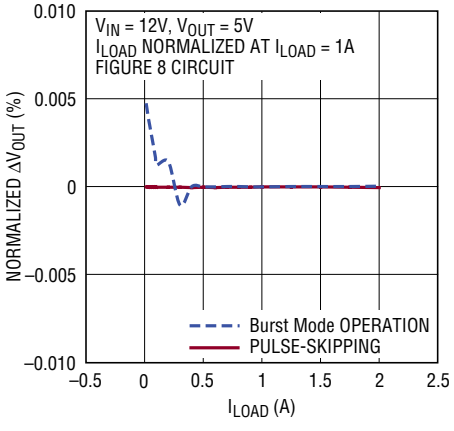
Shutdown Current Over Input Voltage



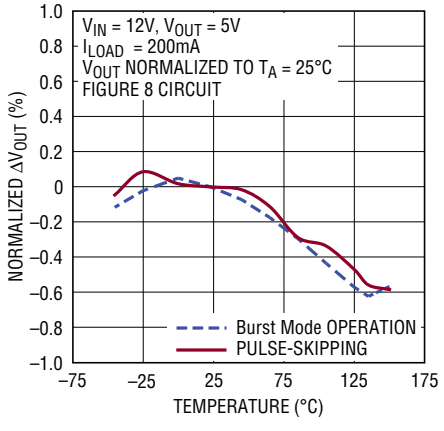
Output Regulation Over Input Voltage



Output Regulation Over Load Current



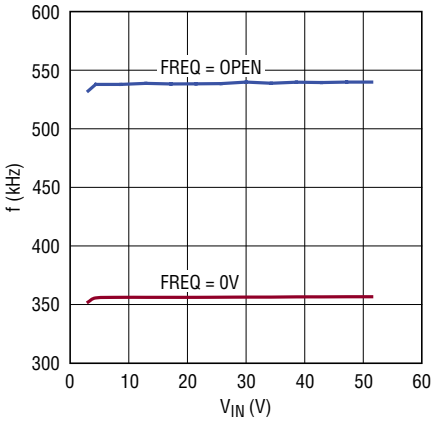
Output Regulation Over Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

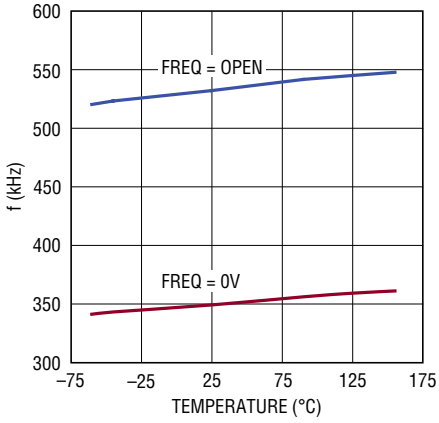
T_A = 25°C, unless otherwise noted.

Free Running Frequency Over Input Voltage



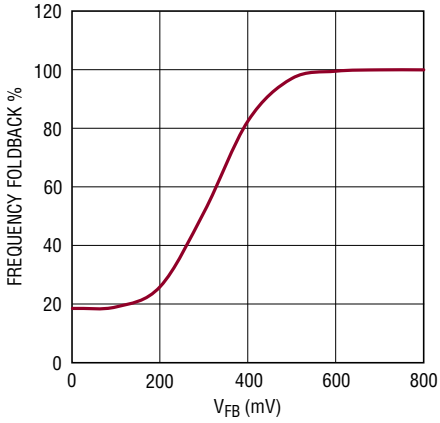
3864 G19

Free Running Frequency Over Temperature



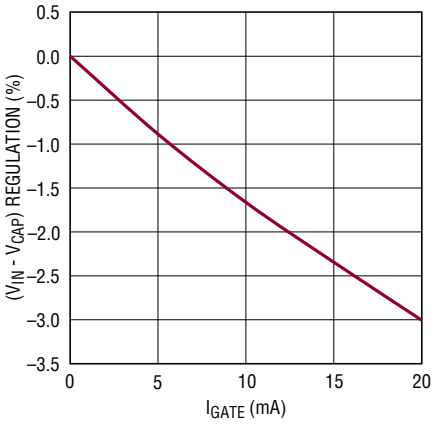
3864 G20

Frequency Foldback % Over Feedback Voltage



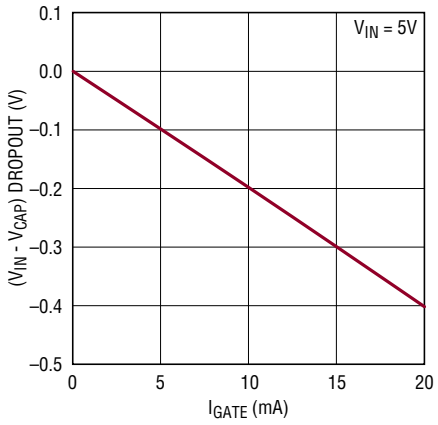
3864 G21

GATE Bias LDO (V_{IN} - V_{CAP}) Load Regulation



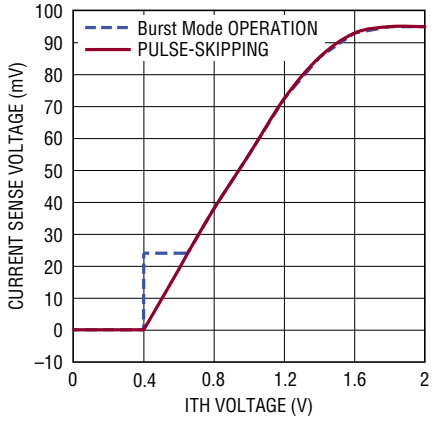
3864 G22

GATE Bias LDO (V_{IN} - V_{CAP}) Dropout Behavior



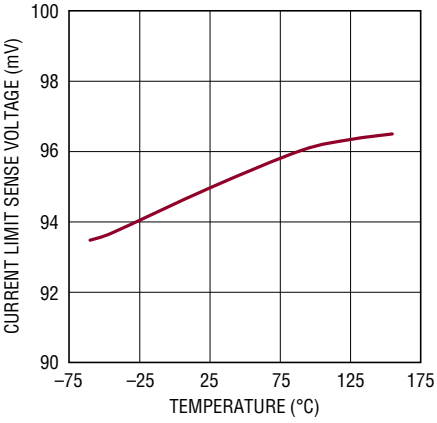
3864 G23

Current Sense Voltage Over ITH Voltage



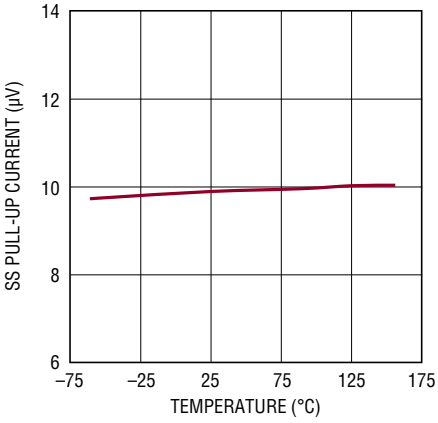
3864 G24

Current Sense Voltage Over Temperature



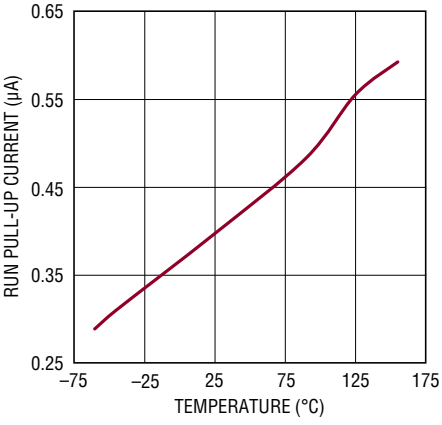
3864 G25

SS Pin Pull-Up Current Over Temperature



3864 G26

RUN Pin Pull-Up Current Over Temperature



3864 G27

PIN FUNCTIONS

PLLIN/MODE (Pin 1): External Reference Clock Input and Burst Mode Enable/Disable. When an external clock is applied to this pin, the internal phase-locked loop will synchronize the turn-on edge of the gate drive signal with the rising edge of the external clock. When no external clock is applied, this input determines the operation during light loading. Floating this pin selects low I_Q (40µA) Burst Mode operation. Pulling to ground selects pulse-skipping mode operation.

FREQ (Pin 2): Switching Frequency Set Point Input. The switching frequency is programmed by an external set-point resistor R_{FREQ} connected between the FREQ pin and signal ground. An internal 20µA current source creates a voltage across the external setpoint resistor to set the internal oscillator frequency. Alternatively, this pin can be driven directly by a DC voltage to set the oscillator frequency. Grounding selects a fixed operating frequency of 350kHz. Floating selects a fixed operating frequency of 535kHz.

SGND (Pin 3): Ground Reference for Small Signal Analog Component (Signal Ground). Signal ground should be used as the common ground for all small signal analog inputs and compensation components. Connect signal ground to power ground (ground reference for power components) only at one point using a single PCB trace.

SS (Pin 4): Soft-Start and External Tracking Input. The LTC3864 regulates the feedback voltage to the smaller of 0.8V or the voltage on the SS pin. An internal 10µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to the final regulated output voltage. Alternatively, another voltage supply connected through a resistor divider to this pin allows the output to track the other supply during start-up.

V_{FB} (Pin 5): Output Feedback Sense. A resistor divider from the regulated output point to this pin sets the output voltage. The LTC3864 will nominally regulate V_{FB} to the internal reference value of 0.8V. If V_{FB} is less than 0.4V, the switching frequency will linearly decrease and fold back to about one-fifth of the internal oscillator frequency to reduce the minimum duty cycle.

ITH (Pin 6): Current Control Threshold and Controller Compensation Point. This pin is the output of the error amplifier and the switching regulator's compensation point. The voltage ranges from 0V to 2.9V, with 0.8V corresponding to zero sense voltage (zero current).

PGOOD (Pin 7): Power Good Indicator Output. This open drain logic output is pulled to ground when the output voltage is outside of a ±10% window around the regulation point. The PGOOD switches states only after a 100µs delay.

RUN (Pin 8): Digital Run Control Input. A RUN voltage above the 1.26V threshold enables normal operation, while a voltage below the threshold shuts down the controller. An internal 0.4µA current source pulls the RUN pin up to about 3.3V. The RUN pin can be connected to an external power supply up to 60V.

CAP (Pin 9): Gate Driver (–) Supply. A low ESR ceramic bypass capacitor of at least 0.47µF or 10X the effective C_{MILLER} of the P-channel power MOSFET, is required from V_{IN} to this pin to serve as a bypass capacitor for the internal regulator. To insure stable low noise operation, the bypass capacitor should be placed adjacent to the V_{IN} and CAP pins and connected using the same PCB metal layer.

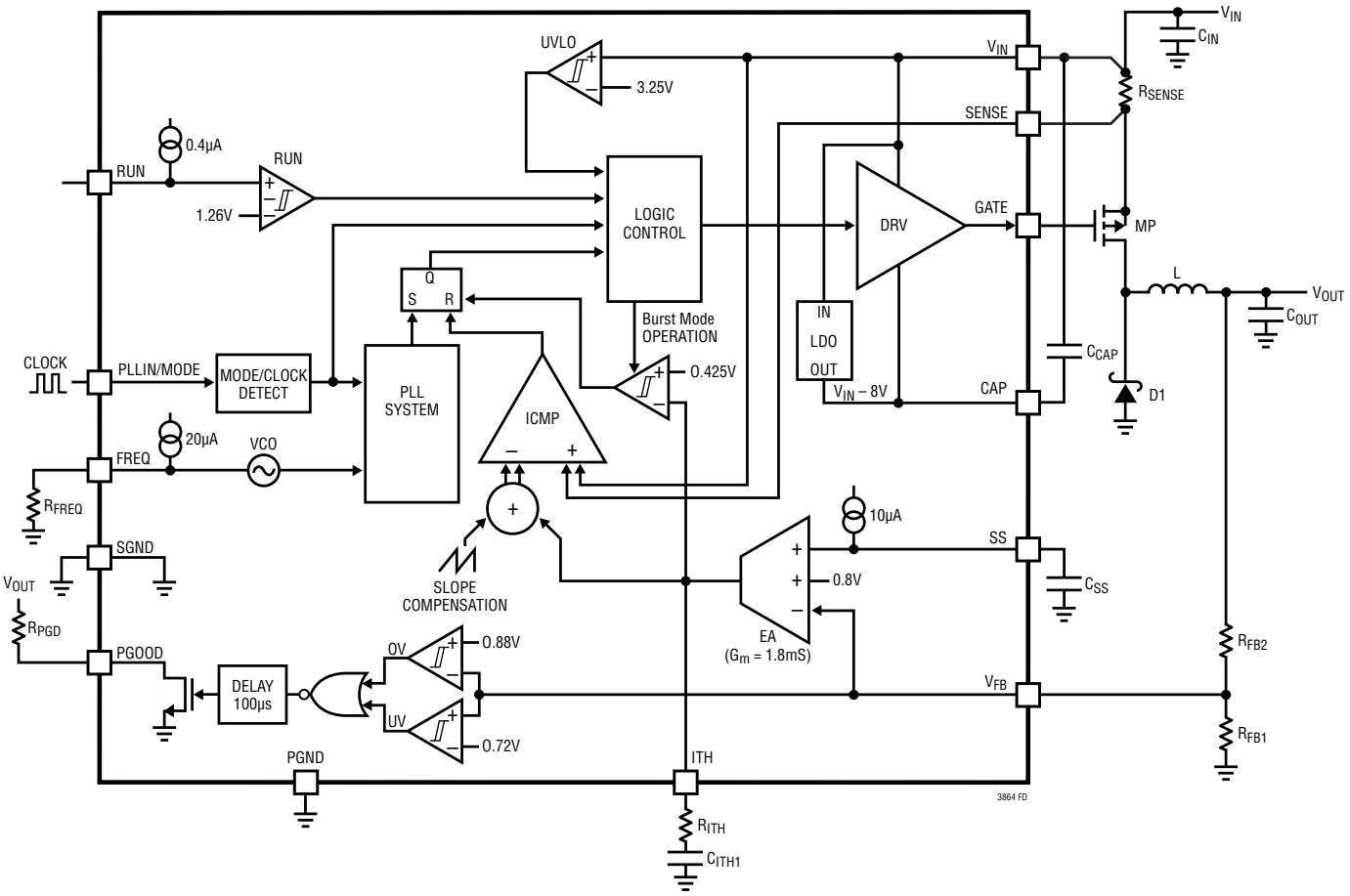
SENSE (Pin 10): Current Sense Input. A sense resistor R_{SENSE} from V_{IN} pin to the SENSE pin sets the maximum current limit. The peak inductor current limit is equal to 95mV/R_{SENSE}. For accuracy, it is important that the V_{IN} pin and the SENSE pin route directly to the current sense resistor and make a Kelvin (4-wire) connection.

V_{IN} (Pin 11): Chip Power Supply. A minimum bypass capacitor of 0.1µF is required from the V_{IN} pin to power ground. For best performance use a low ESR ceramic capacitor placed near the V_{IN} pin.

GATE (Pin 12): Gate Drive Output for External P-Channel MOSFET. The gate driver bias supply voltage (V_{IN}-V_{CAP}) is regulated to 8V when V_{IN} is greater than 8V. The gate driver is disabled when (V_{IN}-V_{CAP}) is less than 3.5V (typical), 3.8V maximum in startup and 3.25V (typical) 3.5V maximum in normal operation.

PGND (Exposed Pad Pin 13): Ground Reference for Power Components (Power Ground). The PGND exposed pad must be soldered to the circuit board for electrical contact and for rated thermal performance of the package. Connect signal ground to power ground only at one point using a single PCB trace.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop (Refer to Functional Diagram)

The LTC3864 uses a peak current-mode control architecture to regulate the output in an asynchronous step-down DC/DC switching regulator. The V_{FB} input is compared to an internal reference by a transconductance error amplifier (EA). The internal reference can be either a fixed 0.8V reference V_{REF} or the voltage input on the SS pin. In normal operation V_{FB} regulates to the internal 0.8V reference voltage. In soft-start or tracking mode, when the SS pin voltage is less than the internal 0.8V reference voltage, V_{FB} will regulate to the SS pin voltage. The error amplifier output connects to the ITH (current [I] threshold [TH]) pin. The voltage level on the ITH pin is then summed with a slope compensation ramp to create the peak inductor current set point.

The peak inductor current is measured through a sense resistor R_{SENSE} placed across the V_{IN} and SENSE pins. The resultant differential voltage from V_{IN} to SENSE is proportional to the inductor current and is compared to the peak inductor current set point. During normal operation the P-channel power MOSFET is turned on when the clock leading edge sets the SR latch through the S input. The P-channel MOSFET is turned off through the SR latch R input when the differential voltage from V_{IN} to SENSE is greater than the peak inductor current set point and the current comparator, ICMP, trips high.

Power CAP and V_{IN} Undervoltage Lockout (UVLO)

Power for the P-channel MOSFET gate driver is derived from the CAP pin. The CAP pin is regulated to 8V below V_{IN} in order to provide efficient P-channel operation. The power for the V_{CAP} supply comes from an internal LDO, which regulates the V_{IN}-CAP differential voltage. A minimum capacitance of 0.47µF (low ESR ceramic) is required between V_{IN} and CAP to assure stability.

For $V_{IN} \leq 8V$, the LDO will be in dropout and the CAP voltage will be at ground, i.e. the V_{IN}-CAP differential voltage will equal V_{IN}. If V_{IN}-CAP is less than 3.25V (typical), the LTC3864 enters a UVLO state where the GATE is prevented from switching and most internal circuitry is shut down. In order to exit UVLO, the V_{IN}-CAP voltage would have to exceed 3.5V (typical).

Shutdown and Soft-Start

When the RUN pin is below 0.7V, the controller and most internal circuits are disabled. In this micropower shutdown state, the LTC3864 draws only 7µA. Releasing the RUN pin allows a small internal pull up current to pull the RUN pin above 1.26V and enable the controller. The RUN pin can be pulled up to an external supply of up to 60V or it can be driven directly by logic levels.

The start-up of the output voltage V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 0.8V internal reference, the V_{FB} pin is regulated to the voltage on the SS pin. This allows the SS pin to be used to program a soft-start by connecting an external capacitor from the SS pin to signal ground. An internal 10µA pull-up current charges this capacitor, creating a voltage ramp on the SS pin. As the SS voltage rises from 0V to 0.8V, the output voltage V_{OUT} rises smoothly from zero to its final value.

Alternatively, the SS pin can be used to cause the start-up of V_{OUT} to track that of another supply. Typically, this requires connecting the SS pin to an external resistor divider from the other supply to ground. (See Applications Information section.) Under shutdown or UVLO, the SS pin is pulled to ground and prevented from ramping up.

If the slew rate of the SS pin is greater than 1.2V/ms, the output will track an internal soft-start ramp instead of the SS pin. The internal soft-start will guarantee a smooth start-up of the output under all conditions, including in the case of a short-circuit recovery where the output voltage will recover from near ground.

Light Load Current Operation (Burst Mode Operation or Pulse-Skipping Mode)

The LTC3864 can be enabled to enter high efficiency Burst Mode operation or pulse-skipping mode at light loads. To select pulse-skipping operation, tie the PLLIN/MODE pin to signal ground. To select Burst Mode operation, float the PLLIN/MODE pin.

In Burst Mode operation, if the V_{FB} is higher than the reference voltage, the error amplifier will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.425V,

OPERATION

the internal sleep signal goes high, enabling sleep mode. The ITH pin is then disconnected from the output of the error amplifier and held at 0.55V.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current to 40µA while the load current is supplied by the output capacitor. As the output voltage and hence the feedback voltage decreases, the error amplifier's output will rise. When the output voltage drops enough, the ITH pin is reconnected to the output of the error amplifier, the sleep signal goes low, and the controller resumes normal operation by turning on the external P-MOSFET on the next cycle of the internal oscillator. In Burst Mode operation, the peak inductor current has to reach at least 25% of current limit for the current comparator, ICMP, to trip and turn the P-MOSFET back off, even though the ITH voltage may indicate a lower current setpoint value.

When the PLLIN/MODE pin is connected for pulse-skipping mode, the LTC3864 will skip pulses during light loads. In this mode, ICMP may remain tripped for several cycles and force the external MOSFET to stay off, thereby skipping pulses. This mode offers the benefits of smaller output ripple, lower audible noise, and reduced RF interference, at the expense of lower efficiency when compared to Burst Mode operation.

Frequency Selection and Clock Synchronization

The switching frequency of the LTC3864 can be selected using the FREQ pin. If the PLLIN/MODE pin is not being driven by an external clock source, the FREQ pin can be tied to signal ground, floated, or programmed through an external resistor. Tying FREQ pin to signal ground selects 350kHz, while floating selects 535kHz. Placing a resistor between FREQ pin and signal ground allows the frequency to be programmed between 50kHz and 850kHz.

The phase-locked loop (PLL) on the LTC3864 will synchronize the internal oscillator to an external clock source when connected to the PLLIN/MODE pin. The PLL forces the turn-on edge of the external P-channel MOSFET to be aligned with the rising edge of the synchronizing signal.

The oscillator's default frequency is based on the operating frequency set by the FREQ pin. If the oscillator's default frequency is near the external clock frequency, only slight adjustments are needed for the PLL to synchronize the external P-channel MOSFET's turn-on edge to the rising edge of the external clock. This allows the PLL to lock rapidly without deviating far from the desired frequency.

The PLL is guaranteed from 75kHz to 750kHz. The clock input levels should be greater than 2V for HI and less than 0.5V for LO.

Power Good and Fault Protection

The PGOOD pin is an open-drain output. An internal N-channel MOSFET pulls the PGOOD pin low when the V_{FB} pin voltage is outside a ±10% window from the 0.8V internal voltage reference. The PGOOD pin is also pulled low when the RUN pin is low (shut down). When the V_{FB} pin voltage is within the ±10% window, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source no greater than 6V. The PGOOD open-drain output has a 100µs delay before it can transition states.

When the V_{FB} voltage is above +10% of the regulated voltage of 0.8V, this is considered as an overvoltage condition and the external P-MOSFET is immediately turned off and prevented from ever turning on until V_{FB} returns below +7.5%.

In the event of an output short circuit or overcurrent condition that causes the output voltage to drop significantly while in current limit, the LTC3864 operating frequency will fold back. Anytime the output feedback V_{FB} voltage is less than 50% of the 0.8V internal reference (i.e., 0.4V), frequency foldback is active. The frequency will continue to drop as V_{FB} drops until reaching a minimum foldback frequency of about 18% of the setpoint frequency. Frequency foldback is designed, in combination with peak current limit, to limit current in start-up and short-circuit conditions. Setting the foldback frequency as a percentage of operating frequency assures that start-up characteristics scale appropriately with operating frequency.

APPLICATIONS INFORMATION

The LTC3864 is a current mode, constant frequency PWM controller for an asynchronous step-down DC/DC regulator with a P-channel power MOSFET acting as the main switch and a Schottky power diode acting as the commutating (catch) diode. The input range extends from 3.5V to 60V. The output range can be programmed from 0.8V to all the way up to V_{IN}. The LTC3864 can transition from regulation to 100% duty cycle when the input voltage drops below the programmed output voltage. Additionally, the LTC3864 offers Burst Mode operation with 40µA quiescent current, which delivers outstanding efficiency in light load operation. The LTC3864 is a low pin count, robust and easy to use solution in applications which require high efficiency and operate with widely varying high voltage inputs.

The typical application on the front page is a basic LTC3864 application circuit. The LTC3864 can sense the inductor current through a high side series sense resistor, R_{SENSE}, placed between V_{IN} and the source of the external P-MOSFET. Once the required output voltage and operating frequency have been determined, external component selection is driven by load requirements, and begins with the selection of inductor and R_{SENSE}. Next, the power MOSFET and catch diode are selected. Finally, input and output capacitors are selected.

Output Voltage Programming

The output voltage is programmed by connecting a feedback resistor divider from the output to the V_{FB} pin as shown in Figure 1. The output voltage in steady state operation is set by the feedback resistors according to the equation:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R_{FB2}}{R_{FB1}}\right)$$

To improve the transient response, a feedforward capacitor C_{FF} may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the GATE signal that drives the external P-MOSFET.

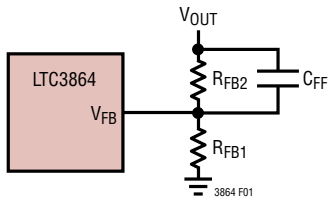


Figure 1. Setting the Output Voltage

Switching Frequency and Clock Synchronization

The choice of operating frequency is a trade-off between efficiency and component size. Lowering the operating frequency improves efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance to maintain low output ripple voltage. Conversely, raising the operating frequency degrades efficiency but reduces component size.

The LTC3864 can free run at a user programmed switching frequency, or it can synchronize with an external clock to run at the clock frequency. When the LTC3864 is synchronized, the GATE pin will phase synchronize with the rising edge of the applied clock in order to turn the external P-MOSFET on. The switching frequency of the LTC3864 is programmed with the FREQ pin, and the external clock is applied at the PLLIN/MODE pin. Table 1 highlights the different states in which the FREQ pin can be used in conjunction with the PLLIN/MODE pin.

Table 1

FREQ PIN	PLLIN/MODE PIN	FREQUENCY
0V	DC Voltage	350kHz
Floating	DC Voltage	535kHz
Resistor to GND	DC Voltage	50kHz to 850kHz
Any of the Above	External Clock	Phase Locked to External Clock

APPLICATIONS INFORMATION

The free-running switching frequency can be programmed from 50kHz to 850kHz by connecting a resistor from FREQ pin to signal ground. The resulting switching frequency as a function of resistance on FREQ pin is shown in Figure 2.

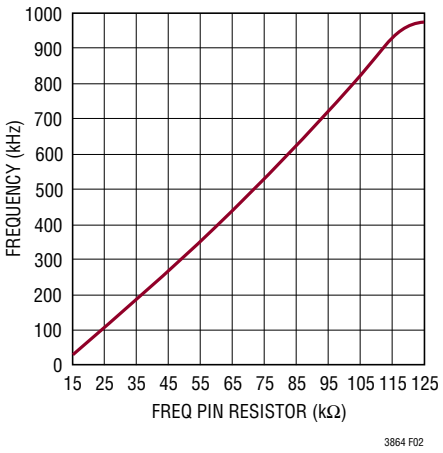


Figure 2. Switching Frequency vs Resistor on FREQ Pin

Set the free-running frequency to the desired synchronization frequency using the FREQ pin so that the internal oscillator is prebiased to approximately the synchronization frequency. While it is not required that the free-running frequency be near the external clock frequency, doing so will minimize synchronization time.

Inductor Selection

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge and transition losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

Given the desired input and output voltages, the inductor value and operation frequency determine the ripple current:

$$\Delta I_L = \left(\frac{V_{OUT}}{f \bullet L}\right)\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and results in lower output ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency, and operating frequency.

A reasonable starting point for ripple current is 40% of $I_{OUT(MAX)}$ at nominal V_{IN}. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\right)\left(1-\frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the inductance value has been determined, the type of inductor must be selected. Core loss is independent of core size for a given inductor value, but it is very dependent on the inductance selected. As inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

High efficiency converters generally cannot tolerate the core loss of low cost powdered iron cores, forcing the use of more expensive ferrite materials. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This will result in an abrupt increase in inductor ripple current and output voltage ripple. Do not allow the core to saturate!

A variety of inductors are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft, Toko, Vishay, Pulse, and Würth.

Current Sensing and Current Limit Programming

The LTC3864 senses the inductor current through a current sense resistor, R_{SENSE}, placed across the V_{IN} and SENSE pins. The voltage across the resistor, V_{SENSE}, is proportional to inductor current and in normal operation is compared to the peak inductor current setpoint. A current limit condition is detected when V_{SENSE} exceeds 95mV. When the current limit threshold is exceeded, the P-channel MOSFET is immediately turned off by pulling the GATE voltage to V_{IN} regardless of the controller input.

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The peak inductor current limit is equal to:

$$I_{L(PEAK)} \cong \left(\frac{95mV}{R_{SENSE}} \right)$$

This inductor current limit would translate to an output current limit based on the inductor ripple:

$$I_{LIMIT} \cong \frac{95mV}{R_{SENSE}} - \frac{\Delta I_L}{2}$$

The SENSE pin is a high impedance input with a maximum leakage of ±2µA. Since the LTC3864 is a peak current mode controller, noise on the SENSE pin can create pulse width jitter. Careful attention must be paid to the layout of R_{SENSE}. To ensure the integrity of the current sense signal, V_{SENSE}, the traces from V_{IN} and SENSE pins should be short and run together as a differential pair and Kelvin (4-wire) connected across R_{SENSE} (Figure 3).

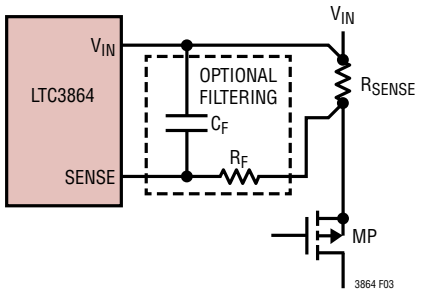

Figure 3. Inductor Current Sensing

The LTC3864 has internal filtering of the current sense voltage which should be adequate in most applications. However, adding a provision for an external filter offers added flexibility and noise immunity, should it be necessary. The filter can be created by placing a resistor from the R_{SENSE} resistor to the SENSE pin and a capacitor across the V_{IN} and SENSE pins.

Power MOSFET Selection

The LTC3864 drives a P-channel power MOSFET that serves as the main switch for the asynchronous step-down converter. Important P-channel power MOSFET parameters include drain-to-source breakdown voltage $V_{BR(DSS)}$, threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, gate-to-drain reverse transfer capacitance C_{RSS}, maximum drain current $I_{D(MAX)}$, and the MOSFET's thermal resistance $\theta_{JC(MOSFET)}$ and $\theta_{JA(MOSFET)}$.

The gate driver bias voltage V_{IN}-V_{CAP} is set by an internal LDO regulator. In normal operation, the CAP pin will be regulated to 8V below V_{IN}. A minimum 0.1µF capacitor is required across the V_{IN} and CAP pins to ensure LDO stability. If required, additional capacitance can be added to accommodate higher gate currents without voltage droop. In shutdown and Burst Mode operation, the CAP LDO is turned off. In the event of CAP leakage to ground, the CAP voltage is limited to 9V by a weak internal clamp from V_{IN} to CAP. As a result, a minimum 10V V_{GS} rated MOSFET is required.

The power dissipated by the P-channel MOSFET when the LTC3864 is in continuous conduction mode is given by:

$$P_{MOSFET} \cong D \bullet I_{OUT}^2 \bullet \rho_\tau \bullet R_{DS(ON)} + V_{IN}^2 \bullet \left(\frac{I_{OUT}}{2} \right) \bullet (C_{MILLER}) \bullet \left[\frac{R_{DN}}{(V_{IN} - V_{CAP}) - V_{MILLER}} + \frac{R_{UP}}{V_{MILLER}} \right] \bullet f$$

where D is duty factor, $R_{DS(ON)}$ is on-resistance of P-MOSFET, ρ_τ is temperature coefficient of on-resistance, R_{DN} is the pull-down driver resistance specified at 0.9Ω typical and R_{UP} is the pull-up driver resistance specified at 2Ω typical. V_{MILLER} is the Miller effective V_{GS} voltage and is taken graphically from the power MOSFET data sheet.

The power MOSFET input capacitance C_{MILLER} is the most important selection criteria for determining the transition loss term in the P-channel MOSFET but is not directly specified on MOSFET data sheets. C_{MILLER} is a combination of several components, but it can be derived from the typical gate charge curve included on most data sheets (Figure 4). The curve is

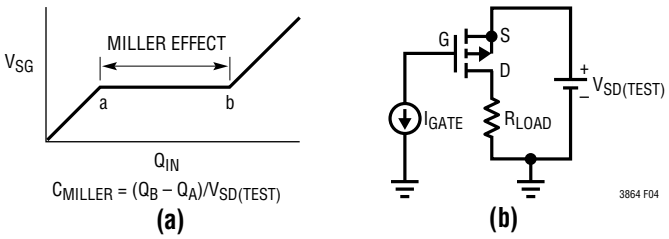

Figure 4. (a) Typical P-MOSFET Gate Charge Characteristics and (b) Test Set-Up to Generate Gate Charge Curve

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generated by forcing a constant current out of the gate of a common-source connected P-MOSFET that is loaded with a resistor, and then plotting the gate voltage versus time. The initial slope is the effect of the gate-to-source and gate-to-drain capacitances. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain voltage rises across the resistor load. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{SD} test voltage, but can be adjusted for different V_{SD} voltages by multiplying by the ratio of the adjusted V_{SD} to the curve specified V_{SD} value. A way to estimate the C_{MILLER} term is to take the change in gate charge from points a and b (or the parameter Q_{GD} on a manufacturer's data sheet) and dividing it by the specified V_{SD} test voltage, $V_{SD(TEST)}$.

$$C_{MILLER} \cong \frac{Q_{GD}}{V_{SD(TEST)}}$$

The term with C_{MILLER} accounts for transition loss, which is highest at high input voltages. For $V_{IN} < 20V$, the high-current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency.

Schottky Diode Selection

When the P-MOSFET is turned off, a power Schottky diode is required to function as a commutating diode to carry the inductor current. The average diode current is therefore dependent on the P-MOSFET's duty factor. The worst case condition for diode conduction is a short-circuit condition where the Schottky must handle the maximum current as its duty factor approaches 100% (and the P-channel MOSFET's duty factor approaches 0%). The diode therefore must be chosen carefully to meet worst case voltage and current requirements. The equation below describes the continuous or average forward diode current rating required, where D is the regulator duty factor.

$$I_{F(AVG)} \cong I_{OUT(MAX)} \bullet (1-D)$$

Once the average forward diode current is calculated, the power dissipation can be determined. Refer to the Schottky diode data sheet for the power dissipation P_{DIODE} as a function of average forward current $I_{F(AVG)}$. P_{DIODE} can also be iteratively determined by the two equations below, where $V_{F(IOUT, TJ)}$ is a function of both $I_{F(AVG)}$ and junction temperature T_J. Note that the thermal resistance $\theta_{JA(DIODE)}$ given in the data sheet is typical and can be highly layout dependent. It is therefore important to make sure that the Schottky diode has adequate heat sinking.

$$T_J \cong P_{DIODE} \bullet \theta_{JA(DIODE)}$$
$$P_{DIODE} \cong I_{F(AVG)} \bullet V_{F(IOUT,TJ)}$$

The Schottky diode forward voltage is a function of both $I_{F(AVG)}$ and T_J, so several iterations may be required to satisfy both equations. The Schottky forward voltage V_F should be taken from the Schottky diode data sheet curve showing Instantaneous Forward Voltage. The forward voltage will increase as a function of both T_J and $I_{F(AVG)}$. The nominal forward voltage will also tend to increase as the reverse breakdown voltage increases. It is therefore advantageous to select a Schottky diode appropriate to the input voltage requirements.

C_{IN} and C_{OUT} Selection

The input capacitance C_{IN} is required to filter the square wave current through the P-channel MOSFET. Use a low ESR capacitor sized to handle the maximum RMS current.

$$I_{CIN(RMS)} \cong I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

The formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{CIN(RMS)} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to derate the capacitor.

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

APPLICATIONS INFORMATION

Since ΔI_L increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, specialty polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Specialty polymer capacitors offer very low ESR but have lower specific capacitance than other types. Tantalum capacitors have the highest specific capacitance, but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects.

The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. When used as input capacitors, care must be taken to ensure that ringing from inrush currents and switching does not pose an overvoltage hazard to the power switch and controller. To dampen input voltage transients, add a small 5µF to 40µF aluminum electrolytic capacitor with an ESR in the range of 0.5Ω to 2Ω. High performance through-hole capacitors may also be used, but an additional ceramic capacitor in parallel is recommended to reduce the effect of lead inductance.

Discontinuous and Continuous Operation

The LTC3864 operates in discontinuous conduction (DCM) until the load current is high enough for the inductor current to be positive at the end of the switching cycle. The output load current at the continuous/discontinuous boundary $I_{OUT(CDB)}$ is given by the following equation:

$$I_{OUT(CDB)} \cong \frac{(V_{IN} - V_{OUT})(V_{OUT} + V_F)}{2 \bullet L \bullet f \bullet (V_{IN} + V_F)}$$

The continuous/discontinuous boundary is inversely proportional to the inductor value. Therefore, if required, $I_{OUT(CDB)}$ can be reduced by increasing the inductor value.

External Soft-Start and Output Tracking

Start-up characteristics are controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the internal 0.8V reference, the LTC3864 regulates the V_{FB} pin voltage to the voltage on the SS pin. When the SS pin is greater than the internal 0.8V reference, the V_{FB} pin voltage regulates to the 0.8V internal reference. The SS pin can be used to program an external soft-start function or to allow V_{OUT} to track another supply during start-up.

Soft-start is enabled by connecting a capacitor from the SS pin to ground. An internal 10µA current source charges the capacitor, providing a linear ramping voltage at the SS pin that causes V_{OUT} to rise smoothly from 0V to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{0.8V}{10\mu A}$$

When the LTC3864 is configured to track another supply, a voltage divider can be used from the tracking supply to the SS pin to scale the ramp rate appropriately. Two common implementations of tracking as shown in Figure 5a are coincident and ratiometric. For coincident tracking, make the divider ratio from the external supply the same as the divider ratio for the feedback voltage. Ratiometric tracking could be achieved by using a different ratio than the feedback (Figure 5b).

Note that the soft-start capacitor charging current is always flowing, producing a small offset error. To minimize this error, select the tracking resistive divider values to be small enough to make this offset error negligible.

Short-Circuit Faults: Current Limit and Foldback

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the LTC3864, the maximum sense voltage is 95mV, measured across the inductor sense resistor R_{SENSE}, placed across the V_{IN} and SENSE pins. The output current limit is approximately:

$$I_{LIMIT} \cong \frac{95mV}{R_{SENSE}} - \frac{\Delta I_L}{2}$$

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The current limit must be chosen to ensure that $I_{LIMIT(MIN)} > I_{OUT(MAX)}$ under all operating conditions. The minimum current limit value should be greater than the inductor current required to produce maximum output power at worst case efficiency. Worst-case efficiency typically occurs at the highest V_{IN}.

Short-circuit fault protection is assured by the combination of current limit and frequency foldback. When the output feedback voltage V_{FB} drops below 0.4V, the operating frequency f will fold back to a minimum value of 0.18 • f when V_{FB} reaches 0V. Both current limit and frequency foldback are active in all modes of operation. In a short-circuit fault condition, the output current is first limited by current limit and then further reduced by folding back the operating frequency as the short becomes more severe.

Short-Circuit Recovery and Internal Soft-Start

An internal soft-start feature guarantees a maximum positive output voltage slew rate in all operational cases. In a short-circuit recovery condition for example, the output recovery rate is limited by the internal soft-start so that output voltage overshoot and excessive inductor current buildup is prevented.

The internal soft-start voltage and the external SS pin operate independently. The output will track the lower of the two voltages. The slew rate of the internal soft-start voltage is roughly 1.2V/ms, which translates to a total soft-start time of 650µs. If the slew rate of the SS pin is greater than 1.2V/ms the output will track the internal soft-start ramp. To assure robust fault recovery, the

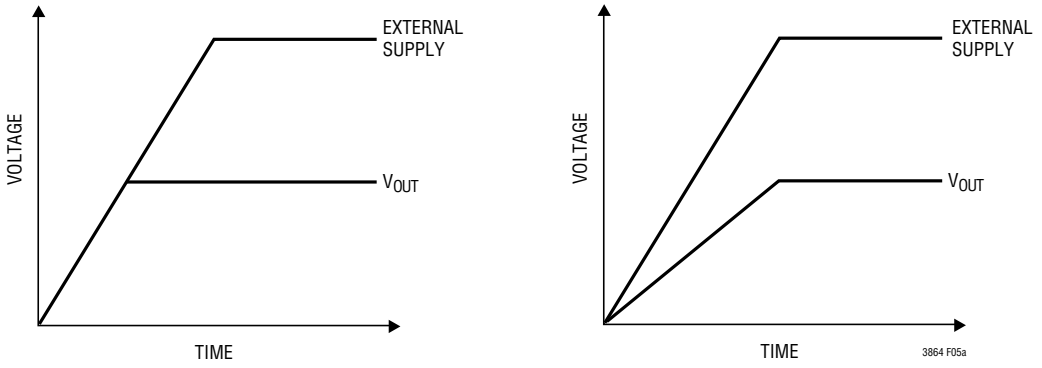

Figure 5(a). Two Different Modes of Output Tracking

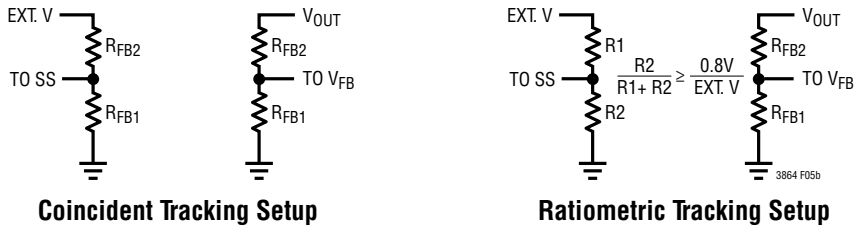

Figure 5(b): Setup for Ratiometric and Coincident Tracking

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internal soft-start feature is active in all operational cases. If a short-circuit condition occurs which causes the output to drop significantly, the internal soft-start will assure a soft recovery when the fault condition is removed.

The internal soft-start assures a clean soft ramp-up from any fault condition that causes the output to droop, guaranteeing a maximum ramp rate in soft-start, short-circuit fault release, or output recovery from drop out. Figure 6 illustrates how internal soft-start controls the output ramp-up rate under varying scenarios.

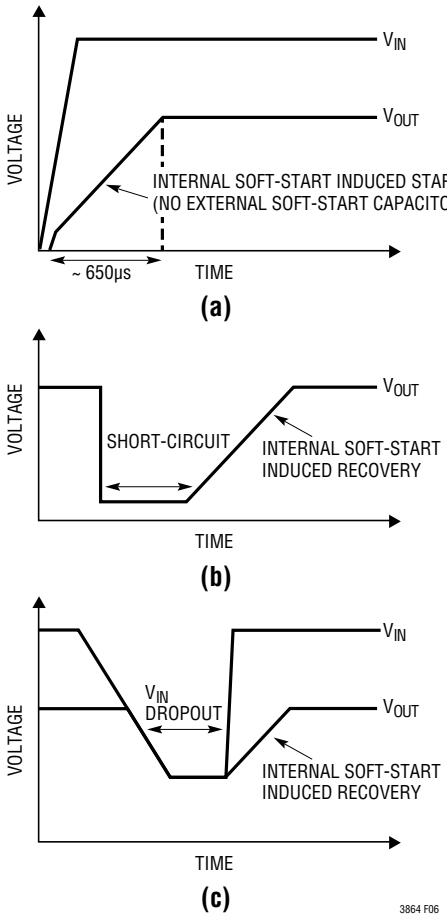

Figure 6. Internal Soft-Start (a) Allows Soft Start-Up without an External Soft-Start Capacitor and Allows Soft Recovery from (b) a Short-Circuit or (c) a V_{IN} Dropout

V_{IN} Undervoltage Lockout (UVLO)

The LTC3864 is designed to accommodate applications requiring widely varying power input voltages from 3.5V to 60V. To accommodate the cases where V_{IN} drops significantly once in regulation, the LTC3864 is guaranteed to operate down to a V_{IN} of 3.5V over the full temperature range.

The implications of both the UVLO rising and UVLO falling specifications must be carefully considered for low V_{IN} operation. The UVLO threshold with V_{IN} rising is typically 3.5V (with a maximum of 3.8V) and UVLO falling is typically 3.25V (with a maximum of 3.5V). The operating input voltage range of the LTC3864 is guaranteed to be 3.5V to 60V over temperature, but the initial V_{IN} ramp must exceed 3.8V to guarantee start-up.

For example, Figure 7 illustrates LTC3864 operation when an automotive battery droops during a cold crank condition. The typical automotive battery is 12V to 14V, which is more than enough headroom above 3.8V for the LTC3864 to start up. Onboard electronics which are powered by a DC/DC regulator require a minimum supply voltage for seamless operation during the cold crank condition, and the battery may droop close to these minimum supply requirements during a cold crank. The DC/DC regulator should not exacerbate the situation by having excessive dropout between the already suppressed battery voltage input and the output of the regulator which power these electronics. As seen in Figure 7, the LTC3864's 100% duty cycle capability allows virtually no dropout (only the $I_{OUT} \bullet (R_{SENSE} + R_{DS(ON)})$ drop across the sense resistor and P-MOSFET if there is a significant I_{OUT}) from the battery to the output. The 3.5V guaranteed UVLO point assures sufficient margin for continuous, uninterrupted operation in extreme cold crank battery drooping conditions. However, additional input capacitance or slower soft start-up time may be required at low V_{IN} (e.g. 3.5V to 4.5V) in order to limit V_{IN} droop caused by inrush currents, especially if the battery or input source has a sufficiently large input impedance.

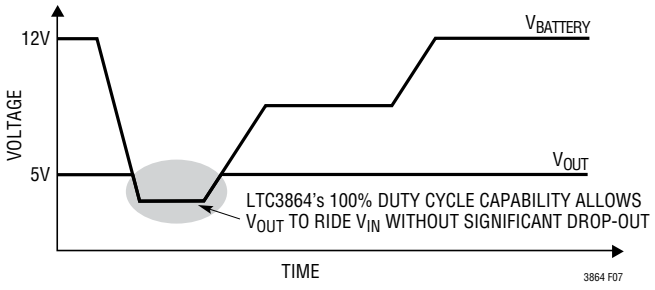

Figure 7. Typical Automotive Cold Crank

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Minimum On-Time Considerations

The minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3864 is capable of turning on the power MOSFET, and is typically 220ns. It is determined by internal timing delays and the gate charge required to turn on the MOSFET. Low-duty-cycle applications may approach this minimum on-time limit, so care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN(MAX)} \bullet f}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will skip cycles. However, the output voltage will continue to regulate.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine the dominant contributors and therefore where efficiency improvements can be made. Percent efficiency can be expressed as:

% Efficiency = 100% - (L1+L2+L3+…)

where L1, L2, L3, etc., are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LTC3864 application circuits.

1. I^2R Loss: I^2R losses result from the P-channel MOSFET resistance, inductor resistance, the current sense resistor, and input and output capacitor ESR. In continuous mode operation the average output current flows through L but is chopped between the P-channel MOSFET and the bottom side Schottky diode. The following equation may be used to determine the total I^2R loss:

$$P_{I^2R} \approx (I^2_{OUT} + \Delta I^2_L/12) \bullet [R_{DCR} + D \bullet (R_{DS(ON)} + R_{SENSE} + R_{ESR(CIN)})] + \Delta I^2_L/12 \bullet R_{ESR(COUT)}$$

2. Transition Loss: Transition loss of the P-channel MOSFET becomes significant only when operating at high input voltages (typically 20V or greater.) The P-channel transition losses ($P_{PMOSTRL}$) can be determined from the following equation:

$$P_{PMOSTRL} = V_{IN}^2 \bullet \left(\frac{I_{OUT}}{2}\right) \bullet (C_{MILLER}) \bullet \left[\frac{R_{DN}}{(V_{IN} - V_{CAP}) - V_{MILLER}} + \frac{R_{UP}}{V_{MILLER}}\right] \bullet f$$

3. Gate Charging Loss: Charging and discharging the gate of the MOSFET will result in an effective gate charging current. Each time the P-channel MOSFET gate is switched from low to high and low again, a packet of charge dQ moves from the capacitor across $V_{IN} - V_{CAP}$ and is then replenished from ground by the internal V_{CAP} regulator. The resulting dQ/dt current is a current out of V_{IN} flowing to ground. The total power loss in the controller including gate charging loss is determined by the following equation:

$$P_{CNTRL} = V_{IN} \bullet (I_Q + f \bullet Q_{G(PMOSFET)})$$

4. Schottky Loss: The Schottky diode loss is most significant at low duty factors (high step down ratios). The critical component is the Schottky forward voltage as a function of junction temperature and current. The Schottky power loss is given by the equation below.

$$P_{DIODE} \cong (1-D) \bullet I_{OUT} \bullet V_{F(IOUT, TJ)}$$

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If changes cause the input current to decrease, then the efficiency has increased. If there is no change in input current, there is no change in efficiency.

OPTI-LOOP® Compensation

OPTI-LOOP compensation, through the availability of the ITH pin, allows the transient response to be optimized for a wide range of loads and output capacitors. The ITH pin not only allows optimization of the control loop behavior

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but also provides a test point for the step-down regulator's DC-coupled and AC-filtered closed-loop response. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at this pin.

The ITH series R_{ITH}-C_{ITH1} filter sets the dominant pole-zero loop compensation. Additionally, a small capacitor placed from the ITH pin to signal ground, C_{ITH2}, may be required to attenuate high frequency noise. The values can be modified to optimize transient response once the final PCB layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. The general goal of OPTI-LOOP compensation is to realize a fast but stable ITH response with minimal output droop due to the load step. For a detailed explanation of OPTI-LOOP compensation, refer to Application Note 76.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Connecting a resistive load in series with a power MOSFET, then placing the two directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load-step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated feedback loop response.

The gain of the loop increases with R_{ITH} and the bandwidth of the loop increases with decreasing C_{ITH1}. If R_{ITH} is increased by the same factor that C_{ITH1} is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. In addition, a feedforward capacitor, C_{FF}, can be added to improve the high frequency response, as shown in Figure 1. Capacitor C_{FF} provides phase lead by creating a high frequency zero with R_{FB2} which improves the phase margin. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate overall performance of the step-down regulator.

In some applications, a more severe transient can be caused by switching in loads with large (>10µF) input capacitors. If the switch connecting the load has low resistance and is driven quickly, then the discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection and soft starting.

Design Example

Consider a step-down converter with the following specifications: V_{IN} = 5V to 55V, V_{OUT} = 5V, $I_{OUT(MAX)}$ = 2A, and f = 350kHz (Figure 8).

The output voltage is programmed according to:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R_{FB2}}{R_{FB1}}\right)$$

If R_{FB1} is chosen to be 80.6k, then R_{FB2} would have to be 422k.

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The FREQ pin is tied to signal ground in order to program the switching frequency to 350kHz. The on-time required at 55V to generate a 5V output can be calculated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \bullet f} = \frac{5V}{55V \bullet 350kHz} \approx 260ns$$

This on-time is larger than LTC3864's minimum on-time with sufficient margin to prevent cycle skipping.

Next, set the inductor value to give 60% worst-case ripple at maximum V_{IN} = 55V.

$$L = \left(\frac{5V}{350kHz \bullet (0.6 \bullet 2A)}\right)\left(1 - \frac{5V}{55V}\right) \approx 10.8\mu H$$

Select 10µH, which is a standard value.

The resulting maximum ripple current is:

$$\Delta I_L = \left(\frac{5V}{350kHz \bullet 10\mu H}\right)\left(1 - \frac{5V}{55V}\right) \approx 1.3A$$

Next, set the R_{SENSE} resistor value to ensure that the converter can deliver a maximum output current of 2.0A with sufficient margin to account for component variations and worst-case operating conditions. Using a 30% margin factor:

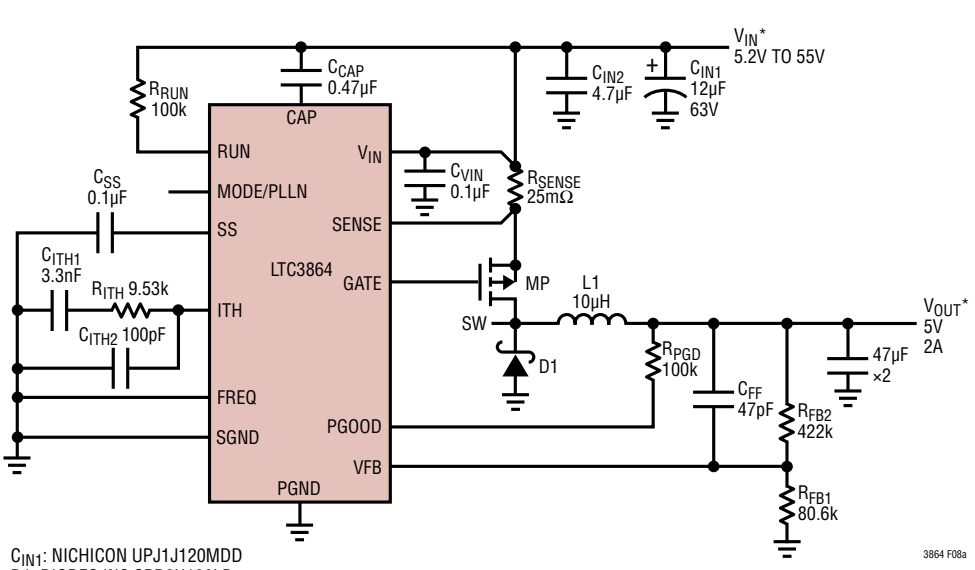
$$R_{SENSE} \cong \frac{95mV}{1.3 \bullet \left(2A + \frac{1.3A}{2}\right)} \approx 27.5m\Omega$$

Use a more readily available 25mΩ sense resistor.

The current limit is:

$$I_{LIMIT} \cong \frac{95mV}{25m\Omega} - \frac{1.3A}{2} \approx 3.15A$$

Next choose a P-channel MOSFET with the appropriate BV_{DSS} and I_D rating. In this example, a good choice is the Fairchild FDMC5614P (BV_{DSS} = 60V, I_D = 5.7A, $R_{DS(ON)}$ = 105mΩ, $\rho_{100°C}$ = 1.5, C_{MILLER} = 100pF, θ_{JA} = 60°C/W). The expected power dissipation and the



CIN1: NICHICON UPJ1J120MDD
D1: DIODES INC SBR3U100LP
L1: TOKO 1217AS-H-100M
MP: FAIRCHILD FDMC5614P

*VOUT FOLLOWS VIN WHEN 3.5V ≤ VIN ≤ 5.2V
SEE DROPOUT BEHAVIOR IN TYPICAL PERFORMANCE CHARACTERISTICS

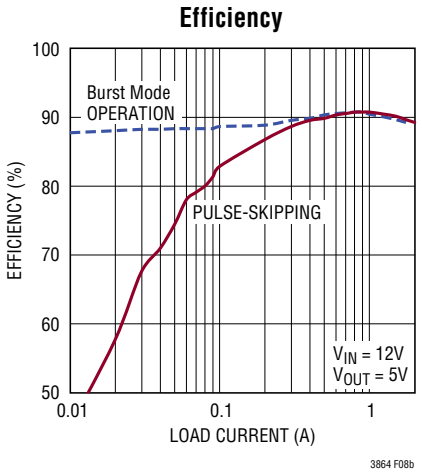


Figure 8. Design Example (5V, 2A 350kHz Step-Down Converter)

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resulting junction temperature for the MOSFET can be calculated at $T_A = 70°C$, $V_{IN(MAX)} = 55V$ and $I_{OUT(MAX)} = 2A$:

$$P_{PMOS} = \frac{5V}{55V}(2A)^2 \bullet 1.5 \bullet 105m\Omega +$$

$$(55V)^2 \bullet (2A/2) \bullet 100pF \bullet \left[\frac{0.9\Omega}{8V-3V}\right] + \frac{2\Omega}{3V} \bullet 350kHz$$

$$\approx 57mW + 90mW = 147mW$$

$$T_J = 70°C + 147mW \bullet 60°C/W \approx 80°C$$

The calculations can be repeated for $V_{IN(MIN)}$ = 5V:

$$P_{PMOS} = \frac{5V}{5V}(2A)^2 \bullet 1.5 \bullet 105m\Omega +$$

$$(5.2V)^2 \bullet 100pF \bullet \left[\frac{0.9\Omega}{5.2V-3V} + \frac{2\Omega}{3V}\right] \bullet 350kHz$$

$$\approx 630mW + 1mW \approx 631mW$$

$$T_J = 70°C + 631mW \bullet 60°C/W \approx 108°C$$

Next choose an appropriate Schottky diode that will handle the power requirements. The Diodes Inc. SBR3U100LP Schottky diode is selected ($V_{F(2A,125°C)} = 0.5V$, $\theta_{JA} = 61°C/W$) for this application. The power dissipation and junction temperature at T_A = 70°C can be calculated as:

$$P_{DIODE} = 2A \bullet \left(1 - \frac{5V}{55V}\right) \bullet 0.5V \approx 909mW$$

$$T_J = 70°C + 909mW \bullet 61°C/W = 125°C$$

These power dissipation calculations show that careful attention to heat sinking will be necessary.

For the input capacitance, a combination of ceramic and electrolytic capacitors are chosen to handle the maximum RMS current of 1A. C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement. For this design, two 47µF ceramic capacitors are chosen to offer low ripple in both normal operation and in Burst Mode operation.

A soft-start time of 8ms can be programmed through a 0.1µF capacitor on the SS pin:

$$C_{SS} = \frac{8ms \bullet 10\mu A}{0.8V} = 0.1\mu F$$

Loop compensation components on the ITH pin are chosen based on load step transient behavior (as described under OPTI-LOOP Compensation) and is optimized for stability. A pull-up resistor is used on the RUN pin for FMEA compliance (see Failure Modes and Effects Analysis).

Gate Driver Component Placement, Layout and Routing

It is important to follow recommended power supply PC board layout practices such as placing external power elements to minimize loop area and inductance in switching paths. Be careful to pay particular attention to gate driver component placement, layout and routing.

The effective C_{CAP} capacitance should be greater than 0.1µF minimum in all operating conditions. Operating voltage and temperature both decrease the rated capacitance to varying degrees depending on dielectric type. The LTC3864 is a PMOS controller with an internal gate driver and bootstrapped LDO that regulates the differential CAP voltage ($V_{IN} - V_{CAP}$) to 8V nominal. The C_{CAP} capacitance needs to be large enough to assure stability and provide cycle-to-cycle current to the PMOS switch with minimum series inductance. We recommend a ceramic 0.47µF 16V capacitor with a high quality dielectric such as X5R or X7R. Some high current applications with large Qg PMOS switches may benefit from an even larger C_{CAP} capacitance.

Figure 9 shows the LTC3864 Generic Application Schematic which includes an optional current sense filter and series gate resistor. Figure 10 illustrates the recommended gate driver component placement, layout and routing of the GATE, V_{IN}, SENSE and CAP pins and key gate driver components. It is recommended that the gate driver layout follow the example shown in Figure 10 to assure proper operation and long term reliability.

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The LTC3864 gate driver should connect to the external power elements in the following manner. First route the V_{IN} pin using a single low impedance isolated trace to the positive R_{SENSE} resistor PAD without connection to the V_{IN} plane. The reason for this precaution is that the V_{IN} pin is internally Kelvin connected to the current sense comparator, internal V_{IN} power and the PMOS gate driver. Connecting the V_{IN} pin to the V_{IN} power plane adds noise and can result in jitter or instability. Figure 10 shows a single V_{IN} trace from the positive R_{SENSE} pad connected to C_{SF}, C_{CAP}, V_{IN} pad and C_{INB}. The total trace length to R_{SENSE} should be minimized and the capacitors C_{SF}, C_{CAP} and C_{INB} should be placed near the V_{IN} pin of the LTC3864.

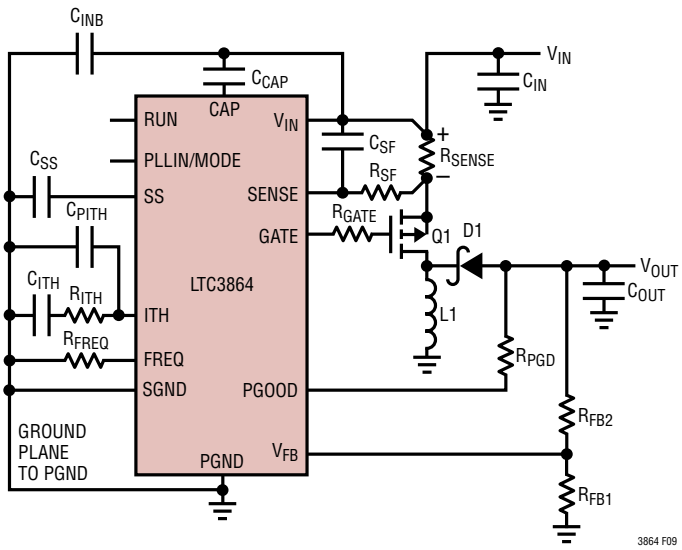

Figure 9. LTC3864 Generic Application Schematic with Optional Current Sense Filter and Series Gate Resistor

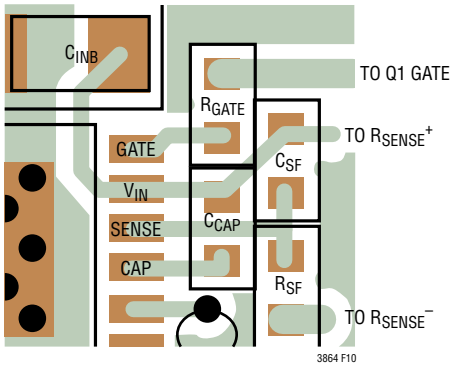

Figure 10. LTC3864 Recommended Gate Driver PC Board Placement, Layout and Routing

C_{CAP} should be placed near the V_{IN} and CAP pins. Figure 10 shows C_{CAP} placed adjacent to the V_{IN} and CAP pins with SENSE routed between the pads. This is the recommended layout and results in the minimum parasitic inductance. The gate driver is capable of providing high peak current. Parasitic inductance in the gate drive and the series inductance between V_{IN} to CAP can cause a voltage spike between V_{IN} and CAP on each switching cycle. The voltage spike can result in electrical over-stress to the gate driver and can result in gate driver failures in extreme cases. It is recommended to follow the example shown in Figure 10 for the placement of C_{CAP} as close as is practical.

R_{GATE} resistor pads can be added with a 0Ω resistor to allow the damping resistor to be added later. The total length of the gate drive trace to the PMOS gate should be minimized and ideally be less than 1cm. In most cases with a good layout the R_{GATE} resistor is not needed. The R_{GATE} resistor should be located near the gate pin to reduce peak current through GATE and minimize reflected noise on the gate pin.

The R_{SF} and C_{SF} pads can be added with a zero ohm resistor for R_{SF} and C_{SF} not populated. In most applications, external filtering is not needed. The current sense filter R_{SF} and C_{SF} can be added later if noise if demonstrated to be a problem.

The bypass capacitor C_{INB} is used to locally filter the V_{IN} supply. C_{INB} should be tied to the V_{IN} pin trace and to the PGND exposed pad. The C_{INB} positive pad should connect to R_{SENSE} positive though the V_{IN} pin trace. The C_{INB} ground trace should connect to the PGND exposed pad connection.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3864.

1. Multilayer boards with dedicated ground layers are preferable for reduced noise and for heat sinking pur-

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poses. Use wide rails and/or entire planes for V_{IN}, V_{OUT} and GND for good filtering and minimal copper loss. If a ground layer is used, then it should be immediately below (and/or above) the routing layer for the power train components which consist of C_{IN}, sense resistor, P-MOSFET, Schottky diode, inductor, and C_{OUT}. Flood unused areas of all layers with copper for better heat sinking.

2. Keep signal and power grounds separate except at the point where they are shorted together. Short signal and power ground together only at a single point with a narrow PCB trace (or single via in a multilayer board). All power train components should be referenced to power ground and all small signal components (e.g., C_{ITH1}, R_{FREQ}, C_{SS} etc.) should be referenced to signal ground.

3. Place C_{IN}, sense resistor, P-MOSFET, inductor, and primary C_{OUT} capacitors close together in one compact area. The junction connecting the drain of P-MOSFET, cathode of Schottky, and (+) terminal of inductor (this junction is commonly referred to as switch or phase node) should be compact but be large enough to handle the inductor currents without large copper losses. Place the sense resistor and source of P-channel MOSFET as close as possible to the (+) plate of C_{IN} capacitor(s) that provides the bulk of the AC current (these are normally the ceramic capacitors), and connect the anode of the Schottky diode as close as possible to the (–) terminal of the same C_{IN} capacitor(s). The high dI/dt loop formed by C_{IN}, the MOSFET, and the Schottky diode should have short leads and PCB trace lengths to minimize high frequency EMI and voltage stress from inductive ringing. The (–) terminal of the primary C_{OUT} capacitor(s) which filter the bulk of the inductor ripple current (these are normally the ceramic capacitors) should also be connected close to the (–) terminal of C_{IN}.

4. Place pins 7 to 12 facing the power train components. Keep high dV/dt signals on GATE and switch away from sensitive small signal traces and components.

5. Place the sense resistor close to the (+) terminal of C_{IN} and source of P-MOSFET. Use a Kelvin (4-wire) connection across the sense resistor and route the traces together as a differential pair into the V_{IN} and SENSE pins. An optional RC filter could be placed near the V_{IN} and SENSE pins to filter the current sense signal.

6. Place the resistive feedback divider $R_{FB1/2}$ as close as possible to the V_{FB} pin. The (+) terminal of the feedback divider should connect to the output regulation point and the (–) terminal of feedback divider should connect to signal ground.

7. Place the ceramic C_{CAP} capacitor as close as possible to V_{IN} and CAP pins. This capacitor provides the gate discharging current for the power P-MOSFET.

8. Place small signal components as close to their respective pins as possible. This minimizes the possibility of PCB noise coupling into these pins. Give priority to V_{FB}, ITH, and FREQ pins. Use sufficient isolation when routing a clock signal into PLLIN /MODE pin so that the clock does not couple into sensitive small signal pins.

Failure Mode and Effects Analysis (FMEA)

A FMEA study on the LTC3864 has been conducted through adjacent pin opens and shorts. The device was tested in a step-down application (Figure 8) from V_{IN} = 12V to V_{OUT} = 5V with a current load of 1A on the output. One group of tests involved the application being monitored while each pin was disconnected from the PC board and left open while all other pins remained intact. The other group of tests involved each pin being shorted to its adjacent pins while all other pins were connected as it would be normally in the application. The results are shown in Table 2.

For FMEA compliance, the following design implementations are recommended:

- If the RUN pin is being pull-up to a voltage greater than 6V, then it is done so through a pull-up resistor (100k to 1M) so that the PGOOD pin is not damaged in case of a RUN to PGOOD short.
- The gate of the external P-MOSFET be pulled through a resistor (20k to 100k) to the input supply, V_{IN} so that the P-MOSFET is guaranteed to turn off in case of a GATE open.

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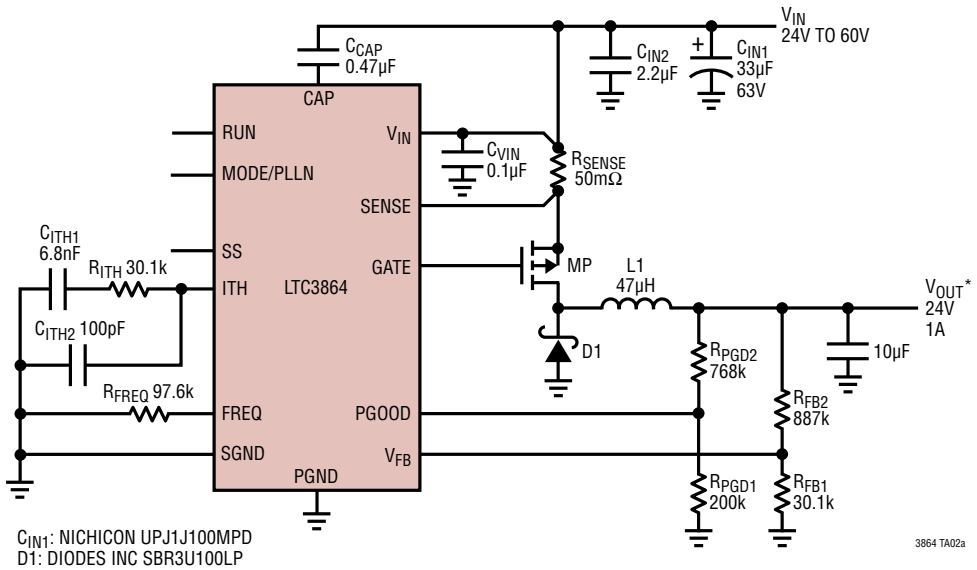
Table 2

FAILURE MODE	V_{OUT}	I_{OUT}	I_{VIN}	f	RECOVERY WHEN FAULT IS REMOVED?	BEHAVIOR
None	5V	1A	453mA	350kHz	N/A	Normal Operation.
Pin Open						
Open Pin 1 (PLLIN/MODE)	5V	1A	453mA	350kHz	OK	Pin already left open in normal application, so no difference.
Open Pin 2 (FREQ)	5V	1A	453mA	535kHz	OK	Frequency jumps to default open value.
Open Pin 3 (GND)	5V	1A	453mA	350kHz	OK	Exposed pad still provides GND connection to device.
Open Pin 4 (SS)	5V	1A	453mA	350kHz	OK	External soft-start removed, but internal soft-start still available.
Open Pin 5 (VFB)	0V	0A	0.7mA	0kHz	OK	Controller stops switching. V_{FB} internally self biases HI to prevent switching.
Open Pin 6 (ITH)	5V	1A	507mA	40kHz	OK	Output still regulating, but the switching is erratic. Loop not stable.
Open Pin 7 (PGOOD)	5V	1A	453mA	350kHz	OK	No PGOOD output, but controller regulates normally.
Open Pin 8 (RUN)	5V	1A	453mA	350kHz	OK	Controller does not start-up.
Open Pin 9 (CAP)	5V	1A	453mA	350kHz	OK	More jitter during switching, but regulates normally.
Open Pin 10 (SENSE)	0V	0A	0.7mA	0kHz	OK	SENSE internally prebiases to 0.6V below V_{IN}. This prevents controller from switching.
Open Pin 11 (V_{IN})	5.4V	1A	597mA	20kHz	OK	V_{IN} able to bias internally through SENSE. Regulates with high V_{OUT} ripple.
Open Pin 12 (GATE)	0V	0A	0.7mA	0kHz	OK	Gate does not drive external power FET, preventing output regulation.
Open Pin 13 (PGND)	5V		453mA	350kHz	OK	Pin 3 (GND) still provides GND connection to device.
Pins Shorted						
Short Pins 1, 2 (PLLIN/MODE and FREQ)	5V	1A	453mA	350kHz	OK	Burst Mode operation disabled, but runs normally as in pulse-skipping mode.
Short Pins 2, 3 (FREQ and GND)	5V	1A	453mA	0kHz	OK	FREQ already shorted to GND, so regulates normally.
Short Pins 3, 4 (GND and SS)	0V	0A	0.7mA	0kHz	OK	SS short to GND prevents device from starting up.
Short Pins 4, 5 (SS and VFB)	1V(DC) $3V_{P-P}$	50mA	9mA	Erratic	OK	V_{OUT} oscillates from 0V to 3V.
Short Pins 5, 6 (VFB and ITH)	3.15V	625mA	181mA	350kHz	OK	Controller loop does not regulate to proper output voltage.
Short Pins 7, 8 (PGOOD and RUN)	5V	1A	453mA	350kHz	OK	Controller does not start-up.
Short Pins 8, 9 (RUN and CAP)	5V	1A	453mA	350kHz	OK	Able to start-up and regulate normally.
Short Pins 9, 10 (CAP and SENSE)	0V	0A	181mA	0kHz	OK	CAP ~ V_{IN}, which prevents turning on external P-MOSFET.
Short Pins 10, 11 (SENSE and VIN)	5V	1A	453mA	50kHz	OK	Regulates with high V_{OUT} ripple.
Short Pins 11, 12 (VIN and GATE)	0V	0A	29mA	0kHz	OK	Power MOSFET is always kept OFF, preventing regulation.

TYPICAL APPLICATIONS

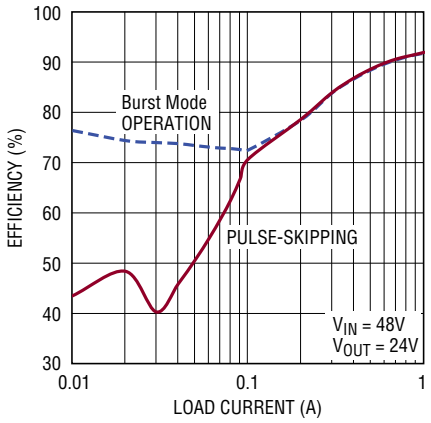
24V to 60V Input, 24V/1A Output at 750kHz



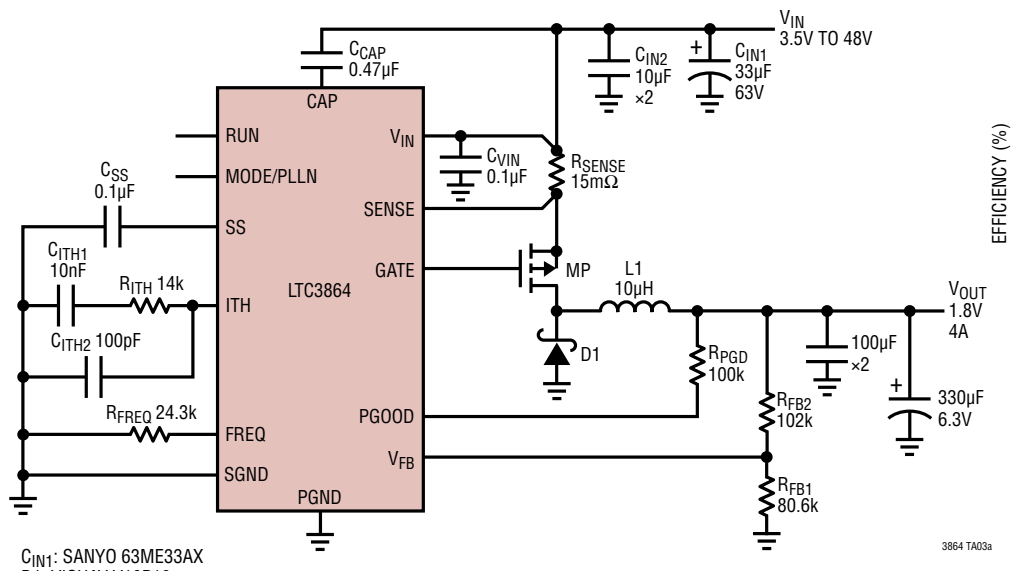
CIN1: NICHICON UPJ1J100MPD
D1: DIODES INC SBR3U100LP
L1: TOKO 1217AS-H-470M
MP: VISHAY/SILICONIX SI7113DN

*VOUT FOLLOWS VIN WHEN 3.5V ≤ VIN ≤ 24V

Efficiency

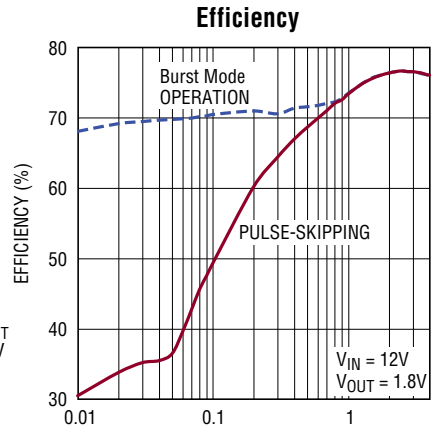


3.5V to 48V Input, 1.8V/4A Output at 100kHz



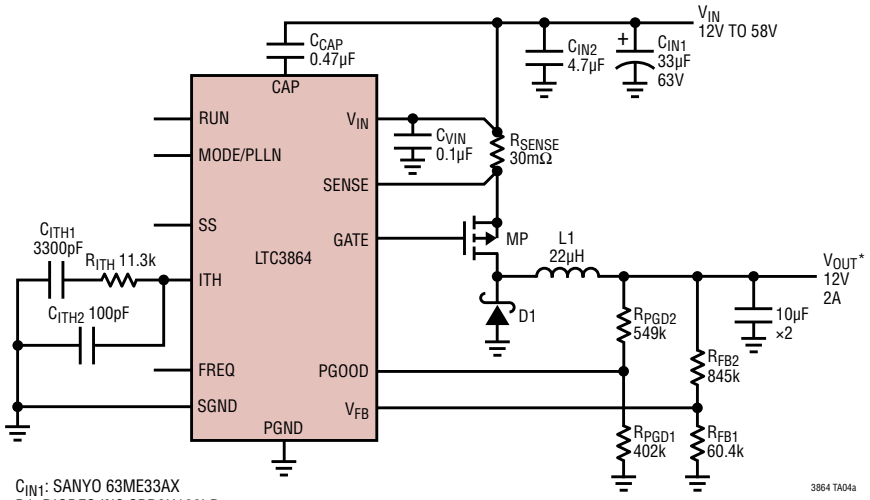
CIN1: SANYO 63ME33AX
D1: VISHAY V10P10
L1: WÜRTH 7447709100
MP: VISHAY/SILICONIX SI7461DP

Efficiency



TYPICAL APPLICATIONS

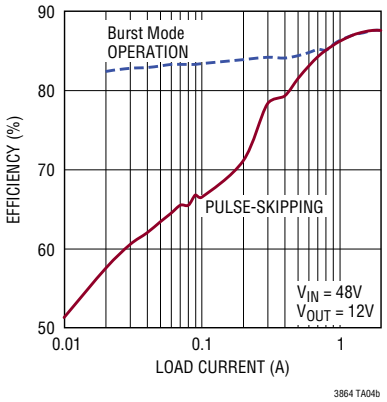
12V to 58V Input, 12V/2A Output at 535kHz



CIN1: SANYO 63ME33AX
D1: DIODES INC SBR3U100LP
L1: TOKO 1217AS-H-220M
MP: VISHAY/SILICONIX SI7465DP

*VOUT FOLLOWS VIN WHEN 3.5V ≤ VIN ≤ 12V

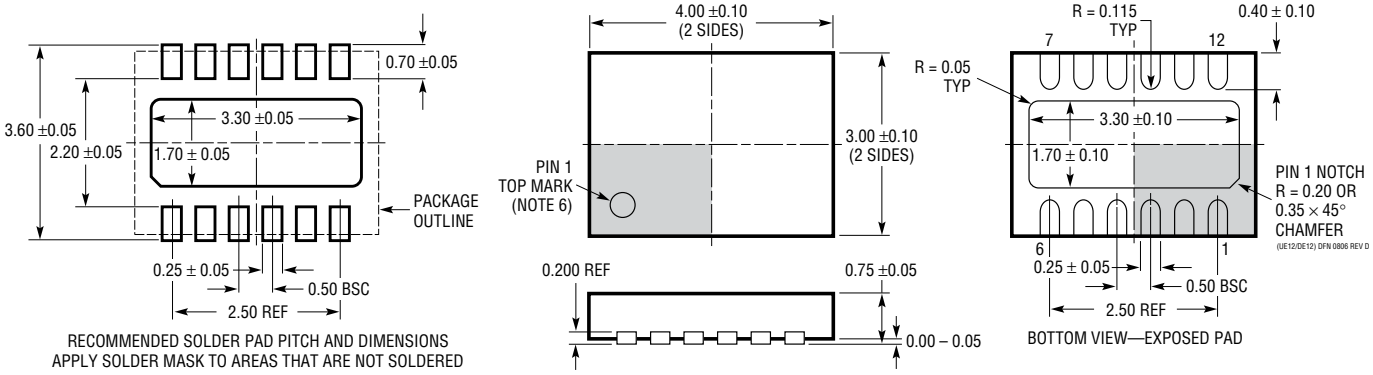
Efficiency



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DE/UE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695 Rev D)

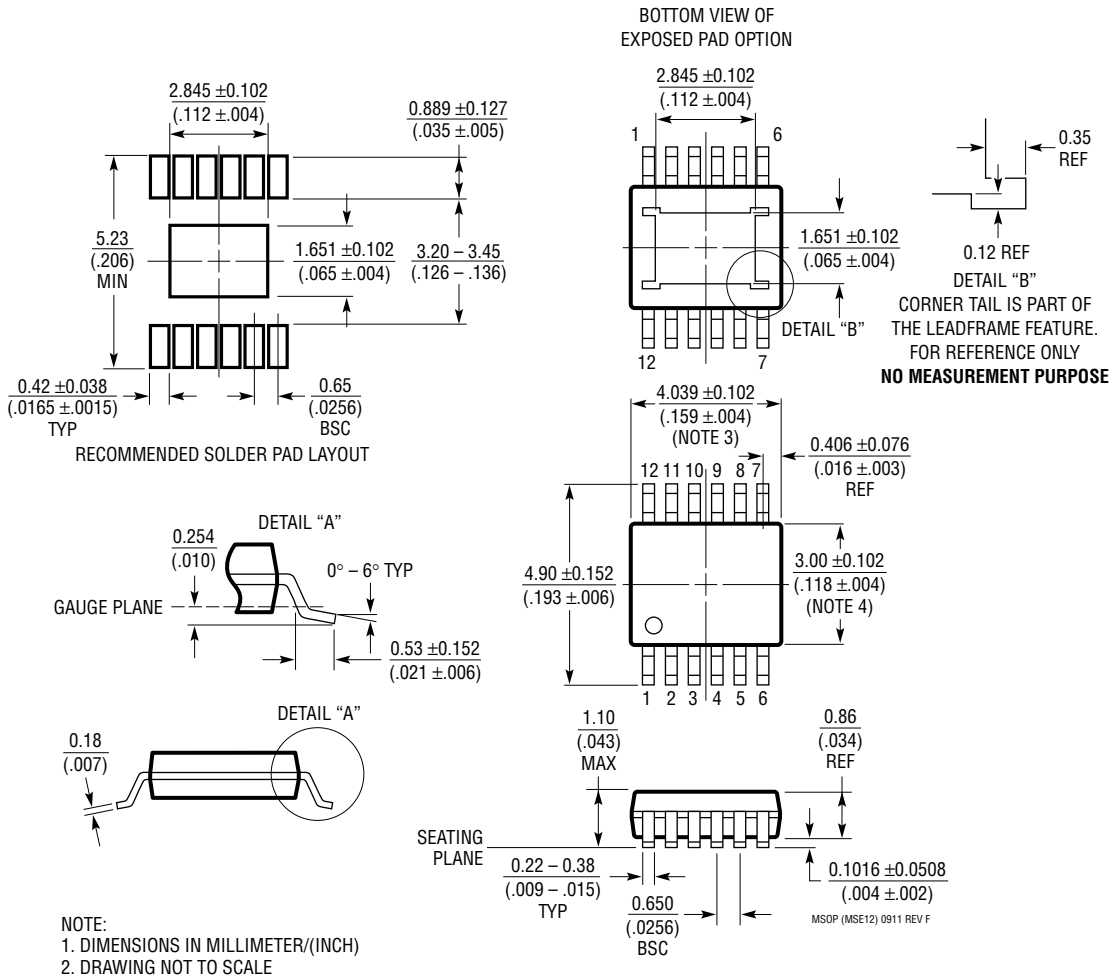


NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev F)



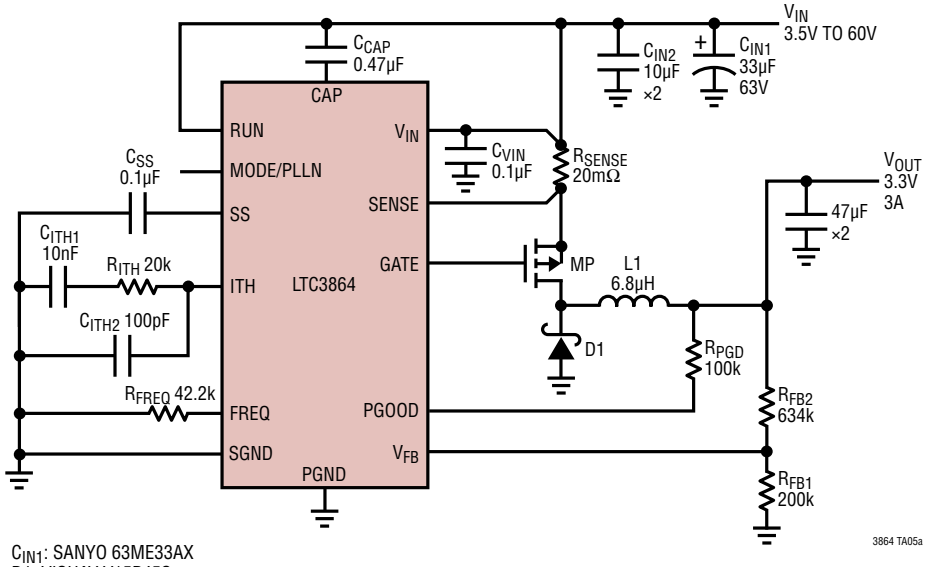
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	6/14	Modified V_{IN} to CAP capacitance	1, 8, 10, 21, 25, 26, 28
		Updated Notes 2 and 3	2

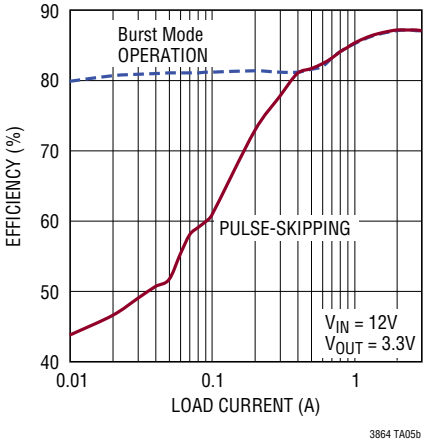
TYPICAL APPLICATION

3.5V to 38V Input, 3.3V/3A Output at 300kHz



C_{IN1}: SANYO 63ME33AX
D1: VISHAY V15P45S
L1: WÜRTH 7447709100
MP: VISHAY/SILICONIX Si7611DN

Efficiency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3891	60V, Low I_Q, Synchronous Step-Down DC/DC Controller	Phase-Lockable Fixed Frequency 50kHz to 900kHz 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA
LTC3890	60V, Low I_Q, Dual 2-Phase Synchronous Step-Down DC/DC Controller	Phase-Lockable Fixed Frequency 50kHz to 900kHz 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA
LTC3824	60V, Low I_Q, Step-Down DC/DC Controller, 100% Duty Cycle	Selectable Fixed Frequency 200kHz to 600kHz 4V≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 40µA, MSOP-10E
LT3845A	60V, Low I_Q, Single Output Synchronous Step-Down DC/DC Controller	Synchronizable Fixed Frequency 100kHz to 600kHz 4V ≤ V_{IN} ≤ 60V, 1.23V ≤ V_{OUT} ≤ 36V, I_Q = 120µA, TSSOP-16
LTC3863	60V Low IQ Inverting DC/DC Controller	PLL Fixed Frequency 75kHz to 750kHz, 3.5V ≤ V_{IN} ≤ 60V –150V ≤ V_{OUT} ≤ –0.4V, I_Q = 70µA, 3mm × 4mm DFN-12, MSOP-12
LTC3834/LTC3834-1 LTC3835/LTC3835-1	Low I_Q, Single Output Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	Phase-Lockable Fixed Frequency 140kHz to 650kHz, 4V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 10V, I_Q = 30µA/80µA
LTC3857/LTC3857-1 LTC3858/LTC3858-1	Low I_Q, Dual Output 2-Phase Synchronous Step-Down DC/DC Controllers with 99% Duty Cycle	Phase-Lockable Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA/170µA
LTC3859AL	Low I_Q, Triple Output Buck/Buck/Boost Synchronous DC/DC Controller	All Outputs Remain in Regulation Through Cold Crank 2.5V ≤ V_{IN} ≤ 38V, $V_{OUT(BUCKS)}$ Up to 24V, $V_{OUT(BOOST)}$ Up to 60V, I_Q = 28µA

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