ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage

V_{CC} 9V

$PV_{CC1,2}$ 14V

Input Voltage

I_{FB}, I_{MAX} ..... –0.3V to 14V

R^+, R^-, FB, $\overline{SHDN}$, FREQSET ..... –0.3V to V_{CC} + 0.3V

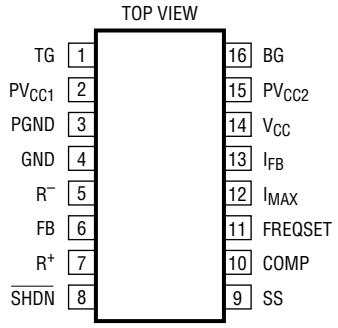
Junction Temperature (Note 9) ..... 125°C

Operating Temperature Range (Note 4) .. –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC3831EGN-1
GN PART MARKING
38311

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC}, PV_{CC1}, PV_{CC2} = 5V, V_{R+} = 1.5V, V_{R-} = GND, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	3	5	8	V
PV_{CC}	PV_{CC1}, PV_{CC2} Voltage	(Note 7)	●	3		13.2	V
V_{UVLO}	Undervoltage Lockout Voltage				2.4	2.9	V
V_{FB}	Feedback Voltage	V_{R+} = 1.5V, V_{R-} = 0V, V_{COMP} = 1.25V	●	0.738	0.75	0.762	V
ΔV_{OUT}	Output Load Regulation Output Line Regulation	I_{OUT} = 0A to 10A (Note 6) V_{CC} = 4.75V to 5.25V			2 0.1		mV mV
I_{VCC}	Supply Current	Figure 1, $V_{\overline{SHDN}}$ = V_{CC} $V_{\overline{SHDN}}$ = 0V	● ●		0.7 1	1.6 10	mA µA
I_{PVCC}	PV_{CC} Supply Current	Figure 1, $V_{\overline{SHDN}}$ = V_{CC} (Note 3) $V_{\overline{SHDN}}$ = 0V	● ●		20 0.1	30 10	mA µA
Δf_{OSC}	Internal Oscillator Frequency	FREQSET Floating	●	230	300	360	kHz
V_{SAWL}	V_{COMP} at Minimum Duty Cycle				1.2		V
V_{SAWH}	V_{COMP} at Maximum Duty Cycle				2.2		V
$V_{COMPMAX}$	Maximum V_{COMP}	V_{FB} = 0V, PV_{CC1} = 7V			2.85		V
$\Delta f_{OSC}/\Delta I_{FREQSET}$	Frequency Adjustment				10		kHz/µA
A_V	Error Amplifier Open-Loop DC Gain		●	50	65		dB
g_m	Error Amplifier Transconductance		●	1600	2000	2400	µmho
I_{COMP}	Error Amplifier Output Sink/Source Current				100		µA
I_{MAX}	I_{MAX} Sink Current	V_{IMAX} = V_{CC} (Note 10)	 ●	9 4	12 12	15 20	µA µA
	I_{MAX} Sink Current Tempco	V_{IMAX} = V_{CC} (Notes 6, 10)			3300		ppm/°C

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC}, PV_{CC1}, PV_{CC2} = 5V, V_{R+} = 1.5V, V_{R-} = GND, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	$\overline{SHDN}$ Input High Voltage		●	2.4			V
V_{IL}	$\overline{SHDN}$ Input Low Voltage		●			0.8	V
I_{IN}	$\overline{SHDN}$ Input Current	$V_{\overline{SHDN}}$ = V_{CC}	●		0.1	1	µA
I_{SS}	Soft-Start Source Current	V_{SS} = 0V, V_{IMAX} = 0V, V_{IFB} = V_{CC}	●	–8	–12	–16	µA
I_{SSIL}	Maximum Soft-Start Sink Current Undercurrent Limit	V_{IMAX} = V_{CC}, V_{IFB} = 0V, V_{SS} = V_{CC} (Note 8), PV_{CC1} = 7V (Note 7)			1.6		mA
R^+	R^+ Input Resistance				53.3		kΩ
t_r, t_f	Driver Rise/Fall Time	Figure 1, PV_{CC1} = PV_{CC2} = 5V (Note 5)	●		80	250	ns
t_{NOV}	Driver Nonoverlap Time	Figure 1, PV_{CC1} = PV_{CC2} = 5V (Note 5)	●	25	120	250	ns
DC_{MAX}	Maximum TG Duty Cycle	Figure 1, V_{FB} = 0V (Note 7), PV_{CC1} = 7V	●	91	95		%

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 3: Supply current in normal operation is dominated by the current needed to charge and discharge the external FET gates. This will vary with the LTC3831-1 operating frequency, operating voltage and the external FETs used.

Note 4: The LTC3831EGN-1 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 5: Rise and fall times are measured using 10% and 90% levels. Duty cycle and nonoverlap times are measured using 50% levels.

Note 6: Guaranteed by design, not subject to test.

Note 7: PV_{CC1} must be higher than V_{CC} by at least 2V for TG to operate at 95% maximum duty cycle and for the current limit protection circuit to be active.

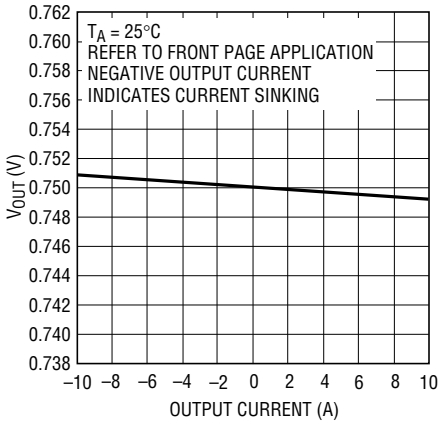
Note 8: The current limiting amplifier can sink but cannot source current. Under normal (not current limited) operation, the output current will be zero.

Note 9: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

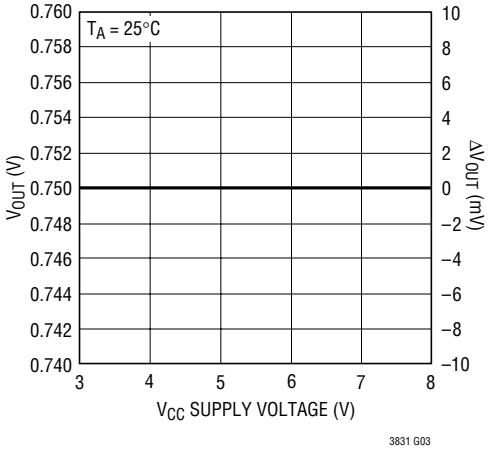
Note 10: The minimum and maximum limits for I_{MAX} over temperature includes the intentional temperature coefficient of 3300ppm/°C. This induced temperature coefficient counteracts the typical temperature coefficient of the external power MOSFET on-resistance. This results in a relatively flat current limit over temperature for the application.

TYPICAL PERFORMANCE CHARACTERISTICS

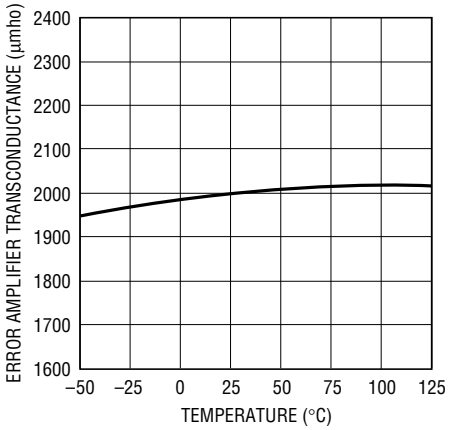
Load Regulation



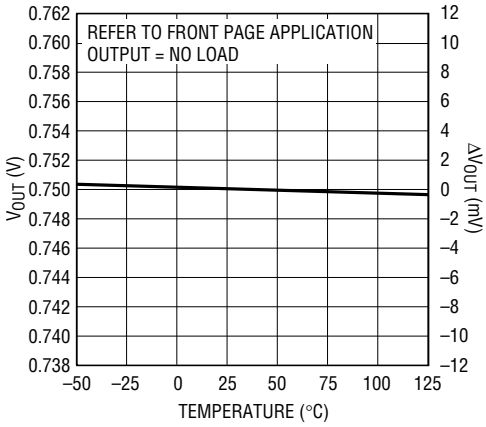
Line Regulation



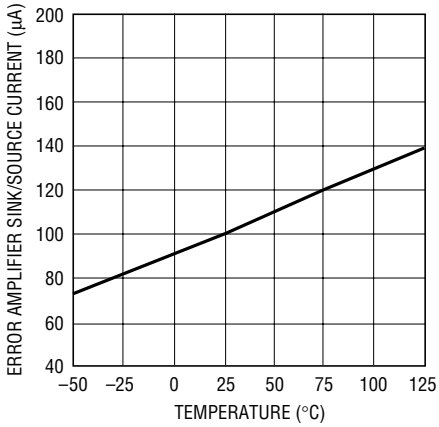
Error Amplifier Transconductance vs Temperature



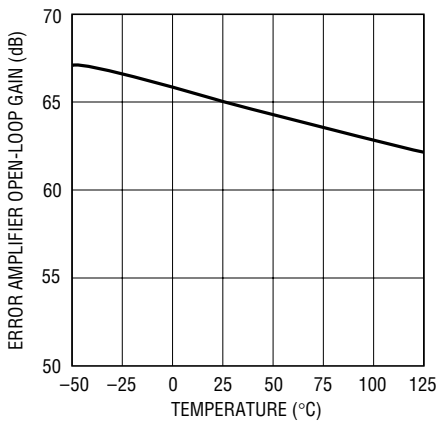
Output Voltage Temperature Drift



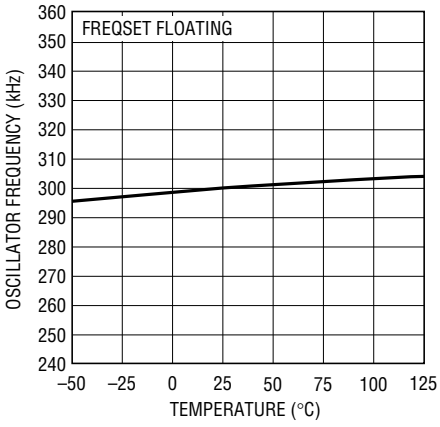
Error Amplifier Sink/Source Current vs Temperature



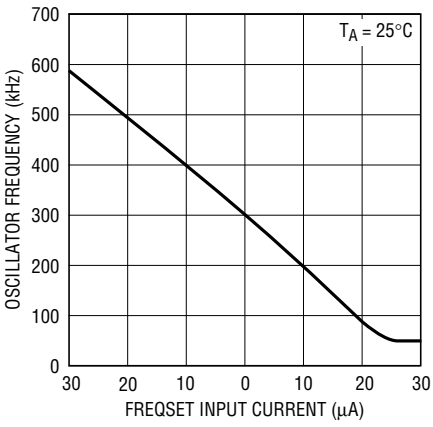
Error Amplifier Open-Loop Gain vs Temperature



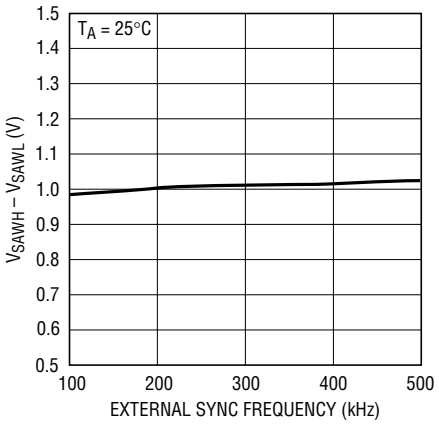
Oscillator Frequency vs Temperature



Oscillator Frequency vs FREQSET Input Current

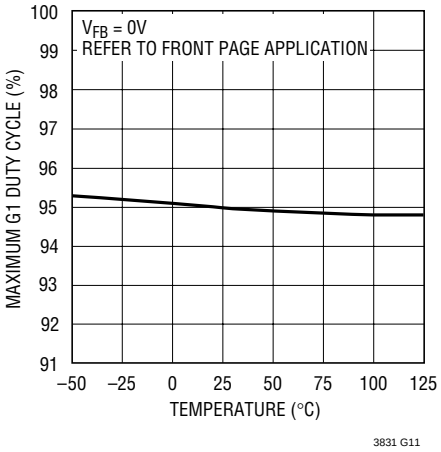


Oscillator (V_{SAWH} – V_{SAWL}) vs External Sync Frequency

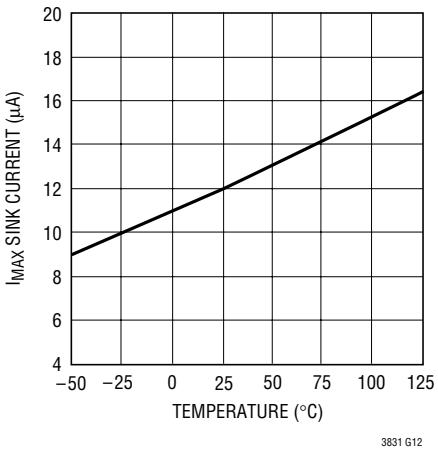


TYPICAL PERFORMANCE CHARACTERISTICS

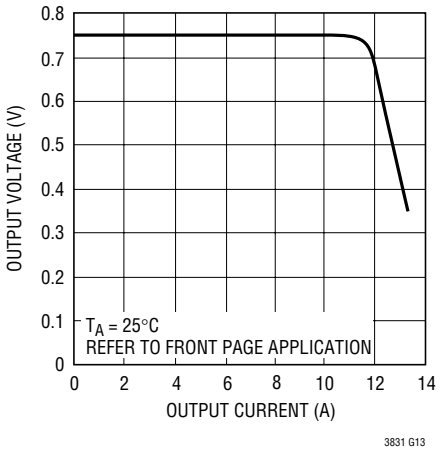
Maximum TG Duty Cycle vs Temperature



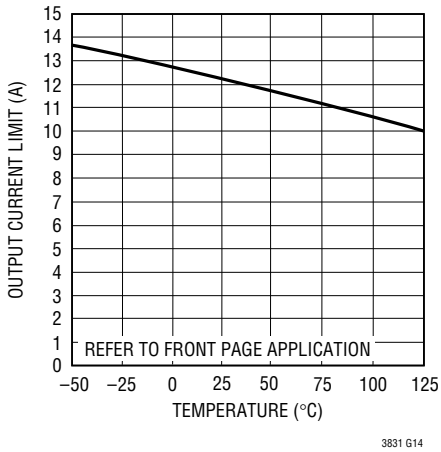
I_{MAX} Sink Current vs Temperature



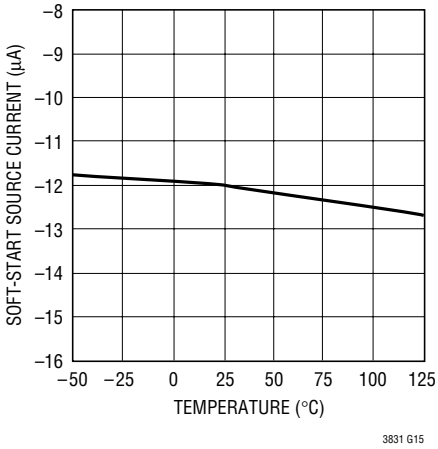
Output Overcurrent Protection



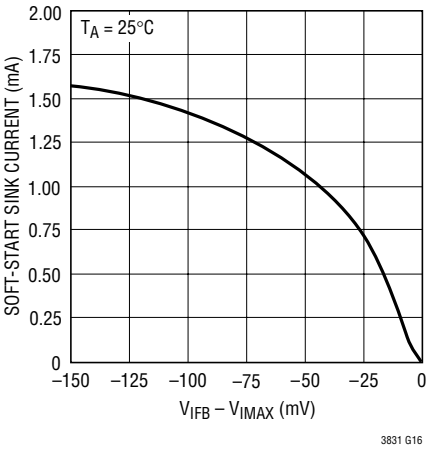
Output Current Limit Threshold vs Temperature



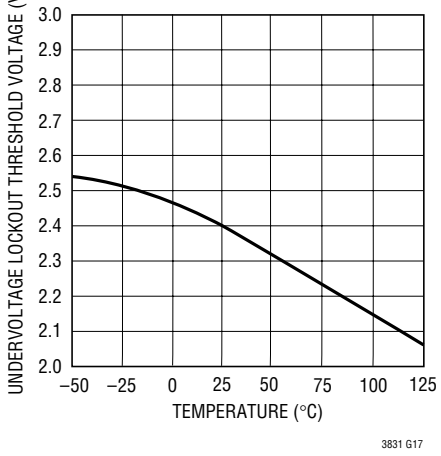
Soft-Start Source Current vs Temperature



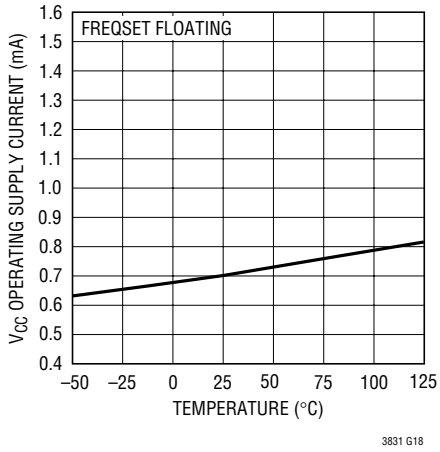
Soft-Start Sink Current vs (V_{IFB} – V_{IMAX})



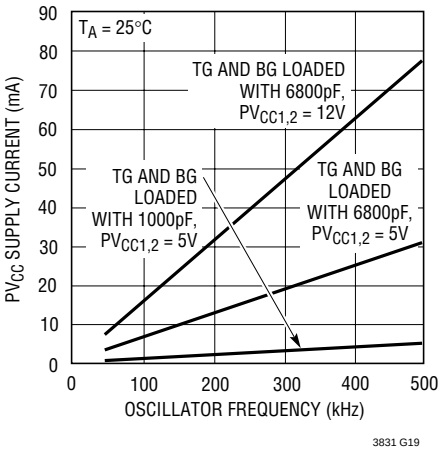
Undervoltage Lockout Threshold Voltage vs Temperature



V_{CC} Operating Supply Current vs Temperature

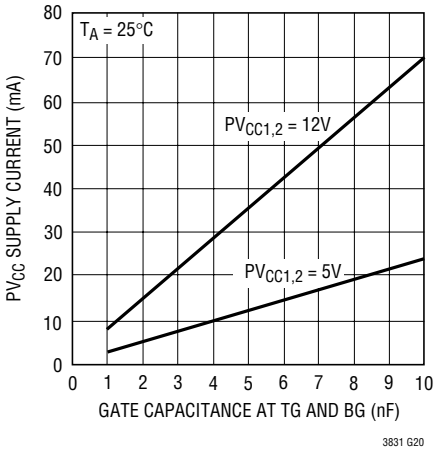


PV_{CC} Supply Current vs Oscillator Frequency

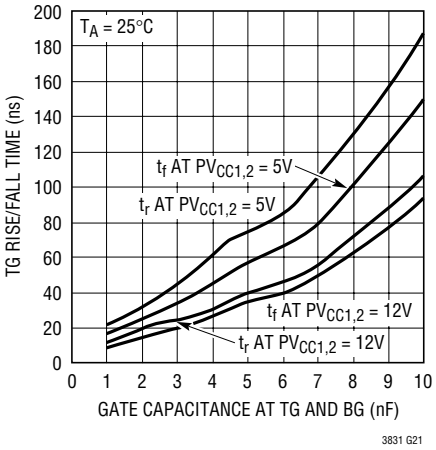


TYPICAL PERFORMANCE CHARACTERISTICS

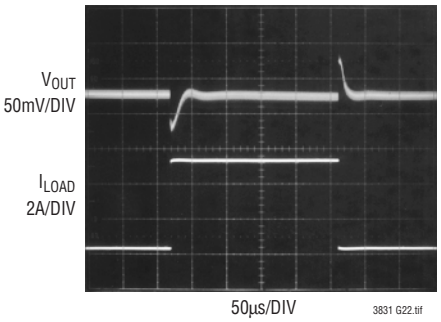
PV_{CC} Supply Current vs Gate Capacitance



TG Rise/Fall Time vs Gate Capacitance



Transient Response



PIN FUNCTIONS

TG (Pin 1): Top Driver Output. Connect this pin to the gate of the upper N-channel MOSFET, Q1. This output swings from PGND to PV_{CC1}. It remains low if BG is high or during shutdown mode.

PV_{CC1} (Pin 2): Power Supply Input for TG. Connect this pin to a potential of at least V_{IN} + $V_{GS(ON)(Q1)}$. For normal operation, PV_{CC1} must also be higher than V_{CC} by at least 2V when TG is high. This allows the use of an external charge pump to power PV_{CC1}.

PGND (Pin 3): Power Ground. Both drivers return to this pin. Connect this pin to a low impedance ground in close proximity to the source of Q2. Refer to the Layout Consideration section for more details on PCB layout techniques.

GND (Pin 4): Signal Ground. All low power internal circuitry returns to this pin. To minimize regulation errors due to ground currents, connect GND to PGND right at the LTC3831-1.

R^-, R^+ (Pins 5, 7): These two pins connect to the internal resistor divider that generate the internal ratiometric reference for the error amplifier. The reference voltage is set at 0.5 • (V_{R+} – V_{R-}).

FB (Pin 6): Feedback Voltage. FB senses the regulated output voltage either directly or through an external resistor divider. The FB pin is servoed to the ratiometric reference under closed-loop conditions. The LTC3831-1 can operate with a minimum V_{FB} of 0.4V and maximum V_{FB} of (V_{CC} – 2V).

$\overline{SHDN}$ (Pin 8): Shutdown. A TTL compatible low level at $\overline{SHDN}$ for longer than 100µs puts the LTC3831-1 into shutdown mode. In shutdown, TG and BG go low, all internal circuits are disabled and the quiescent current drops to 10µA max. A TTL compatible high level at $\overline{SHDN}$ allows the part to operate normally. This pin also double as an external clock input to synchronize the internal oscillator with an external clock.

SS (Pin 9): Soft-Start. Connect this pin to an external capacitor, C_{SS}, to implement a soft-start function. If the LTC3831-1 goes into current limit, C_{SS} is discharged to reduce the duty cycle. C_{SS} must be selected such that during power-up, the current through Q1 will not exceed the current limit level.

COMP (Pin 10): External Compensation. This pin internally connects to the output of the error amplifier and input of the PWM comparator. Use a RC + C network at this pin to compensate the feedback loop to provide optimum

PIN FUNCTIONS

transient response.

FREQSET (Pin 11): Frequency Set. Use this pin to adjust the free-running frequency of the internal oscillator. With the pin floating, the oscillator runs at about 300kHz. A resistor from FREQSET to ground speeds up the oscillator; a resistor to V_{CC} slows it down.

I_{MAX} (Pin 12): Current Limit Threshold Set. I_{MAX} sets the threshold for the internal current limit comparator. If I_{FB} drops below I_{MAX} with TG on, the LTC3831-1 goes into current limit. I_{MAX} has an internal 12µA pull-down to GND. Connect this pin to the main V_{IN} supply at the drain of Q1, through an external resistor to set the current limit threshold. Connect a 0.1µF decoupling capacitor across this resistor to filter switching noise.

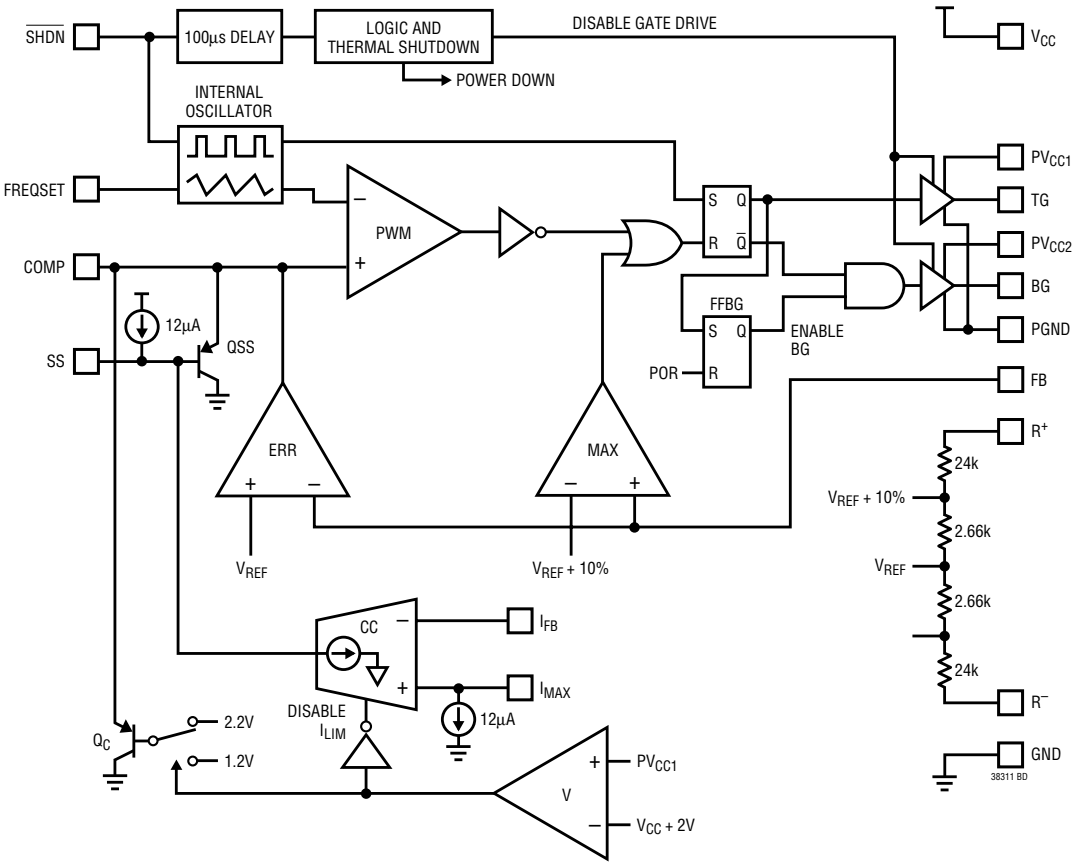
I_{FB} (Pin 13): Current Limit Sense. Connect this pin to the switching node at the source of Q1 and the drain of Q2 through a 1k resistor. The 1k resistor is required to prevent voltage transients from damaging I_{FB}.This pin is used for sensing the voltage drop across the upper N-channel MOSFET, Q1.

V_{CC} (Pin 14): Power Supply Input. All low power internal circuits draw their supply from this pin. This pin requires a 4.7µF bypass capacitor to GND.

PV_{CC2} (Pin 15): Power Supply Input for BG. Connect this pin to the main high power supply.

BG (Pin 16): Bottom Driver Output . Connect this pin to the gate of the lower N-channel MOSFET, Q2. This output swings from PGND to PV_{CC2}. It remains low when TG is high or during shutdown mode. To prevent output undershoot during a soft-start cycle, BG is held low until TG first goes high (FFBG in the Block Diagram).

BLOCK DIAGRAM



TEST CIRCUITS

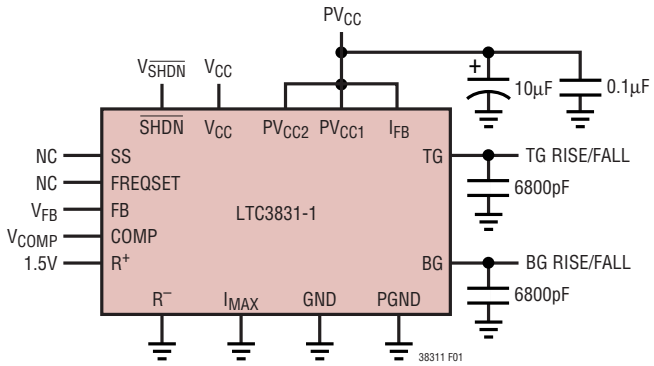


Figure 1

APPLICATIONS INFORMATION

OVERVIEW

The LTC3831-1 is a voltage mode feedback, synchronous switching regulator controller (see Block Diagram) designed for use in high to medium power, DDR memory termination. It includes an onboard PWM generator, a ratiometric reference, two high power MOSFET gate drivers and all necessary feedback and control circuitry to form a complete switching regulator circuit. The PWM loop nominally runs at 300kHz.

The LTC3831-1 is designed to generate an output voltage that tracks at 1/2 of the external voltage connected between the R^+ and R^- pins. The LTC3831-1 can be used to generate the termination voltage, V_{TT}, for interface like the SSTL_2 where V_{TT} is a ratio of the interface supply voltage, V_{DDQ}. It is a requirement in the SSTL_2 interface standard for V_{TT} to track the interface supply voltage to improve noise immunity. Using the LTC3831-1 to supply the interface termination voltage allows large current sourcing and sinking through the termination resistors during bus transitions.

The LTC3831-1 includes a current limit sensing circuit that uses the topside external N-channel power MOSFET as a current sensing element, eliminating the need for an external sense resistor. Also included is an internal soft-start feature that requires only a single external capacitor to operate. In addition, the part features an adjustable oscillator which can free run or synchronize to an external signal with frequencies from 100kHz to 500kHz, allowing added flexibility in external component selection.

THEORY OF OPERATION

Primary Feedback Loop

The LTC3831-1 senses the output voltage of the circuit through the FB pin and feeds this voltage back to the internal transconductance error amplifier, ERR. The error amplifier compares the output voltage to the internal ratiometric reference, V_{REF}, and outputs an error signal to the PWM comparator. V_{REF} is set to 0.5 multiplied by the voltage difference between the R^+ and R^- pins, using an internal resistor divider.

This error signal is compared with a fixed frequency ramp waveform, from the internal oscillator, to generate a pulse width modulated signal. This PWM signal drives the external MOSFETs through the TG and BG pins. The resulting chopped waveform is filtered by L_O and C_{OUT} which closes the loop. Loop compensation is achieved with an external compensation network at the COMP pin, the output node of the error amplifier.

MAX Feedback Loop

An additional comparator in the feedback loop provides high speed output voltage correction in situations where the error amplifier may not respond quickly enough. MAX compares the feedback signal to a voltage 10% above V_{REF}. If the signal is above the comparator threshold, the MAX comparator overrides the error amplifier and forces the loop to minimum duty cycle, 0%. To prevent this

APPLICATIONS INFORMATION

comparator from triggering due to noise, the MAX comparator's response time is deliberately delayed by two to three microseconds. This comparator helps prevent extreme output perturbations with fast output load current transients, while allowing the main feedback loop to be optimally compensated for stability.

Thermal Shutdown

The LTC3831-1 has a thermal protection circuit that disables both gate drivers if activated. If the chip junction temperature reaches 150°C, both TG and BG are pulled low. TG and BG remain low until the junction temperature drops below 125°C, after which, the chip resumes normal operation.

Soft-Start and Current Limit

The LTC3831-1 includes a soft-start circuit that is used for start-up and current limit operation. The SS pin requires an external capacitor, CSS, to GND with the value determined by the required soft-start time. An internal 12µA current source is included to charge C_{SS}. During power-up, the COMP pin is clamped to a diode drop (B-E junction of QSS in the Block Diagram) above the voltage at the SS pin. This prevents the error amplifier from forcing the loop to maximum duty cycle. The LTC3831-1 operates at low duty cycle as the SS pin rises above 0.6V ($V_{COMP} \approx 1.2V$). As SS continues to rise, Q_{SS} turns off and the error amplifier takes over to regulate the output.

The LTC3831-1 includes yet another feedback loop to control operation in current limit. Just before every falling edge of TG, the current comparator, CC, samples and holds the voltage drop measured across the external upper MOSFET, Q1, at the I_{FB} pin. CC compares the voltage at I_{FB} to the voltage at the I_{MAX} pin. As the peak current rises, the measured voltage across Q1 increases due to the drop across the $R_{DS(ON)}$ of Q1. When the voltage at I_{FB} drops below I_{MAX}, indicating that Q1's drain current has exceeded the maximum level, CC starts to pull current out of C_{SS}, cutting the duty cycle and controlling the output current level. The CC comparator pulls current out of the SS pin in proportion to the voltage difference between I_{FB} and I_{MAX}. Under minor overload conditions, the SS pin falls gradually, creating a time delay before current limit takes effect. Very short, mild overloads may not affect the output voltage at all. More significant overload conditions allow the SS pin to reach a steady state, and the output remains at a reduced voltage until the overload is removed. Serious overloads generate a large overdrive at CC, allowing it to pull SS down quickly and preventing damage to the output components. By using the $R_{DS(ON)}$ of Q1 to measure the output current, the current limiting circuit eliminates an expensive discrete sense resistor that would otherwise be required. This helps minimize the number of components in the high current path.

The current limit threshold can be set by connecting an external resistor R_{IMAX} from the I_{MAX} pin to the main V_{IN} supply at the drain of Q1. The value of R_{IMAX} is determined by:

$$R_{IMAX} = (I_{LMAX})(R_{DS(ON)Q1})/I_{IMAX}$$

where:

$I_{LMAX} = I_{LOAD} + (I_{RIPPLE}/2)$

I_{LOAD}= Maximum load current

I_{RIPPLE} = Inductor ripple current

$$= \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_{OSC})(L_O)(V_{IN})}$$

f_{OSC} = LTC3831-1 oscillator frequency = 300kHz

L_O = Inductor value

$R_{DS(ON)Q1}$ = On-resistance of Q1 at I_{LMAX}

I_{IMAX} = Internal 12µA sink current at I_{MAX}

The $R_{DS(ON)}$ of Q1 usually increases with temperature. To keep the current limit threshold constant, the internal 12µA sink current at I_{MAX} is designed with a positive temperature coefficient to provide first order correction for the temperature coefficient of $R_{DS(ON)Q1}$.

In order for the current limit circuit to operate properly and to obtain a reasonably accurate current limit threshold, the I_{IMAX} and I_{FB} pins must be Kelvin sensed at Q1's drain and source pins. In addition, connect a 0.1µF decoupling capacitor across R_{IMAX} to filter switching noise. Otherwise, noise spikes or ringing at Q1's source can cause the

APPLICATIONS INFORMATION

actual current limit to be greater than the desired current limit set point. Due to switching noise and variation of $R_{DS(ON)}$, the actual current limit trip point is not highly accurate. The current limiting circuitry is primarily meant to prevent damage to the power supply circuitry during fault conditions. The exact current level where the limiting circuit begins to take effect will vary from unit to unit as the $R_{DS(ON)}$ of Q1 varies. Typically, $R_{DS(ON)}$ varies as much as ±40% and with ±25% variation on the LTC3831-1's I_{MAX} current, this can give a ±65% variation on the current limit threshold.

The $R_{DS(ON)}$ is high if the V_{GS} applied to the MOSFET is low. This occurs during power up, when PV_{CC1} is ramping up. To prevent the high $R_{DS(ON)}$ from activating the current limit, the LTC3831-1 disables the current limit circuit if PV_{CC1} is less than 2V above V_{CC}. To ensure proper operation of the current limit circuit, PV_{CC1} must be at least 2V above V_{CC} when TG is high. PV_{CC1} can go low when TG is low, allowing the use of an external charge pump to power PV_{CC1}.

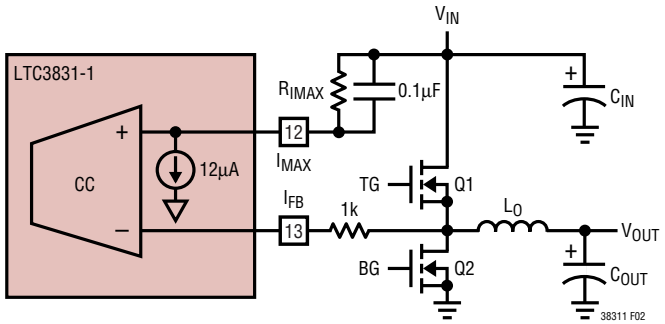


Figure 2. Current Limit Setting

Oscillator Frequency

The LTC3831-1 includes an onboard current controlled oscillator that typically free-runs at 300kHz. The oscillator frequency can be adjusted by forcing current into or out of the FREQSET pin. With the pin floating, the oscillator runs at about 300kHz. Every additional 1µA of current into/out of the FREQSET pin decreases/increases the frequency by 10kHz. The pin is internally servoed to 1.265V. The frequency can be estimated as:

$$f = 300kHz + \frac{1.265V - V_{EXT}}{R_{FSET}} \bullet \frac{10kHz}{1\mu A}$$

where R_{FSET} is a frequency programming resistor connected between FREQSET and the external voltage source V_{EXT}. Connecting an 82k resistor from FREQSET to ground forces 15µA out of the pin, causing the internal oscillator to run at approximately 450kHz. Forcing an external 20µA current into FREQSET cuts the internal frequency to 100kHz. An internal clamp prevents the oscillator from running slower than about 50kHz. Tying FREQSET to V_{CC} forces the chip to run at this minimum speed.

Shutdown

The LTC3831-1 includes a low power shutdown mode, controlled by the logic at the $\overline{SHDN}$ pin. A high at $\overline{SHDN}$ allows the part to operate normally. A low level at $\overline{SHDN}$ for more than 100µs forces the LTC3831-1 into shutdown mode. In this mode, all internal switching stops, the COMP and SS pins pull to ground and Q1 and Q2 turn off. The LTC3831-1 supply current drops to <10µA, although off-state leakage in the external MOSFETs may cause the total V_{IN} current to be somewhat higher, especially at elevated temperatures. If $\overline{SHDN}$ returns high, the LTC3831-1 re-runs a soft-start cycle and resumes normal operation.

External Clock Synchronization

The LTC3831-1 $\overline{SHDN}$ pin doubles as an external clock input for applications that require a synchronized clock. An internal circuit forces the LTC3831-1 into external synchronization mode if a negative transition at the $\overline{SHDN}$ pin is detected. In this mode, every negative transition on the $\overline{SHDN}$ pin resets the internal oscillator and pulls the ramp signal low. This forces the LTC3831-1 internal oscillator to lock to the external clock frequency.

The LTC3831-1 internal oscillator can be externally synchronized from 100kHz to 500kHz. Frequencies above 300kHz can cause a decrease in the maximum obtainable duty cycle as rise/fall time and propagation delay take up a larger percentage of the switch cycle. The low period of this clock signal must not be >100µs or else the LTC3831-1 enters into the shutdown mode.

Figure 3 describes the operation of the external synchronization function. A negative transition at the $\overline{SHDN}$ pin forces the internal ramp signal low to restart a new PWM cycle. Notice that the ramp amplitude is lowered as the

APPLICATIONS INFORMATION

external clock frequency goes higher. The effect of this decrease in ramp amplitude increases the open-loop gain of the controller feedback loop. As a result, the loop crossover frequency increases and it may cause the feedback loop to be unstable if the phase margin is insufficient.

To overcome this problem, the LTC3831-1 monitors the peak voltage of the ramp signal and adjust the oscillator charging current to maintain a constant ramp peak.

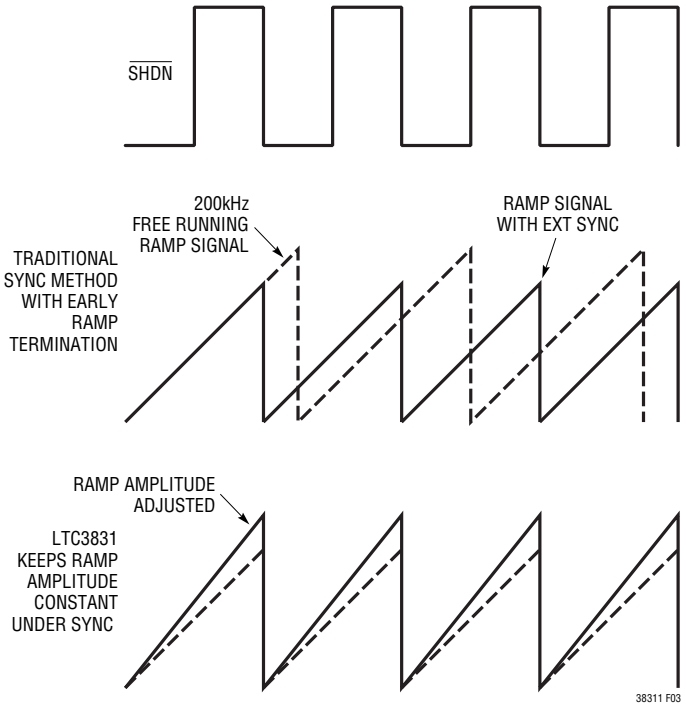


Figure 3. External Synchronization Operation

Input Supply Considerations/Charge Pump

The LTC3831-1 requires four supply voltages to operate: V_{IN} for the main power input, PV_{CC1} and PV_{CC2} for MOSFET gate drive and a clean, low ripple V_{CC} for the LTC3831-1 internal circuitry (Figure 4). V_{IN} is usually connected to V_{DDQ} in most DDR memory termination applications.

The V_{CC} supply can be as low as 3V and the quiescent current is typically 800µA. Place a 4.7µA bypass capacitor as close as possible to this pin. Gate drive for the top N-channel MOSFET Q1 is supplied from PV_{CC1}. This supply must be above V_{IN} by at least one power MOSFET $V_{GS(ON)}$ for efficient operation. In addition, this supply must be higher that V_{CC} by at least 2V for normal operation. An internal level shifter allows PV_{CC1} to operate at voltages above V_{CC} and V_{IN}, up to 14V maximum. This higher voltage can be supplied with a separate supply, or it can be generated using a charge pump.

Gate drive for the bottom MOSFET Q2 is provided through PV_{CC2}. This supply only needs to be above the power MOSFET $V_{GS(ON)}$ for efficient operation. PV_{CC2} can also be driven from the same supply/charge pump for the PV_{CC1}, or it can be connected to a lower supply to improve efficiency.

In a typical low voltage DDR memory termination application, V_{IN} or V_{DDQ} can be a low as 1.5V. If the only available supply for the LTC3831-1 is 3.3V, a tripling charge pump circuit can be added to power the PV_{CC1} and PV_{CC2} pins. This requires sub-logic level threshold power MOSFET with $R_{DS(ON)}$ specified at V_{GS} = 2.5V.

Figure 5 shows a tripling charge pump circuit that powers the PV_{CC1} and PV_{CC2} pins. This circuit provides (V_{CC} + $2V_{IN} - 3V_F$) to PV_{CC1} while Q1 is ON and ($V_{CC} + V_{IN} - 2V_F$) to PV_{CC2} where V_F is the ON voltage of the Schottky diode. The circuit requires the use of Schottky diodes to minimize forward drop across the diodes at start-up. The tripling charge pump circuit will tend to rectify any ringing at the drain of Q2 and can provide well more than (V_{CC} + $2V_{IN}$) at PV_{CC1}. A 12V zener diode may be included from PV_{CC1} to PGND to prevent transients from damaging the circuitry at PV_{CC1} or the gate of Q1.

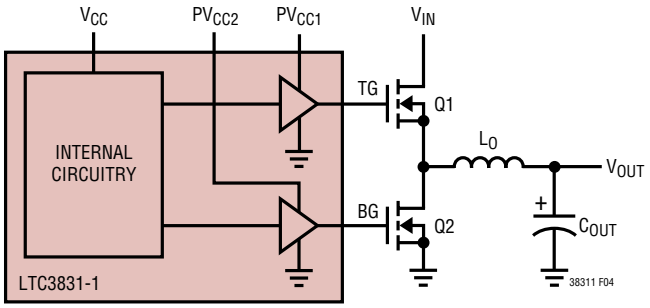


Figure 4. Input Supplies

APPLICATIONS INFORMATION

The charge pump capacitors for PV_{CC1} refresh when the BG pin goes high and the switch node is pulled low by Q2. The BG on time becomes narrow when the LTC3831-1 operates at maximum duty cycle (95% typical) which can occur if the input supply rises more slowly than the soft-start capacitor or the input voltage droops during load transients. If the BG on time gets so narrow that the switch node fails to pull completely to ground, the charge pump voltage may collapse or fail to start causing excessive dissipation in external MOSFET Q1. This is most likely with low V_{CC} voltages and high switching frequencies, coupled with large external MOSFETs that slow the BG and switch node slew rates.

The LTC3831-1 overcomes this problem by sensing the PV_{CC1} voltage when TG is high. If PV_{CC1} is less than 2V above V_{CC}, the maximum TG duty cycle is reduced to 70% by clamping the COMP pin at 1.8V (Q_C in the Block Diagram). This increases the BG on time and allows the charge pump capacitors to be refreshed.

For applications using an external supply to power PV_{CC1}, this supply must also be higher than V_{CC} by at least 2V to ensure normal operation.

Connecting the Ratiometric Reference Input

The LTC3831-1 derives its ratiometric reference, V_{REF}, using an internal resistor divider. The top and bottom of the resistor divider is connected to the R^+ and R^- pins respectively. This permits the output voltage to track at a ratio of the differential voltage at R^+ and R^-.

The LTC3831-1 can operate with a minimum V_{FB} of 0.4V and maximum V_{FB} of (V_{CC} – 2V). With R^- connected to GND, this gives a $V_R{}^+$ input range of 0.8V to (2 • V_{CC} – 4V). If $V_R{}^+$ is higher than the permitted input voltage, increase the V_{CC} voltage to raise the input range.

In a typical DDR memory termination, as shown in the typical application on the front page, R^+ is connected to V_{DDQ}, the supply voltage of the interface, and R^- to GND. The output voltage V_{TT} is connected to the FB pin, so V_{TT} = 0.5 • V_{DDQ}.

If a ratio greater than 0.5 is desired, it can be achieved using an external resistor divider connected to V_{TT} and FB pin. Figure 6 shows an application that generates a V_{TT} of 0.6 • V_{DDQ}.

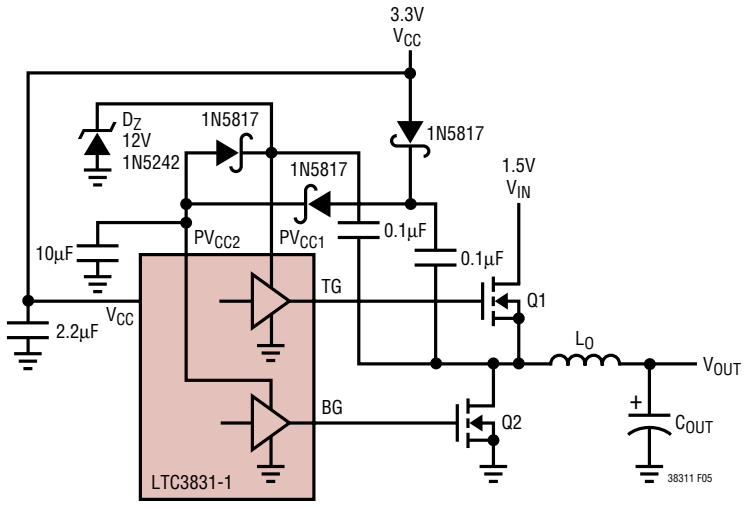


Figure 5. Triple Charge Pump Configuration

APPLICATIONS INFORMATION

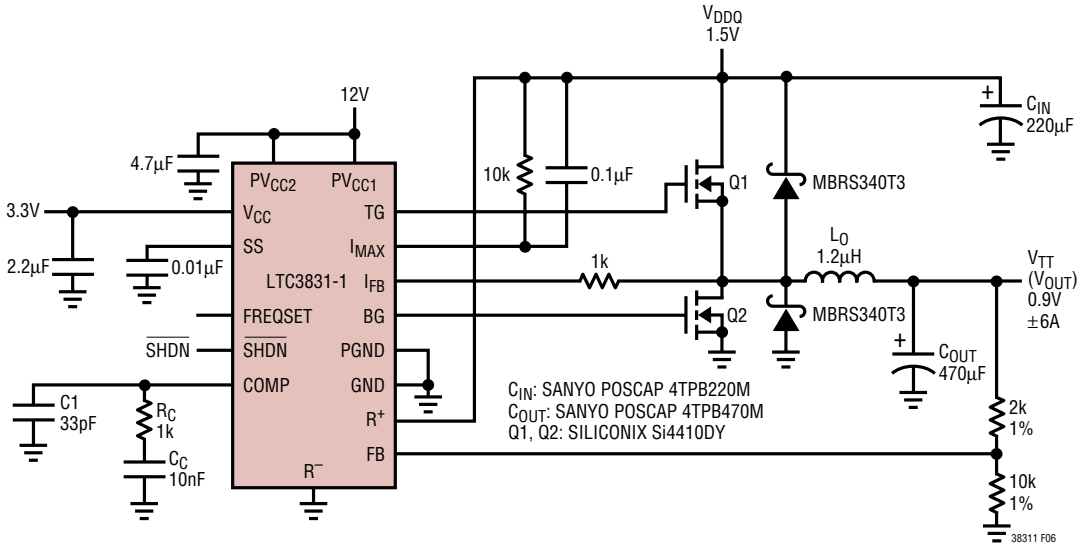


Figure 6. Typical Application with $V_{TT} = 0.6 \bullet V_{DDQ}$

Power MOSFETs

Two N-channel power MOSFETs are required for most LTC3831-1 circuits. These should be selected based primarily on threshold voltage and on-resistance considerations. Thermal dissipation is often a secondary concern in high efficiency designs. The required MOSFET threshold should be determined based on the available power supply voltages and/or the complexity of the gate drive charge pump scheme. In 3.3V input designs where an auxiliary 12V supply is available to power PV_{CC1} and PV_{CC2}, standard MOSFETs with $R_{DS(ON)}$ specified at V_{GS} = 5V or 6V can be used with good results. The current drawn from this supply varies with the MOSFETs used and the LTC3831-1's operating frequency, but is generally less than 50mA.

LTC3831-1 applications that use 5V or lower V_{IN} voltage and tripling charge pumps to generate PV_{CC1} and PV_{CC2}, do not provide enough gate drive voltage to fully enhance standard power MOSFETs. Under this condition, the effective MOSFET $R_{DS(ON)}$ may be quite high, raising the dissipation in the FETs and reducing efficiency. Logic-level or sub-logic level FETs are the recommended choice for 5V or lower voltage systems. Logic-level FETs can be fully enhanced with a tripling charge pump and will operate at maximum efficiency.

After the MOSFET threshold voltage is selected, choose the $R_{DS(ON)}$ based on the input voltage, the output voltage, allowable power dissipation and maximum output current. In a typical LTC3831-1 circuit operating in continuous mode, the average inductor current is equal to the output load current. This current flows through either Q1 or Q2 with the power dissipation split up according to the duty cycle:

$$DC(Q1) = \frac{V_{OUT}}{V_{IN}}$$

$$DC(Q2) = 1 - \frac{V_{OUT}}{V_{IN}} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The $R_{DS(ON)}$ required for a given conduction loss can now be calculated by rearranging the relation $P = I^2R$.

$$R_{DS(ON)Q1} = \frac{P_{MAX(Q1)}}{DC(Q1) \bullet (I_{LOAD})^2} = \frac{V_{IN} \bullet P_{MAX(Q1)}}{V_{OUT} \bullet (I_{LOAD})^2}$$

$$R_{DS(ON)Q2} = \frac{P_{MAX(Q2)}}{DC(Q2) \bullet (I_{LOAD})^2} = \frac{V_{IN} \bullet P_{MAX(Q2)}}{(V_{IN} - V_{OUT}) \bullet (I_{LOAD})^2}$$

P_{MAX} should be calculated based primarily on required efficiency or allowable thermal dissipation. A typical high

APPLICATIONS INFORMATION

efficiency circuit designed for 1.5V input and 0.75V at 5A output might allow no more than 3% efficiency loss at full load for each MOSFET. Assuming roughly 90% efficiency at this current level, this gives a P_{MAX} value of:

(0.75V)(5A/0.9)(0.03) = 0.125W per FET

and a required $R_{DS(ON)}$ of:

$$R_{DS(ON)Q1} = \frac{(1.5V) \bullet (0.125W)}{(0.75V)(5A)^2} = 0.01\Omega$$

$$R_{DS(ON)Q2} = \frac{(1.5V) \bullet (0.125W)}{(1.5V - 0.75V)(5A)^2} = 0.01\Omega$$

Note that while the required $R_{DS(ON)}$ values suggest large MOSFETs, the power dissipation numbers are only 0.125W per device or less; large TO-220 packages and heat sinks are not necessarily required in high efficiency applications. Siliconix Si4410DY or International Rectifier IRF7413 (both in SO-8) or Siliconix SUD50N03-10 (TO-252) or ON Semiconductor MTD20N03HDL (DPAK) are small footprint surface mount devices with $R_{DS(ON)}$ values below 0.03Ω at 5V of V_{GS} that work well in LTC3831-1 circuits. Using a higher P_{MAX} value in the $R_{DS(ON)}$ calculations generally decreases the MOSFET cost and the circuit efficiency and increases the MOSFET heat sink requirements.

Table 1 highlights a variety of power MOSFETs that are for use in LTC3831-1 applications.

Inductor Selection

The inductor is often the largest component in an LTC3831-1 design and must be chosen carefully. Choose the inductor value and type based on output slew rate requirements. The maximum rate of rise of inductor current is set by the inductor's value, the input-to-output voltage differential and the LTC3831-1's maximum duty cycle. In a typical 1.5V input 0.75V output application, the maximum rise time will be:

$$\frac{DC_{MAX} \bullet (V_{IN} - V_{OUT})}{L_O} = \frac{0.713}{L_O} \ \frac{A}{\mu s}$$

where L_O is the inductor value in µH. With proper frequency compensation, the combination of the inductor and output capacitor values determine the transient recovery time. In general, a smaller value inductor improves transient response at the expense of ripple and inductor core saturation rating. A 1µH inductor has a 0.713A/µs rise

Table 1. Recommended MOSFETs for LTC3831-1 Applications

PARTS	$R_{DS(ON)}$ AT 25°C (mΩ)	RATED CURRENT (A)	TYPICAL INPUT CAPACITANCE C_{ISS} (pF)	θ_{JC} (°C/W)	T_{JMAX} (°C)
Siliconix SUD50N03-10 TO-252	19	15 at 25°C 10 at 100°C	3200	1.8	175
Siliconix Si4410DY SO-8	20	10 at 25°C 8 at 70°C	2700		150
ON Semiconductor MTD20N03HDL D PAK	35	20 at 25°C 16 at 100°C	880	1.67	150
Fairchild FDS6670A S0-8	8	13 at 25°C	3200	25	150
Fairchild FDS6680 SO-8	10	11.5 at 25°C	2070	25	150
ON Semiconductor MTB75N03HDL DD PAK	9	75 at 25°C 59 at 100°C	4025	1	150
IR IRL3103S DD PAK	19	64 at 25°C 45 at 100°C	1600	1.4	175
IR IRLZ44 TO-220	28	50 at 25°C 36 at 100°C	3300	1	175
Fuji 2SK1388 TO-220	37	35 at 25°C	1750	2.08	150

Note: Please refer to the manufacturer's data sheet for testing conditions and detailed information.

APPLICATIONS INFORMATION

time in this application, resulting in a 7µs delay in responding to a 5A load current step. During this 7µs, the difference between the inductor current and the output current is made up by the output capacitor. This action causes a temporary voltage droop at the output. To minimize this effect, the inductor value should usually be in the 1µH to 5µH range for most LTC3831-1 circuits. To optimize performance, different combinations of input and output voltages and expected loads may require different inductor values.

Once the required value is known, the inductor core type can be chosen based on peak current and efficiency requirements. Peak current in the inductor will be equal to the maximum output load current plus half of the peak-to-peak inductor ripple current. Ripple current is set by the inductor value, the input and output voltage and the operating frequency. The ripple current is approximately equal to:

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \bullet (V_{OUT})}{f_{OSC} \bullet L_O \bullet V_{IN}}$$

f_{OSC} = LTC3831-1 oscillator frequency = 300kHz

L_O = Inductor value

Solving this equation with our typical 1.5V to 0.75V application with 1µH inductor, we get:

$$\frac{(1.5V - 0.75V) \bullet 0.75V}{300kHz \bullet 1\mu H \bullet 1.5V} = 1.25A_{P-P}$$

Peak inductor current at 5A load:

5A + (1.25A/2) = 5.625A

The ripple current should generally be between 10% and 40% of the output current. The inductor must be able to withstand this peak current without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. Note that in circuits not employing the current limit function, the current in the inductor may rise above this maximum under short circuit or fault conditions; the inductor should be sized accordingly to withstand this additional current. Inductors with gradual saturation characteristics are often the best choice.

Input and Output Capacitors

A typical LTC3831-1 design places significant demands on both the input and the output capacitors. During normal steady load operation, a buck converter like the LTC3831-1 draws square waves of current from the input supply at the switching frequency. The peak current value is equal to the output load current plus 1/2 the peak-to-peak ripple current. Most of this current is supplied by the input bypass capacitor. The resulting RMS current flow in the input capacitor heats it and causes premature capacitor failure in extreme cases. Maximum RMS current occurs with 50% PWM duty cycle, giving an RMS current value equal to $I_{OUT}/2$. A low ESR input capacitor with an adequate ripple current rating must be used to ensure reliable operation. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours (3 months) lifetime at rated temperature. Further derating of the input capacitor ripple current beyond the manufacturer's specification is recommended to extend the useful life of the circuit. Lower operating temperature has the largest effect on capacitor longevity.

The output capacitor in a buck converter under steady-state conditions sees much less ripple current than the input capacitor. Peak-to-peak current is equal to inductor ripple current, usually 10% to 40% of the total load current. Output capacitor duty places a premium not on power dissipation but on ESR. During an output load transient, the output capacitor must supply all of the additional load current demanded by the load until the LTC3831-1 adjusts the inductor current to the new value. ESR in the output capacitor results in a step in the output voltage equal to the ESR value multiplied by the change in load current. A 5A load step with a 0.05Ω ESR output capacitor results in a 250mV output voltage shift; this is 20% of the output voltage for a 1.25V supply! Because of the strong relationship between output capacitor ESR and output load transient response, choose the output capacitor for ESR, not for capacitance value. A capacitor with suitable ESR will usually have a larger capacitance value than is needed to control steady-state output ripple.

Electrolytic capacitors, such as the Sanyo MV-WX series, rated for use in switching power supplies with specified ripple current ratings and ESR, can be used effectively in

APPLICATIONS INFORMATION

LTC3831-1 applications. OS-CON electrolytic capacitors from Sanyo and other manufacturers give excellent performance and have a very high performance/size ratio for electrolytic capacitors. Surface mount applications can use either electrolytic or dry tantalum capacitors. Tantalum capacitors must be surge tested and specified for use in switching power supplies. Low cost, generic tantalums are known to have very short lives followed by explosive deaths in switching power supply applications. Other capacitor series that can be used include Sanyo POSCAPs and the Panasonic SP line.

A common way to lower ESR and raise ripple current capability is to parallel several capacitors. A typical LTC3831-1 application might exhibit 5A input ripple current. Sanyo OS-CON capacitors, part number 10SA220M (220µF/10V), feature 2.3A allowable ripple current at 85°C; three in parallel at the input (to withstand the input ripple current) meet the above requirements. Similarly, Sanyo POSCAP 4TPB470M (470µF/4V) capacitors have a maximum rated ESR of 0.04Ω, three in parallel lower the net output capacitor ESR to 0.013Ω.

Feedback Loop Compensation

The LTC3831-1 voltage feedback loop is compensated at the COMP pin, which is the output node of the error amplifier. The feedback loop is generally compensated with an RC + C network from COMP to GND as shown in Figure 7a.

Loop stability is affected by the values of the inductor, the output capacitor, the output capacitor ESR, the error amplifier transconductance and the error amplifier compensation network. The inductor and the output capacitor create a double pole at the frequency:

$$f_{LC} = 1/\left[2\pi\sqrt{(L_O)(C_{OUT})}\right]$$

The ESR of the output capacitor and the output capacitor value form a zero at the frequency:

$$f_{ESR} = 1/\left[2\pi(ESR)(C_{OUT})\right]$$

The compensation network used with the error amplifier must provide enough phase margin at the 0dB crossover frequency for the overall open-loop transfer function. The zero and pole from the compensation network are:

$f_Z = 1/[2\pi(R_C)(C_C)]$ and

$f_P = 1/[2\pi(R_C)(C1)]$ respectively.

Figure 7b shows the Bode plot of the overall transfer function.

Although a mathematical approach to frequency compensation can be used, the added complication of input and/or output filters, unknown capacitor ESR, and gross operating point changes with input voltage, load current variations, all suggest a more practical empirical method. This can be done by injecting a transient current at the load and using an RC network box to iterate toward the final values, or by obtaining the optimum loop response using a network analyzer to find the actual loop poles and zeros.

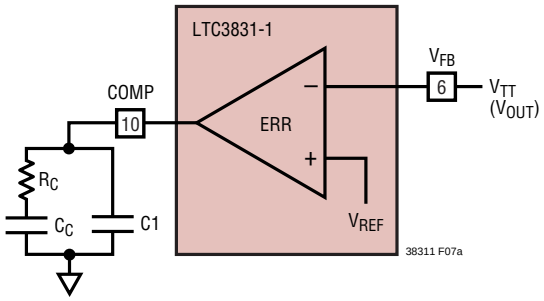


Figure 7a. Compensation Pin Connections

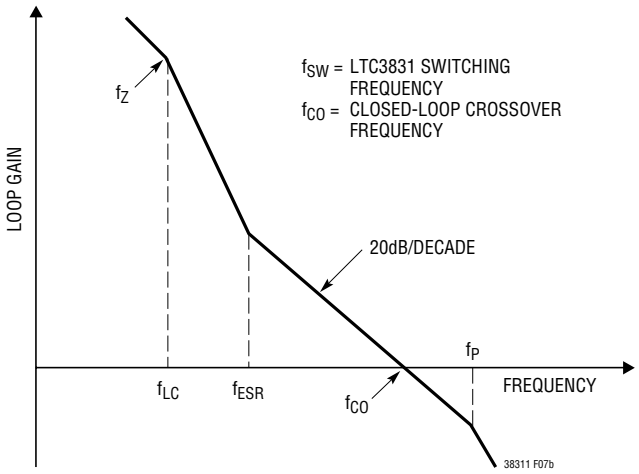


Figure 7b. Bode Plot of the LTC3831-1 Overall Transfer Function

APPLICATIONS INFORMATION

Table 2 shows the suggested compensation component value for 1.5V to 0.75V applications based on the 470µF Sanyo POSCAP 4TPB470M output capacitors.

Table 3 shows the suggested compensation component values for 1.5V to 0.75V applications based on 1500µF Sanyo MV-WX output capacitors.

LAYOUT CONSIDERATIONS

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3831-1. These items are also illustrated graphically in the layout diagram of Figure 8. The thicker lines show the high current paths. Note that at 5A current levels or above, current density in the PC board itself is a serious concern.

Table 2. Recommended Compensation Network for 1.5V to 0.75V Applications Using Multiple Paralleled 470µF Sanyo POSCAP 4TPB470M Output Capacitors

L1 (µH)	C_{OUT} (µF)	R_C (kΩ)	C_C (nF)	C1 (pF)
1.2	1410	5.6	3.3	68
1.2	2820	12	3.3	33
1.2	4700	20	2.2	22
2.4	1410	12	3.3	33
2.4	2820	27	1.5	15
2.4	4700	43	1.0	10
4.7	1410	24	1.5	15
4.7	2820	51	1.0	10
4.7	4700	93	3.3	10

Table 3. Recommended Compensation Network for 1.5V to 0.75V Applications Using Multiple Paralleled 1500µF Sanyo MV-WX Output Capacitors

L1 (µH)	C_{OUT} (µF)	R_C (kΩ)	C_C (nF)	C1 (pF)
1.2	4500	15	2.2	120
1.2	6000	18	2.2	82
1.2	9000	30	1	56
2.4	4500	30	1	56
2.4	6000	39	1	33
2.4	9000	62	1	27
4.7	4500	62	1	27
4.7	6000	82	1	22
4.7	9000	130	1	10

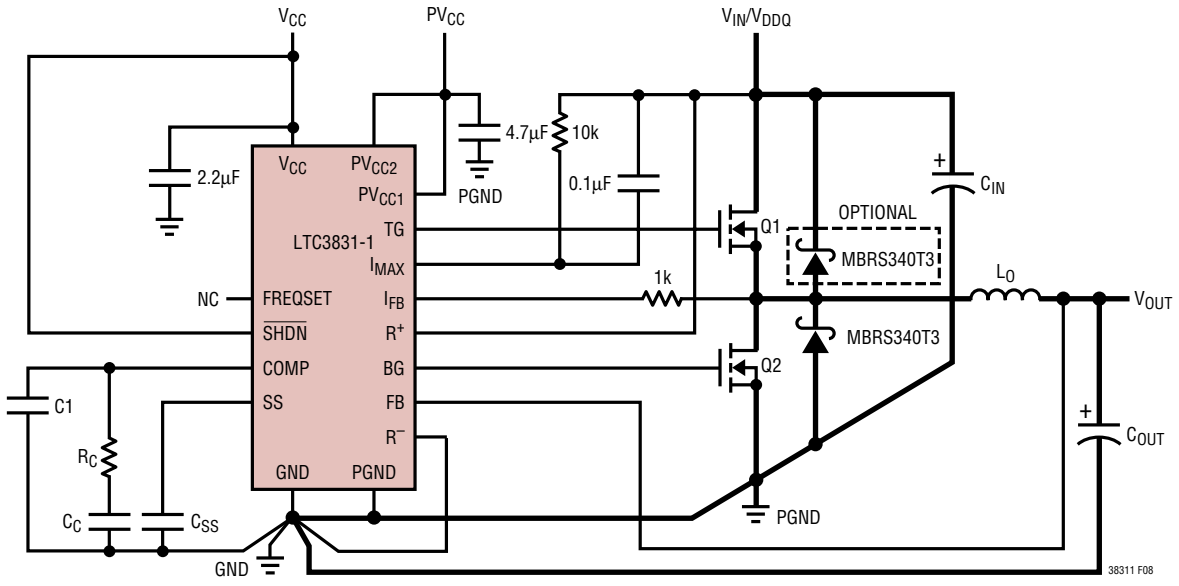


Figure 8. Typical Schematic Showing Layout Considerations

APPLICATIONS INFORMATION

Traces carrying high current should be as wide as possible. For example, a PCB fabricated with *2oz copper* requires a minimum trace width of *0.15" to carry 5A*.

1. In general, layout should begin with the location of the power devices. Be sure to orient the power circuitry so that a clean power flow path is achieved. Conductor widths should be maximized and lengths minimized. After you are satisfied with the power path, the control circuitry should be laid out. It is much easier to find routes for the relatively small traces in the control circuits than it is to find circuitous routes for high current paths.

2. *The GND and PGND pins should be shorted directly at the LTC3831-1*. This helps to minimize internal ground disturbances in the LTC3831-1 and prevents differences in ground potential from disrupting internal circuit operation. This connection should then tie into the ground plane at a single point, preferably at a fairly quiet point in the circuit such as *close to the output capacitors*. This is not always practical, however, due to physical constraints. Another reasonably good point to make this connection is between the output capacitors and the source connection of the bottom MOSFET Q2. Do not tie this single point ground in the trace run between the Q2 source and the input capacitor ground, as this area of the ground plane will be very noisy.

3. The small-signal resistors and capacitors for frequency compensation and soft-start should be located very close to their respective pins and the ground ends connected to the signal ground pin through a separate trace. Do not connect these parts to the ground plane!

4. The V_{CC}, PV_{CC1} and PV_{CC2} decoupling capacitors should be as close to the LTC3831-1 as possible. The 4.7µF and 2.2µF bypass capacitors shown at V_{CC}, PV_{CC1} and PV_{CC2} will help provide optimum regulation performance.

5. The (+) plate of C_{IN} should be connected as close as possible to the drain of the upper MOSFET, Q1. An additional 1µF ceramic capacitor between V_{IN} and power ground is recommended.

6. The V_{FB} pin is very sensitive to pickup from the switching node. Care should be taken to isolate V_{FB} from possible capacitive coupling to the inductor switching signal.

7. In a typical SSTL application, if the R^+ pin is to be connected to V_{DDQ}, which is also the main supply voltage for the switching regulator, do not connect R^+ along the high current flow path; it should be connected to the SSTL interface supply output. R^- should be connected to the interface supply GND.

8. Kelvin sense I_{MAX} and I_{FB} at Q1's drain and source pins.

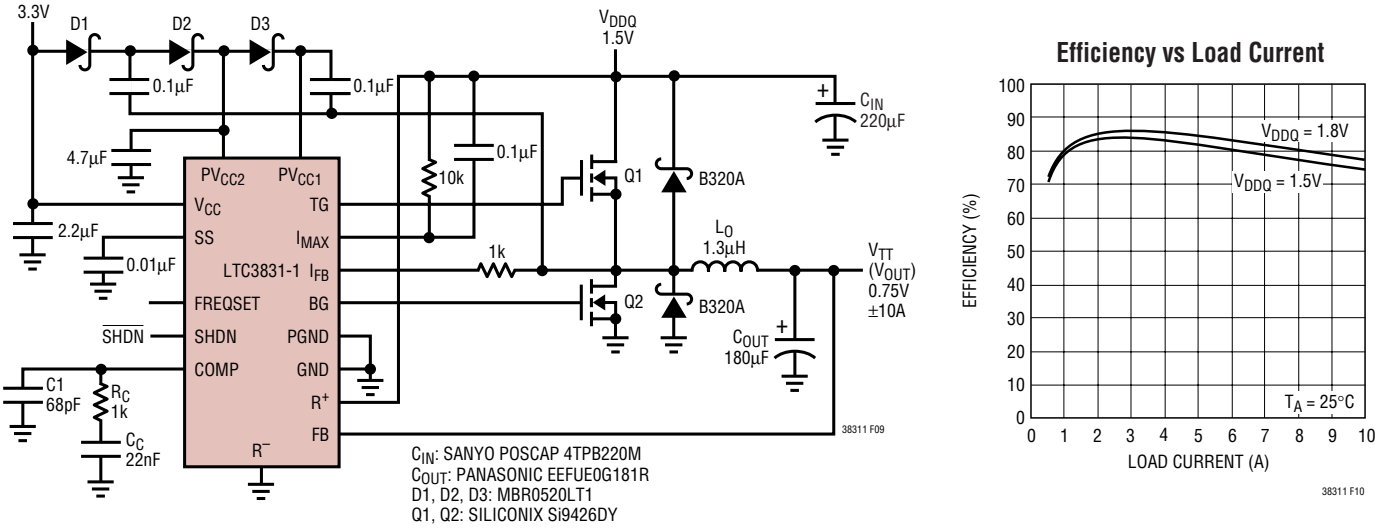
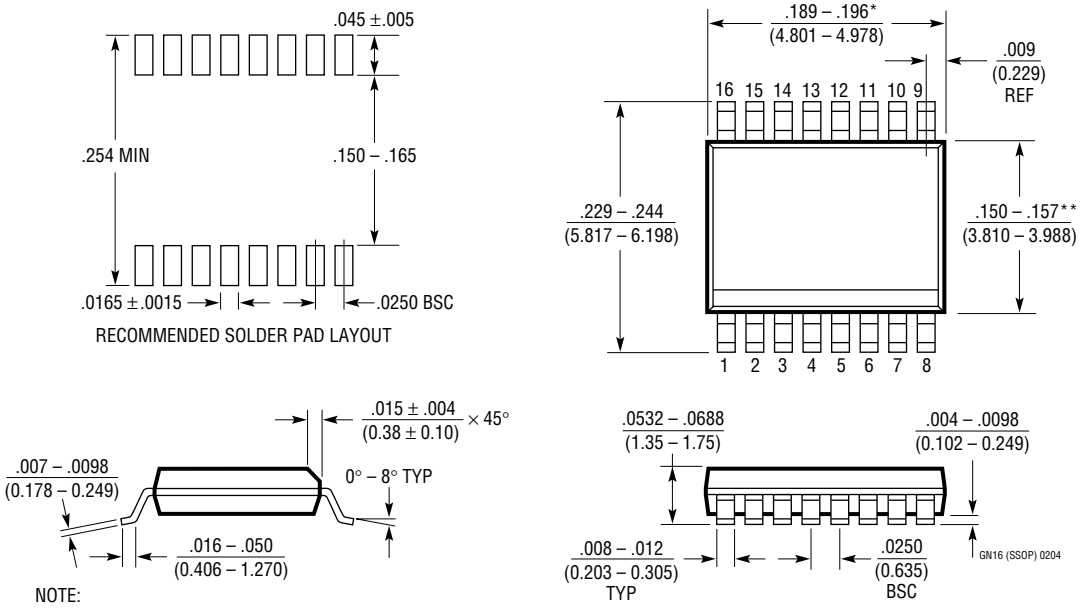


Figure 9. DDR Memory Termination with Triple Charge Pump

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1628/LTC3728	Dual High Efficiency 2-Phase Synchronous Step-Down Controllers	Constant Frequency, Standby 5V and 3.3V LDOs, 3.5V ≤ V_{IN} ≤ 36V
LTC1702	Dual High Efficiency 2-Phase Synchronous Step-Down Controller	550kHz, 25MHz GBW Voltage Mode, V_{IN} ≤ 7V, No R_{SENSE}™
LTC1703	Dual 550kHz Synchronous 2-Phase Switching Regulator Controller with Mobile VID	LTC1702 with Mobile VID for Portable Systems
LTC1705	Dual 550kHz Synchronous 2-Phase Switching Regulator Controller with 5-Bit VID Plus LDO	Provides Core, I/O and CLK Supplies for Portable Systems
LTC1709 Family	2-Phase, 5-Bit Desktop VID Synchronous Step-Down Controllers	Current Mode, V_{IN} to 36V, I_{OUT} Up to 42A, Various VID Tables
LTC1736	Synchronous Step-Down Controller with 5-Bit Mobile VID Control	Fault Protection, Power Good, 3.5V to 36V Input, Current Mode
LTC1778	Wide Operating Range/Step-Down Controller, No R_{SENSE}	V_{IN} Up to 36V, Current Mode, Power Good
LTC1873	Dual Synchronous Switching Regulator with 5-Bit Desktop VID	1.3V to 3.5V Programmable Core Output Plus I/O Output
LTC1929/LTC3729	2-Phase, Synchronous High Efficiency Converter with Mobile VID	Current Mode Ensures Accurate Current Sensing V_{IN} Up to 36V, I_{OUT} Up to 40A
LTC3413	3A, Monolithic Synchronous Regulator for DDR/QDR Memory Termination	Low $R_{DS(ON)}$ Internal Switch: 85mΩ, ±3A Output Current (Sink and Source), V_{OUT} = V_{REF}/2
LTC3708	Dual, 2-Phase, No R_{SENSE} Synchronous Controller with Tracking	Programmable Output Voltage Up/Down Tracking, Very Fast Transient Response, 5V ≤ V_{IN} ≤ 36V
LTC3713	Low Input Voltage, High Power, No R_{SENSE}, Step-Down Synchronous Controller	Minimum V_{IN}: 1.5V, Uses Standard Logic-Level N-Channel MOSFETs
LTC3778	Wide Operating Range, No R_{SENSE}, Step-Down Controller	V_{IN} Up to 36V, Current Mode, Power Good, Stable with Ceramic C_{OUT}
LTC3717	Wide V_{IN} Step-Down Controller for DDR Memory Termination	Current Mode Operation, V_{OUT} = 1/2 V_{IN}, V_{OUT} (V_{TT}) Tracks V_{IN} (V_{DDQ}), No R_{SENSE}, Symmetrical Sink and Source Output Current Limit
LTC3718	Bus termination Supply for Low Votlage V_{IN}	1.5V ≤ V_{IN}, Generates 5V Gate Drive for Standard N-Ch MOSFETs, 2A ≤ I_{OUT} ≤ 25A
LTC3831	High Power Synchronous Switching Regulator Controller for DDR Memory Termination	V_{OUT} Tracks 1/2 of V_{IN} or External Reference
LTC3832	High Power Synchronous Switching Regulator Controller	V_{OUT} as low as 0.6V

No R_{SENSE} is a trademark of Linear Technology Corporation.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT/TP 0304 1K • PRINTED IN USA