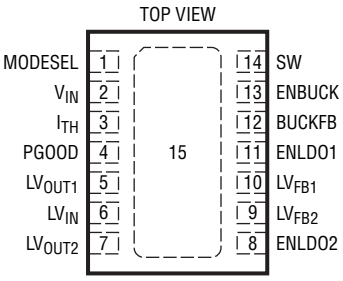
## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{IN}$, $LV_{IN}$ to GND ..... –0.3V to 6V
MODESEL, ENBUCK, ENLDO1,
ENLDO2 to GND..... –0.3V to 6V
BUCKFB to GND..... –0.3V to 6V
$LV_{FB1}$, $LV_{FB2}$ to GND..... –0.3V to 6V
$I_{TH}$ to GND ..... –0.3V to the Lesser of ($V_{IN}$ + 0.3V) or 3V
SW to GND.....–0.3V to the Lesser of ($V_{IN}$ + 0.3V) or 6V
$LV_{OUT1}$, $LV_{OUT2}$
to GND .....–0.3V to the Lesser of ($LV_{IN}$ + 0.3V) or 6V
PGOOD to GND ..... –0.3V to 6V
$LV_{OUT1}$, $LV_{OUT2}$ Short-Circuit
to GND Duration..... Indefinite
Operating Junction Temperature Range
(Note 2).....–40°C to 125°C
Storage Temperature Range..... –65°C to 150°C

## PIN CONFIGURATION




DE PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 43°C/W
EXPOSED PAD (PIN 15) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC3446EDE#PBF | LTC3446EDE#TRPBF | 3446 | 14-Lead (4mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3446IDE#PBF | LTC3446IDE#TRPBF | 3446 | 14-Lead (4mm × 3mm) Plastic DFN | –40°C to 125°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 3.6V unless otherwise specified. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input Voltage Range | (Note 3) | ● | 2.7 | | 5.5 | V |
| $V_{UVLO}$ | $V_{IN}$ Undervoltage Lockout Threshold<br>$V_{IN}$ Undervoltage Lockout Hysteresis | $V_{IN}$ Rising | ● | | 2.37<br>10 | 2.5<br>30 | V<br>mV |
| $I_Q$ | $V_{IN}$ Quiescent Current (Note 4) | | | | | | |
| | Buck Enabled Only, Not Sleeping | $V_{BUCKFB}$ = 0V, $I_{SW}$ = 0mA | | | 310 | 500 | µA |
| | Buck Enabled Only, Sleeping | $V_{BUCKFB}$ = 1V, $I_{SW}$ = 0mA | | | 50 | 75 | µA |
| | One LDO Enabled Only | $V_{LVIN}$ = 1.5V, 10µA LDO Output Load | | | 75 | 100 | µA |
| | All Three Outputs Enabled, Buck Not Sleeping | $V_{BUCKFB}$ = 0V, $I_{SW}$ = 0mA, $V_{LVIN}$ = 1.5V, 10µA Output Load on Each LDO | | | 400 | 600 | µA |
| | All Three Outputs Enabled, Buck Sleeping | $V_{BUCKFB}$ = 1V, $I_{SW}$ = 0mA, $V_{LVIN}$ = 1.5V, 10µA Load on Each LDO | | | 140 | 210 | µA |
| | Shutdown | $V_{ENBUCK}$ = 0V, $V_{ENLDO1}$ = 0V, $V_{ENLDO2}$ = 0V | | | | 1 | µA |



Downloaded from Arrow.com.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 3.6V unless otherwise specified. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{PG(THRESH)}$ | PGOOD Threshold (Note 8) | | ● | | 8 | 10 | % |
| $R_{PGOOD}$ | PGOOD Output Resistance | PGOOD Low, Sinking 1mA | ● | | 87 | 180 | Ω |
| $I_{PGOOD}$ | PGOOD Hi-Z Leakage Current | $V_{PGOOD}$ = 6V | ● | | | 1 | µA |
| **Synchronous Buck Converter** | | | | | | | |
| $I_{BUCKFB}$ | Feedback Current | (Note 5) | ● | | | ±30 | nA |
| $V_{BUCKFB}$ | Regulated Feedback Voltage | (Note 5) | ● | 0.788 | 0.800 | 0.812 | V |
| $\Delta V_{BUCKFB}$ | Feedback Voltage Line Regulation | $V_{IN}$ = 2.7V to 5.5V (Note 5) | ● | | 0.3 | 0.5 | mV/V |
| $I_{MAXP}$ | Maximum Peak Inductor Current | $V_{BUCKFB}$ = 0V, Duty Cycle < 35% | | 1.2 | 1.55 | 2.0 | A |
| $I_{MAXN}$ | NMOS Overcurrent Limit | | | | 1.8 | | A |
| | Feedback Voltage Load Regulation (with Respect to $V_{ITH}$) | $V_{ITH}$ = 0.5V to 1V, $V_{MODESEL}$ = $V_{IN}$ (Note 5) | | | 0.5 | | mV/V |
| $f_{OSC}$ | Oscillator Frequency | | ● | 1.8 | 2.25 | 2.7 | MHz |
| $R_{PFET}$ | $R_{DS(ON)}$ of P-Channel FET | $I_{SW}$ = 500mA | | | 0.13 | | Ω |
| $R_{NFET}$ | $R_{DS(ON)}$ of N-Channel FET | $I_{SW}$ = –500mA | | | 0.14 | | Ω |
| $I_{LSW}$ | SW Leakage | $V_{ENBUCK}$ = 0V, $V_{SW}$ = 0V or 5.5V, $V_{IN}$ = 5.5V | | | | ±1 | µA |
| $V_{ENBUCK}$ | Buck Enable Pin Threshold | | ● | 0.3 | 0.65 | 1 | V |
| $I_{ENBUCK}$ | Buck Enable Pin Leakage Current | $V_{ENBUCK}$ = 5.5V, All Other Pins Grounded | ● | | | 1 | µA |
| $V_{MODESEL}$ | Mode Select Pin Threshold | | ● | 0.3 | 0.65 | 1 | V |
| $I_{MODESEL}$ | Mode Select Pin Leakage Current | $V_{MODESEL}$ = 5.5V, All Other Pins Grounded | ● | | | 1 | µA |
| $g_m$ | Error Amplifier Transconductance | $V_{ITH}$ = 0.6V | | 450 | 700 | 950 | µA/V |
| **Each VLDO: $V_{IN}$ = 3.6V, $V_{LVIN}$ = 1.5V, $V_{LVOUT}$ = 1.2V, Unless Otherwise Specified** | | | | | | | |
| $V_{LVIN}$ | $LV_{IN}$ Pin Operating Voltage | (Note 6) | ● | 0.9 | | 5.5 | V |
| $I_{LVIN}$ | $LV_{IN}$ Pin Operating Current | $I_{OUT}$ = 10µA | ● | | 3 | 20 | µA |
| | $LV_{IN}$ Shutdown Current | $V_{ENLDO}$ = 0V | | | 1.5 | 2 | µA |
| $V_{LVFB}$ | Feedback Pin Regulation Voltage (Note 7) | 1mA ≤ $I_{OUT}$ ≤ 300mA, 1.5V ≤ $V_{LVIN}$ ≤ 5.5V | <br>● | 0.395<br>0.392 | 0.400<br>0.400 | 0.405<br>0.408 | V<br>V |
| $I_{LVFB}$ | Feedback Pin Input Current | $V_{LVFB}$ at Regulation | ● | | 2 | ±10 | nA |
| $I_{LVOUT(MAX)}$ | Continuous Output Current | | ● | 300 | | | mA |
| | Short-Circuit Output Current | | | | 760 | | mA |
| $V_{ENLDOx}$ | LDO Enable Pin Threshold | | ● | 0.3 | 0.65 | 1 | V |
| $I_{ENLDOx}$ | LDO Enable Pin Leakage Current | $V_{ENLDOx}$ = 5.5V, All Other Pins Grounded | ● | | | 1 | µA |
| | Output Voltage Load Regulation (Referred to the $LV_{FB}$ Pin) | $\Delta I_{OUT}$ = 1mA to 300mA | | | –1 | | mV/A |
| | $L_{VFB}$ Line Regulation (with Respect to the $L_{VIN}$ Pin) | $V_{LVIN}$ = 1.5V to 5.5V, $V_{IN}$ = 3.6V, $V_{LVOUT}$ = 1.2V, $I_{OUT}$ = 1mA | | | 7.5 | | µV/V |
| | $L_{VFB}$ Line Regulation (with Respect to the $V_{IN}$ Pin) | $V_{LVIN}$ = 1.5V, $V_{IN}$ = 2.7V to 5.5V, $V_{LVOUT}$ = 1.2V, $I_{OUT}$ = 1mA | | | 0.44 | | mV/V |
| $V_{DO}$ | $LV_{IN}$ – $LV_{OUT}$ Dropout Voltage | $V_{IN}$ = 2.8V, $V_{LVIN}$ = 1.5V, $V_{LVFB}$ = 0.37V, $I_{OUT}$ = 300mA (Note 9) | | | 68 | 175 | mV |
| | $V_{IN}$ to $LV_{OUT}$ Headroom Required for Regulation (Note 3) | $I_{LVOUT}$ = 300mA | ● | | | 1.4 | V |



Downloaded from Arrow.com.

## ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3446 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3446E is guaranteed to meet performance specifications from 0°C to 85°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design characterization and correlation with statistical process controls. The LTC3446I is guaranteed to meet performance specifications over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature ($T_J$, in °C) is calculated from the ambient temperature ($T_A$, in °C) and power dissipation ($P_D$, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where $\theta_{JA}$ (in °C/W) is the package thermal impedance.

**Note 3:** Minimum operating $V_{IN}$ voltage required for the VLDO regulators to stay in regulation is:

$V_{IN} \geq LV_{OUT(MAX)} + 1.4V$ and $V_{IN} \geq 2.7V$

**Note 4:** Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

**Note 5:** The LTC3446 is tested in a feedback loop that connects the BUCKFB pin to the output of the buck converter's error amplifier (i.e., the $I_{TH}$ pin).

**Note 6:** Minimum operating $LV_{IN}$ voltage required for the VLDO regulators to stay in regulation is:

$LV_{IN} \geq L_{VOUT(MAX)} + 100mV$ and $LV_{IN} \geq 0.9V$

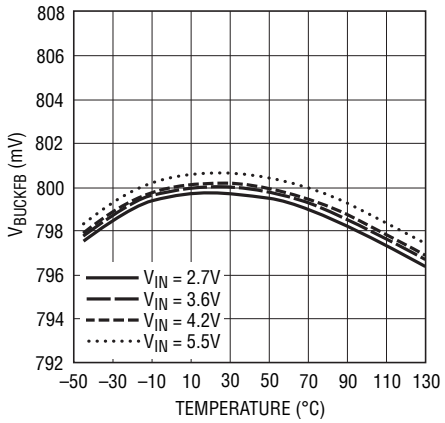
**Note 7:** Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.

**Note 8:** PGOOD assertion indicates that the feedback voltages of all enabled supplies are within the specified percentage of their target values.

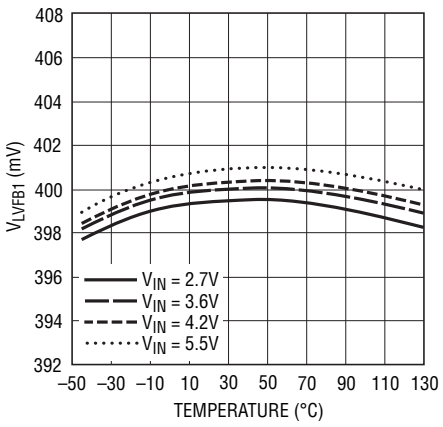
**Note 9:** Dropout voltage in the DFN package is assured by design, characterization and statistical process control.

## TYPICAL PERFORMANCE CHARACTERISTICS

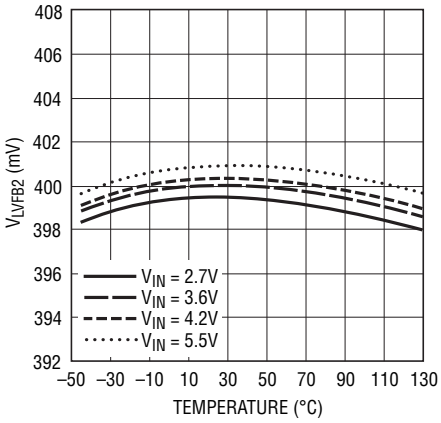
**Buck Regulated Feedback Voltage vs Temperature**




**LDO1 Regulated Feedback Voltage vs Temperature**




**LDO2 Regulated Feedback Voltage vs Temperature**

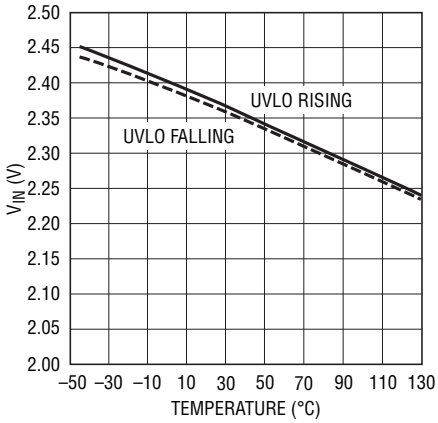




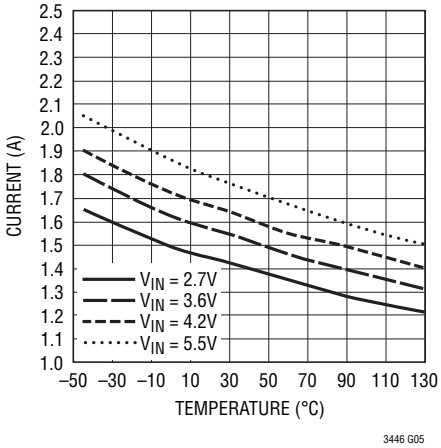

Downloaded from Arrow.com.

# TYPICAL PERFORMANCE CHARACTERISTICS

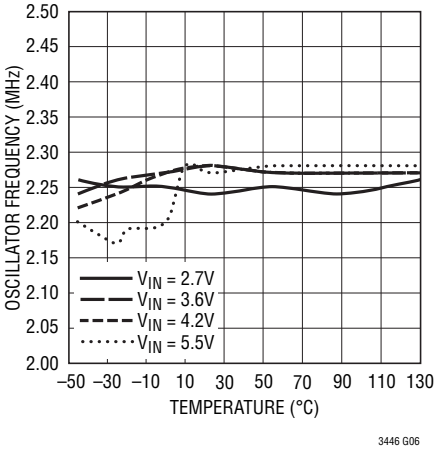
### Undervoltage Lockout Threshold vs Temperature



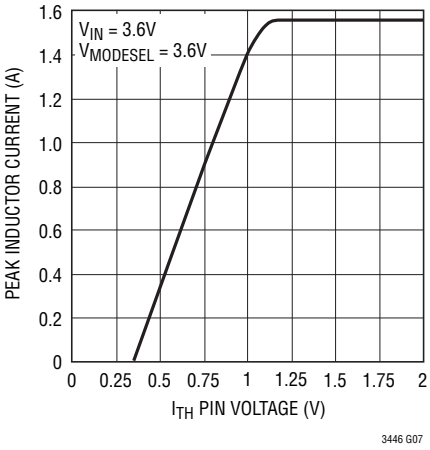

### Maximum Peak Inductor Current



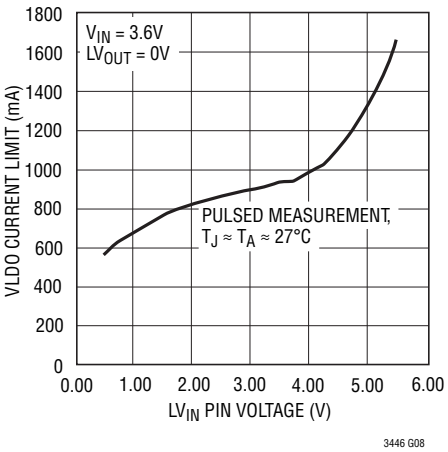

### Oscillator Frequency vs Temperature



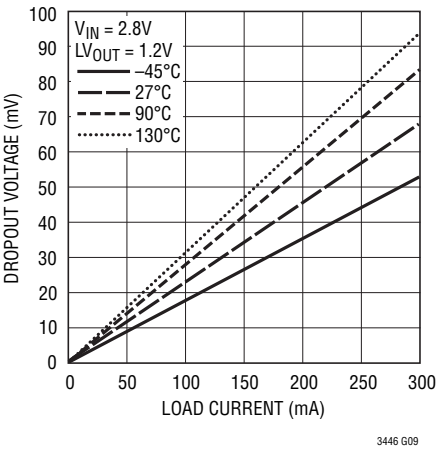

### Peak Inductor Current vs $I_{TH}$ Voltage



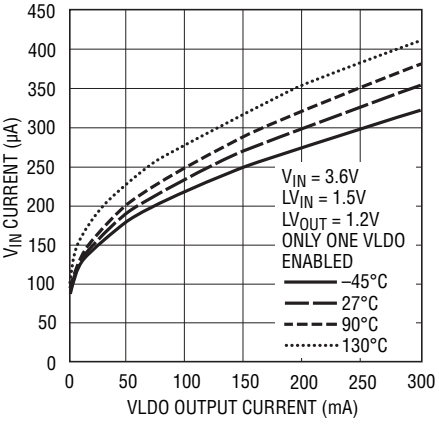

### VLDO Current Limit vs $LV_{IN}$ Voltage



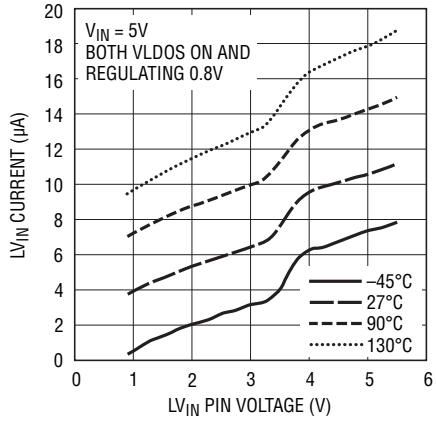

### VLDO Dropout Voltage vs Load Current



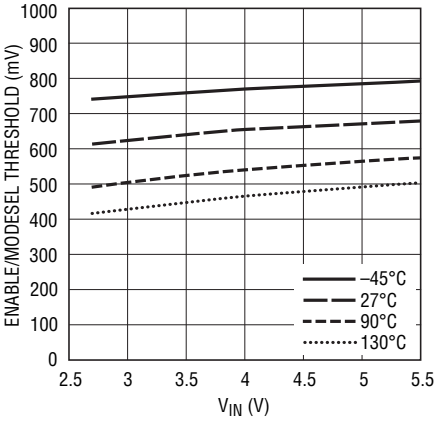

### $V_{IN}$ Bias Current vs VLDO Load Current




### $LV_{IN}$ No-Load Operating Current




### Enable/MODESEL Thresholds

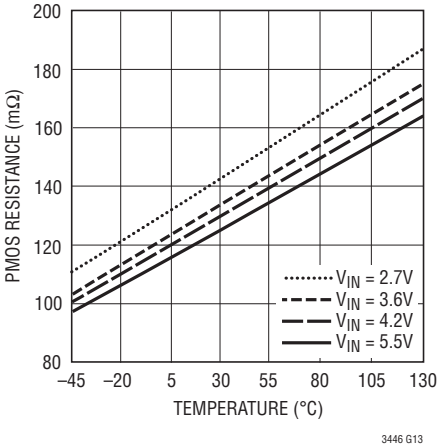




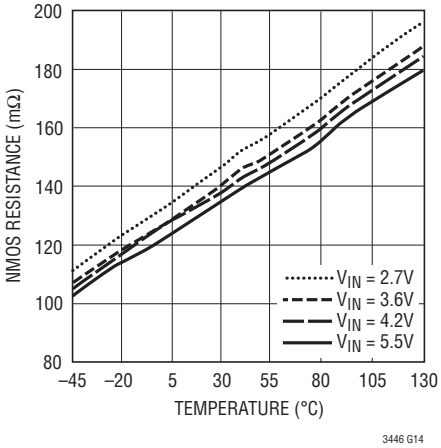

Downloaded from Arrow.com.

## TYPICAL PERFORMANCE CHARACTERISTICS

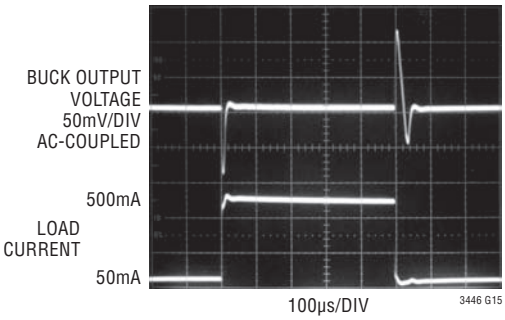
### Buck PMOS Switch On-Resistance




### Buck NMOS Switch On-Resistance

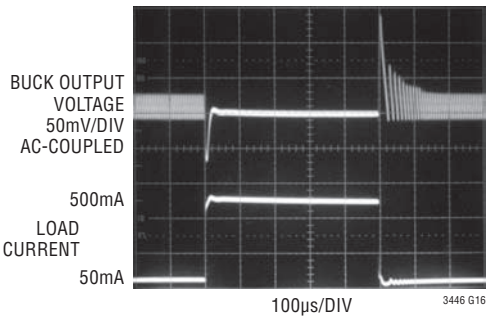



### Buck Transient Response with Burst Mode Defeated



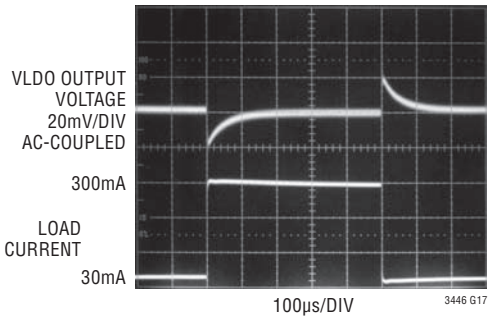

FRONT PAGE APPLICATION CIRCUIT

### Buck Transient Response with Burst Mode Enabled



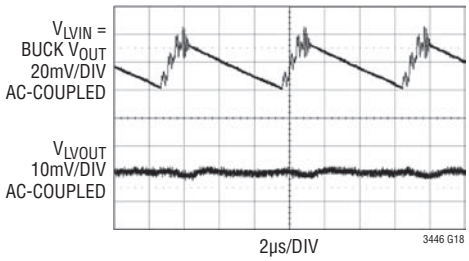

FRONT PAGE APPLICATION CIRCUIT

### VLDO Transient Response




$LV_{OUT}$ = 1.5V OR 1.2V
FRONT PAGE APPLICATION CIRCUIT

### VLDO Rejection of Buck DC/DC Burst Mode Ripple




$V_{LVIN}$ = BUCK $V_{OUT}$ = 1.8V
$V_{IN}$ = 4.2V
$V_{LVOUT}$ = 1.5V
$I_{LVOUT}$ = 50mA
$C_{LVOUT}$ = 2.2µF



Downloaded from Arrow.com.

## PIN FUNCTIONS

**MODESEL (Pin 1):** Chooses Between Burst Mode Operation and Pulse-Skipping Operation at Light Loads. Forcing this pin below 0.3V allows the buck converter to automatically enter Burst Mode operation at light loads. Forcing this pin above 1V disallows entering Burst Mode operation; the buck converter will cycle skip at light loads. Do not leave this pin floating. This is a MOS gate input.

**$V_{IN}$ (Pin 2):** Input Supply to the LTC3446. Must be closely decoupled to GND with a 10µF or greater ceramic capacitor.

**$I_{TH}$ (Pin 3):** Buck Error Amplifier Output and Servo-Loop Compensation Point.

**PGOOD (Pin 4):** Supply Monitor Output, Open-Drain NMOS.

**$LV_{OUT1}$ (Pin 5):** Output of the First VLDO Regulator.

**$LV_{IN}$ (Pin 6):** Input Supply to the LTC3446's VLDO Circuits. Bypass $LV_{IN}$ to GND with at least a 1µF low ESR ceramic capacitor. Typical LTC3446 application circuits will connect this pin to the output of the buck converter but this is not required. The VLDO regulators may be used independently of the buck converter.

**$LV_{OUT2}$ (Pin 7):** Output of the Second VLDO Regulator.

**$LV_{FB2}$ (Pin 9):** Feedback Pin for the Second VLDO Regulator. An output divider should be connected from $LV_{OUT2}$ to $LV_{FB2}$ to set the desired $LV_{OUT2}$ regulated output voltage.

**$LV_{FB1}$ (Pin 10):** Feedback Pin for the First VLDO Regulator. An output divider should be connected from $LV_{OUT1}$ to $LV_{FB1}$ to set the desired $LV_{OUT1}$ regulated output voltage.

**ENLDO1/ENLDO2 (Pin 11/Pin 8):** Enable Pin for the First and Second VLDO Regulators, Respectively. Forcing this pin above 1V enables the corresponding VLDO regulator and forcing this pin below 0.3V shuts it down. Each VLDO regulator draws <1µA of supply current in shutdown. Do not leave this pin floating. This is a MOS gate input.

**BUCKFB (Pin 12):** Buck Converter's Feedback Pin. Receives the feedback voltage from an external resistive divider across the output. External resistance from this pin to ground should be equal to or less than 50k.

**ENBUCK (Pin 13):** Enable Pin for the LTC3446's Buck Converter Circuit. Forcing this pin above 1V enables the buck converter and forcing this pin below 0.3V shuts down the converter. In shutdown, the buck converter draws <1µA of supply current. Do not leave this pin floating. This is a MOS gate input.

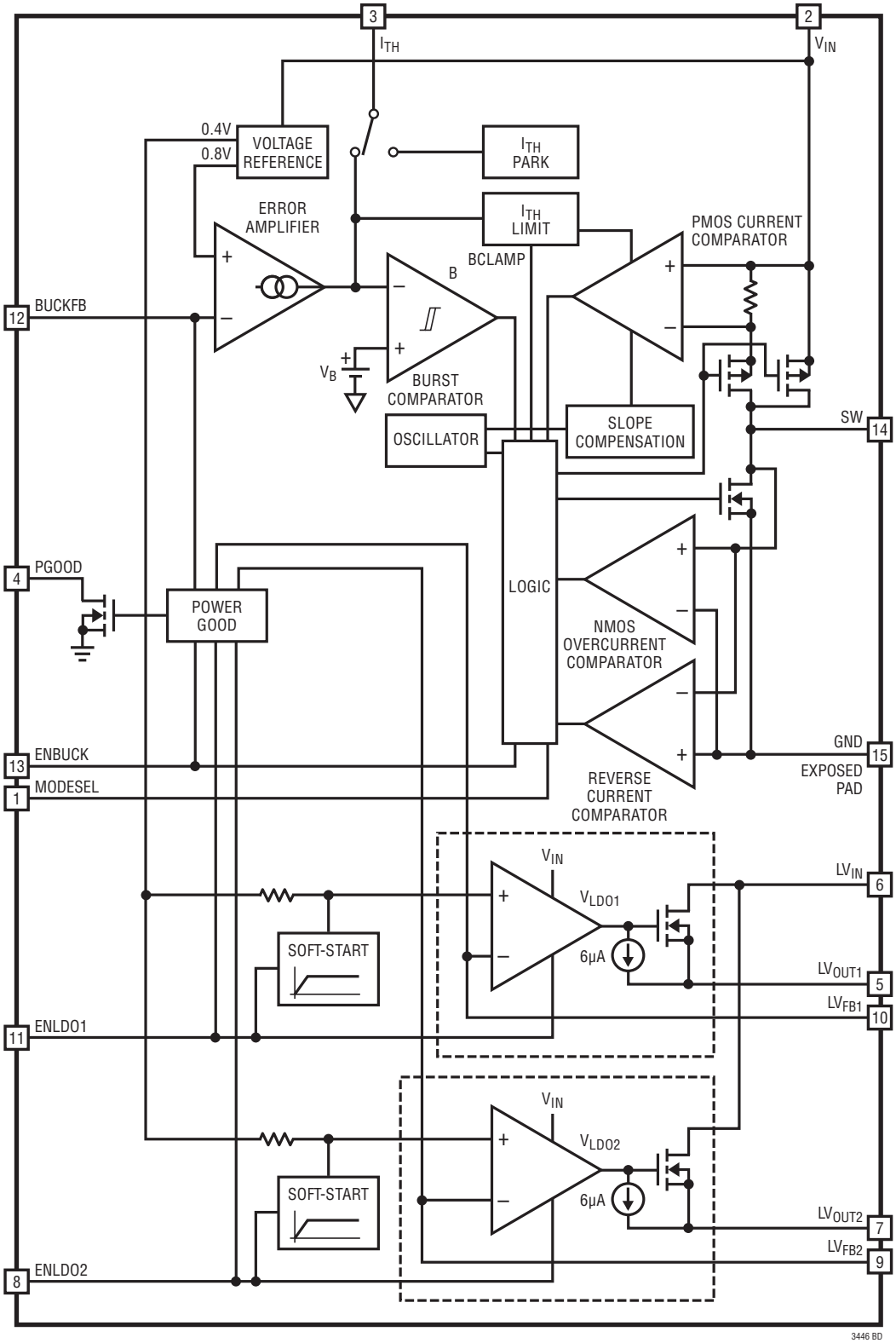
**SW (Pin 14):** Switch Node Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

**GND (Exposed Pad, Pin 15):** Ground. The Exposed Pad is the only ground and must connect to the PCB ground for electrical contact and rated thermal performance.



Downloaded from Arrow.com.

## BLOCK DIAGRAM






Downloaded from Arrow.com.

## OPERATION

The LTC3446 combines a constant frequency, current mode synchronous buck converter with two very low dropout (VLDO) linear DC regulators to provide up to three high efficiency, low voltage outputs from a single higher voltage input source. Each output can be independently enabled and disabled. A power good circuit monitors all three supplies. The LTC3446 incorporates an undervoltage lockout circuit that shuts down the IC when the input voltage drops below about 2.4V to prevent unstable operation.

### SYNCHRONOUS BUCK OPERATION

A buck converter takes power from a high input voltage, $V_{IN}$, and delivers it at a lower output voltage, $V_{OUT}$. The buck converter inside the LTC3446 achieves over 80% efficient power conversion under a wide range of $V_{IN}$, $V_{OUT}$ and load conditions, whereas a linear regulator is limited by physics to a maximum efficiency of $(V_{OUT}/V_{IN}) \times 100\%$.

#### Main Control Loop

During normal operation, the internal oscillator produces a constant frequency 2.25MHz clock. The top power switch (P-channel MOSFET) turns on at the beginning of a clock cycle. Inductor current increases to a peak value which is set by the voltage on the $I_{TH}$ pin. Then the top switch turns off and the energy stored in the inductor flows through the bottom switch (N-channel MOSFET) into the load until the next clock cycle.

The peak inductor current is controlled by the voltage on the $I_{TH}$ pin, which is the output of the error amplifier. This amplifier compares the BUCKFB pin to the 0.8V reference. When the load current increases, the BUCKFB voltage decreases slightly below the reference. This decrease causes the error amplifier to increase the $I_{TH}$ voltage until the average inductor current matches the new load current.

The main control loop is shut down by pulling the ENBUCK pin to ground.

#### Overcurrent Protection

To help avert inductor current runaway in case the buck output is accidentally shorted to ground, the LTC3446 features a bottom switch NMOS overcurrent limit, which works as follows.

When the buck output is shorted to ground, inductor current will rise to its maximum peak level, $I_{MAXP}$, such that on every oscillator cycle the PMOS top switch will turn on for only its minimum duty cycle, and the bottom switch NMOS turns on for the remainder of the cycle. Temporarily ignoring inductor, switch and parasitic resistance drops, which in most applications are designed to be small in order to maximize buck converter efficiency, it is to first order true that when the PMOS is on, the $V_{IN}$ supply voltage is placed across the inductor, increasing the inductor current, but when the NMOS is on, there is no output voltage to be placed across the inductor to reduce its current. Inductor current ratchets up each cycle and could lead to the destruction of the buck IC.

The NMOS overcurrent limit helps prevent this by sensing the current through the NMOS bottom switch, and for as long as this current exceeds the overcurrent limit level, $I_{MAXN}$, it:

1. Keeps the NMOS on, allowing the tiny voltage drops from parasitic resistances to reduce the inductor current.
2. Refuses to allow the PMOS to turn on, preventing any additional energy from being fed into the system.

#### Low Current Operation

The MODESEL pin controls the buck converter's behavior at light load currents to help optimize efficiency, output ripple and noise. When the load is relatively light and MODESEL is grounded, the buck converter automatically switches into Burst Mode operation, which operates the PMOS



Downloaded from Arrow.com.

## OPERATION

switch intermittently based on load demand rather than at a constant frequency. Every switch cycle during Burst Mode operation delivers more energy than would occur in constant frequency operation, minimizing the switching loss per unit of energy delivered. Since the dominant power loss at light loads is gate charge switching loss in the power MOSFETs, operating in Burst Mode operation can dramatically improve light load efficiency. The tradeoff is higher output ripple than in constant frequency operation, as well as the presence of noise below the 2.25MHz clock frequency.

If MODESEL were instead tied to $V_{IN}$, pulse skipping mode is selected. In this mode, the buck converter continues to switch at a constant frequency down to very light loads where it will eventually begin skipping pulses. Because constant frequency operation is extended down to light loads, low output ripple is maintained and any coupled or radiated noise is at or higher than the clock frequency. The tradeoff is lower efficiency compared to Burst Mode operation.

### Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases to 100%, which is known as the dropout condition. In dropout, the PMOS switch is turned on continuously with the output voltage equal to the input voltage minus any voltage drop across the PMOS switch and the external inductor.

### VLDO LINEAR REGULATOR OPERATION

The two micropower, VLDO (very low dropout) linear regulators in the LTC3446 operate from input voltages as low as 0.9V. Each VLDO regulator provides a high accuracy output that is capable of supplying 300mA of output current with a typical dropout voltage of only 70mV. A single ceramic capacitor as small as 1µF is all that is required for output bypassing. A low reference voltage of 400mV allows the VLDO regulators to be programmed to much lower voltages than available in common LDOs.

As shown in the Block Diagram, the $V_{IN}$ input supplies the internal reference and biases the VLDO circuitry while all output current comes directly from the $LV_{IN}$ input for high efficiency regulation. The low per-VLDO quiescent supply currents $I_{LVIN}$ = 4µA, $I_{VIN}$ = 80µA drop to $I_{LVIN}$ < 2µA, $I_{VIN}$ < 1µA in shutdown, are well-suited to battery-powered systems.

Each VLDO includes current limit protection. The fast transient response of the follower output stage overcomes the traditional tradeoff between dropout voltage, quiescent current and load transient response inherent in most LDO regulator architectures. Overshoot detection circuitry is included to bring the output back into regulation when going from heavy to light output loads (“load-dump” handling).

### POWER GOOD CIRCUIT OPERATION

The LTC3446 has a built-in supply monitor. The feedback voltage of each enabled supply is monitored by a window comparator to determine whether it is within 8% of its target value. If they all are, then the PGOOD pin becomes high impedance. If no supply is enabled, or if any enabled supply is more than 8% away from its target, then the PGOOD pin is driven to ground by an internal open-drain NMOS.

The PGOOD pin may be connected through a pull-up resistor to a supply voltage of up to 5.5V, independent of the $V_{IN}$ pin voltage.



Downloaded from Arrow.com.

## APPLICATIONS INFORMATION

A general LTC3446 application circuit is shown in Figure 1. External component selection is driven by output voltage and load requirements. The following text is divided into two sections: the first covers Buck regulator design and the second covers use of the linear VLDO regulators.

### BUCK REGULATOR DESIGN

Buck regulator design begins with the selection of the L1 inductor based on desired ripple current. Once L1 is chosen, $C_{IN}$ and $C_{OUTB}$ can be selected based on output voltage ripple requirements. Output voltage is programmed through R1 and R2, and loop response can be optimized by choice of $R_{ITH}$ and $C_{ITH}$.

#### Inductor Selection

Although the inductor does not influence the operating frequency, the inductor value has a direct effect on ripple current. The inductor ripple current $\Delta I_L$ decreases with higher inductance and increases with higher $V_{IN}$ or $V_{OUTB}$:

$$\Delta I_L = \frac{V_{OUTB}}{f_O \bullet L} \bullet \left(1 - \frac{V_{OUTB}}{V_{IN}}\right)$$

Accepting larger values of $\Delta I_L$ allows the use of low inductances, but results in higher output voltage ripple, greater core losses, and lower output current capability.

A reasonable starting point for setting ripple current is $\Delta I_L = 0.3 \bullet I_{MAXP}$, where $I_{MAXP}$ is the peak switch current limit. The largest ripple current $\Delta I_L$ occurs at the maximum input voltage. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \frac{V_{OUTB}}{f_O \bullet \Delta I_L} \bullet \left(1 - \frac{V_{OUTB}}{V_{IN(MAX)}}\right)$$

The inductor value will also have an effect on Burst Mode operation. The transition from low current operation begins when the peak inductor current falls below a level set by the burst clamp. Lower inductor values result in higher ripple current which causes this to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

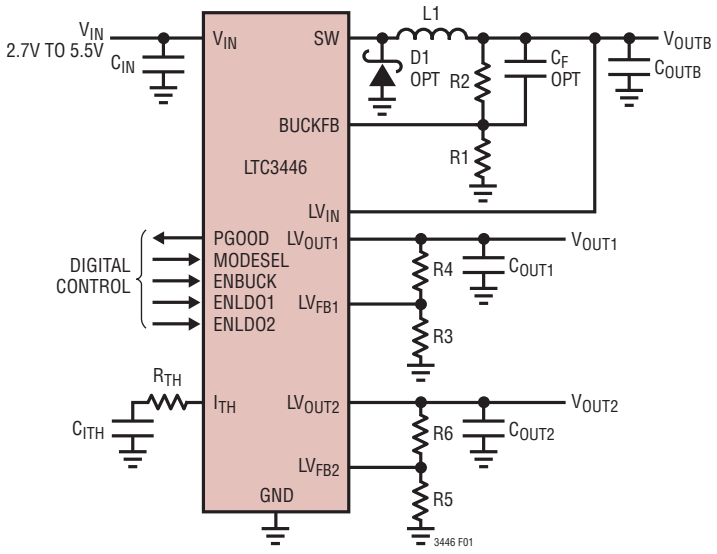



**Figure 1. General LTC3446 Application Circuit**



Downloaded from Arrow.com.

## APPLICATIONS INFORMATION

### Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements and any radiated field/EMI requirements than on what the LTC3446 requires to operate. Table 1 shows some typical surface mount inductors that work well in LTC3446 applications.

**Table 1. Representative Surface Mount Inductors**

| MANUFACTURER | PART NUMBER | VALUE | MAX DC CURRENT | DCR | HEIGHT |
|---|---|---|---|---|---|
| Toko | A914BYW-2R2M-D52LC | 2.2µH | 2.05A | 49mΩ | 2mm |
| Toko | A915AY-2ROM-D53LC | 2µH | 3.3A | 22mΩ | 3mm |
| Coilcraft | D01608C-222 | 2.2µH | 2.3A | 70mΩ | 3mm |
| Coilcraft | LP01704-222M | 2.2µH | 2.4A | 120mΩ | 1mm |
| Sumida | CDRH4D282R2 | 2.2µH | 2.04A | 23mΩ | 3mm |
| Sumida | CDC5D232R2 | 2.2µH | 2.16A | 30mΩ | 2.5mm |
| Taiyo Yuden | N06DB2R2M | 2.2µH | 3.2A | 29mΩ | 3.2mm |
| Taiyo Yuden | N05DB2R2M | 2.2µH | 2.9A | 32mΩ | 2.8mm |
| Murata | LQN6C2R2M04 | 2.2µH | 3.2A | 24mΩ | 5mm |
| Würth | 744042001 | 1µH | 2.6A | 20mΩ | 2mm |

### Catch Diode Selection

Although unnecessary in most applications, a small improvement in efficiency can be obtained in a few applications by including the optional diode D1 shown in Figure 1, which conducts when the synchronous switch is off. When using Burst Mode operation or pulse skip mode, the synchronous switch is turned off at a low current and the remaining current will be carried by the optional diode. It is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode ratings. The main problem with Schottky diodes is that their parasitic capacitance reduces the efficiency, usually negating the possible benefits for LTC3446 circuits. Another problem that a Schottky diode can introduce is higher leakage current at high temperatures, which could reduce the low current efficiency.

Remember to keep lead lengths short and observe proper grounding to avoid ringing and increased dissipation when using a catch diode.

### Input Capacitor ($C_{IN}$) Selection

In continuous mode, the input current of the converter is a square wave with a duty cycle of approximately $V_{OUTB}/V_{IN}$. To prevent large voltage transients, a low equivalent series resistance (ESR) input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{MAX} \frac{\sqrt{V_{OUTB}(V_{IN} - V_{OUTB})}}{V_{IN}}$$

where the maximum average output current $I_{MAX}$ equals the peak current minus half the peak-to-peak ripple current, $I_{MAX} = I_{MAXP} - \Delta I_L/2$.

This formula has a maximum at $V_{IN} = 2V_{OUTB}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case is commonly used to design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours lifetime. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. An additional 0.1µF to 1µF ceramic capacitor is also recommended on $V_{IN}$ for high frequency decoupling, when not using an all ceramic capacitor solution.



Downloaded from Arrow.com.

## APPLICATIONS INFORMATION

### Output Capacitor ($C_{OUTB}$) Selection

The selection of $C_{OUTB}$ is driven by the required ESR to minimize voltage ripple and load step transients. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple ($\Delta V_{OUTB}$) is determined by:

$$\Delta V_{OUTB} \approx \Delta I_L \left( ESR + \frac{1}{8 f_O C_{OUTB}} \right)$$

where f = 2.25MHz, $C_{OUTB}$ = output capacitance and $\Delta I_L$ = ripple current in the inductor. The output ripple is highest at maximum input voltage since $\Delta I_L$ increases with input voltage.

Once the ESR requirements for $C_{OUTB}$ have been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement, except for an all ceramic solution.

In surface mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirement of the application. Aluminum electrolytic, special polymer, ceramic and dry tantulum capacitors are all available in surface mount packages. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR(size) product of any aluminum electrolytic at a somewhat higher price. Special polymer capacitors, such as Sanyo POSCAP, offer very low ESR, but have a lower capacitance density than other types. Tantalum capacitors have the highest capacitance density, but have a larger ESR and it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, avalable in case heights ranging from 2mm to 4mm. Aluminum electrolytic capacitors have a significantly larger ESR, and are often used in extremely cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have the lowest ESR and cost but also have the lowest capacitance density, a high voltage and temperature coefficient and exhibit audible piezoelectric effects. In addition, the high Q of ceramic capacitors along with trace inductance can lead to significant ringing. Other capacitor types include the Panasonic specialty polymer (SP) capacitors.

In most cases, 0.1µF to 1µF of ceramic capacitors should also be placed close to the LTC3446 in parallel with the main capacitors for high frequency decoupling.

### Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. These are tempting for switching regulator use because of their very low ESR. Unfortunately, the ESR is so low that it can cause loop stability problems. Solid tantalum capacitor ESR generates a loop "zero" at 5kHz to 50kHz that is instrumental in giving acceptable loop phase margin. Ceramic capacitors remain capacitive to beyond 300kHz and usually resonate with their ESL before ESR becomes effective. Also, ceramic caps are prone to temperature effects which requires the designer to check loop stability over the operating temperature range. To minimize their large temperature and voltage coefficients, only X5R or X7R ceramic capacitors should be used. A good selection of ceramic capacitors is available from Taiyo Yuden, TDK and Murata.

Great care must be taken when using only ceramic input and output capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the $V_{IN}$ pin. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, the ringing at the input can be large enough to damage the part.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough



Downloaded from Arrow.com.

## APPLICATIONS INFORMATION

to support the load. The time required for the feedback loop to respond is dependent on the compensation components and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, $V_{DROOP}$, is usually about 2 to 3 times the linear drop of the first cycle. Thus, a good place to start is with the output capacitor size of approximately:

$$C_{OUTB} \approx 2.5 \frac{\Delta I_{OUT}}{f_0 \bullet V_{DROOP}}$$

More capacitance may be required depending on the duty cycle and load step requirements.

In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 10µF ceramic capacitor is usually enough for these conditions.

### Setting the Buck Converter's Output Voltage

The buck develops a 0.8V reference voltage between the feedback pin, BUCKFB, and the signal ground as shown in Figure 1. The output voltage is set by a resistive divider according to the following formula:

$$V_{OUTB} \approx 0.8V \left(1 + \frac{R2}{R1}\right)$$

Keep R1 at or less than 50k. Great care should be taken to route the BUCKFB line away from noise sources, such as the inductor or the SW line.

To improve high frequency loop response, a feed forward capacitor, $C_F$, can be added as shown in Figure 1. Capacitor $C_F$ provides phase lead by creating a high frequency zero with R2, improving phase margin.

### Buck Converter Shutdown

The ENBUCK pin enables and shuts down the LTC3446's buck converter. **Do not leave this pin floating!** Tying ENBUCK to ground disables the buck converter. Bringing ENBUCK more than 1V above ground enables the buck.

### Checking Buck Converter Transient Response

The OPTI-LOOP compensation allows the transient response to be optimized for a wide range of loads and output capacitors. The availability of the $I_{TH}$ pin not only allows optimization of the control loop behavior but also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin.

The $I_{TH}$ external components shown in the front page Typical Application circuit will provide an adequate starting point for most applications. The series R-C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and $I_{TH}$ pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, $V_{OUTB}$ immediately shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of $C_{OUT}$. $\Delta I_{LOAD}$ also begins to charge or discharge $C_{OUTB}$ generating a feedback error signal used by the regulator to return $V_{OUTB}$ to its steady-state value. During this recovery time, $V_{OUTB}$ can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop increases with R and the bandwidth of the loop increases with decreasing C.



Downloaded from Arrow.com.

## APPLICATIONS INFORMATION

If R is increased by the same factor that C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Linear Technology Application Note 76.

Although a buck regulator is capable of providing the full output current in dropout, it should be noted that as the input voltage $V_{IN}$ drops toward $V_{OUT}$, the load step capability does decrease due to the decreasing voltage across the inductor. Applications that require large load step capability near dropout should use a different topology such as SEPIC, Zeta or single inductor, positive buck/boost.

In some applications, a more severe transient can be caused by switching in loads with large (>1µF) input capacitors. The discharged input capacitors are effectively put in parallel with $C_{OUTB}$, causing a rapid drop in $V_{OUT}$. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-starting.

### Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3446 circuits: 1) LTC3446 $V_{IN}$ current, 2) switching losses, 3) $I^2R$ losses, 4) other losses.

1) The $V_{IN}$ current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents. $V_{IN}$ current results in a small (<0.1%) loss that increases with $V_{IN}$, even at no load.

2) The switching current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $V_{IN}$ to ground. The resulting dQ/dt is a current out of $V_{IN}$ that is typically much larger than the DC bias current. In continuous mode, $I_{GATECHG} = f_O(QT + QB)$, where QT and QB are the gate charges of the internal top and bottom MOSFET switches. The gate charge losses are proportional to $V_{IN}$ and thus their effects will be more pronounced at higher supply voltages.

3) $I^2R$ Losses are calculated from the DC resistances of the internal switches, $R_{SW}$, and external inductor, RL. In continuous mode, the average output current flowing through inductor L is "chopped" between the internal top and bottom switches. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$R_{SW} = (R_{DS(ON)}TOP)(DC) + (R_{DS(ON)}BOT)(1 – DC)$

4) Other "hidden" losses such as copper trace and internal battery resistances can account for additional efficiency degradations in portable systems. It is very important to include these "system" level losses in the design of a system. The internal battery and fuse resistance losses can be minimized by making sure that $C_{IN}$ has adequate charge storage and very low ESR at the switching frequency. Other losses including diode conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.



Downloaded from Arrow.com.

## APPLICATIONS INFORMATION

### VLDO LINEAR REGULATOR DESIGN

#### Adjustable Output Voltage

Each VLDO regulator's output voltage is set by the ratio of two external resistors as shown in Figure 2. The VLDO regulator servos the output to maintain the $LV_{FB}$ pin voltage at 0.4V (referenced to ground). Thus the current in R1 is equal to 0.4V/R1. For good transient response, stability and accuracy, the current in R1 should be at least 8µA, thus the value of R1 should be no greater than 50k. The current in R2 is the current in R1 plus the $LV_{FB}$ pin bias current. Since the $LV_{FB}$ pin bias current is typically <10nA, it can be ignored in the output voltage calculation. The output voltage can be calculated using the formula in Figure 2. Note that in shutdown, the output is turned off and the divider current will be zero once $C_{OUT}$ is discharged.

Each VLDO regulator operates at a relatively high gain of –0.7µV/mA referred to its $LV_{FB}$ input. Thus a load current change of 1mA to 300mA produces a –0.2mV drop at the $LV_{FB}$ input. To calculate the change referred to the output, simply multiply by the gain of the feedback network (i.e., 1 + R2/R1). For example, to program the output for 1.2V, choose R2/R1 = 2. In this example, an output current change of 1mA to 300mA produces –0.2mV • (1 + 2) = 0.6mV drop at the output.

Because the $LV_{FB}$ pins are relatively high impedance (depending on the resistor dividers used), stray capacitance at these pins should be minimized (<10pF) to prevent phase shift in the error amplifier loop. Additionally, special attention should be given to any stray capacitances that can couple external signals onto the $LV_{FB}$ pins producing undesirable output ripple. For optimum performance, connect each $LV_{FB}$ pin to its resistor divider with a short PCB trace and minimize all other stray capacitance to the $LV_{FB}$ pin.

#### VLDO Regulator Output Capacitance and Transient Response

The VLDO regulators are designed to be stable with a wide range of ceramic output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 1µF with an ESR of 0.05Ω or less is recommended to ensure stability. The VLDO regulators are micropower devices and output transient response will be a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Note that bypass capacitors used to decouple individual components powered by a VLDO regulator will increase the effective output capacitor value. High ESR tantalum and electrolytic capacitors may be used, but a low ESR ceramic capacitor must be in parallel at the output. There is no minimum ESR or maximum capacitor size requirements.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit large voltage and temperature coefficients as shown in Figures 3 and 4. When used with a 2V regulator, a 1µF Y5V capacitor can lose as much as 75% of its intial capacitance over the operating temperature range. The X5R and X7R dielectrics result

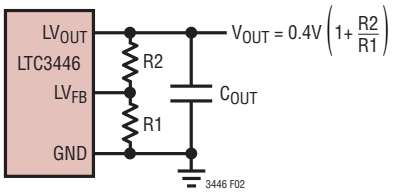



**Figure 2. Programming a VLDO Regulator's Output Voltage**



Downloaded from Arrow.com.

## APPLICATIONS INFORMATION

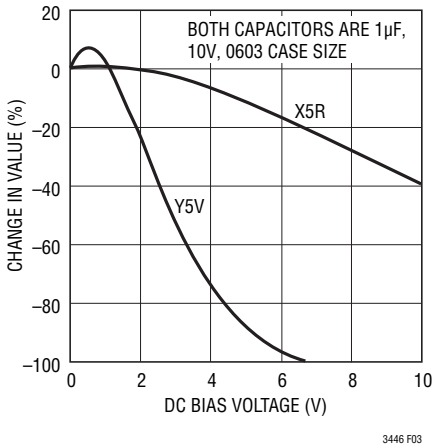



Figure 3. Ceramic Capacitor DC Bias Characteristics

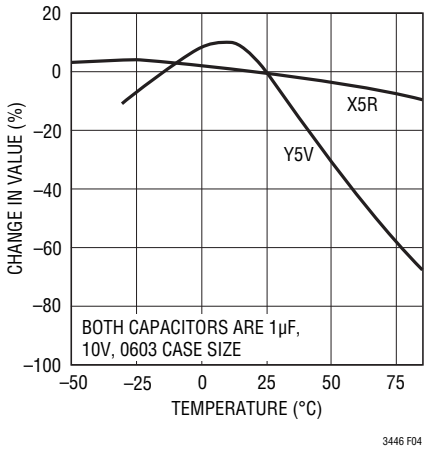



Figure 4. Ceramic Capacitor Temperature Characteristics

in more stable characteristics and are usually more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. In all cases, the output capacitance should never drop below 0.4µF, or instability or degraded performance may occur.

### VLDO Output Short-Circuit Protection

The VLDO regulators have built-in short-circuit limiting. During short-circuit conditions, internal circuitry automatically limits the output current to approximately 760mA.

### VLDO Regulator Soft-Start

Each VLDO regulator includes a soft-start feature to prevent excessive current flow during start-up. When the VLDO regulator is enabled, the soft-start circuitry gradually increases the VLDO regulator reference voltage from 0V to 0.4V over a period of about 600µs. There is a short 700µs delay from the time the part is enabled until the LDO output starts to rise. Figure 5 shows the start-up output waveform.

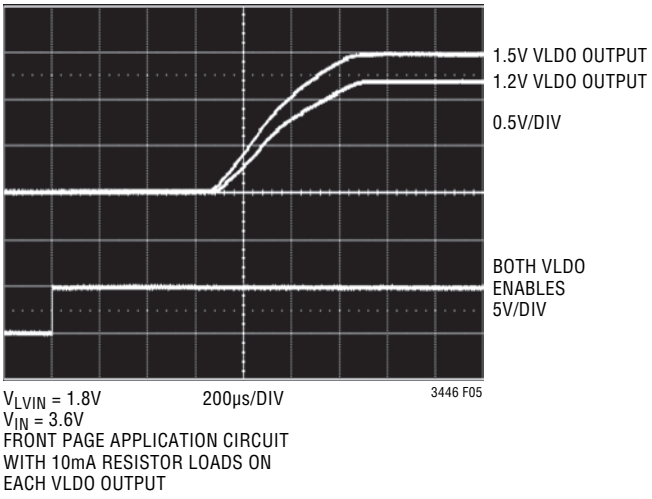


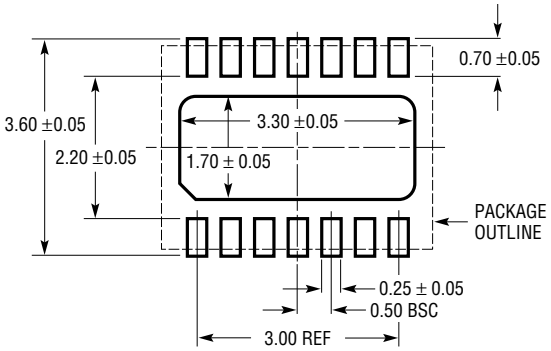

Figure 5. VLDO Regulator Output Start-Up



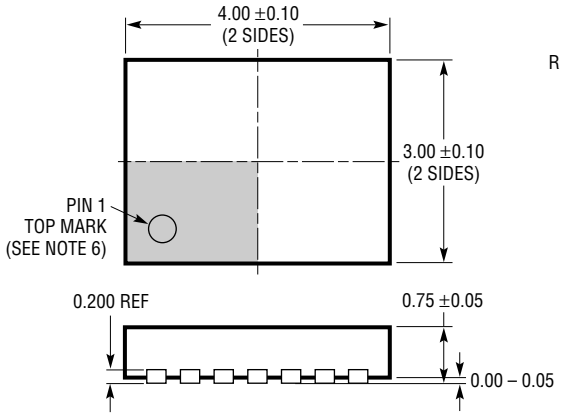
Downloaded from Arrow.com.

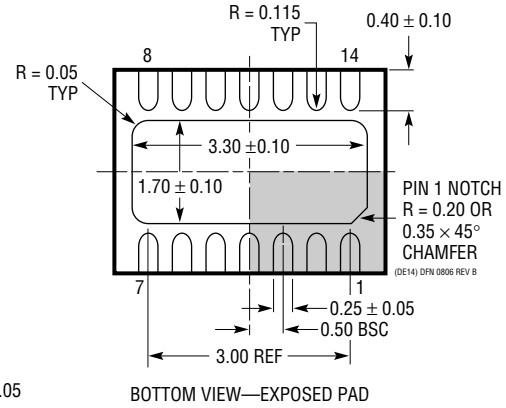
# PACKAGE DESCRIPTION

**DE Package**
**14-Lead Plastic DFN (4mm × 3mm)**
(Reference LTC DWG # 05-08-1708 Rev B)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED




BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



Downloaded from Arrow.com.

## REVISION HISTORY (Revision history begins at Rev E)

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| E | 5/11 | Updated E-grade Temperature Grade to 125°C, Storage Maximum Temperature to 150°C and $\theta_{JA}$ to 43°C/W. | 2 |
| | | Updated PGOOD Output Resistance Maximum Limit. | 3 |
| | | Added $V_{IN}$ to $LV_{OUT}$ Headroom Specification. | 3 |
| | | Updated Note 2. | 4 |
| F | 5/11 | Updated Parameter on $V_{IN}$ to $LV_{OUT}$ specification | 3 |

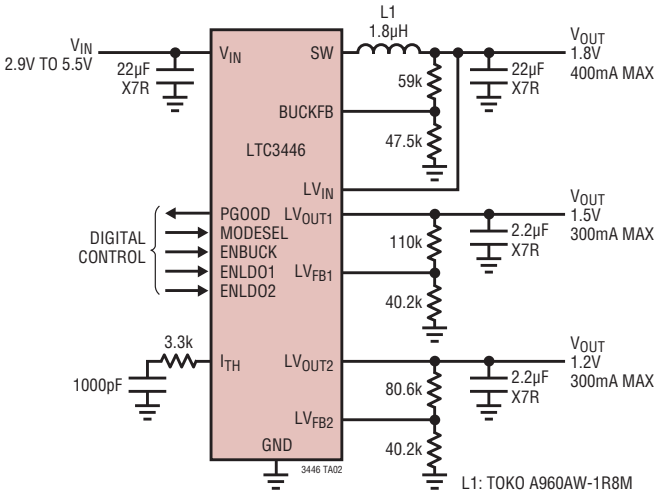


Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.



Downloaded from Arrow.com.

## TYPICAL APPLICATION




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LT3023 | Dual, 2x100mA, Low Noise Micropower LDO | $V_{IN}$: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, $V_{DO}$ = 0.30V, $I_Q$ = 40µA, $I_{SD}$ < 1µA, $V_{OUT}$ = ADJ, DFN, MS Packages, Low Noise < 20µ$V_{RMS(P-P)}$, Stable with 1µF Ceramic Capacitors |
| LT3024 | Dual, 100mA/500mA, Low Noise Micropower LDO | $V_{IN}$: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, $V_{DO}$ = 0.30V, $I_Q$ = 60µA, $I_{SD}$ < 1µA, $V_{OUT}$ = ADJ, DFN, TSSOP Packages, Low Noise < 20µ$V_{RMS(P-P)}$, Stable with 1µF Ceramic Capacitors |
| LTC3025 | 300mA, Micropower VLDO Linear Regulator | $V_{IN}$: 0.9V to 5.5V, $V_{OUT(MIN)}$ = 0.4V, 2.7V to 5.5V Bias Voltage Required, $V_{DO}$ = 45mV, $I_Q$ = 50µA, $I_{SD}$ < 1µA, $V_{OUT}$ = ADJ, DFN Packages, Stable with 1µF Ceramic Capacitors |
| LTC3407 | Dual Synchronous 600mA Synchronous Step-Down DC/DC Regulator | 1.5MHz Constant Frequency Current Mode Operation, $V_{IN}$ from 2.5V to 5.5V, $V_{OUT}$ Down to 0.6V, DFN, MS Packages |
| LTC3407-2 | Dual Synchronous 800mA Synchronous Step-Down DC/DC Regulator, 2.25MHz | 2.25MHz Constant Frequency Current Mode Operation, $V_{IN}$ from 2.5V to 5.5V, $V_{OUT}$ Down to 0.6V, DFN, MS Packages |
| LTC3445 | $I^2C$ Controllable Buck Regulator with Two LDOs and and Backup Battery Input | 600mA, 1.5MHz Current Mode Buck Regulator, $I^2C$ Programmable $V_{OUT}$ from 0.85V to 1.55V, two 50mA LDOs, Backup Battery Input with PowerPath™ Control, QFN Package |
| LTC3555 | High Efficiency USB Power Manager Plus Triple Step-Down DC/DC | Maximizes Available Power from USB Port, Bat-Track™, "Instant On" Operation, 1.5A Maximum Charge Current, 180mΩ Ideal Diode with <50Ω Option, 3.3V/25mA Always-On LDO, Three Synchronous Buck Regulators (400mA/400mA/1A), 4mm × 5mm QFN28 Package |
| LTC3557 | USB Power Manager with Li-Ion/Polymer Charger and Triple Synchrounous Buck Converter | Complete Multifunction ASSP: Linear Power Manager and Three Buck Regulators, Charge Current Programmable Up to 1.5A from Wall Adapter Input, Thermal Regulation, Synchronous Buck Efficiency: >95%, ADJ Outputs: 0.8V to 3.6V at 400mA/400mA/600mA, Bat-Track Adaptive Output Control, 200mΩ Ideal Diode, 4mm × 4mm QFN28 Package |
| LTC3559 | Linear USB Li-Ion Battery Charger with Dual Buck Regulators | Charge Current Programmable Up to 950mA, USB Compatible, Dual Synchronous 400mA Buck Regulators, Efficiency >90%, 3mm × 3mm QFN16 Package |
| LTC3672B-1/ LTC3672B-2 | Fixed-Output Monolithic 400mA Buck Regulator with Dual 150mA LDOs in a 2mm × 2mm DFN | >90% Efficiency, $V_{IN}$: 2.9V to 5.5V, $I_Q$ = 260µA, LTC3672B-1: Buck = 1.8V, LDO1 = 1.2V, LDO2 = 2.8V LTC3672B-2: Buck = 1.2V, LDO1 = 2.8V, LDO2 = 1.8V Consult LTC Factory for Other Voltage Combinations |
| LTC3700 | Step-Down DC/DC Controller with LDO Regulator | $V_{IN}$ from 2.65V to 9.8V, Constant Frequency 550kHz Operation |


Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0511 REV F • PRINTED IN USA
© LINEAR TECHNOLOGY CORPORATION 2006

Downloaded from Arrow.com.