ABSOLUTE MAXIMUM RATINGS

(Note 1)

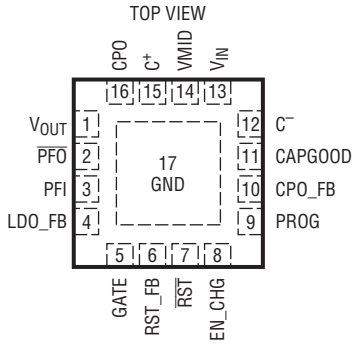
V_{IN}, V_{OUT}, VMID, CPO, $\overline{RST}$, $\overline{PFO}$, CAPGOOD, LDO_FB ..... –0.3V to 6V

EN_CHG, PFI, RST_FB, CPO_FB Voltage..... –0.3V to Max (V_{IN}, CPO) + 0.3V

Operating Junction Temperature Range (Note 3)..... –40 to 125°C

Storage Temperature Range ..... –65 to 150°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 58.7°C/W (NOTE 2)

EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3226EUD#PBF	LTC3226EUD#TRPBF	LFZV	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC3226IUD#PBF	LTC3226IUD#TRPBF	LFZV	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 3). V_{IN} = 3.3V, V_{CPO} = 5V, V_{OUT} = 3.3V, VMID = 1/2 V_{CPO} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Range		●	2.5		5.5	V
$I_{VIN(ST)}$	V_{IN} Quiescent Current in Normal Mode	V_{PFI} > 1.2V, V_{CPO_FB} > 1.2V, V_{IN} < V_{CPO}			10		µA
$I_{CPO(ST)}$	CPO Quiescent Current in Normal Mode	V_{PFI} > 1.2V, V_{CPO_FB} > 1.2V, V_{IN} < V_{CPO}			20		µA
$I_{VOUT(ST)}$	V_{OUT} Quiescent Current in Normal Mode	V_{OUT} = V_{IN}, V_{PFI} > 1.2V, V_{CPO_FB} > 1.2V, V_{IN} < V_{CPO}			5		µA
$I_{CPO(BU)}$	CPO Quiescent Current in Backup Mode	V_{PFI} < 1.2V, V_{LDO_FB} > 0.8V, V_{CPO} > V_{OUT}			24		µA
$I_{VOUT(BU)}$	V_{OUT} Quiescent Current in Backup Mode	V_{IN} = 0V, V_{PFI} < 1.2V, V_{LDO_FB} > 0.8V, V_{CPO} > V_{OUT}			3		µA
Ideal Diode Controller							
$V_{FWD(EDA)}$	External Ideal Diode Forward Voltage (V_{IN}-V_{OUT})	I_{VOUT} = 2mA			15		mV
V_{RTO}	Fast Turn-Off Voltage (V_{IN}-V_{OUT})	V_{IN} Falling			–45		mV
	Fast Turn-On Voltage (V_{IN}-V_{OUT})	V_{OUT} Falling			45		mV
Charge Pump Supercapacitor Charger							
V_{CPO_FB}	CPO_FB Pin Threshold for Entering Sleep Mode		●	1.18	1.21	1.24	V
	CPO_FB Pin Hysteresis for Exiting Sleep Mode				20		mV
I_{CPO_FB}	Charge Pump FB Pin Input Leakage	V_{CPO_FB} = 1.3V	●	–50		50	nA
f_{OSC}	CLK Frequency			0.75	0.9	1.05	MHz
R_{OL}	Effective Open-Loop Output Impedance (Note 4)	V_{CPO} = 4.5V, C_{FLY} = 1µF			6		Ω
V_{PROG}	PROG Pin Servo Voltage	V_{CPO_FB} < 1.2V	●	0.98	1.0	1.02	V
$I_{VIN(ILIM)}$	Input Current Limit	R_{PROG} = 33.3k, V_{CPO} = 0V			360		mA
h_{PROG}	Ratio of V_{IN} Input Current Limit to PROG Pin Current	R_{PROG} = 33.3k, V_{CPO} = 0V			10,500		A/A
$I_{CHRG(1x)}$	CPO Pin Charging Current (1x Mode)	V_{IN} = 3.8V, R_{PROG} = 33.3k, V_{CPO} = 3V			315		mA
$I_{CHRG(2x)}$	CPO Pin Charging Current (2x Mode)	R_{PROG} = 33.3k			157.5		mA
I_{SC}	Short-Circuit Charge Current	PROG Pin Grounded, V_{CPO} = 0V			600		mA
V_{MODE}	V_{IN} to CPO Voltage Differential for Switching Mode from 1x to 2x				200		mV
	1x/2x Mode Comparator Hysteresis				120		mV
V_{CLAMP}	Maximum Voltage Across Either Supercapacitor After Charging		●		2.65	2.75	V
V_{STACK}	Maximum Supercapacitor Stack Voltage		●		5.3	5.5	V
VMID	VMID Output Voltage				2.5		V
	VMID Current Sourcing Capability	VMID < V_{CPO}/2, V_{CPO_FB} > 1.24V			4.5		mA
	VMID Current Sinking Capability	VMID > V_{CPO}/2, V_{CPO_FB} > 1.24V			5.5		mA
	CPO_FB Pin Threshold Voltage (Rising) for CAPGOOD		●	1.09	1.11	1.13	V
	CPO_FB Pin Hysteresis for CAPGOOD				20		mV
	CAPGOOD Output Low Voltage	I_{SINK} = 5mA			65		mV
	CAPGOOD High Impedance Leakage Current	$V_{CAPGOOD}$ = 5V	●			1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 3). V_{IN} = 3.3V, V_{CPO} = 5V, V_{OUT} = 3.3V, VMID = 1/2 V_{CPO} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LDO							
	Minimum CPO Voltage for LDO Operation			2.4			V
V_{LDO_FB}	LDO FB Servo Voltage	I_{VOUT} = 1mA	●	0.76	0.8	0.82	V
	Load Regulation $\Delta V_{LDO\_FB}/\Delta I_{OUT}$	1mA < I_{VOUT} < 2A			2.7		mV/A
	LDO FET $R_{DS(ON)}$	V_{CPO} = 3.6V			200		mΩ
$I_{LDO\_FB(LEAK)}$	LDO_FB Input Leakage Current	V_{LDO_FB} = 0.9V	●	–60		60	nA
I_{LIM}	LDO Current Limit			2	4		A
RST_FB, $\overline{RST}$							
$V_{RST\_FB(TH)}$	RST_FB Threshold (Falling Edge)		●	0.72	0.74	0.76	V
$V_{RST\_FB(HYS)}$	RST_FB Hysteresis				20		mV
$I_{RST\_FB(LEAK)}$	RST_FB Input Leakage Current	V_{RST_FB} = 0.9V	●	–50		50	nA
	$\overline{RST}$ Output Low Voltage	I_{SINK} = 5mA			65		mV
	$\overline{RST}$ High Impedance Leakage Current	$V_{\overline{RST}}$ = 5V	●			1	µA
	$\overline{RST}$ Delay (RST_FB Rising)				290		ms
Power-Fail Comparator							
$V_{PFI(TH)}$	PFI Input Threshold (Falling Edge)		●	1.175	1.2	1.225	V
$V_{PFI(HYS)}$	PFI input Hysteresis				20		mV
$I_{PFI(LEAK)}$	PFI Input Leakage Current	V_{PFI} = 0.5V	●	–50		50	nA
	$\overline{PFO}$ Output Low Voltage	I_{SINK} = 5mA			65		mV
$I_{PFO(LEAK)}$	$\overline{PFO}$ High Impedance Leakage Current	V_{PFO} = 5V	●			1	µA
	PFI Delay to $\overline{PFO}$ (PFI Falling)				0.5		µs
EN_CHG							
V_{IH}	Input High Voltage		●	1.3			V
V_{IL}	Input Low Voltage		●			0.4	V
I_{IH}	Input High Current		●	–1		1	µA
I_{IL}	Input Low Current		●	–1		1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Failure to solder the exposed backside of the package to the PC board ground plane will result in a thermal resistance much greater than 58.7°C/W.

Note 3: The LTC3226 is tested under pulsed load conditions such that $T_A \approx T_J$. The LTC3226E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3226I is guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature, T_J, is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the formula:

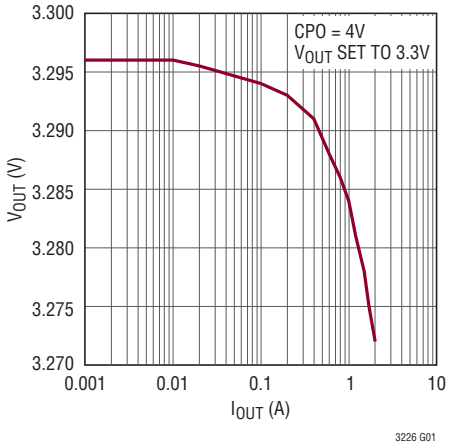
$$T_J = T_A + (P_D \bullet 58.7°C/W)$$

Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated thermal package thermal resistance and the environmental factor.

Note 4: Output not in regulation; $R_{OL} = (2 \bullet V_{IN} – V_{CPO})/I_{CPO}$.

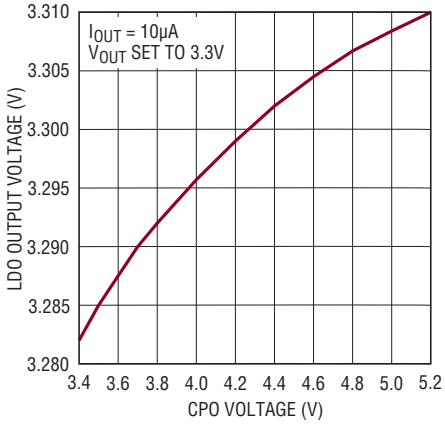
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

LDO Load Regulation



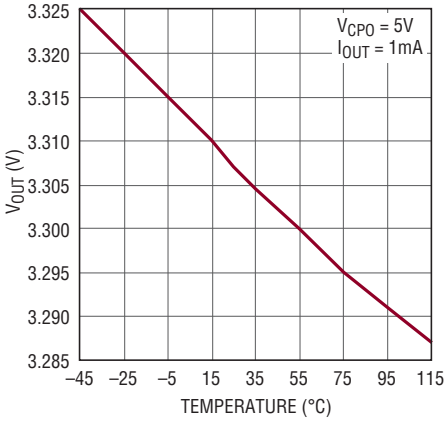
3226 G01

LDO Supply Regulation



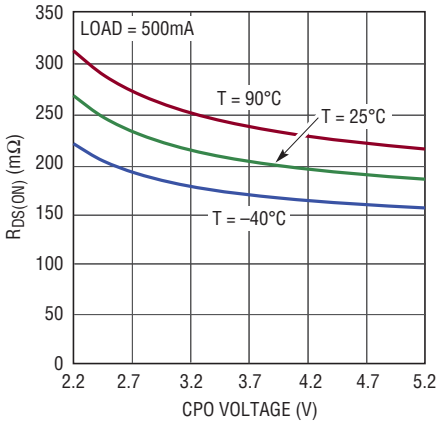
3226 G02

LDO Regulation Voltage vs Temperature



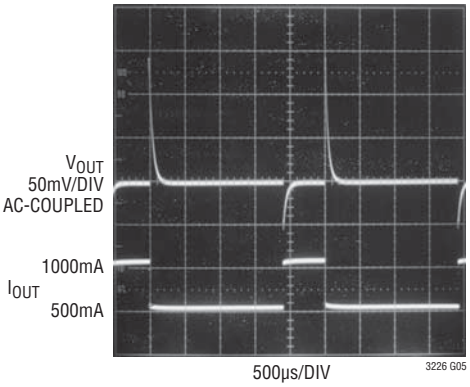
3226 G03

LDO FET On-Resistance vs CPO Voltage and Temperature



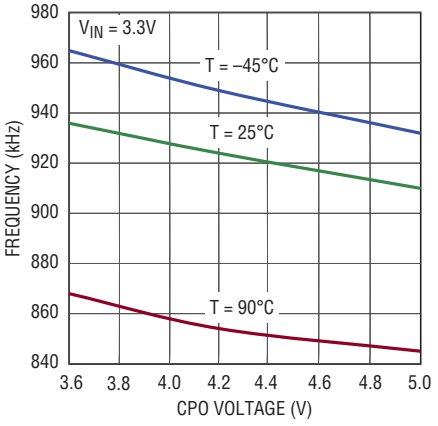
3226 G04

LDO Output Transient Step Response Waveform



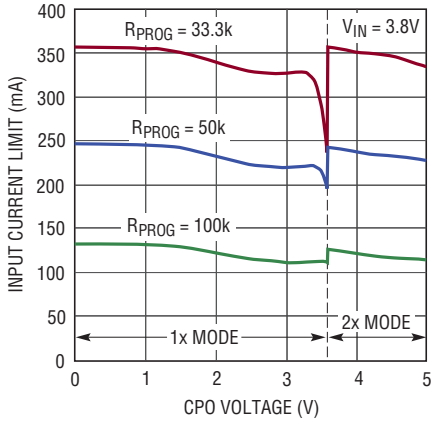
3226 G05

Charge Pump Oscillator Frequency vs V_{CPO} and Temperature



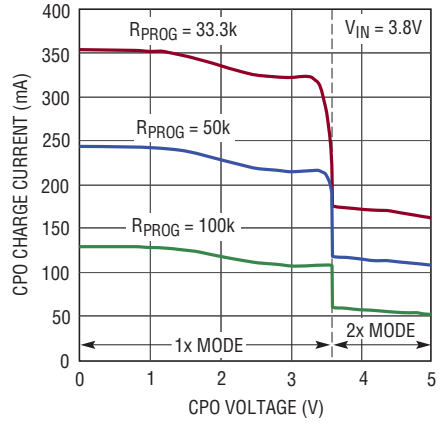
3226 G06

Charge Pump Input Current vs CPO Output Voltage



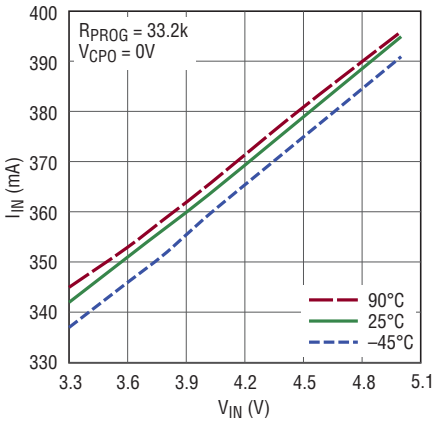
3226 G07

Charge Pump Charging Current vs CPO Output Voltage



3226 G08

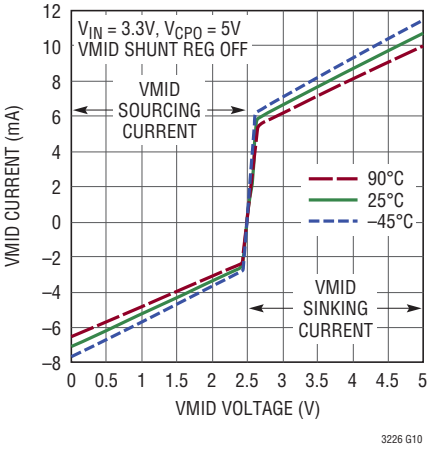
Charge Pump Input Current vs V_{IN} with CPO Grounded



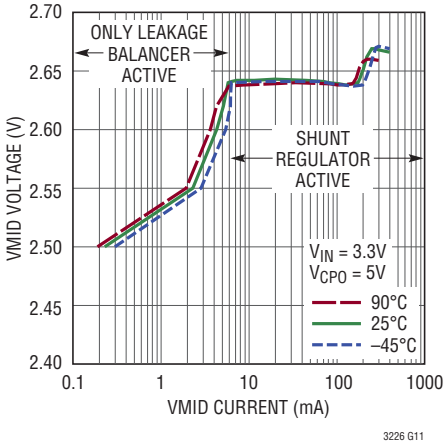
3226 G09

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

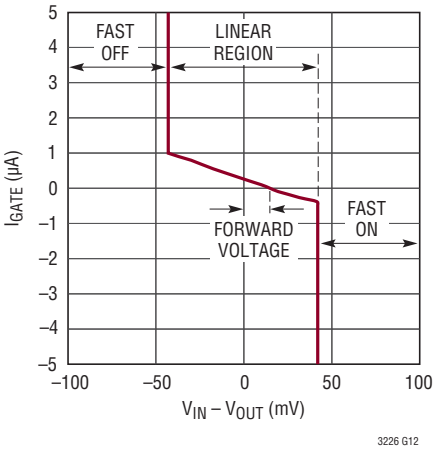
Leakage Balancer Source and Sink Capability



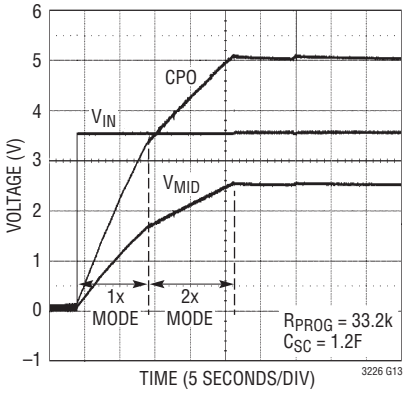
VMID Shunt Regulator Voltage vs Current and Temperature



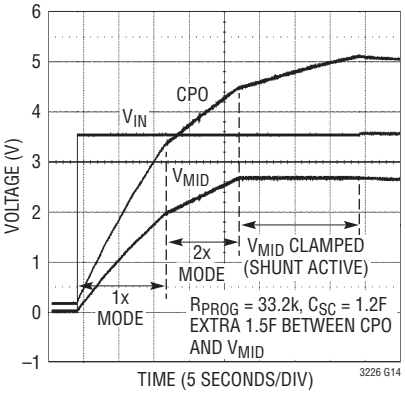
Ideal Diode Gate Current vs (V_{IN}-V_{OUT})



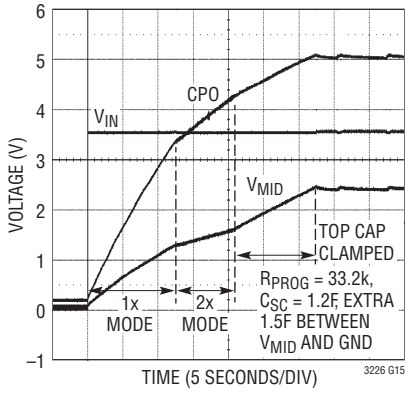
Charge Profile When Top Capacitor = Bottom Capacitor



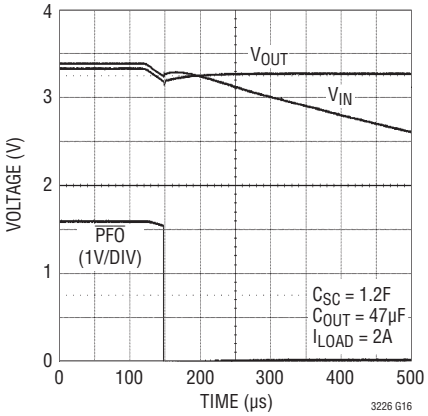
Charge Profile When Top Capacitor > Bottom Capacitor



Charge Profile When Top Capacitor < Bottom Capacitor



Normal-to-Back-Up Mode Switching Transient Waveform



PIN FUNCTIONS

V_{OUT} (Pin 1): Voltage Output. This pin is used to provide power to an external load from either the primary input supply (V_{IN}) or the supercapacitor (CPO) if the primary input supply is not available. V_{OUT} should be bypassed with a low ESR ceramic capacitor of at least 47µF capacitance to GND.

$\overline{PFO}$ (Pin 2): Open-Drain Power-Fail Status Output. This pin is pulled to ground by an internal N-channel MOSFET when the PFI input is below 1.2V. Once the PFI input recovers, this pin becomes high impedance.

PFI (Pin 3): Power-Fail Input. High impedance input to an accurate comparator with a 1.2V falling threshold and 20mV hysteresis. This pin controls the state of the $\overline{PFO}$ output pin and the operating mode of the LTC3226.

LDO_FB (Pin 4): Internal LDO Feedback Pin. The voltage on this pin is compared to the internal reference voltage (0.8V) by the error amplifier to keep the output in regulation. An external resistor divider is required between V_{OUT}, LDO_FB and GND to program the LDO output voltage. See the Applications Information section.

GATE (Pin 5): External FET Gate Pin. This pin is driven by an internal ideal diode controller to regulate V_{OUT} to 15mV below V_{IN}.

RST_FB (Pin 6): Reset Comparator Input. High impedance input to an accurate comparator with a 0.74V falling threshold and 20mV hysteresis. This pin controls the state of the $\overline{RST}$ output pin. An external resistor divider is required between V_{OUT}, RST_FB and GND. It can be the same resistor divider as the LDO_FB divider. See the Applications Information section.

$\overline{RST}$ (Pin 7): Open-Drain Status Output of the RESET Comparator. This pin is pulled to ground by an internal N-channel MOSFET whenever the RST_FB pin voltage falls below 0.74V. Once the RST_FB pin voltage recovers, the pin becomes high impedance after a 290ms delay indicating that V_{OUT} is within 7.5% of its programmed value.

EN_CHG (Pin 8): Enable Pin for the Charge Pump Supercapacitor Charger with an Internal Pull-Up. Tie this pin to a voltage below 0.4V to disable the internal charge pump.

PROG (Pin 9): Charger Input Current Limit Programming Pin. A resistor connected between this pin and GND sets the input current limit for the charger. See the Applications Information section.

CPO_FB (Pin 10): Feedback Pin for the Charge Pump. The voltage on this pin is compared to the internal reference voltage (1.2V) to keep the charge pump output CPO in regulation. An external resistor divider is required between CPO, CPO_FB and GND to program the CPO output voltage. See the Applications Information section.

CAPGOOD (Pin 11): Open-Drain Status Output of the CPO Voltage. This pin is pulled to ground by an internal N-channel MOSFET until CPO_FB pin reaches 1.11V. Once the CPO_FB pin exceeds 1.11V, this pin becomes high impedance indicating that the CPO voltage is within 7.5% of its target value.

C^- (Pin 12): Internal Charge Pump Flying Capacitor Negative Terminal.

V_{IN} (Pin 13): Primary Input Supply. This pin supplies power to the V_{OUT} pin through an external P-channel MOSFET and also to the supercapacitors attached to the CPO and VMID pins. V_{IN} should be bypassed to GND with a low ESR ceramic capacitor of at least 2.2µF depending on the load transient.

VMID (Pin 14): Midpoint of Two Series Supercapacitors.

C^+ (Pin 15): Internal Charge Pump Flying Capacitor Positive Terminal. A 1µF to 10µF X5R or X7R ceramic capacitor should be connected from C^+ to C^-.

CPO (Pin 16): Backup Supply Pin. Connect CPO to the top plate of the top supercapacitor. This pin receives power from V_{IN} through an internal charge pump doubler and supplies power to V_{OUT} through an internal LDO when the primary input supply has failed.

GND (Exposed Pad Pin 17): Ground. The exposed pad should be connected to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the part to achieve optimal thermal performance.

BLOCK DIAGRAM

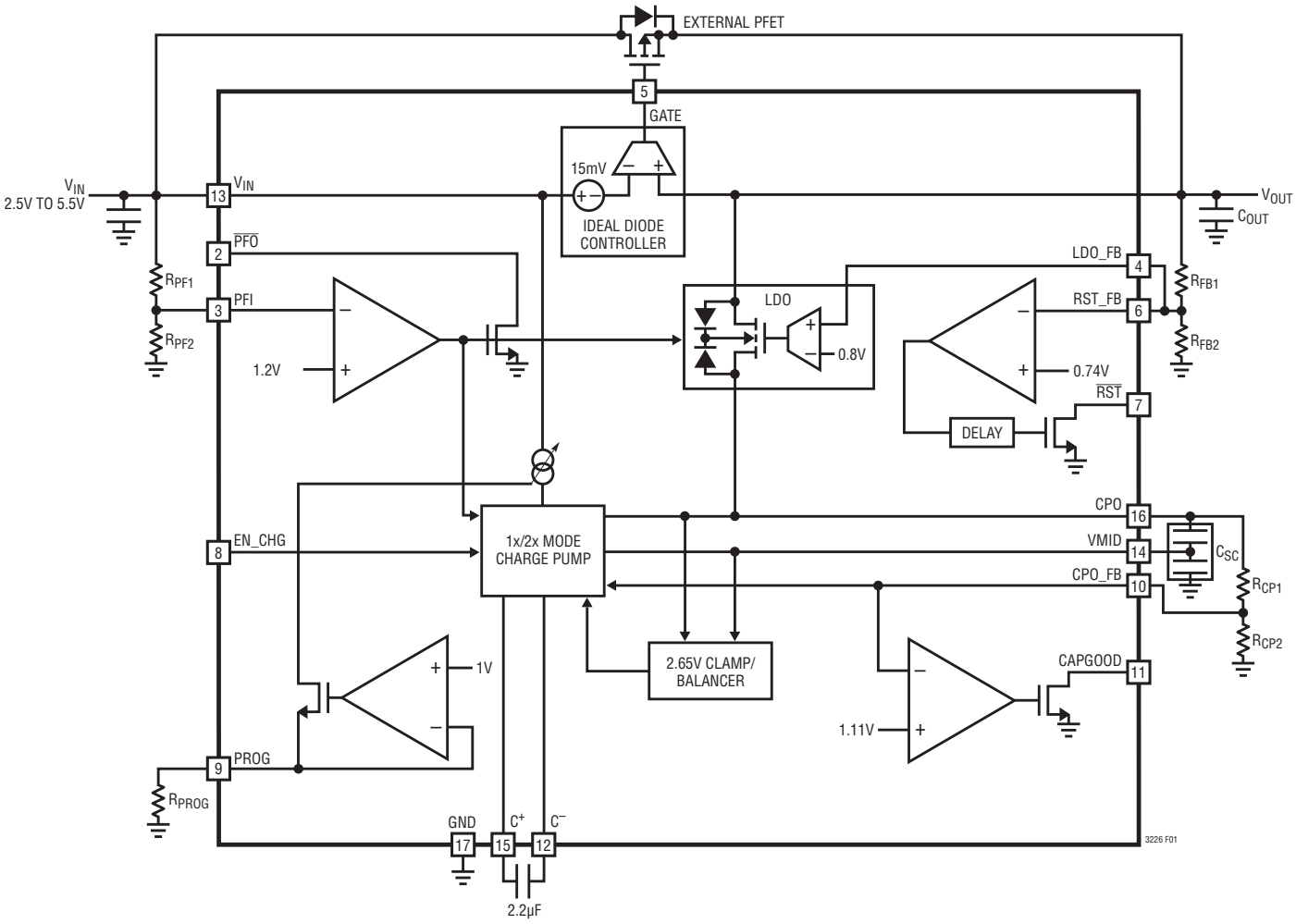


Figure 1. LTC3226 Block Diagram

OPERATION

The LTC3226 is a 2-cell series supercapacitor charger designed to back up a Li-ion battery or any system rail in the range of 2.5V to 5.3V. It has four principal circuit components: a dual mode (1x/2x) charge pump with an integrated balancer and a voltage clamp, an LDO to supply the load current from the charge stored on the supercapacitor, an ideal diode controller to control the gate of the external FET between V_{IN} and V_{OUT}, and a PFI comparator to decide whether to activate the charge pump to charge the supercapacitor stack or to activate the LDO to supply the load when V_{IN} falls below an externally programmed value.

The LTC3226 has two modes of operation: normal and backup. If V_{IN} is above an externally programmable PFI threshold voltage, the part is in normal mode in which power flows from V_{IN} to V_{OUT} through the external FET and the internal charge pump stays on to top off the supercapacitor stack. If V_{IN} is below this PFI threshold, the part is in backup mode. In this mode, the internal charge pump is turned off, the external FET is turned off and the LDO is turned on to supply the load current from the stored charge.

CHARGE PUMP

One of the principal circuit components of the LTC3226 is a dual mode low noise constant frequency (0.9MHz) regulated charge pump which transfers charge from V_{IN} and stores it onto the supercapacitor stack at the CPO pin. The target or termination voltage on the CPO pin is programmed by an external resistor divider using the CPO_FB pin. The input current limit to the charger is programmed by an external resistor between the PROG pin and ground. The charge pump turns on when V_{IN} exceeds the externally programmable PFI threshold. At the beginning of the charge cycle when the CPO pin voltage is less than V_{IN}, the charge pump is in 1x mode (linear mode) in which the charge pump acts as a pass element and charges the supercapacitor with a charge current that is limited by the programmed input current limit. As the CPO voltage rises to within 200mV of the input supply voltage, the charge pump switches to 2x mode (doubler mode) in which the average charge current is approximately equal to half the input current limit. As the CPO voltage exceeds the target value by approximately 1%, the charge pump switches turn off and the charge pump enters the sleep mode. In sleep mode, most of the charge pump control circuitry is turned off to minimize quiescent current. As the supercapacitor discharges due to leakage and internal quiescent current load, the CPO pin voltage slowly drops. When the CPO pin voltage drops 1% below the programmed voltage, the charge pump turns on to replenish charge on the supercapacitor and the cycle continues. The charge pump can be turned off by pulling the EN_CHG pin below 0.4V. However, by default, the charge pump is always enabled via an internal low current pull-up circuit if the EN_CHG pin is left floating.

Voltage Clamp

The LTC3226 charge pump is equipped with circuitry to limit the voltage across any supercapacitor in the stack to a maximum allowable preset voltage of 2.65V. If the voltage across the top capacitor (VMID-V_{CPO}) ever gets to 2.65V before the CPO pin reaches the target voltage, the charge pump stops charging the top of the stack via the CPO pin, switches to 1x mode and delivers charge directly to the bottom capacitor via the VMID pin until the stack voltage reaches its programmed value. If the voltage across the bottom capacitor reaches 2.65V before the stack gets to its target value, the charge pump continues to deliver charge to the top of the stack via the CPO pin and a shunt regulator turns on to bleed charge off of the bottom capacitor and prevents the VMID pin voltage from rising any further. The shunt regulator is able to shunt the maximum allowable charge current which is approximately 315mA (in 1x mode). In the event both capacitors exceed 2.65V, the charge pump enters sleep mode by turning off most of its circuitry.

Leakage Balancer

The LTC3226 is equipped with an internal leakage balancing amplifier which servos the VMID pin voltage to exactly half of the CPO pin voltage. However, it has limited source (~4.5mA) and sink (~5.5mA) capability. It is designed to handle slight mismatch of the supercapacitors due to leakage currents; not to correct any gross mismatch due to defects. The balancer is only active as long as the input supply voltage is above the PFI threshold. The internal balancer eliminates the need for external balancing resistors.

OPERATION

CAPGOOD Status Output

The LTC3226 charge pump includes a comparator to report the status of the supercapacitors via an open-drain NMOS transistor on the CAPGOOD pin. This pin is pulled to ground until the CPO pin voltage rises to within 7.5% of the programmed value. Once the CPO pin is above this threshold, the CAPGOOD pin goes high impedance.

PROG Pin Short-Circuit Protection

Typically the maximum current that the LTC3226 charge pump can deliver is set by the PROG resistor. However, if for any reason, the PROG pin gets shorted to GND, or the user chooses a PROG resistor value which is far smaller than recommended, the charge pump input current is limited to an internally set value of approximately 600mA. Also the maximum current that can be sourced from the PROG pin is limited by an internal resistor to less than 1mA.

LOW DROPOUT REGULATOR (LDO)

Another principal circuit component of the LTC3226 is the low dropout regulator (LDO) which transfers power from the supercapacitor stack to V_{OUT} through a pass element with an $R_{DS(ON)}$ of approximately 200mΩ. This LDO has a current limit internally set to 4A. In the event that the input supply voltage falls below the PFI threshold, the PFI comparator promptly turns on the LDO to supply the necessary load without letting the V_{OUT} rail droop too much. However, to prevent unrestricted current flow from the input to the supercapacitors through the ideal diode, the LDO is turned off until the CPO voltage is greater than V_{IN} by 100mV typical. The LDO output voltage is programmed through an external resistor divider via the LDO_FB pin.

POWER-FAIL (PFI) COMPARATOR

The LTC3226 contains a fast comparator which switches the part from normal to backup mode in the event the input voltage, V_{IN}, falls below an externally programmed threshold voltage. In backup mode, the charge pump shuts off and the LDO powers the load as long as there is enough charge stored on the supercapacitors. The PFI threshold voltage is programmed by an external resistor divider via the PFI pin. The output of the PFI comparator also drives the gate of an open-drain NMOS to report the status via the $\overline{PFO}$ pin. In normal mode, the $\overline{PFO}$ pin is high Impedance but in backup mode, the pin is pulled down to ground.

IDEAL DIODE CONTROLLER

The LTC3226 contains an ideal diode controller which controls the gate of an external PFET connected between the input, V_{IN}, and the output, V_{OUT}, through the GATE pin. Under normal operating conditions, this external FET constitutes the main power path from input to output. For very light loads, the controller maintains a 15mV delta across the FET between the input and output voltage. In the event V_{IN} suddenly drops below V_{OUT}, the controller quickly turns the FET completely off to prevent any reverse conduction from V_{OUT} back to the input supply.

RESET COMPARATOR

The LTC3226 contains a RESET comparator which monitors V_{OUT} under all operating modes via the RST_FB pin and reports the status via an open-drain NMOS transistor on the $\overline{RST}$ pin. At any time, if V_{OUT} falls 7.5% from its programmed value, it pulls the $\overline{RST}$ pin low almost instantaneously. However, on the rising edge the comparator waits 290ms after V_{OUT} crosses the threshold before making the $\overline{RST}$ pin high impedance.

GLOBAL THERMAL SHUTDOWN

The LTC3226 includes a global thermal shutdown which shuts down the entire part in the event the die temperature exceeds 152°C. It resumes normal operation once the temperature drops by about 15°C to approximately 137°C.

APPLICATIONS INFORMATION

Programming the Supercapacitor Termination Voltage (CPO)

The termination voltage of the supercapacitor stack on the CPO pin can be programmed for any voltage between 2.5V to 5.3V by using a resistor divider from the CPO pin to GND via the CPO_FB pin such that:

$$V_{CPO} = V_{CPO\_FB} \bullet \left(1 + \frac{R_{CP1}}{R_{CP2}}\right)$$

where V_{CPO_FB} is 1.2V. See the block diagram in Figure 1. Typical values for R_{CP1} and R_{CP2} are in the range of 40k to 5M.

Programming the Input Current Limit for the Charger

The input current limit for the LTC3226 charge pump is programmed by using a single resistor from the PROG pin to ground. The input current limit is typically 10,500 times the current out of the PROG pin. The PROG pin voltage always servos to 1V as long as the part is not in sleep mode. The program resistor and the input current limit are calculated using the following equations:

$$R_{PROG} = 10{,}500 \bullet \frac{1V}{I_{VIN(ILIM)}},\ I_{VIN(ILIM)} = 10{,}500 \bullet \frac{1V}{R_{PROG}}$$

where $I_{VIN(ILIM)}$ is the input current limit for the charge pump charger. The maximum allowable input current limit of 315mA can be achieved by using a PROG resistor of 33.2k. To maximize the charge transfer rate, the charge pump operates in 1x mode when the supercapacitor voltage is less than the input voltage and the charge current out of CPO pin is only limited by the programmed input current limit. However, in 2x mode, the average charge current is approximately half the input current limit.

Programming the Input Voltage Threshold for the Power-Fail Comparator

The input voltage threshold below which the power-fail status pin $\overline{PFO}$ indicates a power-fail condition and the LTC3226 switches the internal LDO on can be programmed by using a resistor divider from the V_{IN} pin to GND via the PFI pin such that:

$$V_{IN(PFO\_HI\_LO)} = V_{PFI} \bullet \left(1 + \frac{R_{PF1}}{R_{PF2}}\right)$$

where V_{PFI} is 1.2V. See Figure 1. Typical values for R_{PF1} and R_{PF2} are in the range of 40k to 5M. For a smooth transition from normal to back-up mode, the PFI threshold should be set 50mV to 100mV above the programmed LDO output voltage, V_{OUT}.

The input voltage above which the power-fail status pin $\overline{PFO}$ is high impedance and the supercapacitor charger and the ideal diode are enabled is:

$$V_{IN(PFO\_LO\_HI)} = \left(V_{PFI} + V_{PFI(HYS)}\right) \bullet \left(1 + \frac{R_{PF1}}{R_{PF2}}\right)$$

where $V_{PFI(HYS)}$ is the hysteresis of the PFI comparator. It is internally set to a typical value of 20mV.

The hysteresis can be increased externally by adding a resistor, R_H, in series with a diode, D1, between the $\overline{PFO}$ and PFI pins as shown in Figure 2. This network will increase the low-to-high V_{IN} threshold for $\overline{PFO}$ while keeping the high-to-low threshold intact. The increase in hysteresis at the input can be calculated as shown:

$$\Delta V_{IN(HYS)} = \left(V_{PFI} + V_{PFI(HYS)} - V_F\right) \bullet \frac{R_{PF1}}{R_H}$$

APPLICATIONS INFORMATION

where V_F is the forward voltage of the diode. As an example, if R_{PF1} = 200k, R_{PF2} = 120k, R_H = 2M, and V_F = 0.4V, the additional hysteresis provided by this network can be calculated using the above equation as follows:

$$\Delta V_{IN(HYS)} = (1.2 + 0.02 - 0.4)\,V \bullet \frac{200k\Omega}{2M\Omega} = 82mV$$

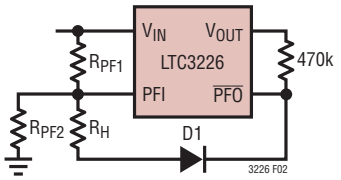


Figure 2. Increasing PFI Comparator Hysteresis Externally

Programming the LDO Output Voltage (V_{OUT})

The LDO output voltage in backup mode can be programmed for any voltage between 2.5V to 5.3V by using a resistor divider from the V_{OUT} pin to GND via the LDO_FB pin such that:

$$V_{OUT} = V_{LDO\_FB} \bullet \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where V_{LDO_FB} is 0.8V. See the Block Diagram in Figure 1. Typical values for R_{FB1} and R_{FB2} are in the range of 40k to 500k. Too small a resistor will result in a large quiescent current whereas too large a resistor coupled with LDO_FB pin capacitance will create an additional pole and may cause loop instability.

Programming the Reset Threshold

The threshold for the reset comparator can be programmed by using a resistor divider from the V_{OUT} pin to GND via the RST_FB pin such that:

$$V_{OUT} = V_{RST\_FB} \bullet \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where V_{RST_FB} is 0.74V. See Figure 1. Typical values for R_{FB1} and R_{FB3} are in the range of 40k to 5M. In most applications, the LDO_FB and RST_FB pins can be shorted together and only one resistor divider between V_{OUT} and GND is needed to set V_{OUT} and the reset threshold 7.5% below the V_{OUT} programmed voltage. However, the reset threshold can be set independent of V_{OUT} by an additional resistor divider.

Effective Open-Loop Output Resistance (R_{OL}) of the Charge Pump

The effective open-loop output resistance (R_{OL}) of a charge pump determines the strength of a charge pump. The value of this parameter depends on many factors such as the oscillator frequency (f_{OSC}), value of the flying capacitor (C_{FLY}), the nonoverlap time, the internal switch resistances (R_S), and the ESR of the external capacitors. A first order approximation of R_{OL} is given below:

$$R_{OL} \cong 2 \sum_{S=1to4} R_S + \frac{1}{f_{OSC} \bullet C_{FLY}}$$

For the LTC3226 charge pump, the sum of the switch resistances is approximately 2.5Ω in a typical application where V_{IN} = 3.3V and V_{CPO} = 5V. For C_{FLY} = 1µF and f_{OSC} = 1MHz, the effective open-loop output resistance of the charge pump can be approximated from the above equation as follows:

$$R_{OL} \cong 2 \bullet 2.5\Omega + \frac{1}{1MHz \bullet 1\mu F} = 6\Omega$$

Maximum Available Charge Current

In the absence of any internal current limit, the maximum available current out of a charge pump in 2x mode can be calculated from the charge pump input and output voltage and the effective open-loop output resistance R_{OL} using the following equation:

$$I_{CHRG} = \frac{2V_{IN} - V_{CPO}}{R_{OL}}$$

For example, if the LTC3226 charge pump ($R_{OL} \cong 6\Omega$) has to charge a supercapacitor to 5V from 2.5V input, the charge current available when V_{CPO} = 4.8V can be calculated as follows:

$$I_{CHRG} = \frac{2 \bullet 2.5V - 4.8V}{6\Omega} = 33.3mA$$

APPLICATIONS INFORMATION

So even if the charge pump input current limit is programmed for 315mA (R_{PROG} = 33.2k), the actual charge current will be considerably less than 157.5mA (half of programmed limit) in 2x mode for very low input supply. For V_{IN} = 2.5V, the CPO voltage above which the charge current will decrease from the programmed value of 157.5mA (R_{PROG} = 33.2k) can be calculated from the previous equation as follows:

$$V_{CPO} = (2 \bullet 2.5V - 157.5mA \bullet 6\Omega) = 4.055V$$

Choosing the LDO Output Capacitor

In the event V_{IN} falls below the programmed PFI threshold, the PFI comparator turns off the charge pump and turns on the internal LDO to supply the load from the backed-up supercapacitor storage. However, due to the delay associated with the PFI comparator and LDO circuitry, it could be up to 2µs before the LDO is capable of supplying the load demand at V_{OUT}. In order to prevent V_{OUT} from drooping too much during this transition, a 47µF ceramic capacitor is recommended at the V_{OUT} terminal. For any output capacitance, C_{OUT}, delay, Δt, and load current, I_{LOAD}, the drop in V_{OUT}, ΔV, can be calculated using the following equation:

$$I_{LOAD} = C_{OUT} \bullet \frac{\Delta V}{\Delta t}$$

For example, if V_{OUT} can not tolerate more than 100mV drop under a maximum load of 2A during this transition, the minimum capacitance required at the LDO output can be calculated using the above equation as follows:

$$C_{OUT(MIN)} = 2A \bullet \frac{2\mu s}{100mV} = 40\mu F$$

Charging a Single Supercapacitor

The LTC3226 can also be used to charge a single supercapacitor by connecting two series-connected matched ceramic capacitors with a minimum capacitance of 100µF in parallel with the supercapacitor as shown in Figure 3.

Supercapacitor Manufacturers

Refer to the following table for supercapacitor manufacturers.

Table 1. Supercapacitor Manufacturers

CAP-XX	www.cap-xx.com
NESS CAP	www.nesscap.com
Maxwell	www.maxwell.com
Bussmann	www.cooperbussmann.com
AVX	www.avx.com
Illinois Capacitor	www.illinoiscapacitor.com
Tecate Group	www.tecategroup.com

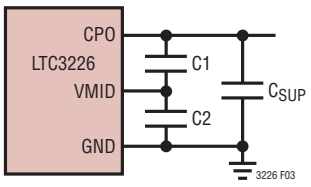


Figure 3. Charging a Single Supercapacitor

Board Layout Considerations

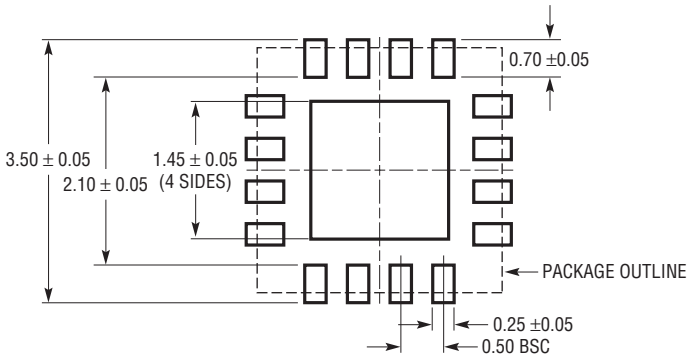
Due to high switching frequency and high transient currents produced by the LTC3226 charge pump, careful board layout is necessary for optimum performance. A true ground plane and short connections to all of the external capacitors will improve performance.

Also, to be able to deliver maximum load current from the LDO under all conditions, it is critical that the exposed metal pad on the backside of the QFN package has a good thermal contact to the PC board ground plane. Lack of proper thermal contact can cause the junction temperature to exceed the threshold for thermal shutdown.

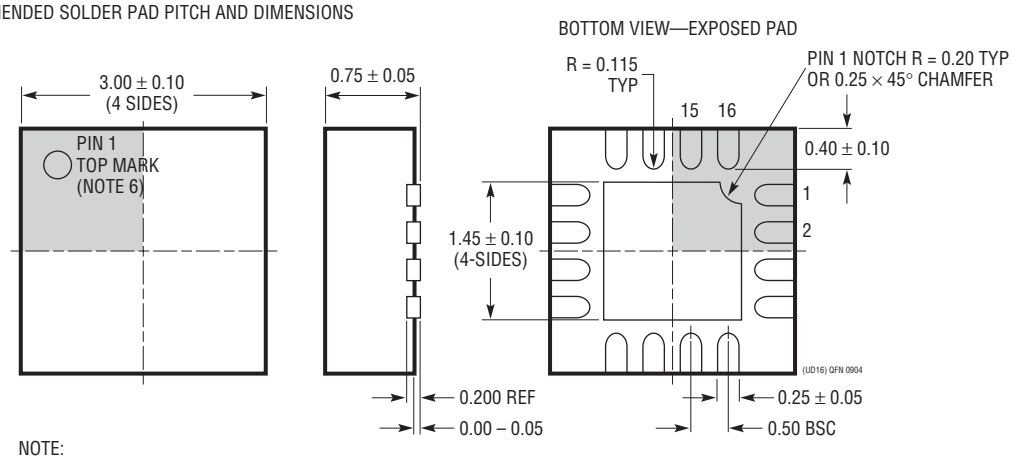
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



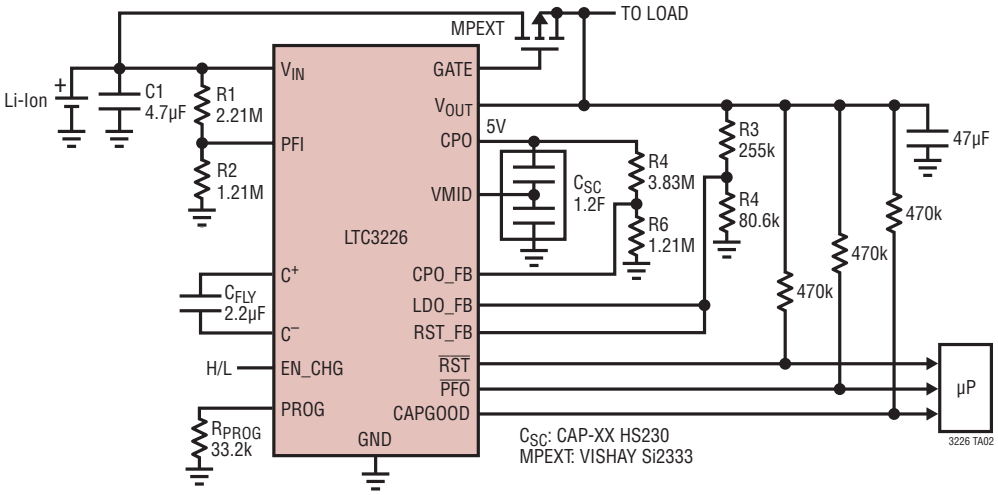
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	5/12	Added Note 3 to operating junction temperature range	2
		Modified basic default conditions for Electrical Characteristics	3, 4
		Modified test conditions for Note 3	4

TYPICAL APPLICATION

Li-Ion Backup Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3225/ LTC3225-1	150mA Supercapacitor Charger	Low Noise, Constant Frequency Charging of Two Series Supercapacitors. Automatic Cell Balancing Prevents Capacitor Overvoltage During Charging. Programmable Charge Current (Up to 150mA). Selectable 2.4V or 2.65V Regulation per Cell (LTC3225), Selectable 2V or 2.25V Regulation per Cell (LTC3225-1). 2mm × 3mm DFN Package
LT3485	Photoflash Capacitor Chargers with Output Voltage Monitor and Integrated IGBT Drive	Integrated IGBT Driver; Voltage Output Monitor; Uses Small Transformers: 5.8mm × 5.8mm × 3mm. Operates from Two AA Batteries, Single Cell Li-Ion or Any Supply from 1.8V Up to 10V. No Output Voltage Divider Needed; No External Schottky Diode Required. Charges Any Size Photoflash Capacitor; 10-Lead (3mm × 3mm) DFN Package
LTC3625/ LTC3625-1	1A High Efficiency 2-Cell Supercapacitor Charger with Automatic Cell Balancing	High Efficiency Step-Up/Step-Down Charging of Two Series Supercapacitors. Automatic Cell Balancing Prevents Capacitor Overvoltage During Charging. Programmable Charging Current Up to 500mA (Single Inductor), 1A (Dual Inductor). V_{IN} = 2.7V to 5.5V, Selectable 2.4V/2.65V Regulation per Cell (LTC3625). Selectable 2V/2.25V Regulation per Cell (LTC3625-1), Low No-Load Quiescent Current: 23µA. 12-lead 3mm × 4mm DFN Package
LT3750	Capacitor Charger Controller	Charges Any Size Capacitor; Easily Adjustable Output Voltage. Drives High Current NMOS FETs; Primary-Side Sense—No Output Voltage Divider Necessary. Wide Input Range: 3V to 24V; Drives Gate to V_{CC} – 2V. 10-Lead MS Package
LT3751	High Voltage Capacitor Charger Controller with Regulation	Charges Any Size Capacitor; Low Noise Output in Voltage Regulation Mode. Stable Operation Under a No-Load Condition; Integrated 2A MOSFET Gate Driver with Rail-to-Rail Operation for $V_{CC} \leq$ 8V. Selectable 5.6V or 10.5V Internal Gate Drive Voltage Clamp; User-Selectable Over/Undervoltage Detect. Easily Adjustable Output Voltage; Primary or Secondary Side Output Voltage Sense. Wide Input V_{CC} Voltage Range (5V to 24V). 20-Pin QFN 4mm × 5mm and 20-Lead TSSOP Packages
LTC4425	Supercapacitor Charger with Current Limited Ideal Diode	Constant-Current/Constant-Voltage Linear Charger for 2-cell Series Supercapacitor Stack. V_{IN}: Li-Ion/Polymer Battery, a USB Port, or a 2.7V to 5.5V Current-Limited Supply. 2A Charge Current, Auto Cell Balancing, 20µA Quiescent Current, Shutdown Current <2µA. Low Profile 12-Pin 3mm × 3mm DFN or a 12-Lead MSOP Package

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
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