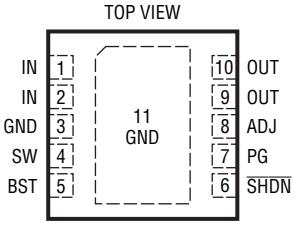
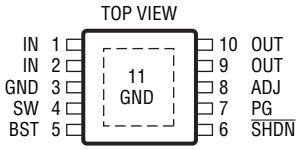
ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{BST} to GND ..... –0.3V to 6V
V_{IN} to GND ..... –0.3V to 6V
PG to GND ..... –0.3V to 6V
$\overline{SHDN}$ to GND ..... –0.3V to 6.3V
ADJ to GND ..... –0.3V to (V_{IN} + 0.3V)
Output Short-Circuit Duration ..... Indefinite
Operating Junction Temperature Range
(Note 8) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (MSE, Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3026EDD#PBF	LTC3026EDD#TRPBF	LBHW	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3026IDD#PBF	LTC3026IDD#TRPBF	LBHW	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3026EMSE#PBF	LTC3026EMSE#TRPBF	LTBJB	10-Lead Plastic MSOP	–40°C to 125°C
LTC3026IMSE#PBF	LTC3026IMSE#TRPBF	LTBJB	10-Lead Plastic MSOP	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3026EDD	LTC3026EDD#TR	LBHW	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3026IDD	LTC3026IDD#TR	LBHW	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3026EMSE	LTC3026EMSE#TR	LTBJB	10-Lead Plastic MSOP	–40°C to 125°C
LTC3026IMSE	LTC3026IMSE#TR	LTBJB	10-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS (BOOST ENABLED, L_{SW} = 10µH)

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 1.5V, V_{OUT} = 1.2V, C_{IN} = C_{BST} = 4.7µF, C_{OUT} = 10µF (all capacitors ceramic) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage	(Note 2)	●	1.14		3.5	V
I_{IN}	Operating Current	I_{OUT} = 0mA, V_{OUT} = 0.8V, $V_{\overline{SHDN}}$ = V_{IN}, V_{IN} = 1.2V I_{OUT} = 0mA, V_{OUT} = 1.2V, $V_{\overline{SHDN}}$ = V_{IN}, V_{IN} = 1.5V I_{OUT} = 0mA, V_{OUT} = 1.2V, $V_{\overline{SHDN}}$ = V_{IN}, V_{IN} = 2.5V I_{OUT} = 0mA, V_{OUT} = 1.2V, $V_{\overline{SHDN}}$ = V_{IN}, V_{IN} = 3.5V			1160 950 640 400		µA µA µA µA
$I_{IN\overline{SHDN}}$	Shutdown Current	$V_{\overline{SHDN}}$ = 0V, V_{IN} = 3.5V	●		0.6	20	µA
	Inductor Size Requirement Inductor Peak Current Requirement			4.7 150	10	40	µH mA
V_{BST}	Boost Output Voltage Range	$V_{\overline{SHDN}}$ = V_{IN}		4.8	5	5.2	V
$V_{BSTUVLO}$	Boost Undervoltage Lockout		●	4.0	4.2	4.4	V
	Boost Output Drive (Note 3)	V_{IN} < 1.4V V_{IN} ≥ 1.4V			7 10		mA mA

(BOOST DISABLED, V_{SW} = 0V or Floating)

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 1.5V, V_{OUT} = 1.2V, V_{BST} = 5V, C_{IN} = C_{BST} = 1µF, C_{OUT} = 10µF (all capacitors ceramic) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage	(Note 2)	●	1.14		5.5	V
I_{IN}	Operating Current	I_{OUT} = 100µA, $V_{\overline{SHDN}}$ = V_{IN}, 1.2V ≤ V_{IN} ≤ 5V	●		95	200	µA
$I_{IN\overline{SHDN}}$	Shutdown Current	$V_{\overline{SHDN}}$ = 0V, V_{IN} = 3.5V	●		0.6	20	µA
V_{BST}	Boost Operating Voltage (Note 7)	$V_{\overline{SHDN}}$ = V_{IN}	●	4.5	5	5.5	V
$V_{BSTUVLO}$	Undervoltage Lockout		●	4.0	4.25	4.4	V
I_{BST}	Boost Operating Current	I_{OUT} = 100µA, $V_{\overline{SHDN}}$ = V_{IN}	●		175	275	µA
$I_{BST\overline{SHDN}}$	Boost Shutdown Current	$V_{\overline{SHDN}}$ = 0V			1	5	µA

(BOOST ENABLED or DISABLED)

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 1.5V, V_{OUT} = 1.2V, C_{IN} = C_{BST} = 1µF, C_{OUT} = 10µF (all capacitors ceramic) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{ADJ}	Regulation Voltage (Note 5)	1mA ≤ I_{OUT} ≤ 1.5A, 1.14V ≤ V_{IN} ≤ 3.5V, V_{BST} = 5V, V_{OUT} = 0.8V 1mA ≤ I_{OUT} ≤ 1.5A, 1.14V ≤ V_{IN} ≤ 3.5V, V_{BST} = 5V, V_{OUT} = 0.8V	 ●	0.397 0.395	0.4 0.4	0.403 0.405	V V
OUT	Programming Range		●	0.4		2.6	V
	Dropout Voltage (Note 6)	V_{IN} = 1.5V, V_{ADJ} = 0.38, I_{OUT} = 1.5A	●		100	250	mV
I_{ADJ}	ADJ Input Current	V_{ADJ} = 0.4V	●	–100		100	nA
I_{OUT}	Continuous Output Current	$V_{\overline{SHDN}}$ = V_{IN}	●	1.5			A
I_{LIM}	Output Current Current Limit				3		A
e_n	Output Voltage Noise	f = 10Hz to 100kHz, I_L = 800mA Boost Disabled Boost Enabled			 110 210		 μV_{RMS} μV_{RMS}

ELECTRICAL CHARACTERISTICS (BOOST ENABLED or DISABLED)

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 1.5V, V_{OUT} = 1.2V, C_{IN} = C_{BST} = 1µF, C_{OUT} = 10µF (all capacitors ceramic) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IH\overline{SHDN}}$	$\overline{SHDN}$ Input High Voltage	1.14V ≤ V_{IN} ≤ 3.5V 3.5V ≤ V_{IN} ≤ 5.5V	● ●	1.0 1.2			V V
$V_{IL\overline{SHDN}}$	$\overline{SHDN}$ Input Low Voltage	1.14V ≤ V_{IN} ≤ 5.5V	●			0.4	V
$I_{IH\overline{SHDN}}$	$\overline{SHDN}$ Input High Current	$\overline{SHDN}$ = V_{IN}		–1		1	µA
$I_{IL\overline{SHDN}}$	$\overline{SHDN}$ Input Low Current	$\overline{SHDN}$ = 0V		–1		1	µA
V_{OLPG}	PG Output Low Voltage	I_{PG} = 2mA	●		0.1	0.4	V
I_{OHPG}	PG Output High Leakage Current	V_{PG} = 5.5V			0.01	1	µA
PG	Output Threshold (Note 4)	PG High to Low PG Low to High		–12 –10	–9 –7	–6 –4	% %

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. This IC has overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 125°C when overtemperature is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 2: Minimum Operating Voltage required for regulation is:

$V_{IN} \geq V_{OUT(MIN)} + V_{DROPOUT}$

Note 3: When using BST to drive loads other than LTC3026s, the load must be high impedance during start-up (i.e. prior to PG going high).

Note 4: PG threshold expressed as a percentage difference from the "V_{ADJ} Regulation Voltage" as given in the table.

Note 5: Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.

Note 6: Dropout voltage is minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to $V_{IN} - V_{DROPOUT}$.

Note 7: To maintain correct regulation

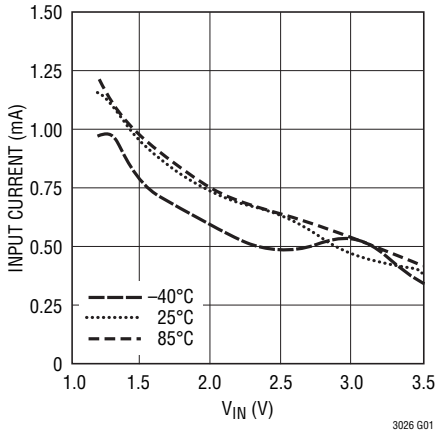
$V_{OUT} \leq V_{BST} - 2.4V$

Note 8: The LTC3026 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3026E is guaranteed to meet specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3026I is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

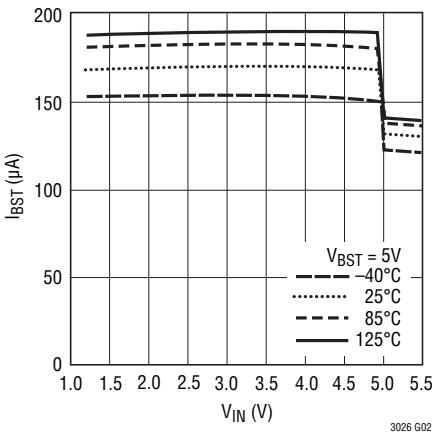
$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

TYPICAL PERFORMANCE CHARACTERISTICS

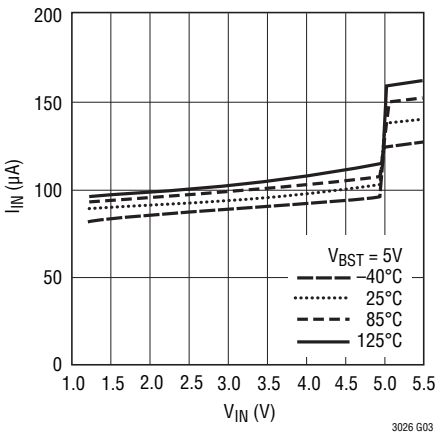
IN Supply Current with Boost Converter Enabled



BST Supply Current with Boost Converter Disabled

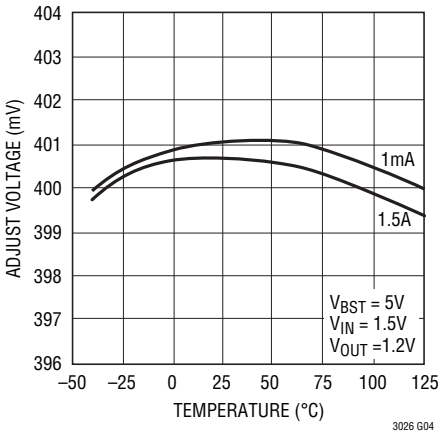


IN Supply Current with Boost Converter Disabled

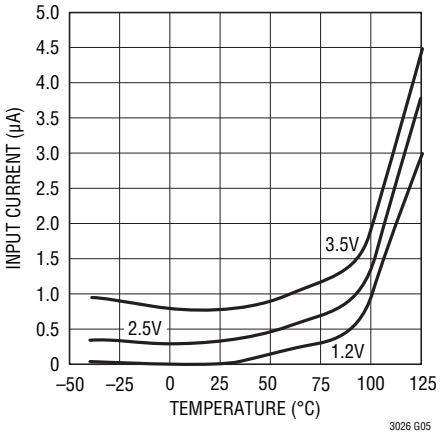


TYPICAL PERFORMANCE CHARACTERISTICS

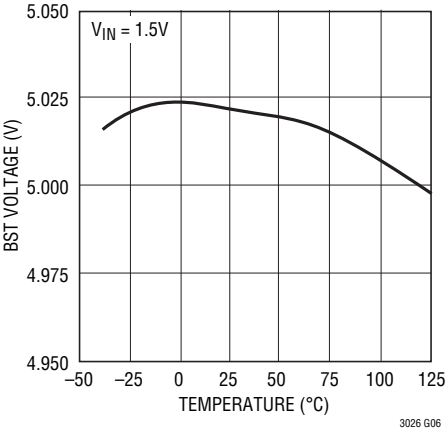
ADJ Voltage vs Temperature



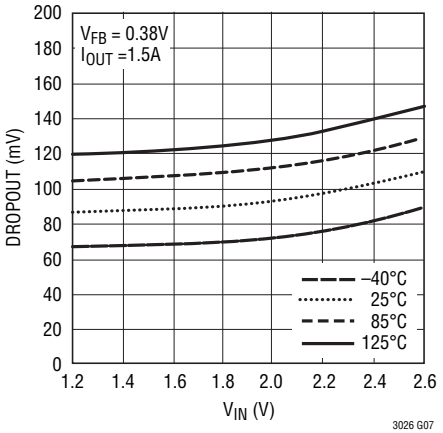
IN Shutdown Current



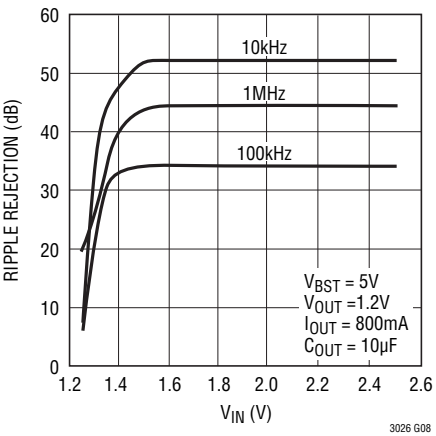
BST Voltage vs Temperature



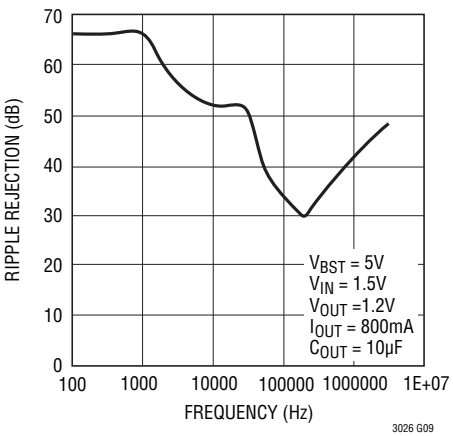
Dropout Voltage vs Input Voltage



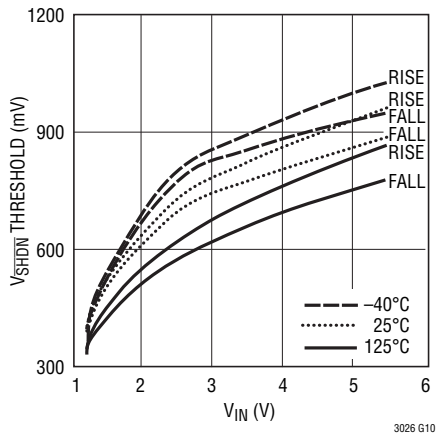
Ripple Rejection



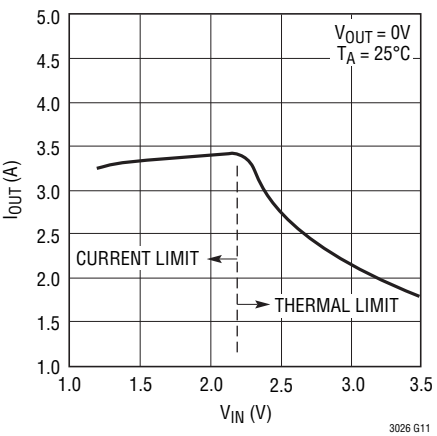
Ripple Rejection



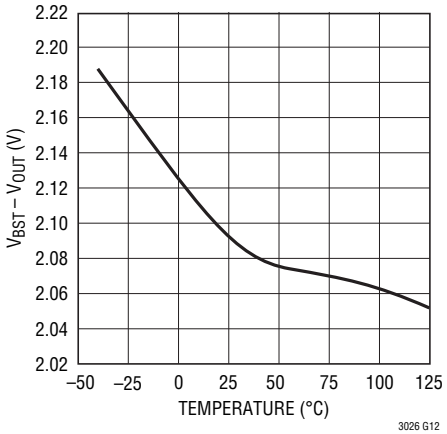
Shutdown Threshold



Output Current Limit

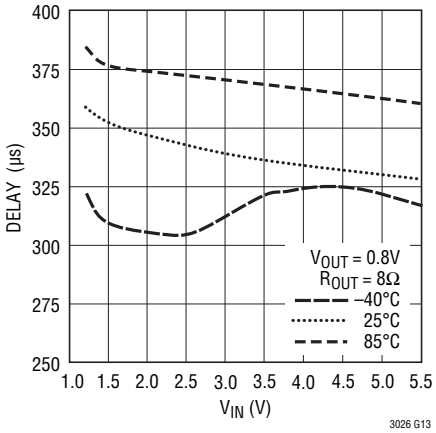


BST to OUT Headroom Voltage

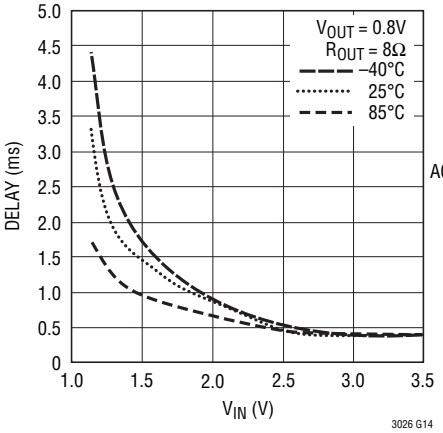


TYPICAL PERFORMANCE CHARACTERISTICS

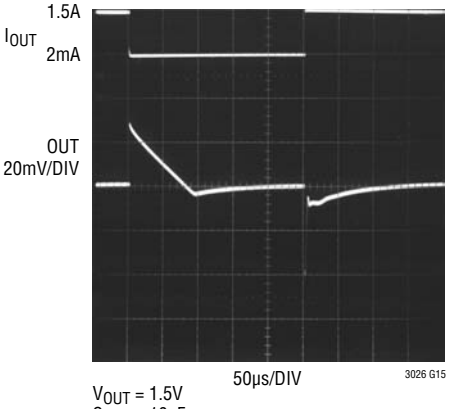
Delay from Enable to PG with Boost Disabled



Delay from Enable to PG with Boost Enabled

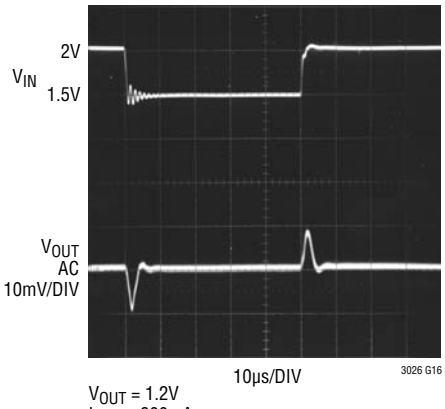


Output Load Transient Response



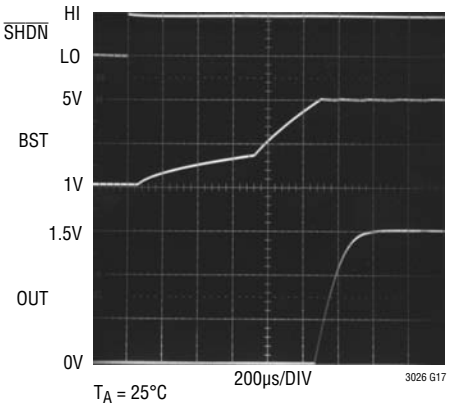
VOUT = 1.5V
COUT = 10µF
VIN = 1.7V
VBST = 5V

IN Supply Transient Response



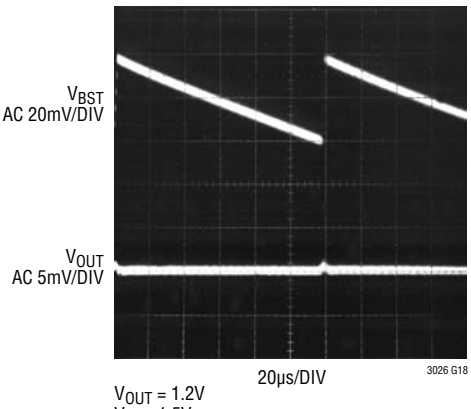
VOUT = 1.2V
IOUT = 800mA
COUT = 10µF
VBST = 5V
TA = 25°C

BST/OUT Start-Up



TA = 25°C
ROUT = 1Ω
VIN = 1.7V

BST Ripple and Feedthrough to OUT



VOUT = 1.2V
VIN = 1.5V
IOUT = 1A
COUT = 10µF
LSW = 10µH
TA = 25°C

PIN FUNCTIONS

IN (Pins 1, 2): Input Supply Voltage. Output load current is supplied directly from IN. The IN pin should be locally bypassed to ground if the LTC3026 is more than a few inches away from another source of bulk capacitance. In general, the output impedance of a battery rises with frequency, so it is usually advisable to include an input bypass capacitor when supplying IN from a battery. A capacitor in the range of 0.1µF to 4.7µF is usually sufficient.

GND (Pin 3, Exposed Pad Pin 11): Ground and Heat Sink. Connect the exposed pad to the PCB ground plane or large pad for optimum thermal performance.

SW (Pin 4): Boost Switching Pin. This is the boost converter switching pin. A 4.7µH to 40µH inductor able to handle a peak current of 150mA is connected from this pin to V_{IN}. The boost converter can be disabled by floating this pin. This allows the use of an external boosted supply from a second LTC3026 or other source. See Operating with Boost Converter Disabled section for more information.

BST (Pin 5): Boost Output Voltage Pin. With boost converter enabled bypass the BST pin with a ≥4.7µF low ESR ceramic capacitor to GND (C_{BST}). BST does not load V_{IN} when in shutdown, but is diode connected to IN through the external inductor, thus, will not go to ground with V_{IN} present. Users should not present any loads to the BST pin (with boost enabled) until PG signals that regulation has been achieved. When providing an external BST voltage (i.e. boost converter disabled) a 1µF low ESR ceramic capacitor can be used.

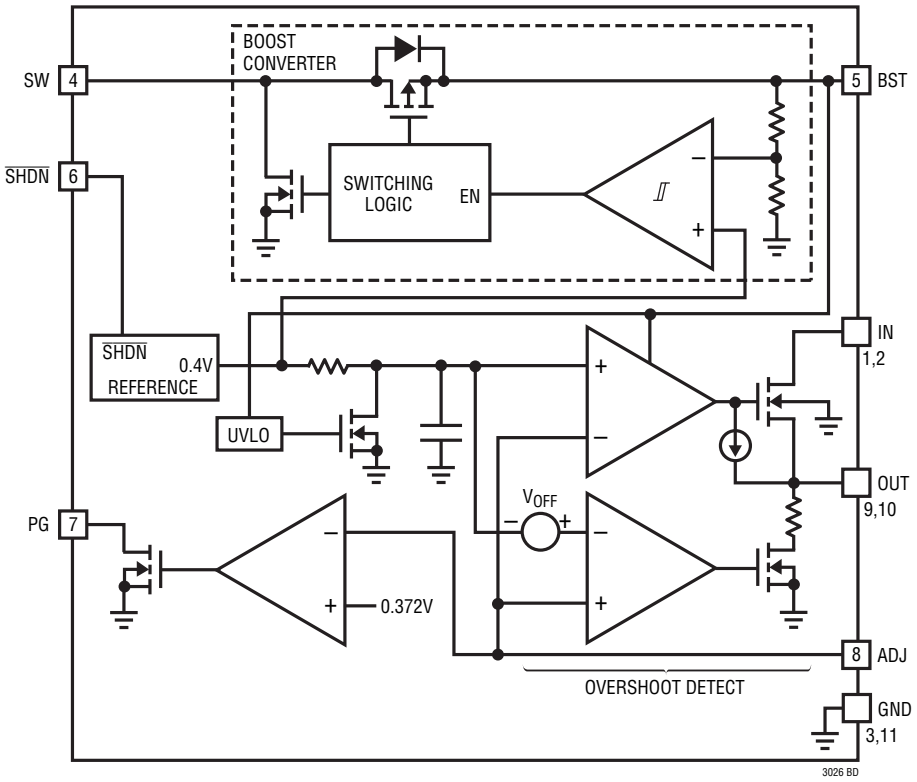
$\overline{\text{SHDN}}$ (Pin 6): Shutdown Input Pin, Active Low. This pin is used to put the LTC3026 into shutdown. The $\overline{\text{SHDN}}$ pin current is typically less than 10nA. The $\overline{\text{SHDN}}$ pin cannot be left floating and must be tied to a valid logic level (such as IN) if not used.

PG (Pin 7): Power Good Pin. When PG is high impedance OUT is in regulation, and low impedance when OUT is in shutdown or out of regulation.

ADJ (Pin 8): Output Adjust Pin. This is the input to the error amplifier. It has a typical bias current of 0.1nA flowing into the pin. The ADJ pin reference voltage is 0.4V referenced to ground. The output voltage range is 0.4V to 2.6V and is typically set by connecting ADJ to a resistor divider from OUT to GND. See Figure 2.

OUT (Pins 9, 10): Regulated Output Voltage. The OUT pins supply power to the load. A minimum output capacitance of 5µF is required to ensure stability. Larger output capacitors may be required for applications with large transient loads to limit peak voltage transients. See the Applications Information section for more information on output capacitance.

BLOCK DIAGRAM



OPERATION

The LTC3026 is a VLDO (very low dropout) linear regulator which operates from input voltages as low as 1.14V. The LDO uses an internal NMOS transistor as the pass device in a source-follower configuration. The BST pin provides the higher supply necessary for the LDO circuitry while the output current comes directly from the IN input for high efficiency regulation. The BST pin can either be supplied off-chip by an external 5V source or it can be generated through the internal boost converter of the LTC3026.

Boost Converter Operation

For applications where an external 5V supply is not available, the LTC3026 contains an internal boost converter to produce the necessary 5V supply for the LDO. The boost converter utilizes Burst Mode® operation to achieve high efficiency for the relatively low current levels needed for the LDO circuitry. The boost converter requires only a small chip inductor between the IN and SW pins and a small 4.7µF capacitor at BST.

The operation of the boost converter is described as follows. During the first half of the switching cycle, an internal NMOS switch between SW and GND turns on, ramping the inductor current. A peak comparator senses when the inductor current reaches 100mA, at which point the NMOS is turned off and an internal PMOS between SW and BST turns on, transferring the inductor current to the BST pin. The PMOS switch continues to deliver power to BST until the inductor current approaches zero, at which point the PMOS turns off and the NMOS turns back on, repeating the switching cycle.

A burst comparator with hysteresis monitors the voltage on the BST pin. When BST is above the upper threshold of the comparator, no switching occurs. When BST falls below the comparator's lower threshold, switching commences and the BST pin gets charged. The upper and lower thresholds of the burst comparator are set to maintain a 5V supply at BST with approximately 40mV to 50mV of ripple.

Care must be taken not to short the BST pin to GND, since the body diode of the internal PMOS transistor connects the BST and SW pins. Shorting BST to GND with an inductor connected between IN and SW can ramp the inductor current to destructive levels, potentially destroying the inductor and/or the part.

Operating with Boost Converter Disabled

The LTC3026 has an option to disable the internal boost converter. With the boost converter disabled, the LTC3026 becomes a bootstrapped device and the BST pin must be driven by an external 5V supply, or driven by the BST pin of a second LTC3026 with the boost converter enabled. The recommended method for disabling the boost converter is to simply float the SW pin. With the SW pin floating no energy can be transferred to BST which effectively disables the boost converter.

A single LTC3026 boost converter can be used to drive multiple bootstrapped LTC3026s with the internal boost converters disabled. Thus a single inductor can be used to power two (or possibly more) functioning LTC3026s. In cases where all LTC3026s have the same input supply (IN) the internal boost converters of the bootstrapped LTC3026s can be disabled by floating the SW pin. If the LTC3026s are not all connected to the same input supply then the internal boost converters of the bootstrapped LTC3026s are disabled by floating the SW pin.

LDO Operation

An undervoltage lockout comparator (UVLO) senses the BST pin voltage to ensure that the bias supply for the LDO is greater than 4.2V before enabling the LDO. If BST is below 4.2V, the UVLO shuts down the LDO, and OUT is pulled to GND through the external divider.

OPERATION

The LDO provides a high accuracy output capable of supplying 1.5A of output current with a typical dropout voltage of only 100mV. A single ceramic capacitor as small as 10µF is all that is required for output bypassing. A low reference voltage allows the LTC3026 output to be programmed to much lower voltages than available in common LDOs (range of 0.4V to 2.6V).

The devices also include current limit and thermal overload protection, and will survive an output short-circuit indefinitely. The fast transient response of the follower output stage overcomes the traditional trade-off between dropout voltage, quiescent current and load transient response inherent in most LDO regulator architectures, see Figure 1.

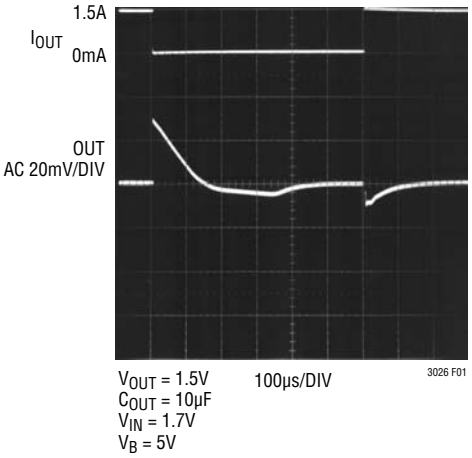


Figure 1. Output Load Step Response

The LTC3026 also includes a soft-start feature to prevent excessive current flow at V_{IN} during start-up. When the LDO is enabled, the soft-start circuitry gradually increases the LDO reference voltage from 0V to 0.4V over a period of approximately 200µs, see Figure 2.

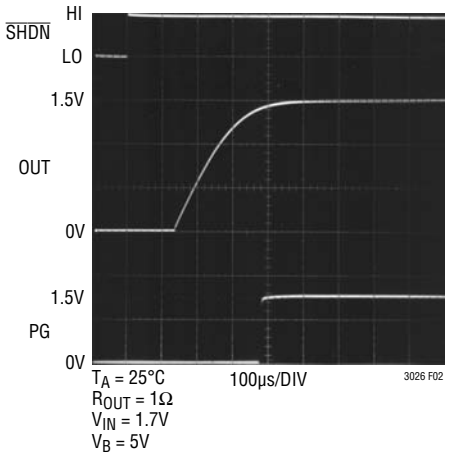


Figure 2. Soft-Start with Boost Disable

Adjustable Output Voltage

The output voltage is set by the ratio of two external resistors as shown in Figure 3. The device servos the output to maintain the ADJ pin voltage at 0.4V (referenced to ground). Thus, the current in R1 is equal to 0.4V/R1. For good transient response, stability and accuracy the current in R1 should be at least 80µA, thus, the value of R1 should be no greater than 5k. The current in R2 is the current in R1 plus the ADJ pin bias current. Since the ADJ pin bias current is typically <10nA it can be ignored in the output voltage calculation. The output voltage can be calculated using the formula in Figure 3. Note that in shutdown the output is turned off and the divider current will be zero once C_{OUT} is discharged.

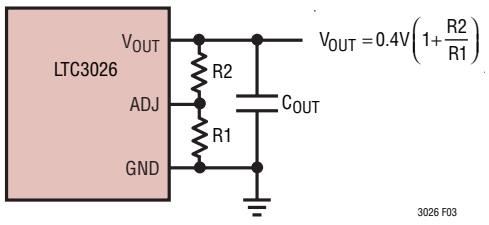


Figure 3. Programming the LTC3026

OPERATION

The LTC3026 operates at a relatively high gain of 270µV/A referred to the ADJ input. Thus, a load current change of 1mA to 1.5A produces a 400µV drop at the ADJ input. To calculate the change in the output, simply multiply by the gain of the feedback network (i.e. 1 + R2/R1). For example, to program the output for 1.2V choose R2/R1 = 2. In this example an output current change of 1mA to 1.5A produces –400µV • (1 + 2) = 1.2mV drop at the output.

Power Good Operation

The LTC3026 includes an open-drain power good (PG) output pin with hysteresis. If the chip is in shutdown or under UVLO conditions (V_{BST} < 4.25V), PG is low impedance to ground. PG becomes high impedance when V_{OUT} rises to 93% of its regulation voltage. PG stays high impedance until V_{OUT} falls back down to 91% of its regulation value. A pull-up resistor can be inserted between PG and a positive logic supply (such as IN, OUT, BST, etc.) to signal a valid power good condition. V_{IN} should be the minimum operating voltage (1.14V) or greater for PG to function correctly.

Output Capacitance and Transient Response

The LTC3026 is designed to be stable with a wide range of ceramic output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. An output capacitor of 10µF or greater with an ESR of 0.05Ω or less is recommended to ensure stability.

The LTC3026 is a micropower device and output transient response will be a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Note that bypass capacitors used to decouple individual components powered by the LTC3026 will increase the effective output capacitor value. High ESR tantalum and electrolytic capacitors may be used, but a low ESR ceramic capacitor must be in parallel at the output. There is no minimum ESR or maximum capacitor size requirements.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients as shown in Figures 4 and 5. When used with a 2V regulator, a 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

A minimum capacitance of 5µF must be maintained at all times on the LTC3026 LDO output.

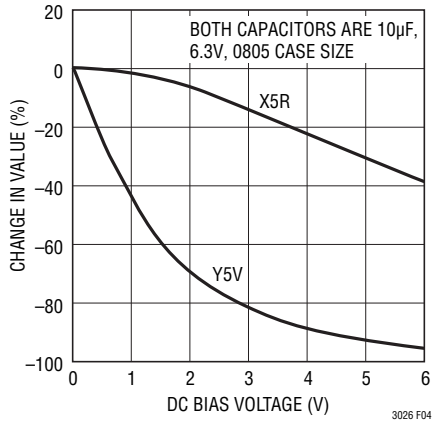


Figure 4. Ceramic Capacitor DC Bias Characteristics

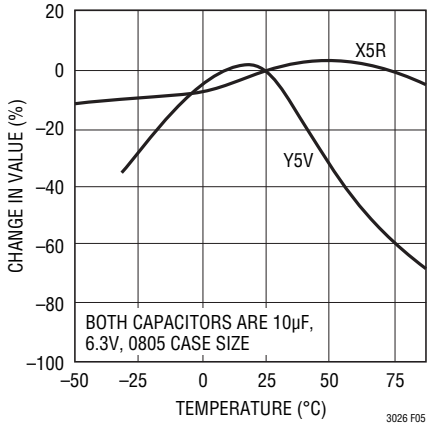


Figure 5. Ceramic Capacitor Temperature Characteristics

OPERATION

Boost Converter Component Selection

A 10µH chip inductor with a peak saturation current (I_{SAT}) of at least 150mA is recommended for use with the internal boost converter. The inductor value can range between 4.7µH to 40µH, but values less than 10µH result in higher switching frequency, increased switching losses, and lower max output current available at the BST pin. See Table 1 for a list of component suppliers.

Table 1. Inductor Vendor Information

SUPPLIER	PART NUMBER	WEBSITE
Coilcraft	0603PS-103KB	www.coilcraft.com
Murata	LQH2MCN100K02	www.murata.com
Taiyo Yuden	LB2016T100M	www.t-yuden.com
TDK	NLC252018T-100K	www.TDK.com

It is also recommended that the BST pin be bypassed to ground with a 4.7µF or greater ceramic capacitor. Larger values of capacitance will not reduce the size of the BST ripple much, but will decrease the ripple frequency proportionally. The BST pin should maintain 1µF of capacitance at all times to ensure correct operation (See the "Output Capacitance and Transient Response" section about capacitor selection). High ESR tantalum and electrolytic capacitors may be used, but a low ESR ceramic must be used in parallel for correct operation.

Thermal Considerations

The power handling capability of the device will be limited by the maximum rated junction temperature (125°C). The majority of the power dissipated in the device will be the output current multiplied by the input/output voltage differential: $(I_{OUT})(V_{IN} – V_{OUT})$. Note that the BST current is less than 200µA even under heavy loads, so its power consumption can be ignored for thermal calculations.

The LTC3026 has internal thermal limiting designed to protect the device during momentary overload conditions. For continuous normal conditions, the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface mount devices, heat sinking is accomplished by using the heat-spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through holes can also be used to spread the heat generated by power devices.

A junction-to-ambient thermal coefficient of 40°C/W is achieved by connecting the exposed pad of the MSOP or DFN package directly to a ground plane of about 2500mm^2.

Calculating Junction Temperature

Example: Given an output voltage of 1.2V, an input voltage of 1.8V ±4%, an output current range of 0mA to 1A and a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

The power dissipated by the device will be approximately:

$$I_{OUT(MAX)}(V_{IN(MAX)} – V_{OUT})$$

where:

$I_{OUT(MAX)}$ = 1A
$V_{IN(MAX)}$ = 1.87V

so:

$$P = 1A(1.87V – 1.2V) = 0.67W$$

Even under worst-case conditions LTC3026's BST pin power dissipation is only about 1mW, thus can be ignored. The junction to ambient thermal resistance will be on the order of 40°C/W. The junction temperature rise above ambient will be approximately equal to:

$$0.67W(40°C/W) = 26.8°C$$

The maximum junction temperature will then be equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$$T_A = 26.8°C + 50°C = 76.8°C$$

Short-Circuit/Thermal Protection

The LTC3026 has built-in output short-circuit current limiting as well as overtemperature protection. During short-circuit conditions, internal circuitry automatically limits the output current to approximately 3A. At higher

OPERATION

temperatures, or in cases where internal power dissipation cause excessive self heating on-chip, the thermal shutdown circuitry will shut down the boost converter and LDO when the junction temperature exceeds approximately 150°C. It will reenable the converter and LDO once the junction temperature drops back to approximately 140°C. The LTC3026 will cycle in and out of thermal shutdown without latchup or damage until the overstress condition is removed. Long term overstress (T_J > 125°C) should be avoided as it can degrade the performance or shorten the life of the part.

Reverse Input Current Protection

The LTC3026 features reverse input current protection to limit current draw from any supplementary power source at the output. Figure 6 shows the reverse output current limit for constant input and output voltages cases. Note: Positive input current represents current flowing into the V_{IN} pin of LTC3026.

With V_{OUT} held at or below the output regulation voltage and V_{IN} varied, IN current flow will follow Figure 6's curves. I_{IN} reverse current ramps up to about 16µA as the V_{IN} approaches V_{OUT}. Reverse input current will spike up as V_{IN} approaches within about 30mV of V_{OUT} as the reverse current protection circuitry is disabled and normal operation resumes. As V_{IN} transitions above V_{OUT} the reverse current transitions into short-circuit current as long as V_{OUT} is held below the regulation voltage.

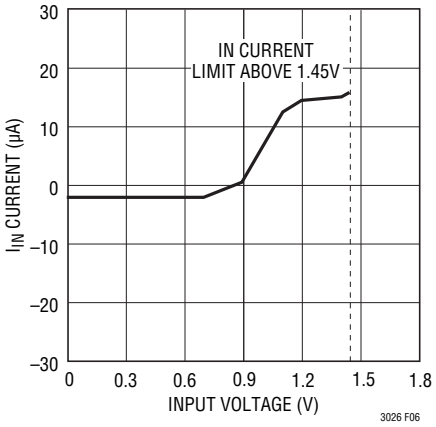


Figure 6. Input Current vs Input Voltage

Layout Considerations

Connection from BST and OUT pins to their respective ceramic bypass capacitor should be kept as short as possible. The ground side of the bypass capacitors should be connected directly to the ground plane for best results or through short traces back to the GND pin of the part. Long traces will increase the effective series ESR and inductance of the capacitor which can degrade performance.

With the boost converter enabled, the SW pin will be switching between ground and 5V whenever the BST pin needs to be recharged. The transition edge rates of the SW pin can be quite fast (~10ns). Thus care must be taken to make sure the SW node does not couple capacitively to other nodes (especially the ADJ pin). Additionally, stray capacitance to this node reduces the efficiency and amount of current available from the boost converter. For these reasons it is recommended that the SW pin be connected to the switching inductor with as short a trace as possible. If the user has any sensitive nodes near the SW node, a ground shield may be placed between the two nodes to reduce coupling.

Because the ADJ pin is relatively high impedance (depending on the resistor divider used), stray capacitance at this pin should be minimized (<10pF) to prevent phase shift in the error amplifier loop. Additionally special attention should be given to any stray capacitances that can couple external signals onto the ADJ pin producing undesirable output ripple. For optimum performance connect the ADJ pin to R1 and R2 with a short PCB trace and minimize all other stray capacitance to the ADJ pin.

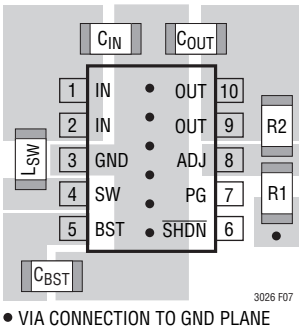
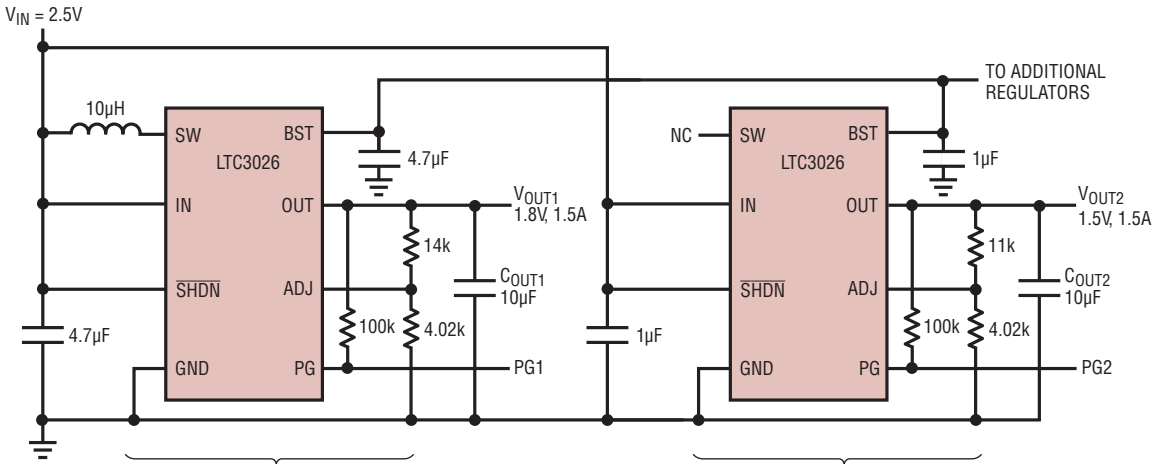


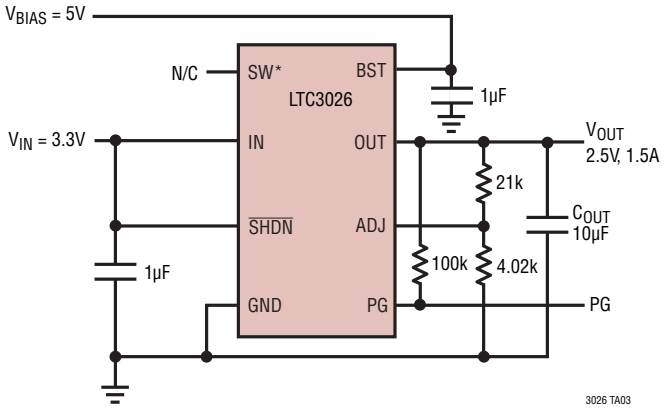
Figure 7. Suggested Layout

TYPICAL APPLICATIONS

Using 1 Boost with Multiple Regulators



2.5V Output from 3.3V Supply with External 5V Bias

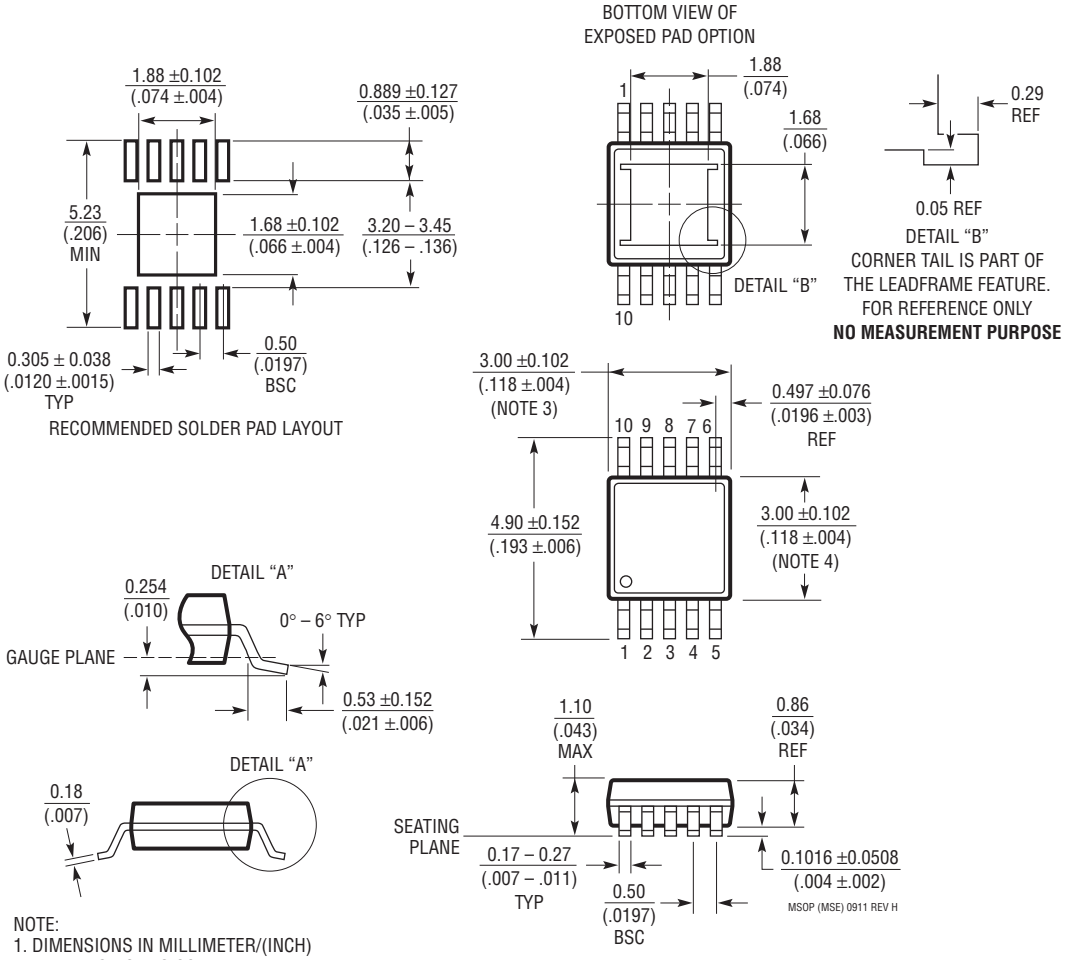


* SEE OPERATING WITH BOOST CONVERTER DISABLED SECTION FOR INFORMATION ON DISABLING BOOST CONVERTER.

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev H)

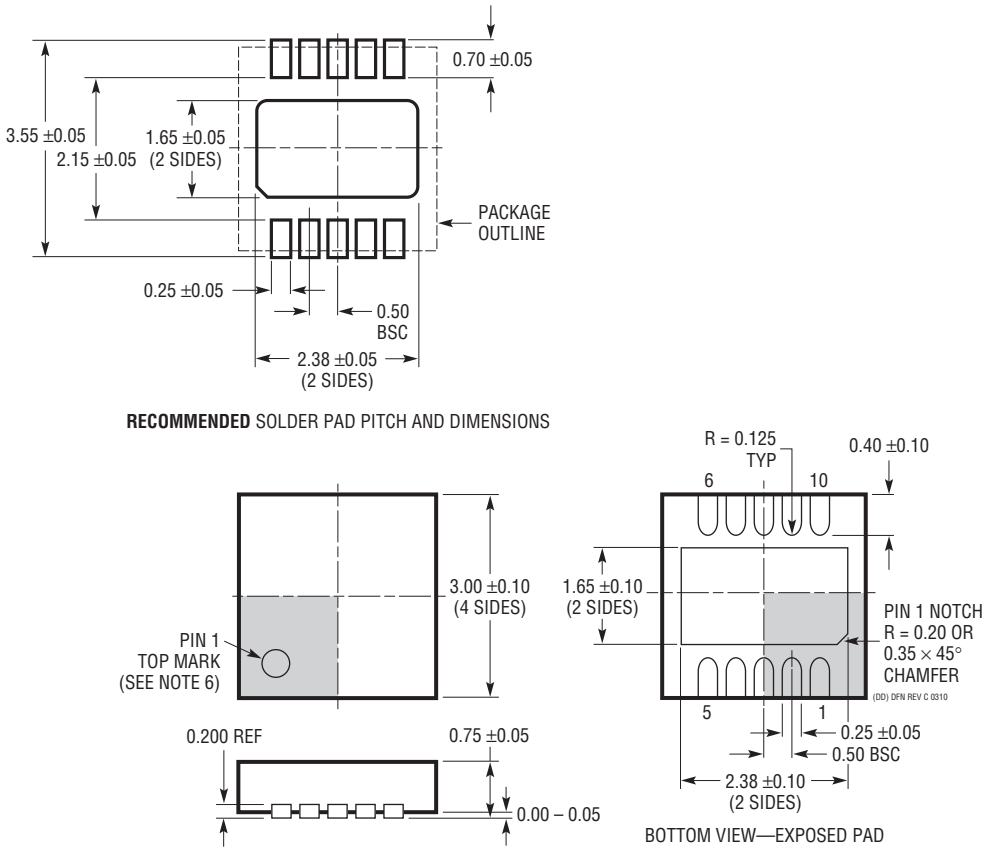


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



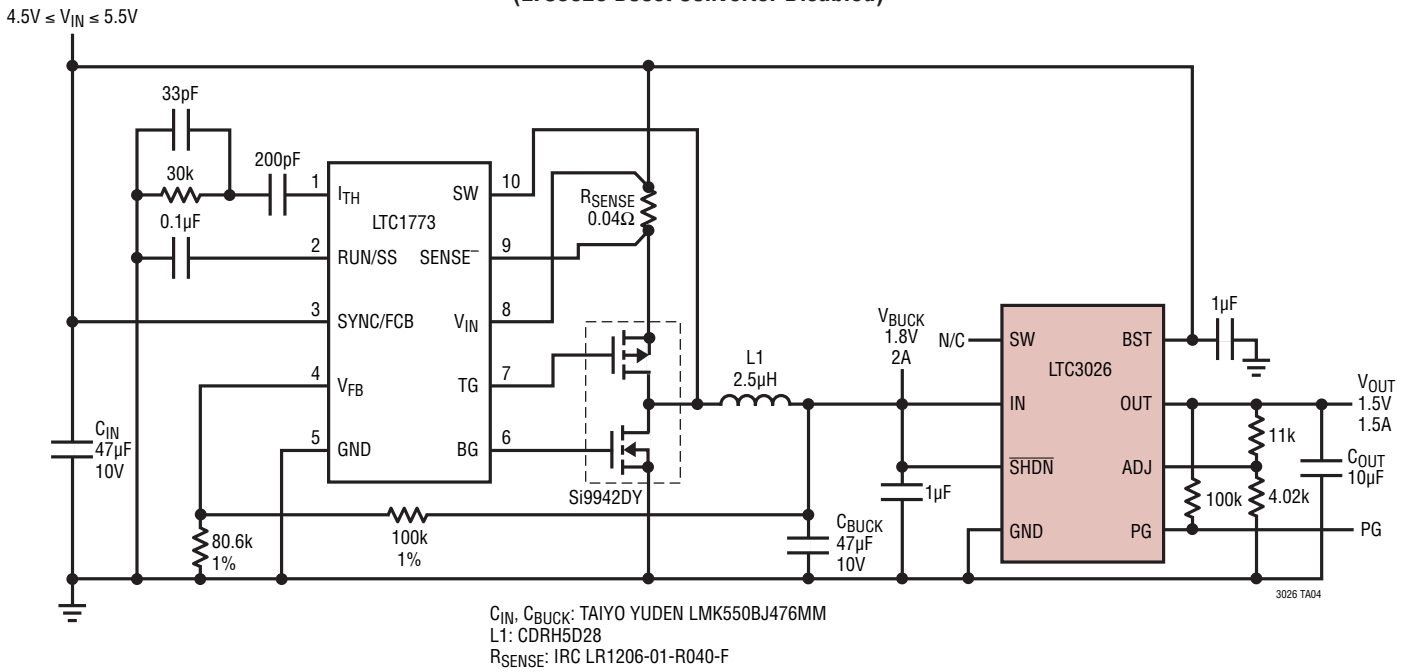
NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	3/10	Addition to Absolute Maximum Ratings	1
		Changes to Electrical Characteristics	3, 4
		Changes to Pin Functions	7,
		Changes to Operation Section	9
		Changes to Typical Applications	14, 18
		Additions to Related Parts	18
E	5/11	Remove I-grade in Note 8.	4
F	8/12	Added I-grade ordering information	2
		Updated I-grade testing assurances, Note 8	4
		Modified boost converter disablement methodology	7, 9
		Modified Boost with Multiple Regulators schematic and deleted note	14

TYPICAL APPLICATION

Efficient, Low Noise 1.5V Output from 1.8V DC/DC Buck Converter
(LTC3026 Boost Converter Disabled)



C_{IN}, C_{BUCK}: TAIYO YUDEN LMK550BJ476MM
L1: CDRH5D28
R_{SENSE}: IRC LR1206-01-R040-F

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1761	100mA, Low Noise LDO in ThinSOT™	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, ThinSOT Package
LT1762	150mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, MS8 Package
LT1763	500mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, SO-8 Package
LT1764A	3A, Fast Transient Response, Low Noise LDO	340mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN} = 2.7V to 20V, TO-220 and DD Packages
LT1844	150mA, Very Low Dropout LDO	80mV Dropout Voltage, Low Noise <30µV_{RMS}, V_{IN} = 1.6V to 6.5V, Stable with 1µF Output Capacitors, ThinSOT Package
LT1962	300mA, Low Noise LDO	270mV Dropout Voltage, Low Noise 20µV_{RMS}, V_{IN} = 1.8V to 20V, MS8 Package
LT1963A	1.5A Low Noise, Fast Transient Response LDO	340mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN} = 2.5V to 20V, TO-220, DD, SOT-223 and SO-8 Packages
LT1964	200mA, Low Noise, Negative LDO	340mV Dropout Voltage, Low Noise 30µV_{RMS}, V_{IN} = –1.8V to –20V, ThinSOT Package
LT1965	1.1A, Low Noise, Low Dropout Linear Regulator	290mV Dropout Voltage, Low Noise 40µV_{RMS}, V_{IN} = 1.8V to 20V, TO-220, DDPak, MSOP and 3mm × 3mm DFN Packages
LTC3025	300mA Micropower VLDO Linear Regulator	45mV Dropout Voltage, Low Noise 80µV_{RMS}, V_{IN} = 0.9V to 5.5V, Low I_Q: 54µA, 2mm × 2mm 6-Lead DFN Package
LT3080/LT3080-1	1.1A, Parallelable, Low Noise, Low Dropout Linear Regulator	300mV Dropout Voltage (2 Supply), Low Noise 40µV_{RMS}, V_{IN} = 1.2V to 36V, V_{OUT} = 0V to 35.7V, Directly Parallelable, TO-220, SOT-223, MSOP-8 and 3mm × 3mm DFN Packages
LT3150	Fast Transient Response, VLDO Regulator Controller	0.035mV Dropout Voltage via External FET, V_{IN} = 1.3V to 10V

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