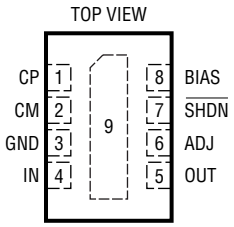
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{IN} to GND ..... –0.3V to 6V
$\overline{SHDN}$ to GND ..... –0.3V to 6V
CP, CM, BIAS to GND ..... –0.3V to 6V
ADJ to GND ..... –0.3V to 6V
V_{OUT} to GND ..... –0.3V to 6V
Operating Junction Temperature
(Note 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C
Output Short Circuit Duration ..... Indefinite

PACKAGE/ORDER INFORMATION



DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 76°C/W
EXPOSED PAD (PIN 9) IS GND,MUST BE SOLDERED TO PCB

ORDER PART NUMBER	DDB PART MARKING
LTC3035EDDB	LBRM

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, V_{OUT} = 3.3V, C_{FLY} = 0.1µF, C_{OUT} = 1µF, C_{IN} = 1µF, C_{BIAS} = 1µF (all capacitors ceramic) unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage (Note 4)		●	1.7		5.5	V
V_{BIAS} Output Voltage Range	2.63V ≤ V_{IN} ≤ 5.5V 1.7V ≤ V_{IN} ≤ 2.63V	● ●	4.8 1.85 • V_{IN}	5 1.90 • V_{IN}	5.3 1.95 • V_{IN}	V V
V_{OUT} Output Voltage Range		●	V_{ADJ}		3.6	V
V_{IN} Operating Current	I_{OUT} = 10µA	●		100	200	µA
V_{IN} Shutdown Current	V_{SHDN} = 0V			1	5	µA
V_{ADJ} Regulation Voltage (Note 5)	1mA ≤ I_{OUT} ≤ 300mA, 1.7V ≤ V_{IN} ≤ 5.5V, V_{OUT} = 1.5V	●	0.392	0.4	0.408	V
I_{ADJ} ADJ Input Current	V_{ADJ} = 0.4V	●	–50	0	50	nA
OUT Load Regulation (Referred to ADJ Pin)	I_{OUT} = 1mA to 300mA			–0.2		mV
Dropout Voltage (Note 6)	V_{IN} = 1.7V, V_{ADJ} = 0.37V, I_{OUT} = 300mA	●		45	100	mV
I_{OUT} Continuous Output Current		●	300			mA
I_{OUT} Short Circuit Output Current	V_{ADJ} = V_{OUT} = 0			760		mA
V_{OUT} Output Noise Voltage	F = 10Hz to 100kHz, I_{OUT} = 150mA			150		µVrms
V_{IH} $\overline{SHDN}$ Input High Voltage		●	1.1			V
V_{IL} $\overline{SHDN}$ Input Low Voltage		●			0.3	V
I_{IH} $\overline{SHDN}$ Input High Current	$\overline{SHDN}$ = V_{IN}		–1		1	µA
I_{IL} $\overline{SHDN}$ Input Low Current	$\overline{SHDN}$ = 0V		–1		1	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: The LTC3035 regulator is tested and specified under pulse load conditions such that $T_J \approx T_A$. The LTC3035 is 100% production tested at 25°C. Performance at –40°C and 125°C is assured by design, characterization and correlation with statistical process control.

Note 4: Min Operating Input Voltage required for regulation is:
$V_{IN} \geq V_{OUT} + V_{DROPOUT}$ and $V_{IN} \geq 1.7V$

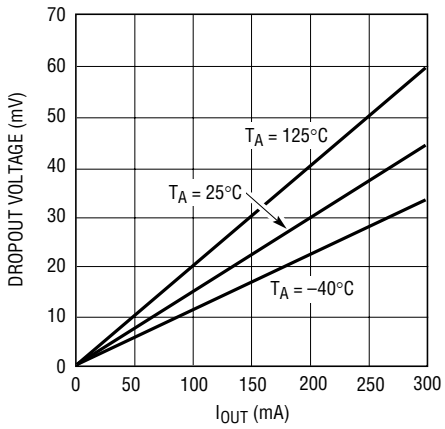
ELECTRICAL CHARACTERISTICS

Note 5: Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited.

Note 6: Dropout voltage is minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to $V_{IN} - V_{DROPOUT}$.

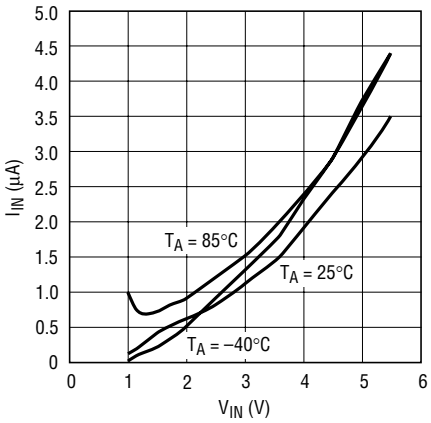
TYPICAL PERFORMANCE CHARACTERISTICS

Dropout Voltage vs Load Current



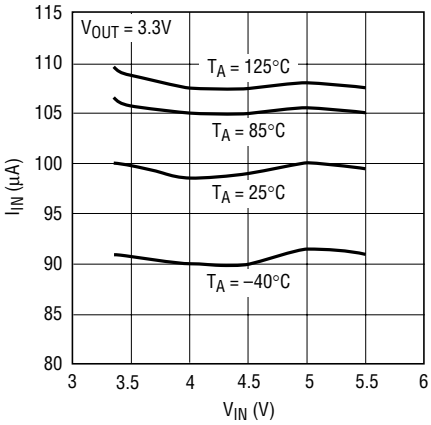
3035 G01

V_{IN} Shutdown Current



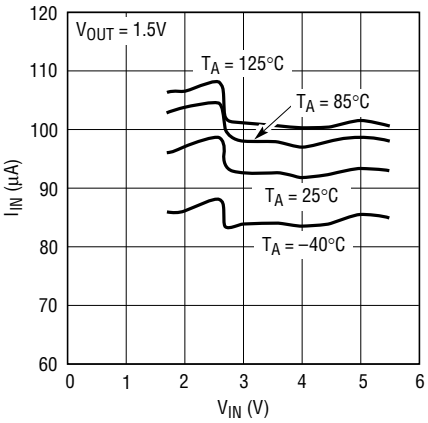
LT1108 • TPC12

V_{IN} No Load Operating Current



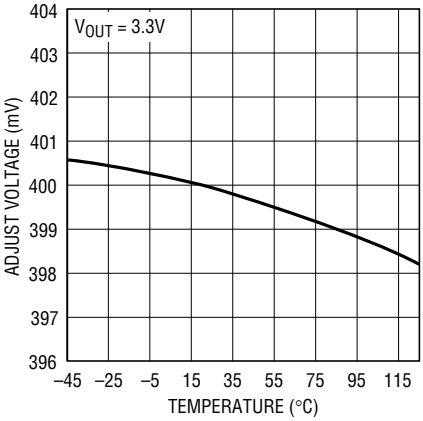
3035 G03

V_{IN} No Load Operating Current



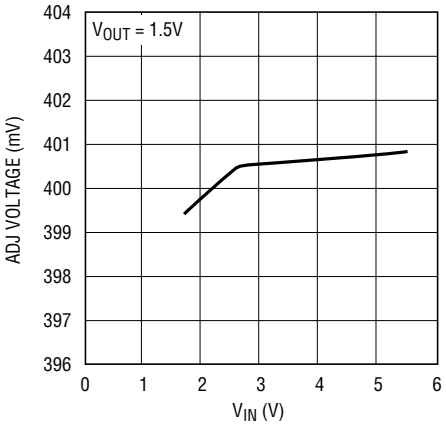
3035 G04

ADJ Voltage vs Temperature



3035 G05

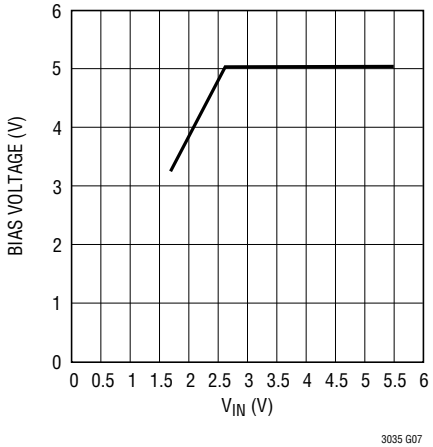
ADJ Voltage vs Input Voltage



3035 G06

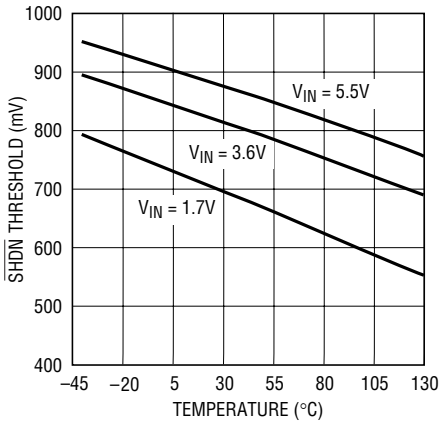
TYPICAL PERFORMANCE CHARACTERISTICS

BIAS Voltage vs Input Voltage



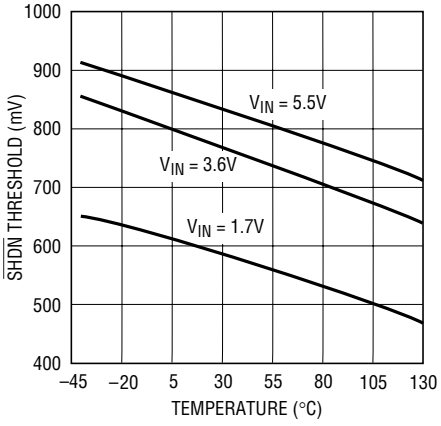
3035 G07

$\overline{SHDN}$ Threshold (Rising) vs Temperature



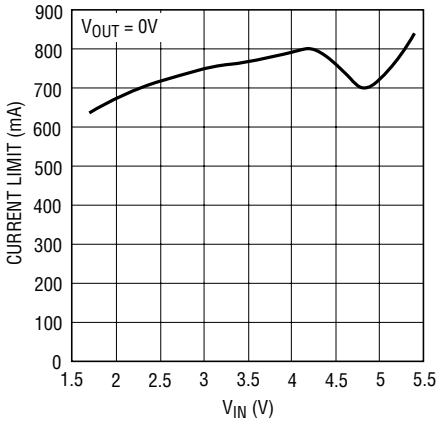
3035 G08

$\overline{SHDN}$ Threshold (Falling) vs Temperature



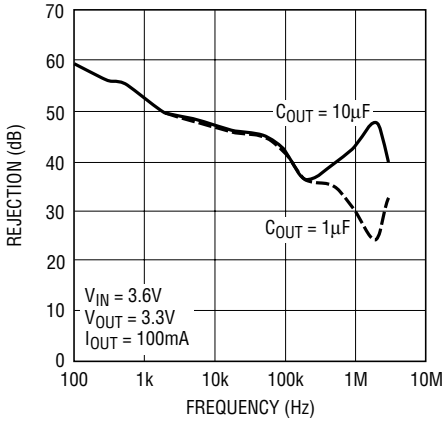
3035 G09

Current Limit vs Input Voltage



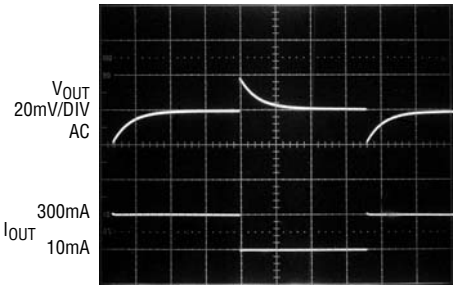
3035 G10

V_{IN} Ripple Rejection vs Frequency



3035 G13

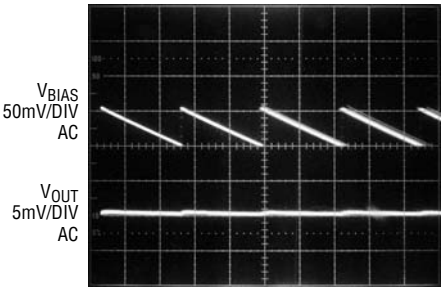
Transient Response



V_{IN} = 3.6V 200µs/DIV
V_{OUT} = 3.3V
C_{OUT} = 1µF

3035 G11

BIAS Output Ripple



V_{IN} = 3.6V 500µs/DIV
V_{OUT} = 3.3V
C_{BST} = 1µF
C_{FLY} = 0.1µF
C_{OUT} = 1µF
I_{OUT} = 1mA

3035 G12

PIN FUNCTIONS

CP (Pin 1): Flying Capacitor Positive Terminal.

CM (Pin 2): Flying Capacitor Negative Terminal.

GND (Pin 3): Ground. Connect to a ground plane.

IN (Pin 4): Input Supply Voltage. The output load current is supplied directly from IN. The IN pin should be locally bypassed to ground if the LTC3035 is more than a few inches away from another source of bulk capacitance. In general, the output impedance of a battery rises with frequency, so it is usually adviseable to include an input bypass capacitor when supplying IN from a battery. A capacitor of 1µF is usually sufficient.

OUT (Pin 5): Regulated Output Voltage. The OUT pin supplies power to the load. A minimum ceramic output capacitor of at least 1µF is required to ensure stability. Larger output capacitors may be required for applications with large transient loads to limit peak voltage transients. See the Applications Information section for more information on output capacitance.

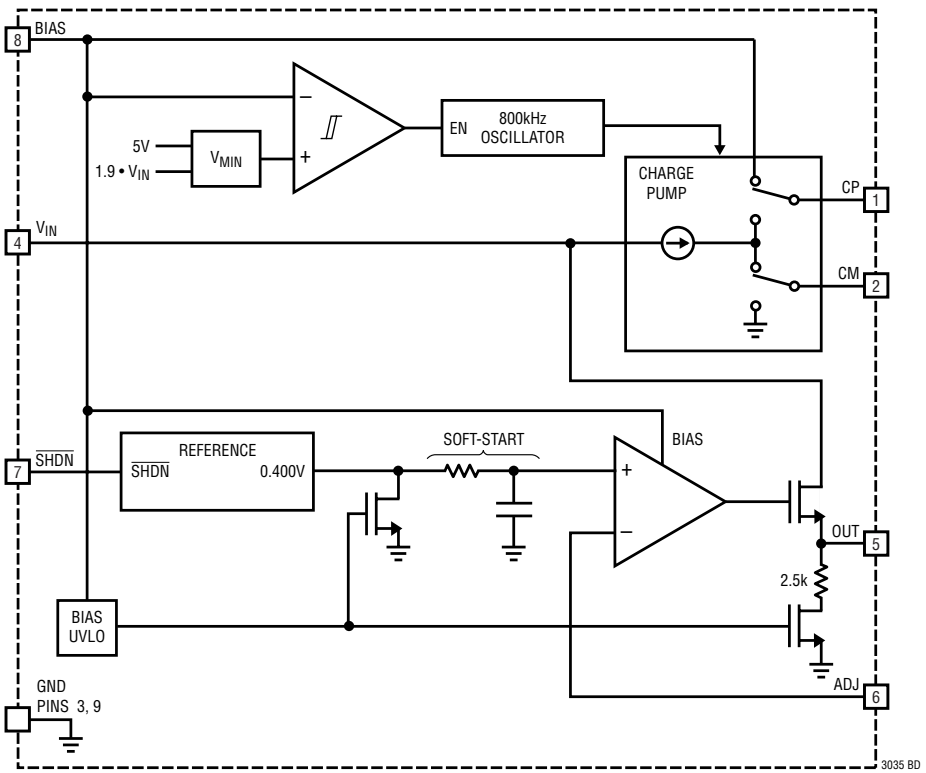
ADJ (Pin 6): Adjust Input Pin. This is the input to the error amplifier. The ADJ pin reference voltage is 0.4V referenced to ground. The output voltage range is 0.4V to 3.6V and is set by connecting ADJ to a resistor divider from OUT to GND.

$\overline{\text{SHDN}}$ (Pin 7): Shutdown Input, Active Low. This pin is used to put the LTC3035 into shutdown. The $\overline{\text{SHDN}}$ pin current is typically less than 10nA. The $\overline{\text{SHDN}}$ pin cannot be left floating and must be tied to a valid logic level if not used.

BIAS (Pin 8): BIAS Output Voltage Pin. BIAS is the output of the charge pump and provides the high side supply for the LTC3035 LDO circuitry. This pin should be locally bypassed to ground by a 1µF or greater capacitor as close as possible to the pin. Nothing else should be connected to this pin.

Exposed Pad (Pin 9): Ground and Heat Sink. Must be soldered to PCB ground plane or large pad for optimal thermal performance.

BLOCK DIAGRAM



APPLICATIONS INFORMATION (Refer to Block Diagram)

The LTC3035 is a VLDO (very low dropout) linear regulator which operates from input voltages between 1.7V and 5.5V. The LDO uses an internal NMOS transistor as the pass device in a source-follower configuration. The internal charge pump generator provides the high supply necessary for the LDO circuitry while the output current comes directly from the IN input for high efficiency regulation.

Charge Pump Operation

The LTC3035 contains a charge pump to produce the necessary bias voltage supply for the LDO. The charge pump utilizes Burst Mode operation to achieve high efficiency for the relatively low current levels needed for the LDO circuitry. The charge pump requires only a small 0.1µF flying capacitor between the CP and CM pins and a 1µF bypass capacitor at BIAS.

An internal oscillator centered at 800kHz controls the two-phase switching cycle of the charge pump. During the first phase a current source charges the flying capacitor between V_{IN} and GND. During the second phase, the capacitor's positive terminal connects to BIAS and the current source drives the capacitor's minus terminal, delivering charge to the BIAS bypass capacitor and increasing its voltage.

A burst comparator with hysteresis monitors the voltage on the BIAS pin. When BIAS is above the upper threshold of the comparator, the oscillator is disabled and no switching occurs. When BIAS falls below the comparator's lower threshold, the oscillator is enabled and the BIAS pin gets charged. The thresholds of the burst comparator are dynamically adjusted to maintain a DC level shown by Figure 1. BIAS regulates to 1.9 • V_{IN} or 5V, whichever voltage is lower. The voltage ripple at BIAS is controlled to approximately 1% of its DC value.

LDO Operation

An undervoltage lockout comparator (UVLO) senses the BIAS voltage to ensure that the BIAS supply for the LDO is greater than 90% of its regulation value before enabling the LDO. Once the LDO gets enabled, the UVLO threshold switches to 50% of its regulation value. Thus the BIAS voltage must fall below 50% of its regulation voltage

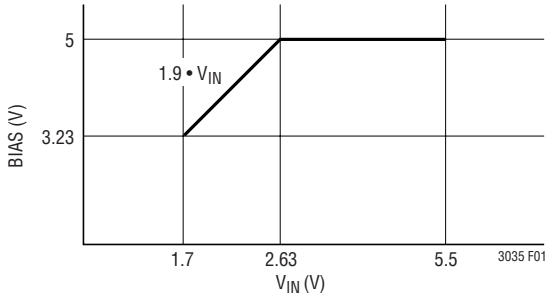


Figure 1. LTC3035 BIAS Voltage vs V_{IN} Voltage

before the LDO disables. When the LDO is disabled, OUT is pulled to GND through the external divider and an internal 2.5k resistor.

The LDO provides a high accuracy output capable of supplying 300mA of output current with a typical dropout voltage of only 45mV. A single ceramic capacitor as small as 1µF is all that is required for output bypassing. The low reference voltage allows the LTC3035 output to be programmed from 0.4V to 3.6V.

As shown in the Block Diagram, the charge pump output at BIAS supplies the LDO circuitry while the output current comes directly from the IN input for high efficiency regulation. The low quiescent supply current, I_{IN} = 100µA, drops to I_{IN} = 1µA typical in shutdown making the LTC3035 an ideal choice for use in battery-powered systems.

The device also includes current limit, thermal overload protection, and reverse output current protection. The fast transient response of the follower output stage overcomes the traditional tradeoff between dropout voltage, quiescent current and load transient response inherent in most LDO regulator architectures. The LTC3035 also includes overshoot detection circuitry which brings the output back into regulation when going from heavy to light output loads (see Figure 2).

The LTC3035 also includes a soft-start feature to prevent excessive current flow during start-up. After the BIAS voltage reaches regulation, the soft-start circuitry gradually increases the LDO reference voltage from 0V to 0.4V over a period of about 600µs. There is a short 700µs delay from the time BIAS reaches regulation until the LDO output starts to rise (see Figure 3).

APPLICATIONS INFORMATION

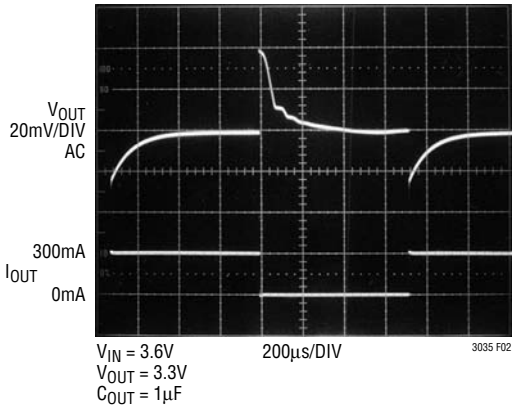


Figure 2. Output Step Response

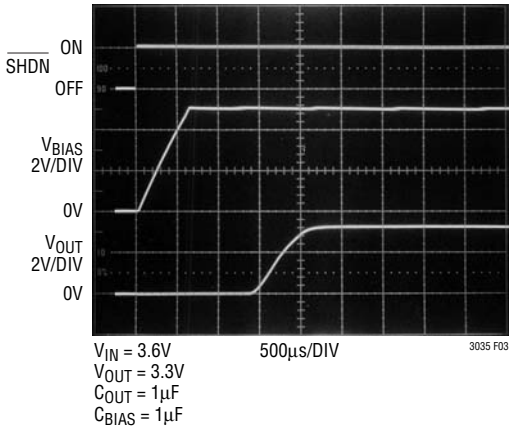


Figure 3. Bias and Output Start-Up Waveforms

Adjustable Output Voltage

The output voltage is set by the ratio of two external resistors as shown in Figure 4. The device servos the output to maintain the ADJ pin voltage at 0.4V (referenced to ground). Thus the current in R1 is equal to 0.4V/R1. For good transient response, stability and accuracy the current in R1 should be at least 8µA, thus the value of R1 should be no greater than 50k. The current in R2 is the current in R1 plus the ADJ pin bias current. Since the ADJ pin bias current is typically <10nA it can be ignored in the output voltage calculation. The output voltage can be calculated using the formula in Figure 4. Note that in shutdown the output is turned off and the divider current will be zero once C_{OUT} is discharged.

The LTC3035 operates at a relatively high gain of –0.7µV/mA referred to the ADJ input. Thus a load

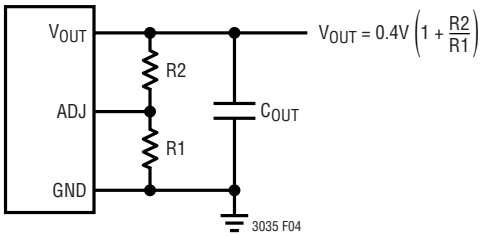


Figure 4. Programming the LTC3035

current change of 1mA to 300mA produces a –0.2mV drop at the ADJ input. To calculate the change refered to the output simply multiply by the gain of the feedback network (i.e., 1 + R2/R1). For example, to program the output for 3.3V choose R2/R1 = 7.25. In this example an output current change of 1mA to 300mA produces –0.2mV • (1 + 7.25) = 1.65mV drop at the output.

Output Capacitance and Transient Response

The LTC3035 is designed to be stable with a wide range of ceramic output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. An output capacitor of 1µF or greater with an ESR of 0.05Ω or less is recommended to ensure stability. The LTC3035 is a micropower device and output transient response will be a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Note that bypass capacitors used to decouple individual components powered by the LTC3035 will increase the effective output capacitor value. High ESR tantalum and electrolytic capacitors may be used, but a low ESR ceramic capacitor must be in parallel at the output. There is no minimum ESR or maximum capacitor size requirements.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients as shown in Figures 5 and 6. When used with a 3.3V regulator, a 1µF Y5V capacitor can lose as much as 80% of its rated capacitance over the operating

APPLICATIONS INFORMATION

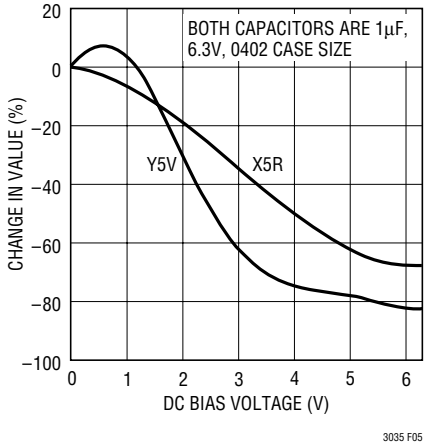


Figure 5. Ceramic Capacitor DC Bias Characteristics

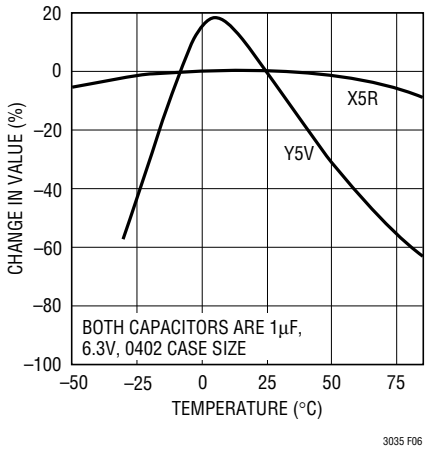


Figure 6. Ceramic Capacitor Temperature Characteristics

temperature range. The X5R only loses about 40% of its rated capacitance over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature and bias voltage, while the X5R is less expensive and is available in higher values. In all cases, the output capacitance should never drop below 0.4µF, or instability or degraded performance may occur.

Charge Pump Component Selection

The flying capacitor controls the strength of the charge pump. In order for the charge pump to deliver its maximum available current, a 0.1µF or greater ceramic capacitor should be used. *Warning: A polarized capacitor such as tantalum or aluminum should never be used for the flying capacitor since its voltage can reverse upon start-up of the LTC3035. Low ESR ceramic capacitors should always be used for the flying capacitor.*

A 1µF or greater low ESR (<0.1Ω) ceramic capacitor is recommended to bypass the BIAS pin. Larger values of capacitance will not reduce the size of the BIAS ripple much, but will decrease the ripple frequency proportionally. The BIAS pin should maintain 0.4µF of capacitance at all times to ensure correct operation. High ESR tantalum and electrolytic capacitors may be used, but a low ESR ceramic must be used in parallel for correct operation. It is also recommended that IN be bypassed to ground with a 1µF or greater ceramic capacitor.

Thermal Considerations

The power handling capability of the device will be limited by the maximum rated junction temperature (125°C). The power dissipated by the device will be the output current multiplied by the input/output voltage differential:

$$(I_{OUT})(V_{IN} – V_{OUT})$$

The LTC3035 has internal thermal limiting designed to protect the device during momentary overload conditions. For continuous normal conditions, the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface mount devices, heat sinking is accomplished by using the heat-spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through holes can also be used to spread the heat generated by power devices.

A junction to ambient thermal coefficient of 76°C/W is achieved by connecting the Exposed Pad of the DFN package directly to a ground plane of about 2500mm^2.

OPERATION

Calculating Junction Temperature

Example: Given an output voltage of 1.5V, an input voltage of 1.8V to 3V, an output current range of 0mA to 100mA and a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

The power dissipated by the device will be approximately:

$I_{OUT(MAX)}(V_{IN(MAX)} - V_{OUT})$

where:

$I_{OUT(MAX)} = 100mA$

$V_{IN(MAX)} = 3V$

so:

$P = 100mA(3V - 1.5V) = 0.15W$

Even under worst-case conditions LTC3035's BIAS pin power dissipation is only about 1mW, thus can be ignored. The junction to ambient thermal resistance will be on the order of 76°C/W. The junction temperature rise above ambient will be approximately equal to:

$0.15W(76°C/W) = 11.4°C$

The maximum junction temperature will then be equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$T = 50°C + 11.4°C = 61.4°C$

Short-Circuit/Thermal Protection

The LTC3035 has built-in output short-circuit current limiting as well as over temperature protection. During short-circuit conditions, internal circuitry automatically limits the output current to approximately 760mA. At higher temperatures, or in cases where internal power dissipation causes excessive self heating on chip, the thermal shutdown circuitry will shut down the charge pump and LDO when the junction temperature exceeds approximately 155°C. It will reenable the converter and LDO once the junction temperature drops back to approximately 140°C. The LTC3035 will cycle in and out of thermal shutdown without latch-up or damage until the overstress condition is removed. Long term overstress (T_J>125°C) should be avoided as it can degrade the performance or shorten the life of the part.

Layout Considerations

Connection from the BIAS and OUT pins to their respective ceramic bypass capacitor should be kept as short as possible. The ground side of the bypass capacitors should be connected directly to the ground plane for best results or through short traces back to the GND pin of the part. Long traces will increase the effective series ESR and inductance of the capacitor which can degrade performance.

The CP and CM pins of the charge pump are switching nodes. The transition edge rates of these pins can be quite fast (~10ns). Thus care must be taken to make sure these nodes do not couple capacitively to other nodes (especially the ADJ pin). Place the flying capacitor as close as possible to the CP and CM pins for optimum charge pump performance.

Because the ADJ pin is relatively high impedance (depending on the resistor divider used), stray capacitance at this pin should be minimized (<10pF) to prevent phase shift in the error amplifier loop. Additional special attention should be given to any stray capacitances that can couple external signals onto the ADJ pin producing undesirable output ripple. For optimum performance connect the ADJ pin to R1 and R2 with a short PCB trace and minimize all other stray capacitance to the ADJ pin. Figure 7 shows an example layout for the LTC3035.

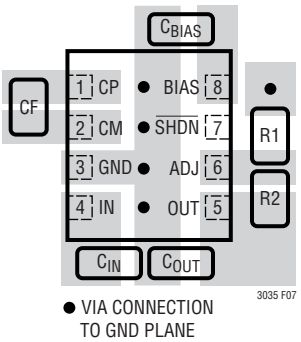
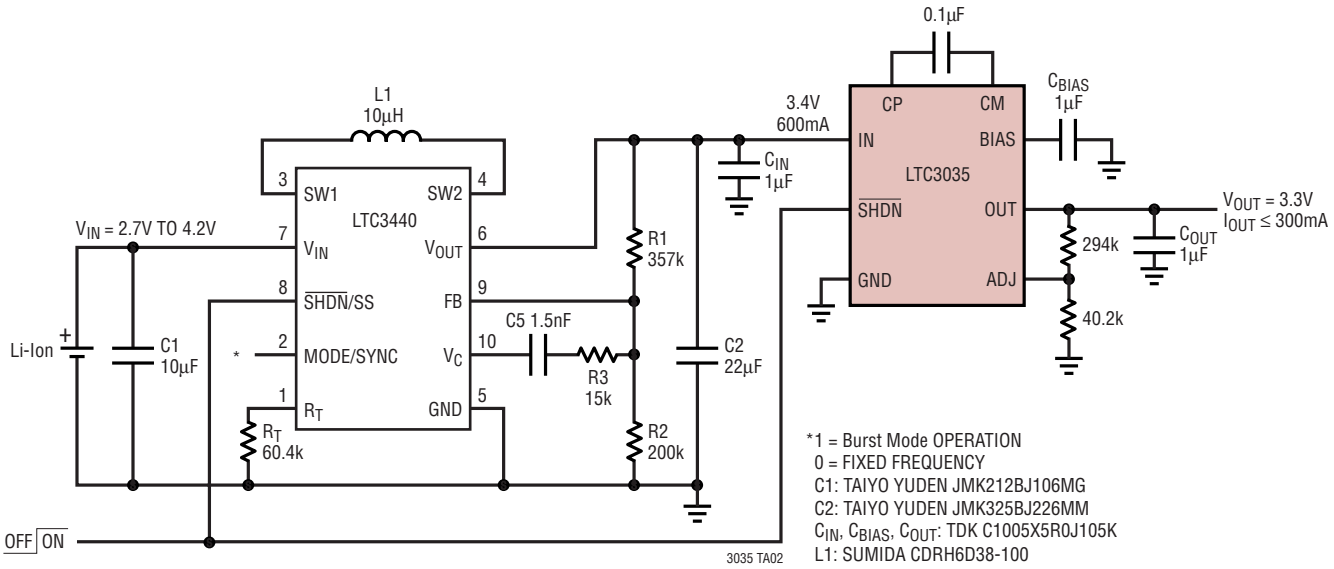


Figure 7. Suggested Layout

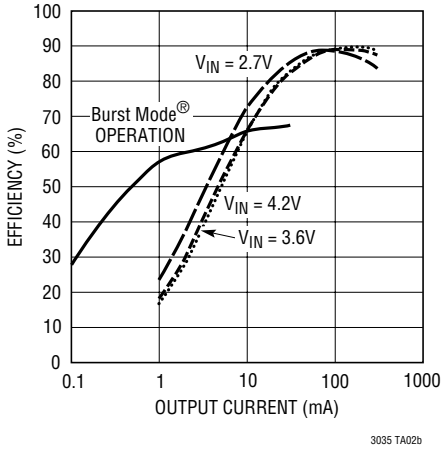
TYPICAL APPLICATION

Low Noise Li-Ion to 3.3V Supply



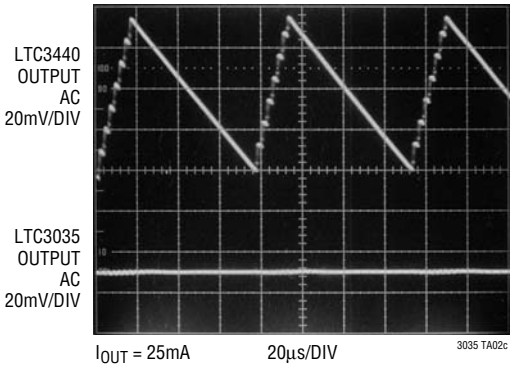
*1 = Burst Mode OPERATION
0 = FIXED FREQUENCY
C1: TAIYO YUDEN JMK212BJ106MG
C2: TAIYO YUDEN JMK325BJ226MM
C_{IN}, C_{BIAS}, C_{OUT}: TDK C1005X5R0J105K
L1: SUMIDA CDRH6D38-100

Efficiency vs Output Current



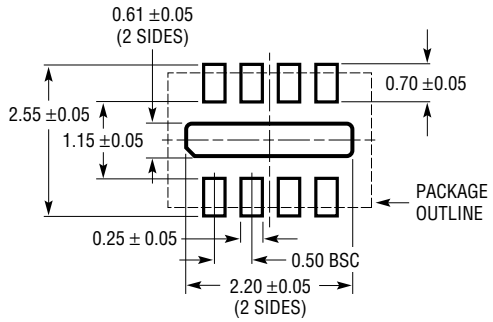
Burst Mode IS A REGISTERED TRADEMARK OF LINEAR TECHNOLOGY CORPORATION

Ripple Rejection

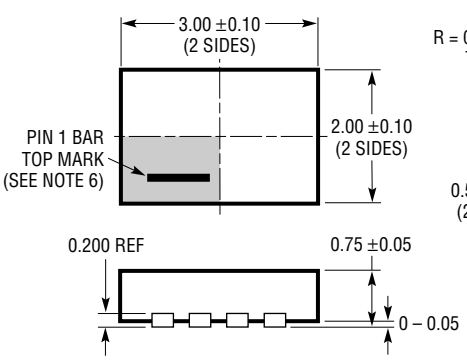


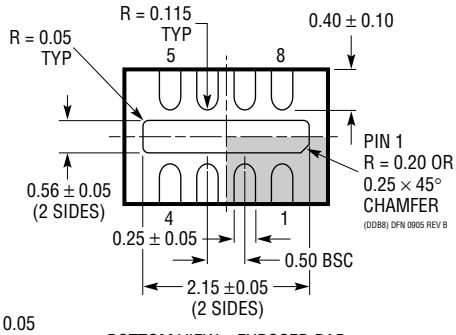
PACKAGE DESCRIPTION

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



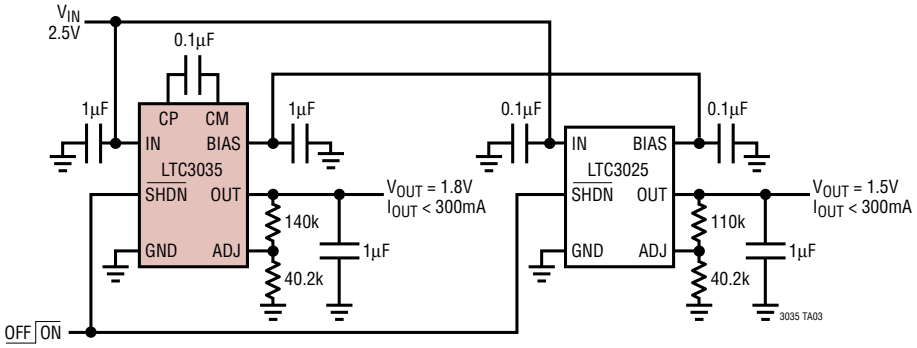


BOTTOM VIEW—EXPOSED PAD

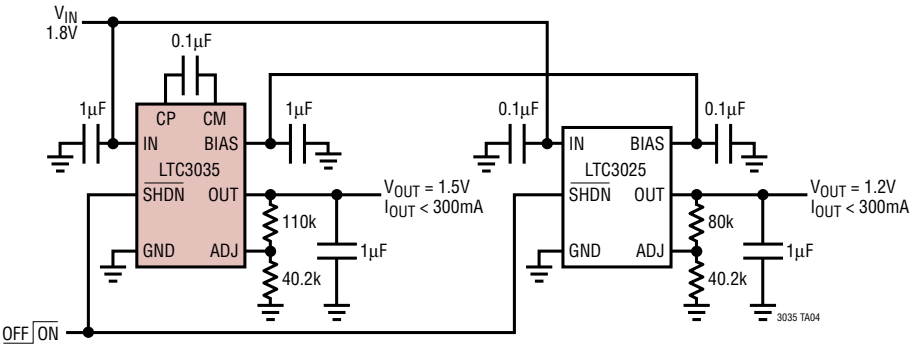
NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATIONS

Dual LDO Output (1.8V, 1.5V) from 2.5V Supply Rail



Dual LDO Output (1.5V, 1.2V) from 1.8V Supply Rail



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1761	100mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 20µA, I_{SD} < 1µA, V_{OUT} = Adj, 1.5V, 1.8V, 2V, 2.5V, 2.8V, 3V, 3.3V, 5V, ThinSOT™ Package. Low Noise < 20µV_{RMSP-P}, Stable with 1µF Ceramic Capacitors
LT1762	150mA, Low Noise Micropower LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 25µA, I_{SD} < 1µA, V_{OUT} = Adj, 2.5V, 3V, 3.3V, 5V, MS8 Package. Low Noise < 20µV_{RMSP-P}
LT1763	500mA, Low Noise Micropower LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 30µA, I_{SD} < 1µA, V_{OUT} = 1.5, 1.8V, 2.5V, 3V, 3.3V, 5V, S8 Package. Low Noise < 20µV_{RMSP-P}
LTC1844	150mA, Very Low Dropout LDO	V_{IN}: 1.6V to 6.5V, $V_{OUT(MIN)}$ = 1.25V, V_{DO} = 0.08V, I_Q = 40µA, I_{SD} < 1µA, V_{OUT} = Adj, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V, ThinSOT Package. Low Noise < 30µV_{RMSP-P}, Stable with 1µF Ceramic Capacitors
LT1962	300mA, Low Noise Micropower LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.27V, I_Q = 30µA, I_{SD} < 1µA, V_{OUT} = 1.5, 1.8V, 2.5V, 3V, 3.3V, 5V, MS8 Package. Low Noise < 20µV_{RMSP-P}
LT3020	100mA, Low Voltage, VLDO	V_{IN}: 0.9V to 10V, $V_{OUT(MIN)}$ = 0.20V, V_{DO} = 0.15V, I_Q = 120µA, I_{SD} < 3µA, V_{OUT} = Adj, DFN, MS8 Package
LTC3025	300mA, Micropower VLDO Linear Regulator	V_{IN}: 0.9V to 5.5V, V_{BIAS}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.4V, V_{DO} = 0.05V, I_Q = 54µA, I_{SD} < 1µA, V_{OUT} = Adj, DFN Package. Stable with 1µF Ceramic Capacitors
LTC3026	1.5A, Low Input Voltage VLDO Linear Regulator	V_{IN}: 1.14V to 3.5V (Boost Enabled), 1.14V to 5.5V (External 5V Boost), $V_{OUT(MIN)}$ = 0.4V, V_{DO} = 0.15V, I_Q = 400µA, I_{SD} < 1µA, V_{OUT} = Adj, DFN, MSOP Packages. Stable with 10µF Ceramic Capacitors

ThinSOT is a trademark of Linear Technology Corporation.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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