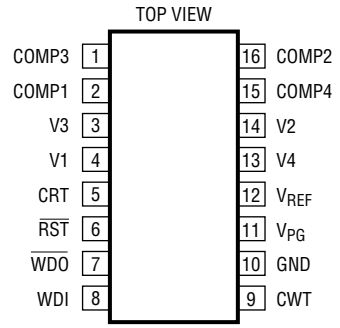
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2, 3)

V1, V2, V3, V4, V_{PG} ..... –0.3V to 7V
$\overline{RST}$ (LTC2901-1/LTC2901-3) ..... –0.3V to 7V
RST (LTC2901-2/LTC2901-4) ..... –0.3V to (V2 + 0.3V)
COMPX ..... –0.3V to 7V
CWT, WDI, $\overline{WDO}$ ..... –0.3V to 7V
V_{REF}, CRT, TOL ..... –0.3V to (V_{CC} + 0.3V)
Reference Load Current (I_{VREF}) ..... ±1mA
V4 Input Current (–ADJ Mode) ..... –1mA

Operating Temperature Range
LTC2901-1C/LTC2901-2C/
LTC2901-3C/LTC2901-4C ..... 0°C to 70°C
LTC2901-1I/LTC2901-2I/
LTC2901-3I/LTC2901-4I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

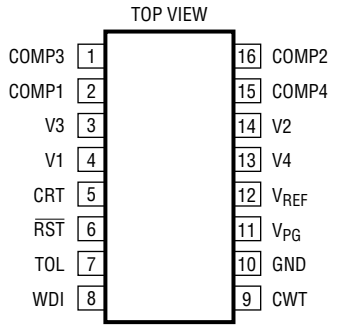
PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC2901-1CGN LTC2901-2CGN LTC2901-1IGN LTC2901-2IGN
GN16 PART MARKING
29011 29012 29011I 29012I



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC2901-3CGN LTC2901-4CGN LTC2901-3IGN LTC2901-4IGN
GN16 PART MARKING
29013 29014 29013I 29014I

Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/ Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, unless otherwise noted. (Notes 3, 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{RT50}	5V, 5% Reset Threshold 5V, 10% Reset Threshold	V1 Input Threshold	● ●	4.600 4.350	4.675 4.425	4.750 4.500	V V
V_{RT33}	3.3V, 5% Reset Threshold 3.3V, 10% Reset Threshold	V1, V2 Input Threshold	● ●	3.036 2.871	3.086 2.921	3.135 2.970	V V
V_{RT30}	3V, 5% Reset Threshold 3V, 10% Reset Threshold	V2 Input Threshold	● ●	2.760 2.610	2.805 2.655	2.850 2.700	V V
V_{RT25}	2.5V, 5% Reset Threshold 2.5V, 10% Reset Threshold	V2, V3 Input Threshold	● ●	2.300 2.175	2.338 2.213	2.375 2.250	V V
V_{RT18}	1.8V, 5% Reset Threshold 1.8V, 10% Reset Threshold	V3, V4 Input Threshold	● ●	1.656 1.566	1.683 1.593	1.710 1.620	V V
V_{RT15}	1.5V, 5% Reset Threshold 1.5V, 10% Reset Threshold	V3, V4 Input Threshold	● ●	1.380 1.305	1.403 1.328	1.425 1.350	V V
V_{RTA}	ADJ, 5% Reset Threshold ADJ, 10% Reset Threshold	V3, V4 Input Threshold	● ●	0.492 0.466	0.500 0.473	0.508 0.481	V V
V_{RTAN}	–ADJ Reset Threshold	V4 Input Threshold	●	–18	0	18	mV
V_{CC}	Minimum Internal Operating Voltage	$\overline{RST}$, COMPX in Correct Logic State; V_{CC} Rising Prior to Program	●			1	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, unless otherwise noted. (Notes 3, 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CCMINP}	Minimum Required for Programming	V_{CC} Rising	●			2.42	V
V_{CCMINC}	Minimum Required for Comparators	V_{CC} Falling	●			2.32	V
V_{REF}	Reference Voltage	$V_{CC} \geq 2.3V$, $I_{VREF} = \pm 1mA$, $C_{REF} \leq 1000pF$					
		TOL Low	●	1.192	1.210	1.228	V
		TOL High	●	1.128	1.146	1.163	V
V_{PG}	Programming Voltage Range	$V_{CC} \geq V_{CCMINP}$	●	0		V_{REF}	V
I_{VPG}	V_{PG} Input Current	$V_{PG} = V_{REF}$	●			±20	nA
I_{V1}	V1 Input Current	V1 = 5V, I_{VREF} = 12µA, (Note 5)	●		43	75	µA
I_{V2}	V2 Input Current	V2 = 3.3V	●		0.8	2	µA
I_{V3}	V3 Input Current	V3 = 2.5V	●		0.52	1.2	µA
		V3 = 0.55V (ADJ Mode)	●	–15		15	nA
I_{V4}	V4 Input Current	V4 = 1.8V	●		0.34	0.8	µA
		V4 = 0.55V (ADJ Mode)	●	–15		15	nA
		V4 = –0.05V (–ADJ Mode)	●	–15		15	nA
$I_{CRT(UP)}$	CRT Pull-Up Current	V_{CRT} = 0V	●	–1.4	–2	–2.6	µA
$I_{CRT(DN)}$	CRT Pull-Down Current	V_{CRT} = 1.3V	●	10	20	30	µA
t_{RST}	Reset Time-Out Period	C_{RT} = 1500pF	●	5	7	9	ms
t_{UV}	V_X Undervoltage Detect to $\overline{RST}$ or COMPX	V_X Less Than Reset Threshold V_{RTX} by More Than 1%			150		µs
V_{OL}	Output Voltage Low $\overline{RST}$, COMPX	I_{SINK} = 2.5mA; V1 = 3V, V2 = 3V; V3, V4 = 0V; V_{PG} = 0V	●		0.15	0.4	V
		I_{SINK} = 100µA; V2 = 1V; V1, V3, V4 = 0V	●		0.05	0.3	V
		I_{SINK} = 100µA; V1 = 1V; V2, V3, V4 = 0V	●		0.05	0.3	V
V_{OH}	Output Voltage High $\overline{RST}$, $\overline{WDO}$, COMPX (Note 6)	I_{SOURCE} = 1µA	●	V2 – 1			V
V_{OL}	Output Voltage Low $\overline{WDO}$	I_{SINK} = 2.5mA; V1 = 5V, V2 = 3.3V; V3, V4 = 1V; V_{PG} = 0V	●		0.15	0.4	V
V_{OH}	Output Voltage High $\overline{RST}$ (LTC2901-2/LTC2901-4) (Note 7)	I_{SOURCE} = 200µA	●	0.8 • V2			V
$I_{CWT(UP)}$	CWT Pull-Up Current	V_{CWT} = 0V	●	–1.4	–2	–2.6	µA
$I_{CWT(DN)}$	CWT Pull-Down Current	V_{CWT} = 1.3V	●	10	20	30	µA
t_{WD}	Watchdog Time-Out Period	C_{WT} = 1500pF	●	20	30	40	ms
V_{IH}	WDI Input Threshold High	V_{CC} = 3.3V to 5.5V	●			1.6	V
V_{IL}	WDI Input Threshold Low	V_{CC} = 3.3V to 5.5V	●	0.4			V
t_{WP}	WDI Input Pulse Width	V_{CC} = 3.3V	●	150			ns
I_{WDI}	WDI Pull-Up Current	V_{WDI} = 0V			–10		µA
Digital Input TOL							
V_{IL}	TOL Low Level Input Voltage	V_{CC} = 3.3V to 5.5V	●			$0.3V_{CC}$	V
V_{IH}	TOL High Level Input Voltage	V_{CC} = 3.3V to 5.5V	●	$0.7V_{CC}$			V
I_{INTOL}	TOL Input Current	TOL = V_{CC}	●		±0.1	±1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive, all voltages are referenced to GND unless otherwise noted.

Note 3: The greater of V1, V2 is the internal supply voltage (V_{CC}).

Note 4: 10% thresholds apply to the LTC2901-3/LTC2901-4 only when the TOL pin is set to a logic high.

Note 5: Under static no-fault conditions, V1 will necessarily supply quiescent current. If at any time V2 is larger than V1, V2 must be capable of supplying the quiescent current, programming (transient) current and reference load current.

Note 6: The output pins $\overline{RST}$, $\overline{WDO}$ and COMPX have internal pull-ups to V2 of typically 6µA. However, external pull-up resistors may be used when faster rise times are required or for V_{OH} voltages greater than V2.

Note 7: The push-pull $\overline{RST}$ output pin on the LTC2901-2/LTC2901-4 is *actively* pulled up to V2.

TEST CIRCUITS

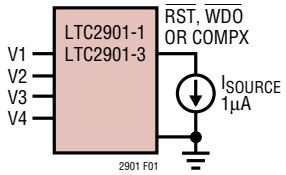


Figure 1. $\overline{RST}$, $\overline{WDO}$, COMPX V_{OH} Test

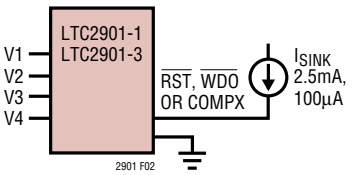


Figure 2. $\overline{RST}$, $\overline{WDO}$, COMPX V_{OL} Test

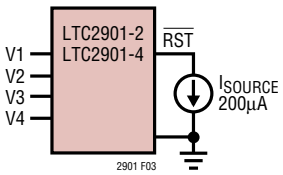
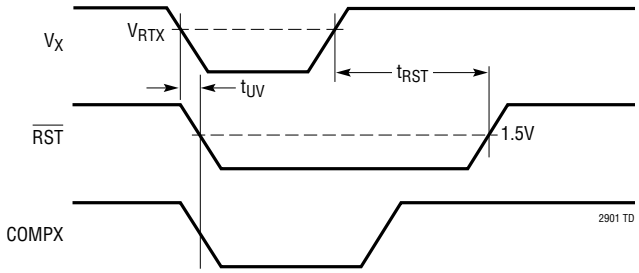


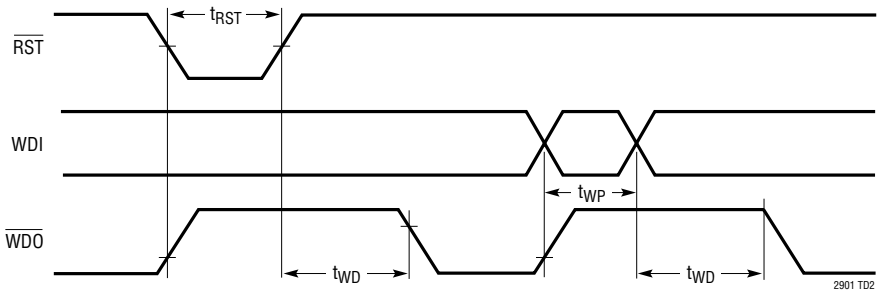
Figure 3. Active Pull-Up $\overline{RST}$ V_{OH} Test

TIMING DIAGRAMS

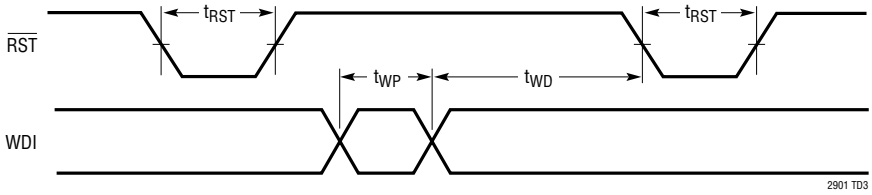
V_X Monitor Timing



Watchdog Timing (LTC2901-1/LTC2901-2)

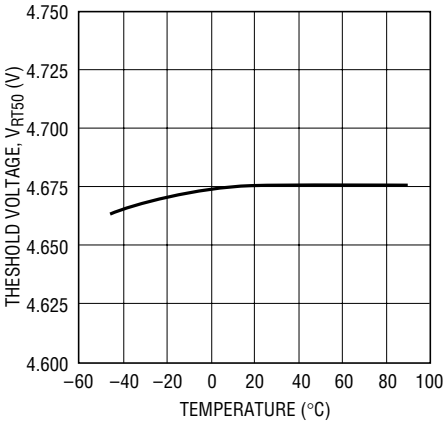


Watchdog Timing (LTC2901-3/LTC2901-4)

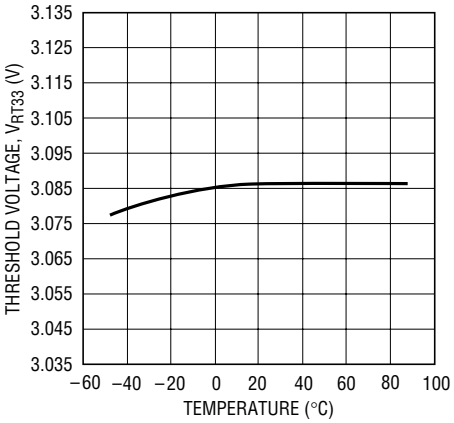


TYPICAL PERFORMANCE CHARACTERISTICS

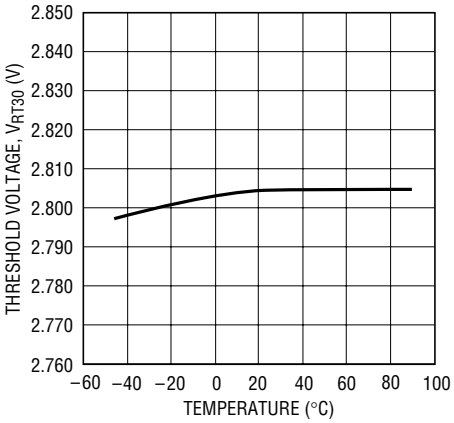
5V Threshold Voltage vs Temperature



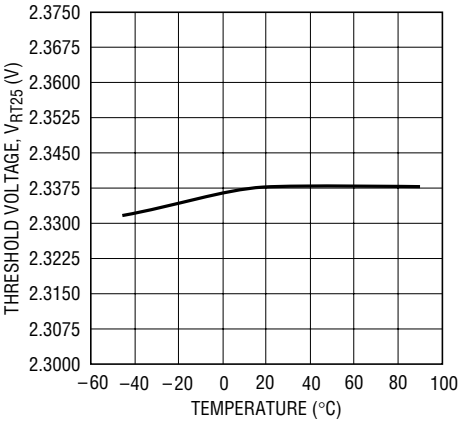
3.3V Threshold Voltage vs Temperature



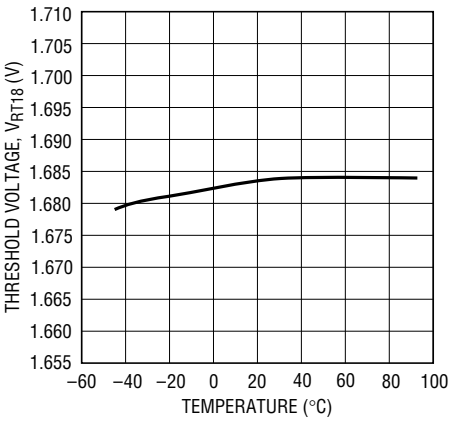
3V Threshold Voltage vs Temperature



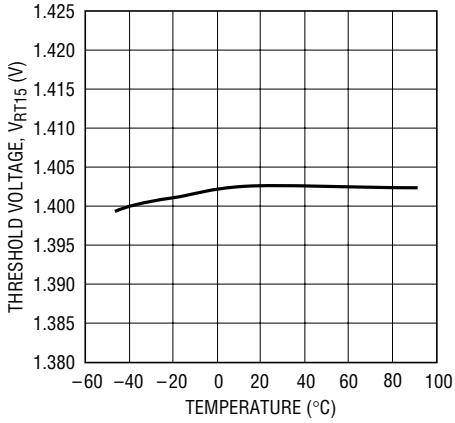
2.5V Threshold Voltage vs Temperature



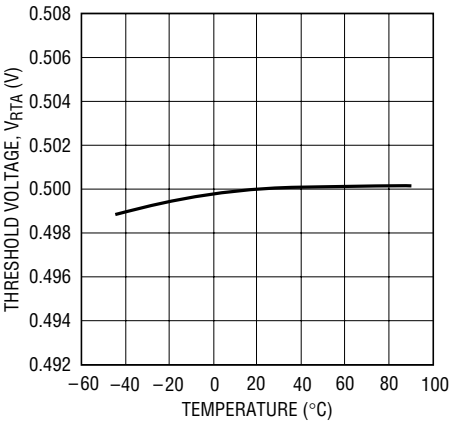
1.8V Threshold Voltage vs Temperature



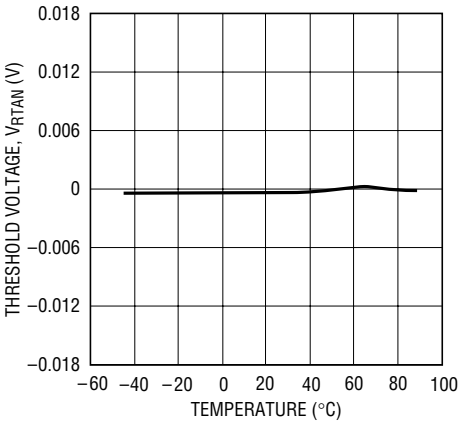
1.5V Threshold Voltage vs Temperature



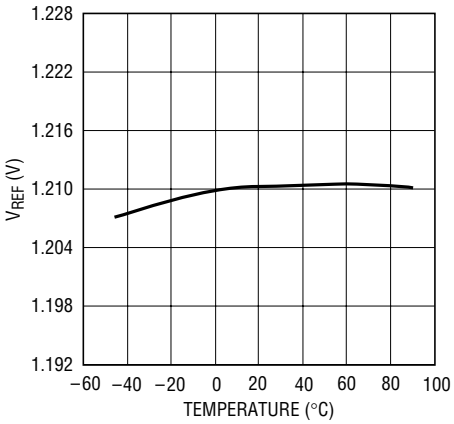
ADJ Threshold Voltage vs Temperature



–ADJ Threshold Voltage vs Temperature

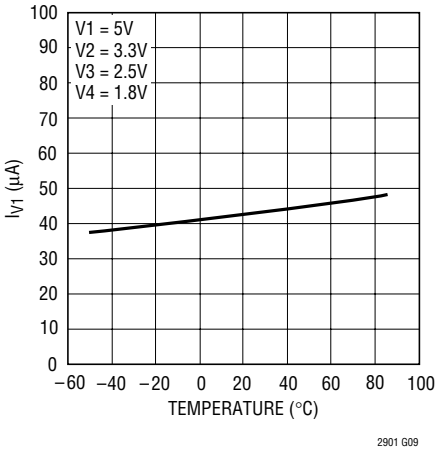


V_{REF} vs Temperature

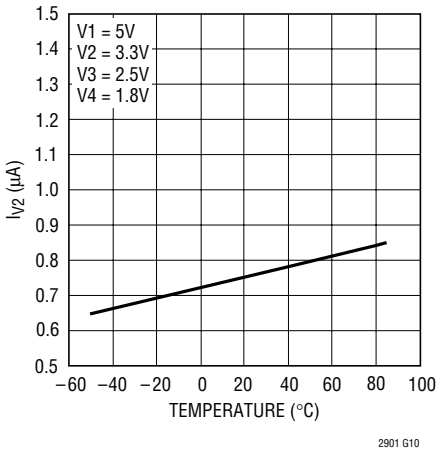


TYPICAL PERFORMANCE CHARACTERISTICS

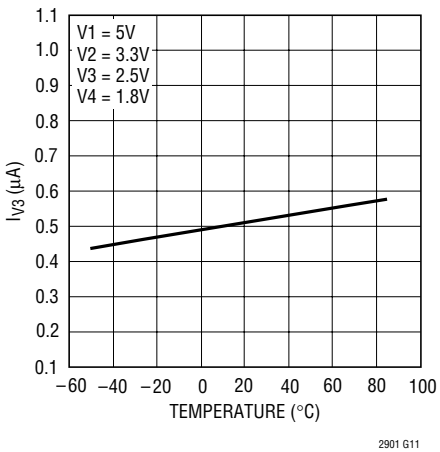
I_{V1} vs Temperature



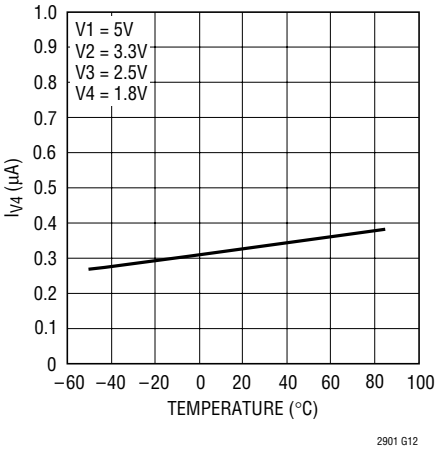
I_{V2} vs Temperature



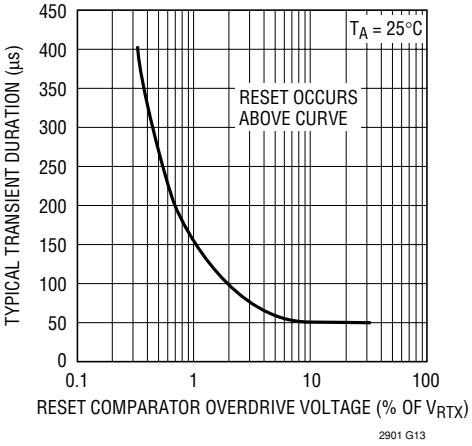
I_{V3} vs Temperature



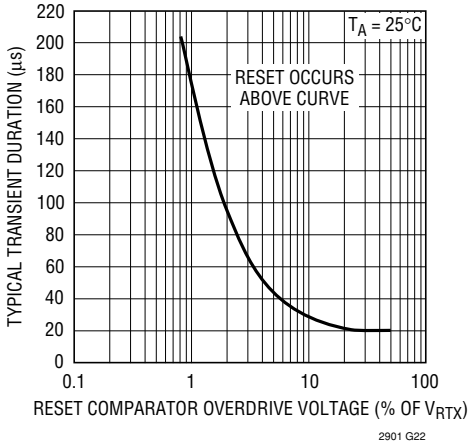
I_{V4} vs Temperature



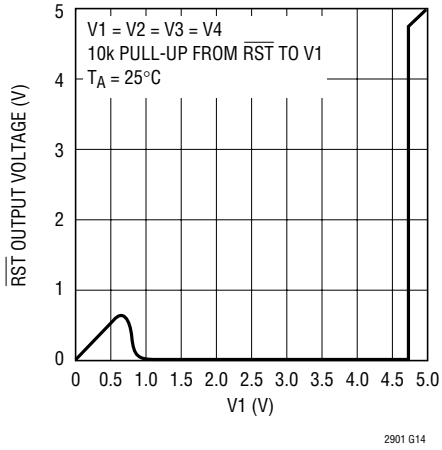
Typical Transient Duration vs Comparator Overdrive (V1, V2)



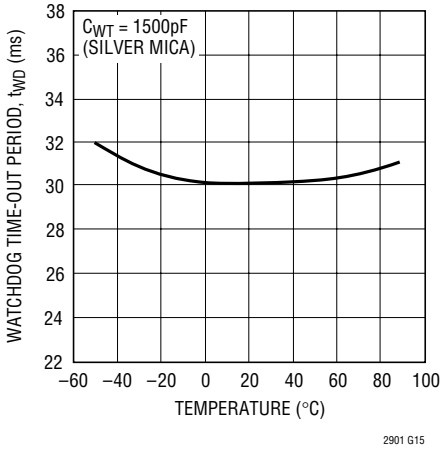
Typical Transient Duration vs Comparator Overdrive (V3, V4)



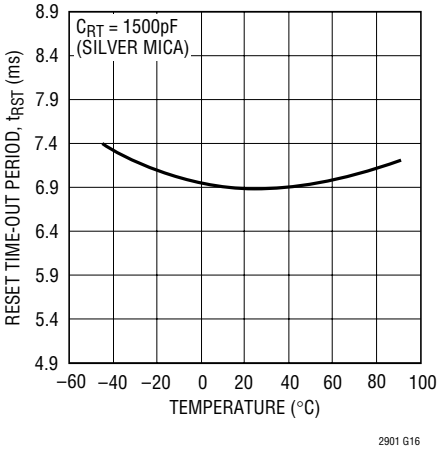
$\overline{RST}$ Output Voltage vs V1, V_{PG} = 0V



Watchdog Time-Out Period vs Temperature

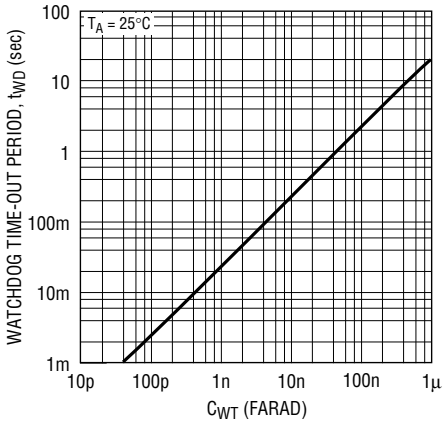


Reset Time-Out Period vs Temperature

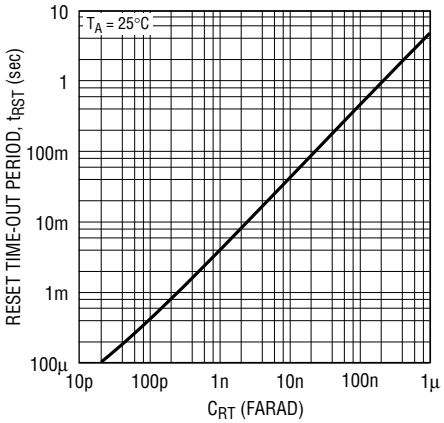


TYPICAL PERFORMANCE CHARACTERISTICS

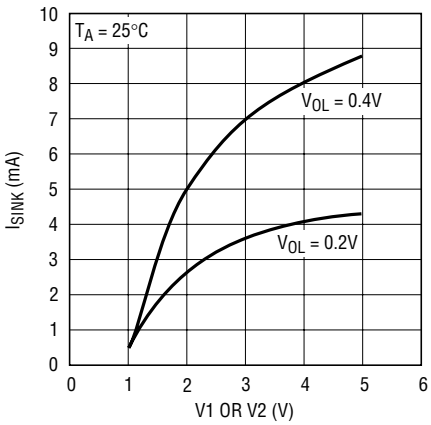
Watchdog Time-Out Period vs Capacitance



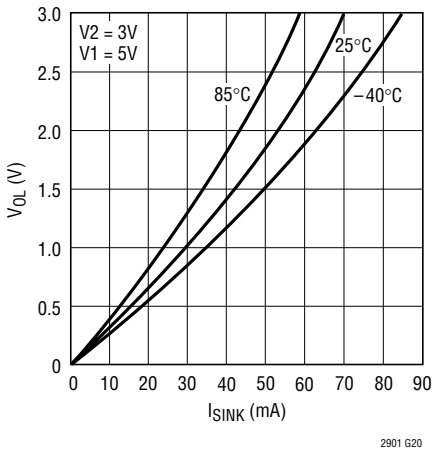
Reset Time-Out Period vs Capacitance



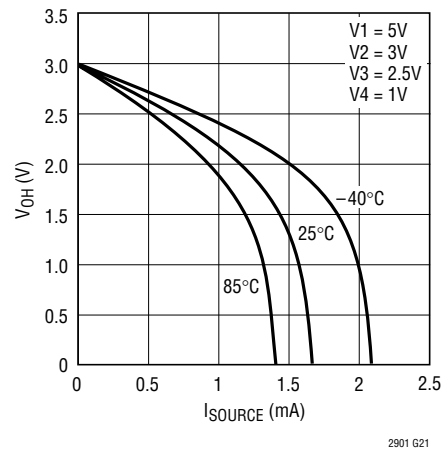
$\overline{RST}$, $\overline{WDO}$, COMPX I_{SINK} vs Supply Voltage



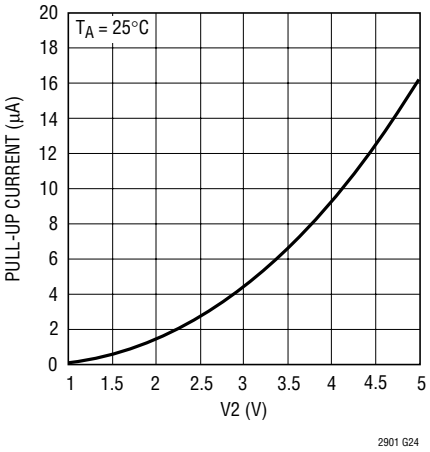
$\overline{RST}$, $\overline{WDO}$, COMPX Voltage Output Low vs Output Sink Current



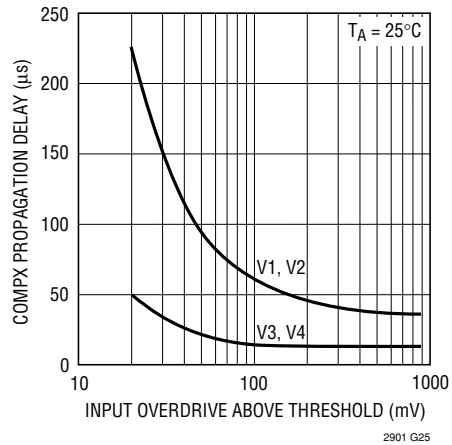
$\overline{RST}$ High Level Output Voltage vs Output Source Current (LTC2901-2/LTC2901-4)



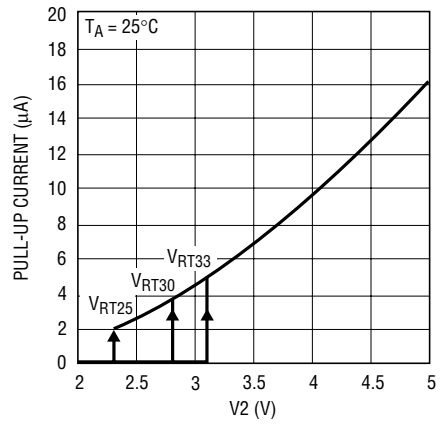
COMPX and $\overline{WDO}$ Pull-Up Current vs V2 (COMPX and $\overline{WDO}$ Held at 0V)



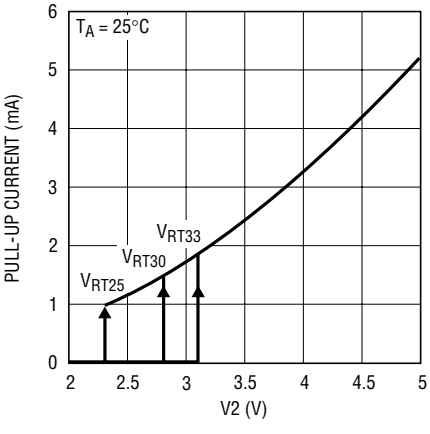
COMPX Propagation Delay vs Input Overdrive Above Threshold



$\overline{RST}$ Pull-Up Current vs V2 (LTC2901-1/LTC2901-3)



$\overline{RST}$ Pull-Up Current vs V2 (LTC2901-2/LTC2901-4)



PIN FUNCTIONS

COMP3 (Pin 1): Comparator Output 3. Nondelayed, active high logic output with weak pull-up to V2. Pulls high when V3 is above reset threshold. May be pulled greater than V2 using external pull-up.

COMP1 (Pin 2): Comparator Output 1. Nondelayed, active high logic output with weak pull-up to V2. Pulls high when V1 is above reset threshold. May be pulled greater than V2 using external pull-up.

V3 (Pin 3): Voltage Input 3. Select from 2.5V, 1.8V, 1.5V or ADJ. See Table 1 for details.

V1 (Pin 4): Voltage Input 1. Select from 5V or 3.3V. See Table 1 for details. The greater of (V1, V2) is also V_{CC} for the device. Bypass this pin to ground with a 0.1µF (or greater) capacitor.

CRT (Pin 5): Reset Delay Time Programming Pin. Attach an external capacitor (C_{RT}) to GND to set a reset delay time of 4.6ms/nF. Leaving the pin open generates a minimum delay of approximately 50µs. A 47nF capacitor will generate a 216ms reset delay time.

$\overline{\text{RST}}$ (Pin 6): Reset Logic Output. Active low with weak pull-up to V2 (LTC2901-1/LTC2901-3) or active pull-up to V2 (LTC2901-2/LTC2901-4). Pulls low when any voltage input is below the reset threshold and held low for the programmed delay time after all voltage inputs are above threshold. May be pulled above V2 using an external pull-up (LTC2901-1/LTC2901-3 only).

$\overline{\text{WDO}}$ (Pin 7): LTC2901-1/LTC2901-2 Watchdog Output. Active low logic output with weak pull-up to V2. May be pulled greater than V2 using external pull-up. The watchdog output pulls low if the watchdog timer is allowed to time out and remains low until set high by the next WDI transistion or anytime $\overline{\text{RST}}$ is low. The watchdog timer is enabled when $\overline{\text{RST}}$ is high.

TOL (Pin 7): LTC2901-3/LTC2901-4 Digital Input for Supply Tolerance Selection (5% or 10%). A logic low selects 5% thresholds; a logic high selects 10% thresholds.

WDI (Pin 8): Watchdog Input. A logic input whose rising or falling edge must occur on this pin (while $\overline{\text{RST}}$ is high) within the selected watchdog time-out period, prohibiting a high-to-low transition on the $\overline{\text{WDO}}$ pin (LTC2901-1/LTC2901-2). The watchdog time-out period is set by the value of the capacitor that is attached to the CWT pin. A rising or falling edge on the WDI pin clears the voltage on the C_{WT} capacitor, preventing $\overline{\text{WDO}}$ from going low. When disabling the watchdog function, tie CWT to GND.

For the LTC2901-3/LTC2901-4, a watchdog time-out due to a missed WDI edge issues an $\overline{\text{RST}}$ pulse on the $\overline{\text{RST}}$ pin (the WDO function is merged into the $\overline{\text{RST}}$ function).

CWT (Pin 9): Watchdog Time-Out Programming Pin. Attach a capacitor (C_{WT}) between CWT and GND to set a watchdog time-out period of 20ms/nF. Leaving the pin open generates a minimum time-out of approximately 200µs. A 47nF capacitor will generate a 940ms watchdog time-out period.

GND (Pin 10): Ground.

V_{PG} (Pin 11): Voltage Threshold Combination Select Input. Connect to an external 1% resistive divider between V_{REF} and GND to select 1 of 16 combinations of preset and/or ±adjustable voltage thresholds (see Table 1). Do not add capacitance on the V_{PG} pin.

V_{REF} (Pin 12): Buffered Reference Voltage. A 1.210V nominal reference used for programming voltage (V_{PG}) and for the offset of negative adjustable applications. The buffered reference can source and sink up to 1mA. The reference can drive a bypass capacitor of up to 1000pF without oscillation.

V4 (Pin 13): Voltage Input 4. Select from 1.8V, 1.5V, ADJ or –ADJ. See Table 1 for details.

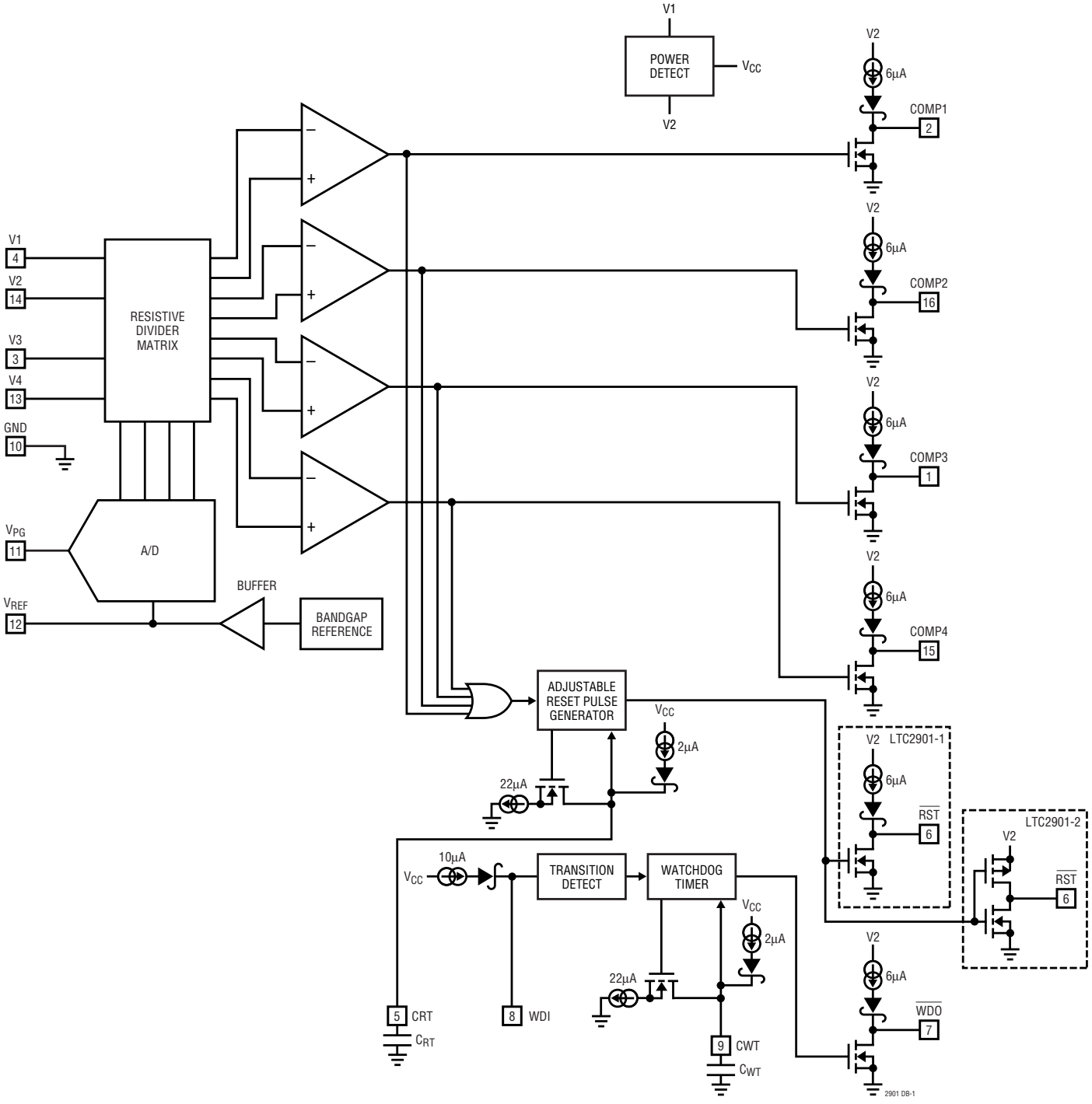
V2 (Pin 14): Voltage Input 2. Select from 3.3V, 3V or 2.5V. See Table 1 for details. The greater of (V1, V2) is also V_{CC} for device. Bypass this pin to ground with a 0.1µF (or greater) capacitor. All logic outputs (COMP1, COMP2, COMP3, COMP4, $\overline{\text{RST}}$, $\overline{\text{WDO}}$) are weakly pulled up to V2 (LTC2901-1/LTC2901-3). $\overline{\text{RST}}$ is actively pulled up to V2 in the LTC2901-2/LTC2901-4.

COMP4 (Pin 15): Comparator Output 4. Nondelayed, active high logic output with weak pull-up to V2. Pulls high when V4 is above reset threshold. May be pulled greater than V2 using external pull-up.

COMP2 (Pin 16): Comparator Output 2. Nondelayed, active high logic output with weak pull-up to V2. Pulls high when V2 is above reset threshold. May be pulled greater than V2 using external pull-up.

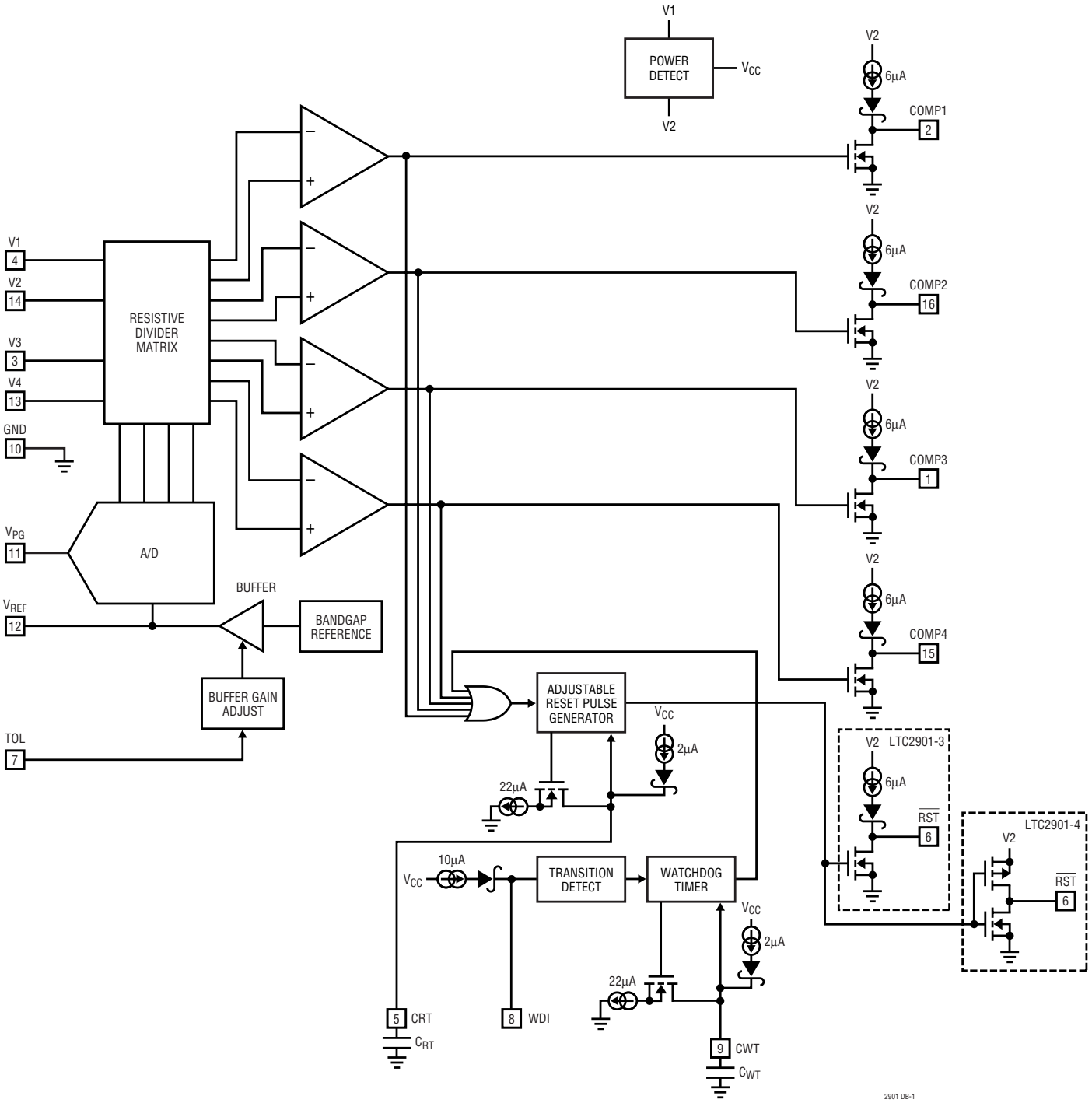
BLOCK DIAGRAM

LTC2901-1/LTC2901-2



BLOCK DIAGRAM

LTC2901-3/LTC2901-4



APPLICATIONS INFORMATION

Power-Up

The greater of V1, V2 is the internal supply voltage (V_{CC}). On power-up, V_{CC} will power the drive circuits for the $\overline{RST}$ and the COMPX pins. This ensures that the $\overline{RST}$ and COMPX outputs will be low as soon as V1 or V2 reaches 1V. The $\overline{RST}$ and COMPX outputs will remain low until the part is programmed. After programming, if any one of the V_X inputs is below its programmed threshold, $\overline{RST}$ will be a logic low. Once all the V_X inputs rise above their thresholds, an internal timer is started and $\overline{RST}$ is released after the programmed delay time. If $V_{CC} < (V3 - 1)$ and $V_{CC} < 2.4V$, the V3 input impedance will be low (1kΩ typ).

Monitor Programming

The LTC2901 input voltage combination is selected by placing the recommended resistive divider from V_{REF} to GND and connecting the tap point to V_{PG}, as shown in Figure 4. Table 1 offers recommended 1% resistor values for the various modes. The last column in Table 1 specifies optimum V_{PG}/V_{REF} ratios (±0.01) to be used when programming with a ratiometric DAC.

During power-up, once V1 or V2 reaches 2.4V max, the monitor enters a programming period of approximately

Table 1. Voltage Threshold Programming

MODE	V1 (V)	V2 (V)	V3 (V)	V4 (V)	R1 (kΩ)	R2 (kΩ)	$\frac{V_{PG}}{V_{REF}}$
0	5.0	3.3	ADJ	ADJ	Open	Short	0.000
1	5.0	3.3	ADJ	–ADJ	93.1	9.53	0.094
2	3.3	2.5	ADJ	ADJ	86.6	16.2	0.156
3	3.3	2.5	ADJ	–ADJ	78.7	22.1	0.219
4	3.3	2.5	1.5	ADJ	71.5	28.0	0.281
5	5.0	3.3	2.5	ADJ	66.5	34.8	0.344
6	5.0	3.3	2.5	1.8	59.0	40.2	0.406
7	5.0	3.3	2.5	1.5	53.6	47.5	0.469
8	5.0	3.0	2.5	ADJ	47.5	53.6	0.531
9	5.0	3.0	ADJ	ADJ	40.2	59.0	0.594
10	3.3	2.5	1.8	1.5	34.8	66.5	0.656
11	3.3	2.5	1.8	ADJ	28.0	71.5	0.719
12	3.3	2.5	1.8	–ADJ	22.1	78.7	0.781
13	5.0	3.3	1.8	–ADJ	16.2	86.6	0.844
14	5.0	3.3	1.8	ADJ	9.53	93.1	0.906
15	5.0	3.0	1.8	ADJ	Short	Open	1.000

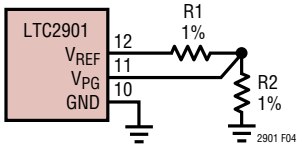


Figure 4. Monitor Programming

150µs during which the voltage on the V_{PG} pin is sampled and the monitor is configured to the desired input combination. Do not add capacitance to the V_{PG} pin. Immediately after programming, the comparators are enabled and supply monitoring will begin.

Supply Monitoring

The LTC2901 is a low power, high accuracy programmable quad supply monitoring circuit with four nondelayed monitor outputs, a common reset output and a watchdog timer. Watchdog and reset timing are both adjustable using external capacitors. Single pin programming selects 1 of 16 input voltage monitor combinations. All four voltage inputs must be above predetermined thresholds for the reset not to be invoked. The LTC2901 will assert the reset and comparator outputs during power-up, power-down and brownout conditions on any one of the voltage inputs.

The inverting inputs on the V3 and/or V4 comparators are set to 0.5V when the positive adjustable modes are selected (Figure 5). The tap point on an external resistive divider, connected between the positive voltage being sensed and ground, is connected to the high impedance noninverting inputs (V3, V4). The trip voltage is calculated from:

$$V_{TRIP} = 0.5V\left(1+\frac{R3}{R4}\right)$$

In the negative adjustable mode, the noninverting input on the V4 comparator is connected to ground (Figure 6). The tap point on an external resistive divider, connected between the negative voltage being sensed and the V_{REF} pin, is connected to the high impedance inverting input (V4). V_{REF} provides the necessary level shift required to operate at ground. The trip voltage is calculated from:

$$V_{TRIP} = -V_{REF}\left(\frac{R3}{R4}\right); V_{REF} = 1.210V\ Nominal$$

APPLICATIONS INFORMATION

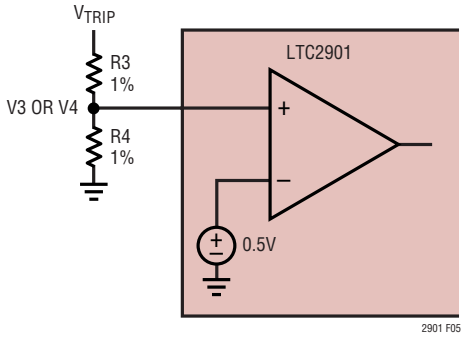


Figure 5. Setting the Positive Adjustable Trip Point

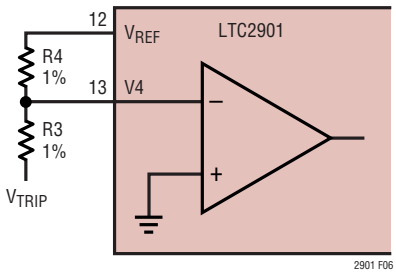


Figure 6. Setting the Negative Adjustable Trip Point

In a negative adjustable application, the minimum value for R4 is limited by the sourcing capability of V_{REF} (±1mA). With no other load on V_{REF}, R4 (minimum) is:

$1.21V \div 1mA = 1.21k\Omega$.

Tables 2 and 3 offer suggested 1% resistor values for various adjustable applications.

Once the resistor divider is set in the 5% tolerance mode (LTC2901-3/LTC2901-4), there is no need to change the divider for the 10% mode because the internal and external reference is scaled accordingly, moving the trip point by –5%.

Although all four supply monitor comparators have built-in glitch immunity, bypass capacitors on V1 and V2 are recommended because the greater of V1 or V2 is also the V_{CC} for the device. Filter capacitors on the V3 and V4 inputs are allowed.

Power-Down

On power-down, once any of the V_X inputs drop below their threshold, RST and COMPX are held at a logic low. A logic low of 0.4V is guaranteed until both V1 and V2 drop below 1V. If the bandgap reference becomes invalid (V_{CC} < 2V typ), the part will reprogram once V_{CC} rises above 2.4V max.

Table 2. Suggested 1% Resistor Values for the ADJ Inputs

V_{SUPPLY} (V)	V_{TRIP} (V)	R3 (kΩ)	R4 (kΩ)
12	11.25	2150	100
10	9.4	1780	100
8	7.5	1400	100
7.5	7	1300	100
6	5.6	1020	100
5	4.725	845	100
3.3	3.055	511	100
3	2.82	464	100
2.5	2.325	365	100
1.8	1.685	237	100
1.5	1.410	182	100
1.2	1.120	124	100
1	0.933	86.6	100
0.9	0.840	68.1	100

Table 3. Suggested 1% Resistor Values for the –ADJ Input

V_{SUPPLY} (V)	V_{TRIP} (V)	R3 (kΩ)	R4 (kΩ)
–2	–1.87	187	121
–5	–4.64	464	121
–5.2	–4.87	487	121
–10	–9.31	931	121
–12	–11.30	1130	121

Monitor Output Rise and Fall Time Estimation

All of the outputs ($\overline{RST}$, COMPX, $\overline{WDO}$) have strong pull-down capability. If the external load capacitance (C_{LOAD}) for a particular output is known, output fall time (10% to 90%) is estimated using:

$$t_{FALL} \approx 2.2 \bullet R_{PD} \bullet C_{LOAD}$$

where R_{PD} is the on-resistance of the internal pull-down transistor. The typical performance curve (V_{OL} vs I_{SINK}) demonstrates that the pull-down current is somewhat linear versus output voltage. Using the 25°C curve, R_{PD} is estimated to be approximately 40Ω. Assuming a 150pF load capacitance, the fall time is about 13.2ns.

Although the outputs are considered to be "open-drain," they do have a weak pull-up capability (see COMPX or $\overline{RST}$

APPLICATIONS INFORMATION

Pull-Up Current vs V2 curve). Output rise time (10% to 90%) is estimated using:

$$t_{RISE} \approx 2.2 \bullet R_{PU} \bullet C_{LOAD}$$

where R_{PU} is the on-resistance of the pull-up transistor. The on-resistance as a function of the V2 voltage at room temperature is estimated using:

$$R_{PU} = \frac{6 \bullet 10^5}{V2 - 1} \Omega$$

with V2 = 3.3V, R_{PU} is about 260k. Using 150pF for load capacitance, the rise time is 86µs. If the output needs to pull up faster and/or to a higher voltage, a smaller external pull-up resistor may be used. Using a 10k pull-up resistor, the rise time is reduced to 3.3µs for a 150pF load capacitance.

The LTC2901-2 has an active pull-up to V2 on the $\overline{RST}$ output. The typical performance curve ($\overline{RST}$ Pull-Up Current vs V2 curve) demonstrates that the pull-up current is somewhat linear versus the V2 voltage and R_{PU} is estimated to be approximately 625Ω. A 150pF load capacitance makes the rise time about 206ns.

Watchdog Timer

The watchdog circuit typically monitors a µP's activity. The µP is required to change the logic state of the WDI pin on a periodic basis in order to clear the watchdog timer and prevent the $\overline{WDO}$ pin (LTC2901-1/LTC2901-2) from going low. Whenever $\overline{RST}$ is low, the watchdog timer is cleared and $\overline{WDO}$ is set high. The watchdog timer is started when $\overline{RST}$ pulls high. Subsequent edges received on the WDI pin will clear the watchdog timer. The timer will continue to run until the watchdog timer times out. Once the watchdog timer times out, internal circuitry will bring the $\overline{WDO}$ pin low. $\overline{WDO}$ will remain low and the watchdog timer will remain cleared until the next edge is received on the WDI pin or until $\overline{RST}$ goes low.

In the LTC2901-3/LTC2901-4, there is no $\overline{WDO}$ pin. Instead, the $\overline{RST}$ pin is pulled low for the programmed reset time-out period whenever a WDI edge is missed. In this manner, a full system reset can be issued after a watchdog failure.

To disable the watchdog timer, simply ground the CWT pin (Pin 9). With CWT held at ground, any reset event will force $\overline{WDO}$ high indefinitely. It is safe to leave the WDI pin (Pin 8) unconnected because the weak internal pull-up (10µA typ) will pull WDI high. Tying WDI to V1 or ground is also allowed, but grounding the WDI pin will force the pull-up current to be drawn continuously.

Selecting the Reset Timing Capacitor

The reset time-out period is adjustable in order to accommodate a variety of microprocessor applications. The reset time-out period, t_{RST}, is adjusted by connecting a capacitor, C_{RT}, between the CRT pin and ground. The value of this capacitor is determined by:

$$C_{RT} = t_{RST} \bullet 217 \bullet 10^{-9}$$

with C_{RT} in Farads and t_{RST} in seconds. The C_{RT} value per millisecond of delay can also be expressed as C_{RT}/ms = 217 (pF/ms).

Leaving the CRT pin unconnected will generate a minimum reset time-out of approximately 50µs. Maximum reset time-out is limited by the largest available low leakage capacitor. The accuracy of the time-out period will be affected by capacitor leakage (the nominal charging current is 2µA) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

Selecting the Watchdog Timing Capacitor

The watchdog time-out period is adjustable and can be optimized for software execution. The watchdog time-out period, t_{WD}, is adjusted by connecting a capacitor, C_{WT}, between the CWT pin and ground. Given a specified watchdog time-out period, the capacitor is determined by:

$$C_{WT} = t_{WD} \bullet 50 \bullet 10^{-9}$$

with C_{WT} in Farads and t_{WD} in seconds. The C_{WT} value per millisecond of delay can also be expressed as C_{WT}/ms = 50 (pF/ms).

Leaving the CWT pin unconnected will generate a minimum watchdog time-out of approximately 200µs. Maximum time-out is limited by the largest available low leakage capacitor. The accuracy of the time-out period will be affected by capacitor leakage (the nominal charging current is 2µA) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

APPLICATIONS INFORMATION

Monitoring Power Supply Controller Activity

Figure 7 demonstrates how the LTC2901 can be used to monitor switcher activity. The monitor is configured to supervise 3.3V, 2.5V, 1.8V and one adjustable input. Because 2.5V does not exist in this application, the V2 input is tied to the V1 (3.3V) input. The feedback voltage on the LTC1772 (0.8V typ) is monitored with the adjustable input (V4). The $\overline{RST}$ pin will go high 216ms (C_{RT} = 47nF) after the 3.3V and 1.8V supplies and the feedback voltage are above threshold. Individual input status is available at the COMPX pins.

While the voltage monitors can detect low voltage or shorted inputs, the watchdog circuit can be used to detect an open circuit to the primary load. With the CWT pin unconnected, the watchdog time-out is approximately 200µs. At low load currents on the 1.8V supply, the LTC1772 will go into Burst Mode® operation. With an open-ciruit load, the duty cycle at the gate of M1 will drop, and the pulse spacing will exceed the watchdog time-out period. The $\overline{WDO}$ pin will go low indicating the low load condition. The $\overline{WDO}$ pin will return high on the next pulse to the gate of M1. The $\overline{WDO}$ pin will remain high if the load is restored.

Ensuring Reset Valid for V_{CC} Down to 0V (LTC2901-2/LTC2901-4)

Some applications require the reset output ($\overline{RST}$) to be valid with V_{CC} down to 0V. The LTC2901-2 is designed to handle this requirement with the addition of an external resistor from $\overline{RST}$ to ground. The resistor will provide a path for stray charge and/or leakage currents, preventing the $\overline{RST}$ output from floating to undetermined voltages when connected to high impedance (such as CMOS logic inputs). The resistor value should be small enough to provide effective pull-down without excessively loading the active pull-up circuitry. Too large a value may not pull down well enough. A 100k resistor from $\overline{RST}$ to ground is satisfactory for most applications.

Burst Mode is a registered trademark of Linear Technology Corporation.

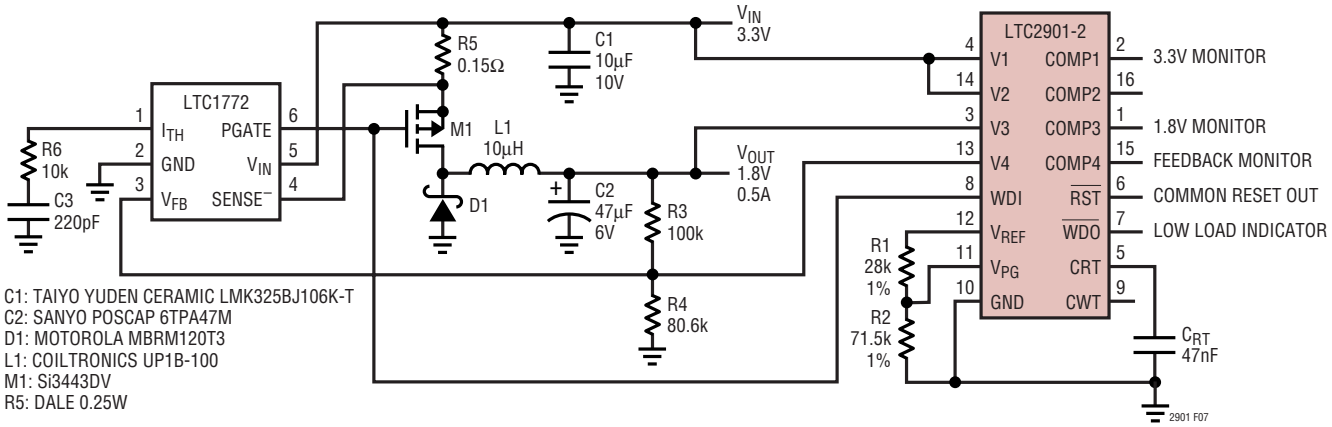
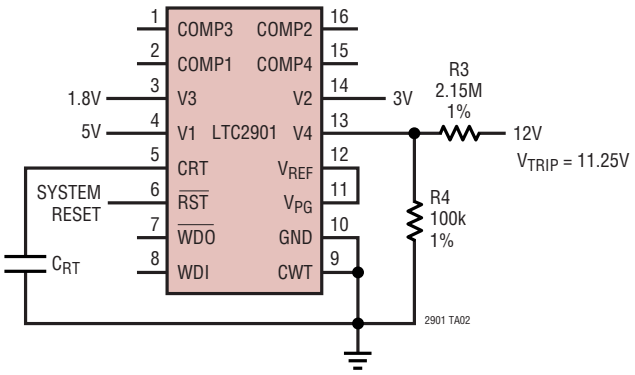


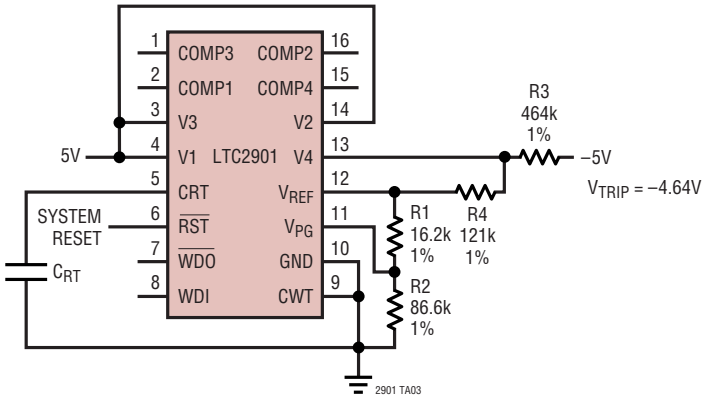
Figure 7. Monitor Input, Output, Feedback Voltage and Low Load Conditions on DC/DC Controller

TYPICAL APPLICATIONS

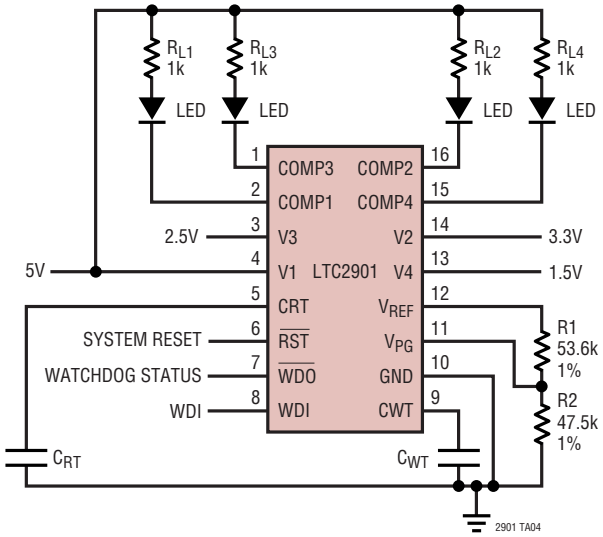
Quad Supply Monitor with Watchdog Timer Disabled 5V, 3V, 1.8V, 12V (ADJ)



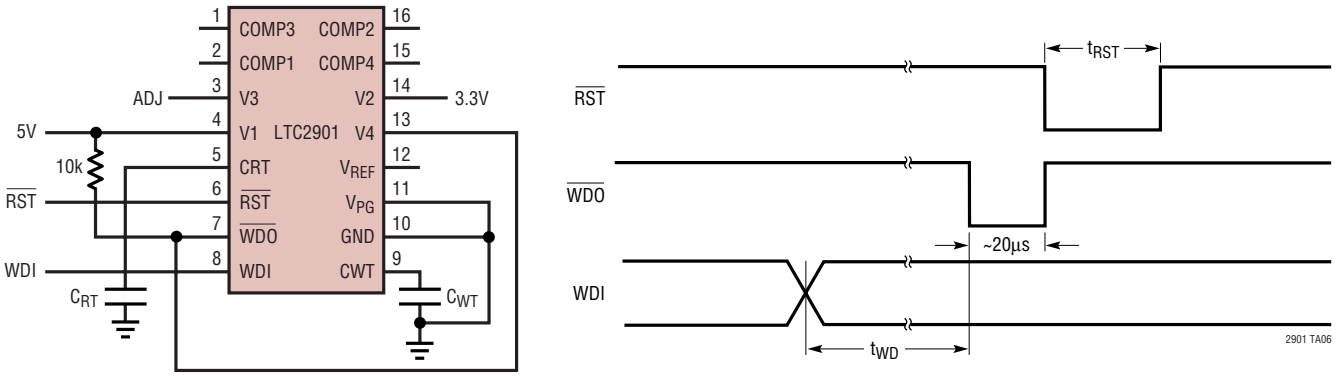
5V, –5V Monitor with Watchdog Timer Disabled and Unused V2, V3 Inputs Pulled Above Trip Thresholds



Quad Supply Monitor with LED Undervoltage Indicators 5V, 3.3V, 2.5V, 1.5V

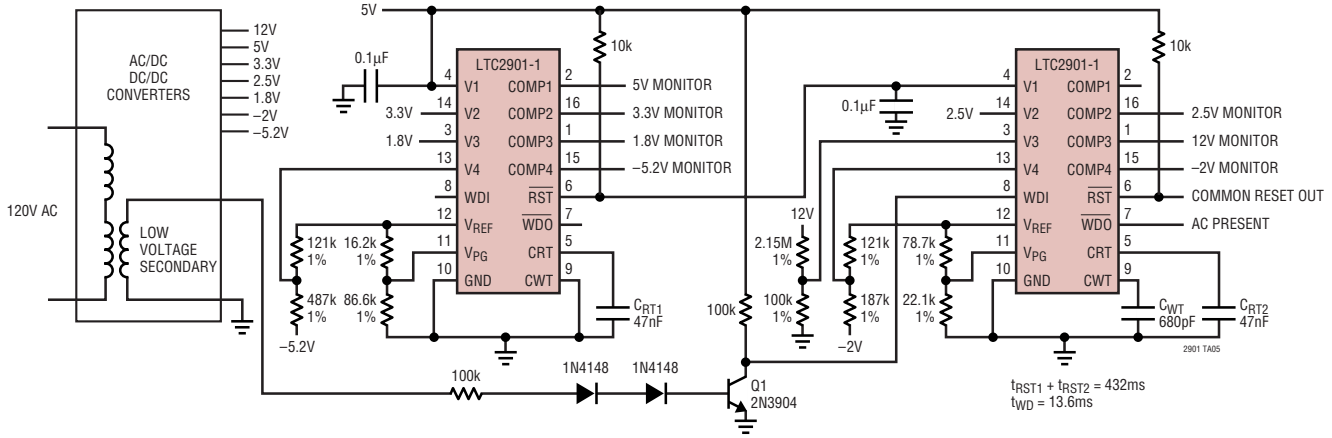


Generate $\overline{\text{RESET}}$ Pulse Through Watchdog Timeout (LTC2901-1/LTC2901-2)



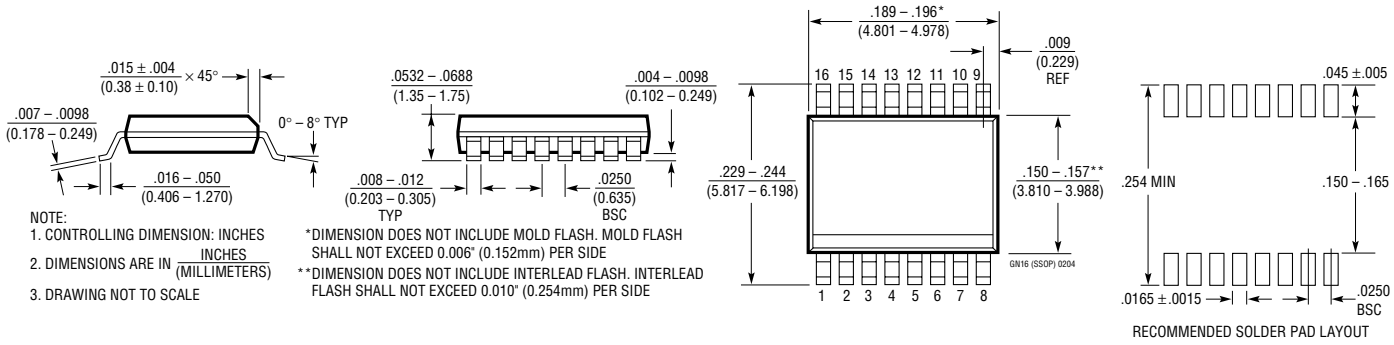
TYPICAL APPLICATION

Monitor Seven Supplies (12V, 5V, 3.3V, 2.5V, 1.8V, –2V, –5.2V) with Sequenced Reset and AC Present Indication



PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC694-3.3	3.3V Supply Monitor, Watchdog Timer and Battery Backup	2.9V Threshold
LTC1326	Micropower Precision Triple Supply Monitor for 5V, 3.3V and ADJ	4.725V, 3.118V, 1V Thresholds (±0.75%)
LTC1726-2.5	Micropower Triple Supply Monitor for 2.5V, 3.3V and ADJ	Adjustable $\overline{\text{RESET}}$ and Watchdog Time-Outs
LTC1727-2.5/LTC1727-5	Micropower Triple Supply Monitors with Open-Drain Reset	Individual Monitor Outputs in MSOP
LTC1728-1.8/LTC1728-3.3	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC2900	Programmable Quad Supply Monitor	Adjustable Reset Timer, 10-Lead MSOP and 3mm × 3mm 10-Lead DFN
LTC2902	Programmable Quad Supply Monitor	Adjustable Reset Timer, Supply Tolerance and Margining Functions, 16-Lead Narrow SSOP
LTC2903	Precision Quad Supply Monitor in 6-Lead SOT-23	A Variety of Factory Trimmed Voltage Combinations
LTC2904/LTC2905 LTC2906/LTC2907	Precision Dual Supply Monitors	Pin Selectable Thresholds
LTC2908	Precision Six Supply Monitor	8-Lead SOT-23 and DFN Packages

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT 0807 REV B • PRINTED IN USA