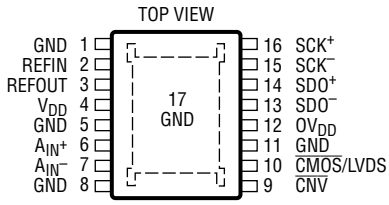
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Supply Voltage (OV_{DD}) 3V
Analog Input Voltage
  A_{IN+}, A_{IN-} (Note 3) ..... –0.3V to (V_{DD} + 0.3V)
  REFIN, REFOUT ..... –0.3V to (V_{DD} + 0.3V)
  $\overline{CNV}$ (Note 15) ..... –0.3V to (V_{DD} + 0.3V)
Digital Input Voltage
(Note 3) ..... (GND – 0.3V) to (OV_{DD} + 0.3V)
Digital Output Voltage
(Note 3) ..... (GND – 0.3V) to (OV_{DD} + 0.3V)
Power Dissipation 200mW
Operating Temperature Range
  LTC2310C ..... 0°C to 70°C
  LTC2310I ..... –40°C to 85°C
  LTC2310H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



MSE PACKAGE
16-LEAD (4mm × 5mm) PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC2310-14#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2310CMSE-14#PBF	LTC2310CMSE-14#TRPBF	231014	16-Lead Plastic MSOP	0°C to 70°C
LTC2310IMSE-14#PBF	LTC2310IMSE-14#TRPBF	231014	16-Lead Plastic MSOP	–40°C to 85°C
LTC2310HMSE-14#PBF	LTC2310HMSE-14#TRPBF	231014	16-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN+}	Absolute Input Range (A_{IN+})	(Note 5)	●	0		V_{DD}	V
V_{IN-}	Absolute Input Range (A_{IN-})	(Note 5)	●	0		V_{DD}	V
$V_{IN+} – V_{IN-}$	Input Differential Voltage Range	$V_{IN} = V_{IN+} – V_{IN-}$	●	–REFOUT		REFOUT	V
V_{CM}	Common Mode Input Range	$V_{CM} = (V_{IN+} + V_{IN-})/2$	●	0		V_{DD}	V
I_{IN}	Analog Input DC Leakage Current		●	–1		1	µA
C_{IN}	Analog Input Capacitance				10		pF
CMRR	Input Common Mode Rejection Ratio	f_{IN} = 2.2MHz			85		dB
V_{IHCNV}	$\overline{CNV}$ High Level Input Voltage		●	1.3			V
V_{ILCNV}	$\overline{CNV}$ Low Level Input Voltage		●			0.5	V
V_{INCNV}	$\overline{CNV}$ Input Current	V_{IN} = 0V to V_{DD}	●	–10		10	µA

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	14			Bits
	No Missing Codes		●	14			Bits
	Transition Noise				0.5		LSB_{RMS}
INL	Integral Linearity Error	(Note 6)	●	–2.5	±0.8	2.5	LSB
DNL	Differential Linearity Error		●	–0.99	±0.25	0.99	LSB
BZE	Bipolar Zero-Scale Error	(Note 7)	●	–5	0	5	LSB
	Bipolar Zero-Scale Error Drift				0.01		LSB/°C
FSE	Bipolar Full-Scale Error	V_{REFOUT} = 4.096V (REFIN Grounded) (Note 7)	●	–10	±3	10	LSB
	Bipolar Full-Scale Error Drift	V_{REFOUT} = 4.096V (REFIN Grounded)			15		ppm/°C

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and A_{IN} = –1dBFS (Notes 4, 8).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	f_{IN} = 500kHz, V_{REFOUT} = 4.096V, Internal Reference f_{IN} = 500kHz, V_{REFOUT} = 5V, External Reference	●	75.5	81.7 82		dB dB
SNR	Signal-to-Noise Ratio	f_{IN} = 500kHz, V_{REFOUT} = 4.096V, Internal Reference f_{IN} = 500kHz, V_{REFOUT} = 5V, External Reference	●	76	82 82.6		dB dB
THD	Total Harmonic Distortion	f_{IN} = 500kHz, V_{REFOUT} = 4.096V, Internal Reference f_{IN} = 500kHz, V_{REFOUT} = 5V, External Reference	●		–93 –90	–78	dB dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 500kHz, V_{REFOUT} = 4.096V, Internal Reference f_{IN} = 500kHz, V_{REFOUT} = 5V, External Reference	●	78	97 95		dB dB
	–3dB Input Bandwidth				100		MHz
	Aperture Delay				500		ps
	Aperture Jitter				1		ps_{RMS}
	Transient Response	Full-Scale Step			3		ns

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REFOUT}	REFOUT Output Voltage	4.75V < V_{DD} < 5.25V 3.13V < V_{DD} < 3.47V	● ●	4.082 2.042	4.096 2.048	4.110 2.054	V V
	REFOUT Input Voltage	4.75V < V_{DD} < 5.25V, REFIN = 0V (Note 5) 3.13V < V_{DD} < 3.47V, REFIN = 0V (Note 5)	● ●	0.5 0.5		V_{DD} V_{DD}	V V
	REFOUT Temperature Coefficient	(Note 14)	●		3	20	ppm/°C
	REFOUT Short-Circuit Current	V_{DD} = 5.25V, Forcing Output to GND	●			30	mA
	REFOUT Line Regulation	V_{DD} = 4.75V to 5.25V			0.3		mV/V
	REFOUT Load Regulation	I_{REFOUT} < 2mA			0.5		mV/mA
	REFOUT Input Resistance (External Reference Mode)	REFIN = 0V			60		kΩ
I_{REFOUT}	REFOUT Input Current (External Reference Mode)	REFIN = 0V, REFOUT = 4.096V (Notes 9, 10)			350		µA

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REFIN}	REFIN Output Voltage	3.13V < V_{DD} < 3.47V 4.75V < V_{DD} < 5.25V	● ●	1.245 1.245	1.25 1.25	1.255 1.255	V V
	REFIN Input Voltage	3.13V < V_{DD} < 3.47V (Note 5) 4.75V < V_{DD} < 5.25V (Note 5)	● ●	1 1		1.85 1.45	V V
	REFIN Short-Circuit Current	V_{DD} = 5.25V, Forcing Output to GND	●			250	µA
V_{IL} (V_{REFIN})	REFIN Low Level Input Voltage (External Reference Mode)	3.13V < V_{DD} < 3.47V 4.75V < V_{DD} < 5.25V	● ●			0.5 0.5	V V

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS Digital Inputs and Outputs							
V_{IH}	High Level Input Voltage		●	0.8 • OV_{DD}			V
V_{IL}	Low Level Input Voltage		●			0.2 • OV_{DD}	V
I_{IN}	Digital Input Current	V_{IN} = 0V to OV_{DD}	●	–10		10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	I_O = –500µA	●	OV_{DD} – 0.2			V
V_{OL}	Low Level Output Voltage	I_O = 500µA	●			0.2	V
I_{OZ}	Hi-Z Output Leakage Current	V_{OUT} = 0V to OV_{DD}	●	–10		10	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = OV_{DD}			10		mA
LVDS Digital Inputs and Outputs							
V_{ID}	LVDS Differential Input Voltage	100Ω Differential Termination, OV_{DD} = 2.5V	●	240		600	mV
V_{IS}	LVDS Common Mode Input Voltage	100Ω Differential Termination, OV_{DD} = 2.5V	●	1		1.45	V
V_{OD}	LVDS Differential Output Voltage	100Ω Differential Load, LVDS Mode, OV_{DD} = 2.5V	●	100	250	300	mV
V_{OS}	LVDS Common Mode Output Voltage	100Ω Differential Load, LVDS Mode, OV_{DD} = 2.5V	●	0.85	1.2	1.4	V
V_{OD_LP}	Low Power LVDS Differential Output Voltage	100Ω Differential Load, Low Power, LVDS Mode, OV_{DD} = 2.5V	●	50	125	200	mV
V_{OS_LP}	Low Power LVDS Common Mode Output Voltage	100Ω Differential Load, Low Power, LVDS Mode, OV_{DD} = 2.5V	●	0.9	1.2	1.4	V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage	5V Operation 3.3V Operation	● ●	4.75 3.13		5.25 3.47	V V
OV_{DD}	Supply Voltage		●	1.71		2.63	V
I_{VDD}	Supply Current	2Msps Sample Rate ($A_{IN}^+ = A_{IN}^-$ = 0V)	●		6.8	11	mA
I_{NAP}	Nap Mode Current	Conversion Done (I_{VDD})	●		2.8	4	mA
I_{SLEEP}	Sleep Mode Current	V_{DD} = 3.3V, Sleep Mode (I_{VDD} + I_{OVDD})	●		0.1	10	µA
CMOS I/O Mode							
I_{OVDD}	Supply Current	2Msps Sample Rate (C_L = 5pF)	●		0.5	1	mA
$P_{D\_3.3V}$	Power Dissipation	V_{DD} = 3.3V 2Msps Sample Rate ($A_{IN}^+ = A_{IN}^-$ = 0V)			25		mW
	Nap Mode	V_{DD} = 3.3V Conversion Done (I_{VDD} + I_{OVDD})			7.5		mW
	Sleep Mode	V_{DD} = 3.3V Sleep Mode (I_{VDD} + I_{OVDD})			0.3		µW
P_{D_5V}	Power Dissipation	V_{DD} = 5V 2Msps Sample Rate ($A_{IN}^+ = A_{IN}^-$ = 0V)	●		35	55	mW
	Nap Mode	V_{DD} = 5V Conversion Done (I_{VDD} + I_{OVDD})	●		14	20	mW
	Sleep Mode	V_{DD} = 5V Sleep Mode (I_{VDD} + I_{OVDD})	●		0.5	40	µW
LVDS I/O Mode							
I_{OVDD}	Supply Current	2Msps Sample Rate (R_L = 100Ω)	●		2.7	4	mA
$P_{D\_3.3V}$	Power Dissipation	V_{DD} = 3.3V 2Msps Sample Rate ($A_{IN}^+ = A_{IN}^-$ = 0V)			30		mW
	Nap Mode	V_{DD} = 3.3V Conversion Done (I_{VDD} + I_{OVDD})			14		mW
	Sleep Mode	V_{DD} = 3.3V Sleep Mode (I_{VDD} + I_{OVDD})			0.3		µW
P_{D_5V}	Power Dissipation	V_{DD} = 5V 2Msps Sample Rate ($A_{IN}^+ = A_{IN}^-$ = 0V)	●		40	60	mW
	Nap Mode	V_{DD} = 5V Conversion Done (I_{VDD} + I_{OVDD})	●		20	30	mW
	Sleep Mode	V_{DD} = 5V Sleep Mode (I_{VDD} + I_{OVDD})	●		0.5	50	µW

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS, LVDS I/O Modes							
f_{SMPL}	Maximum Sampling Frequency		●			2	Msps
t_{CYC}	Time Between Conversions	(Note 11)	●	500		1000000	ns
t_{ACQ}	Acquisition Time	(Note 11)	●	280			ns
t_{CONV}	Conversion Time		●	220			ns
$t_{READOUT}$	Readout Time		●	250			ns
t_{CNVH}	$\overline{CNV}$ High Time		●	30			ns
$t_{DCNVSCKL}$	SCK Quiet Time from $\overline{CNV}\downarrow$	(Note 11)	●	220			ns
$t_{DSCKLCNVH}$	SCK Delay Time to $\overline{CNV}\uparrow$	(Note 11)	●	0			ns
t_{SCK}	SCK Period	(Notes 12, 13)	●	15.6			ns
t_{SCKH}	SCK High Time		●	5			ns
t_{SCKL}	SCK Low Time		●	5			ns

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{DSCKSDOV}$	SDO Data Valid Delay from SCK↓	C_L = 5pF (Note 11)	●		4	7.4	ns
t_{HSDO}	SDO Data Remains Valid Delay from SCK↓	C_L = 5pF (Note 11)	●	2			ns
$t_{DCNVSDOV}$	Bus Acquisition Time from $\overline{CNV}$↓	C_L = 5pF (Note 11)	●		2.5	5	ns
$t_{DCNVSDOZ}$	Bus Relinquish Time After $\overline{CNV}$↑	(Note 11)	●			5	ns
t_{WAKE}	REFOUT Wake-Up Time	C_{REFOUT} = 10µF			10		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground.

Note 3: When these pin voltages are taken below ground, or above V_{DD} or OV_{DD}, they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground, or above V_{DD} or OV_{DD}, without latch-up.

Note 4: V_{DD} = 5V, OV_{DD} = 2.5V, REFOUT = 4.096V, f_{SMPL} = 2MHz.

Note 5: Recommended operating conditions.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Bipolar zero error is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 000 and 1111 1111 1111 111. Full-scale bipolar error is the worst-case of –FS or +FS untrimmed deviation from ideal first and last code transitions and includes the effect of offset error.

Note 8: All specifications in dB are referred to a full-scale ±4.096V input with REFOUT = 4.096V.

Note 9: When REFOUT is overdriven, the internal reference buffer must be turned off by setting REFIN = 0V.

Note 10: f_{SMPL} = 2MHz, I_{REFOUT} varies proportionally with sample rate.

Note 11: Guaranteed by design, not subject to test.

Note 12: Parameter tested and guaranteed at OV_{DD} = 1.71V and OV_{DD} = 2.5V.

Note 13: t_{SCK} of 15.6ns minimum allows a shift clock frequency up to 64MHz for falling edge capture.

Note 14: Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

Note 15: $\overline{CNV}$ is driven from a low jitter digital source, typically at OV_{DD} logic levels. This input pin has a TTL style input that will draw a small amount of current.

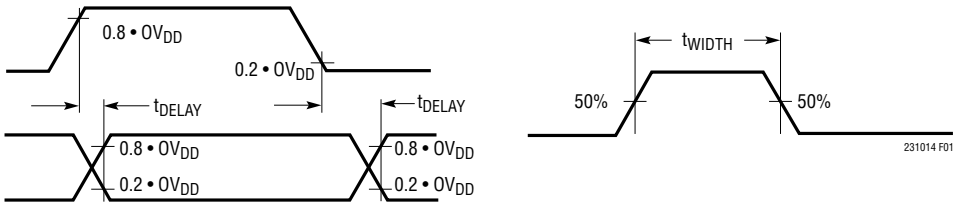
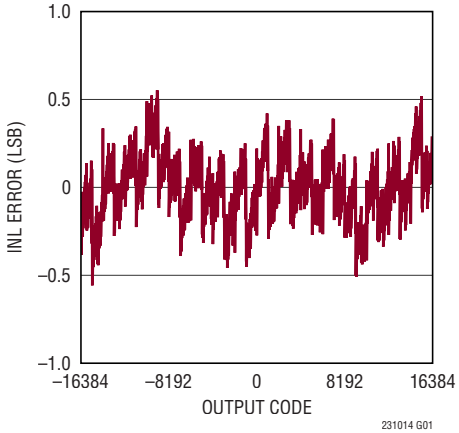


Figure 1. Voltage Levels for Timing Specifications

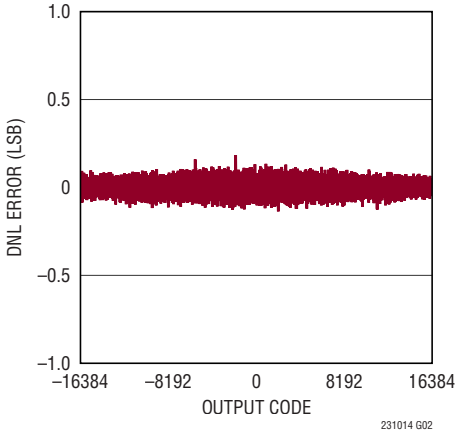
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFOUT = 4.096V, f_{SMPL} = 2Msps, unless otherwise noted.

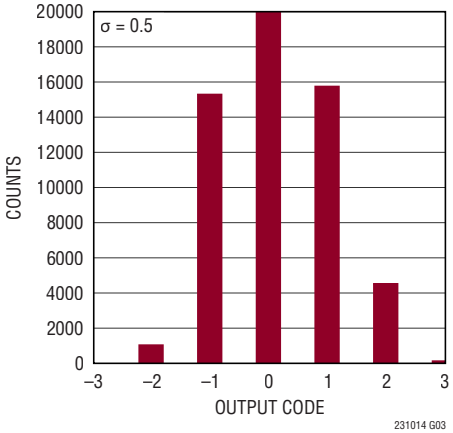
Integral Nonlinearity vs Output Code



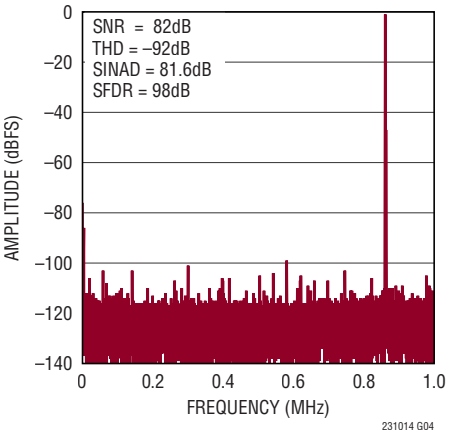
Differential Nonlinearity vs Output Code



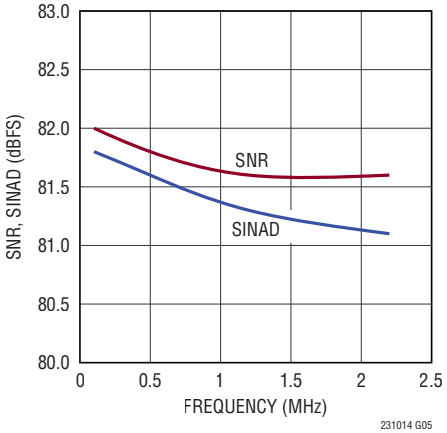
DC Histogram for 64k Samples



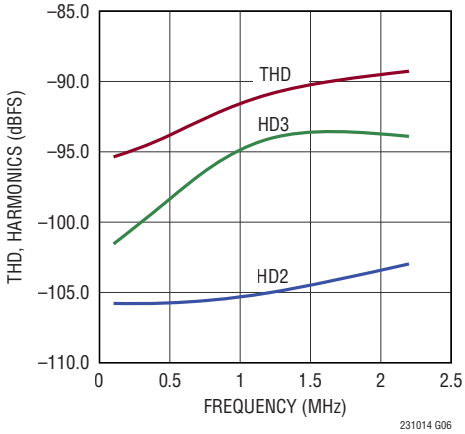
32k Point FFT, f_{SMPL} = 2Msps, f_{IN} = 1150kHz



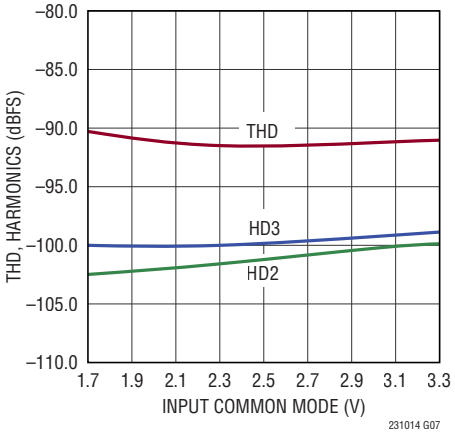
SNR, SINAD vs Input Frequency (100kHz to 2.2MHz)



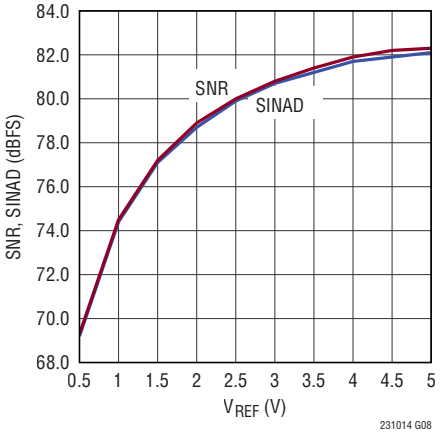
THD, Harmonics vs Input Frequency (100kHz to 2.2MHz)



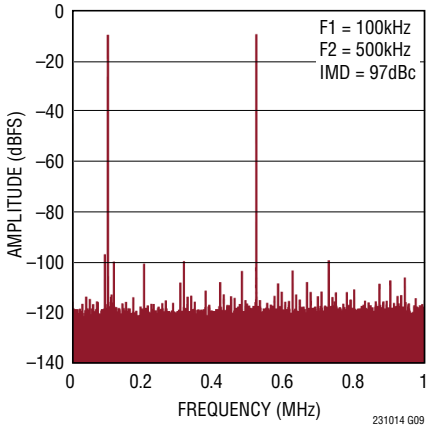
THD, Harmonics vs Input Common Mode (100kHz to 1.2MHz)



SNR, SINAD vs Reference Voltage, f_{IN} = 500kHz



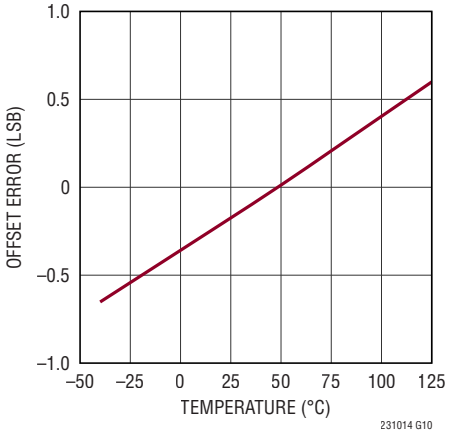
8k Point FFT, IMD, f_{SMPL} = 2Msps, A_{IN}^+ = 100kHz, A_{IN}^- = 500kHz



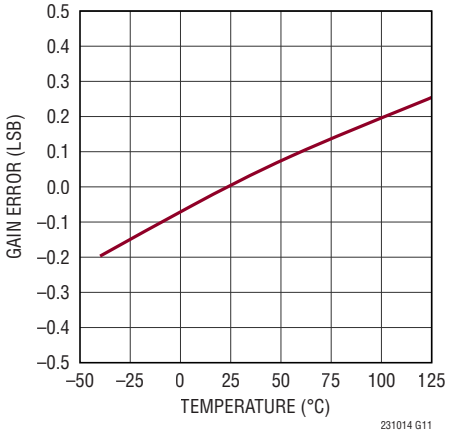
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFOUT = 4.096V, f_{SMPL} = 2Msps, unless otherwise noted.

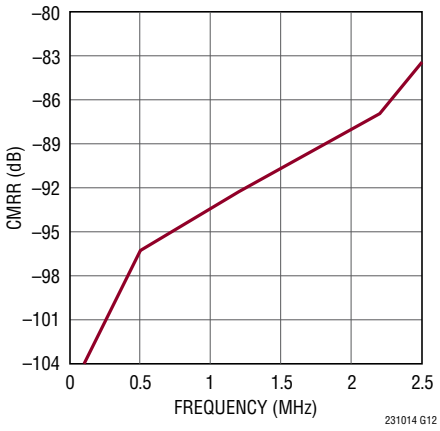
Offset Error vs Temperature



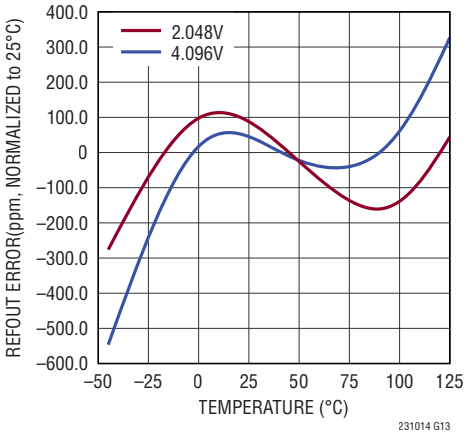
Gain Error vs Temperature



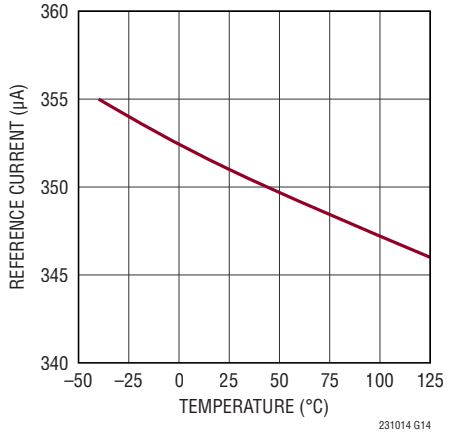
CMRR vs Input Frequency



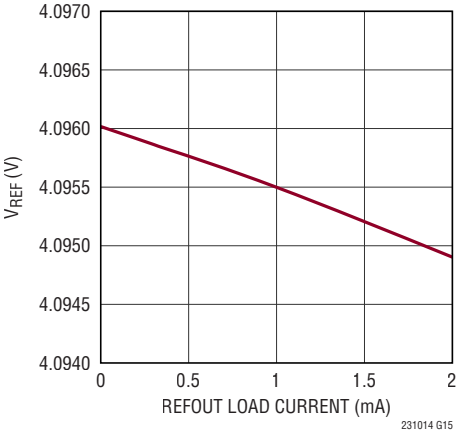
REFOUT Output vs Temperature



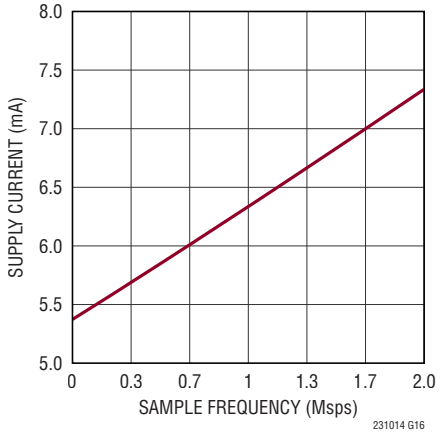
I_{REFOUT} vs Temperature, V_{REF} = 4.096V



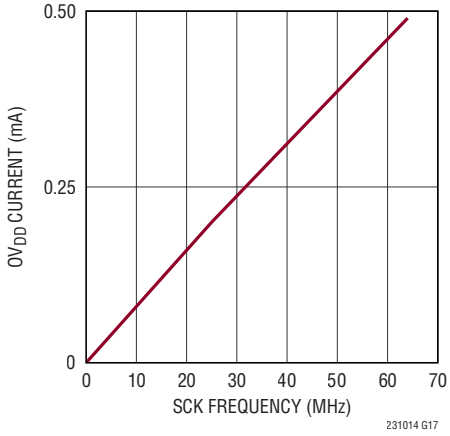
REFOUT Output Load Regulation



Supply Current vs Sample Frequency



OV_{DD} Current vs SCK Frequency, C_{LOAD} = 10pF



PIN FUNCTIONS

GND (Pins 1, 5, 8, 11): Ground. These pins and the exposed pad (Pin 17) must be tied directly to a solid ground plane.

REFIN (Pin 2): Reference Buffer 1.25V Input/Output. An onboard buffer nominally outputs 1.25V to this pin. This pin should be decoupled closely to the pin (no vias) with a 10µF (X5R, 0805 size) ceramic capacitor. The internal buffer driving this pin may be overdriven with an external reference. The REFIN pin, when pulled to GND disables the REFOUT pin buffer allowing an external reference to drive REFOUT directly.

REFOUT (Pin 3): Reference Buffer Output. An onboard buffer nominally outputs 4.096V to this pin. This pin should be decoupled closely to the pin (no vias) with a 10µF (X5R, 0805 size) ceramic capacitor. The internal buffer driving this pin may be disabled by grounding the REFIN pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25V to V_{DD}.

V_{DD} (Pin 4): Power Supply. Bypass V_{DD} to GND with a 1µF ceramic capacitor close to the V_{DD} pin.

A_{IN}^+, A_{IN}^- (Pins 6, 7): Analog Differential Input Pins. Full-scale range (A_{IN}^+ to A_{IN}^-) is ±REFOUT voltage. These pins can be driven from V_{DD} to GND.

$\overline{CNV}$ (Pin 9): Convert Input. When this pin is driven low, the conversion phase is initiated and output data is clocked out after the conversion delay (t_{CONV}). This input pin is a TTL style input typically driven at OV_{DD} levels with a low jitter pulse, but it is bound to V_{DD} levels. This pin is unaffected by the $\overline{CMOS}$/LVDS pin.

$\overline{CMOS}$/LVDS (Pin 10): I/O mode select. Ground this pin to enable CMOS mode, tie to OV_{DD} to enable LVDS mode. Float this pin to enable low power LVDS mode.

OV_{DD} (Pin 12): I/O Interface Digital Power. The range of OV_{DD} is 1.71V to 2.5V. This supply is nominally set to the same supply as the host interface (CMOS: 1.8V or 2.5V, LVDS: 2.5V). Bypass OV_{DD} to GND with a 1µF ceramic capacitor close to the OV_{DD} pin.

Exposed Pad (Pin 17): Ground. Solder this pad to ground.

CMOS I/O Mode

SDO^+ (Pin 14): Serial Data Output. The conversion result is shifted MSB first on each falling edge of SCK. The result is output on SDO^+. The logic level is determined by OV_{DD}. Do not connect SDO^- (Pin 13).

SCK^+ (Pin 16): Serial Data Clock Input. The falling edge of this clock shifts the conversion result MSB first onto the SDO pins. Drive SCK^+ with a single-ended clock. The logic level is determined by OV_{DD}. Do not connect SCK^- (Pin 15).

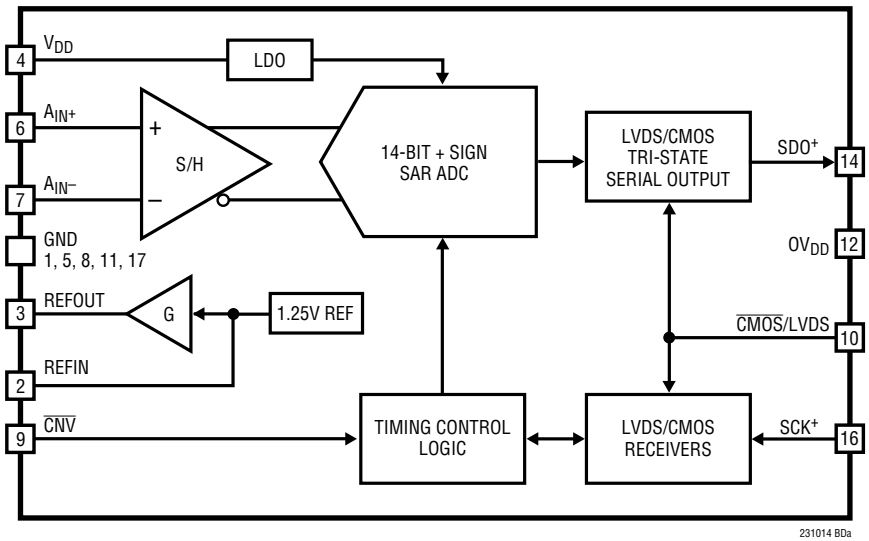
LVDS I/O Mode

SDO^+, SDO^- (Pins 14, 13): Serial Data Output. The conversion result is shifted MSB first on each falling edge of SCK. The result is output differentially on SDO^+ and SDO^-. These pins must be differentially terminated by an external 100Ω resistor at the receiver (FPGA).

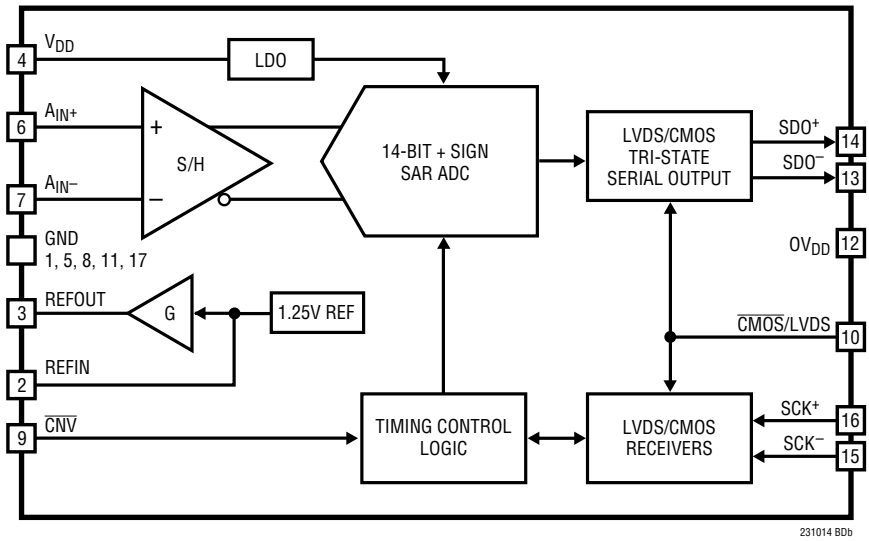
SCK^+, SCK^- (Pins 16, 15): Serial Data Clock Input. The falling edge of this clock shifts the conversion result MSB first onto the SDO pins. Drive SCK^+ and SCK^- with a differential clock. These pins must be differentially terminated by an external 100Ω resistor at the receiver (ADC).

FUNCTIONAL BLOCK DIAGRAM

CMOS I/O Mode

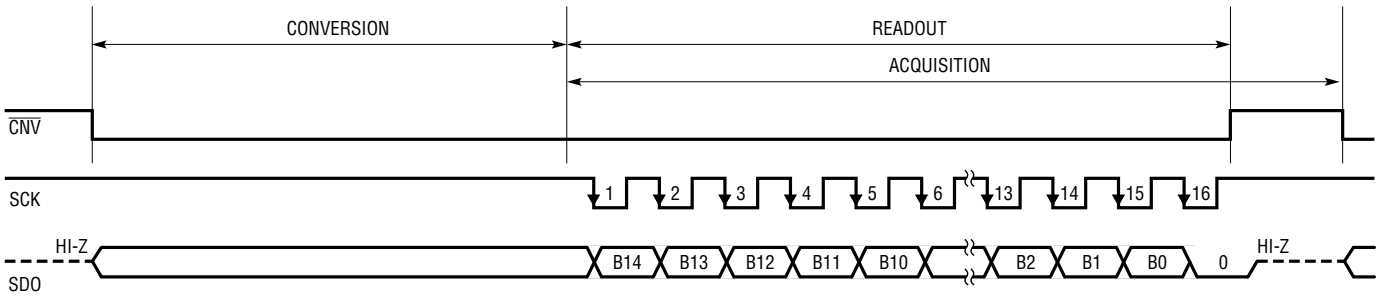


LVDS I/O Mode



TIMING DIAGRAM

CMOS, LVDS I/O Modes



SERIAL DATA BITS B[14:0] CORRESPOND TO CURRENT CONVERSION

231014 TD

APPLICATIONS INFORMATION

OVERVIEW

The LTC2310-14 is a low noise, high speed 14-bit + sign successive approximation register (SAR) ADC with differential inputs and a wide input common mode range. Operating from a single 3.3V or 5V supply, the LTC2310-14 has an $8V_{P-P}$ differential input range, making it ideal for applications which require a wide dynamic range. The LTC2310-14 achieves ±2LSB INL guaranteed, no missing codes at 14 bits and 82dB SNR typical.

The LTC2310-14 has an onboard reference buffer and low drift (20ppm/°C max) 4.096V temperature-compensated reference. The LTC2310-14 also has a high speed SPI-compatible serial interface that supports CMOS or LVDS. The fast 2Msps throughput with no cycle latency makes the LTC2310-14 ideally suited for a wide variety of high speed applications. The LTC2310-14 dissipates only 35mW operating at a 5V supply. Nap and sleep modes are also provided to reduce the power consumption of the LTC2310-14 during inactive periods for further power savings.

CONVERTER OPERATION

The LTC2310-14 operates in two phases. During the acquisition phase, the sample capacitor is connected to the analog input pins A_{IN+} and A_{IN-} to sample the differential analog input voltage, as shown in Figure 3. A falling edge on the $\overline{CNV}$ pin initiates a conversion. During the conversion phase, the 15-bit CDAC is sequenced through a successive approximation algorithm for each input SCK pulse, effectively comparing the sampled input with binary-weighted fractions of the reference voltage (e.g., $V_{REFOUT}/2$, $V_{REFOUT}/4$ … $V_{REFOUT}/32768$) using a differential comparator. At the end of conversion, the CDAC output approximates the sampled analog input. The ADC control logic then prepares the 15-bit digital output code for serial transfer. The data is clocked out on each falling edge of the SCK input clock.

TRANSFER FUNCTION

The LTC2310-14 digitizes the full-scale voltage of 2 × REFOUT into 2^{15} levels, resulting in an LSB size of 250µV with REFOUT = 4.096V. The ideal transfer function is shown in Figure 2. The output data is in 2's complement format.

Analog Input

The differential inputs of the LTC2310-14 provide great flexibility to convert a wide variety of analog signals with no configuration required. The LTC2310-14 digitizes the difference voltage between the A_{IN+} and A_{IN-} pins while supporting a wide common mode input range. The analog input signals can have an arbitrary relationship to each other, provided that they remain between V_{DD} and GND. The LTC2310-14 can also digitize more limited classes of analog input signals such as pseudo-differential unipolar/bipolar and fully differential with no configuration required.

The analog inputs of the LTC2310-14 can be modeled by the equivalent circuit shown in Figure 3. The back-to-back diodes at the inputs form clamps that provide ESD

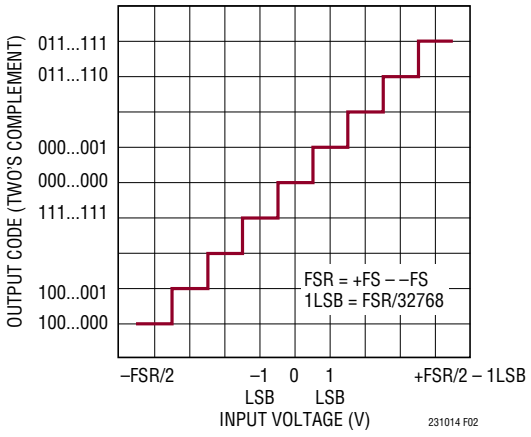


Figure 2. LTC2310-14 Transfer Function

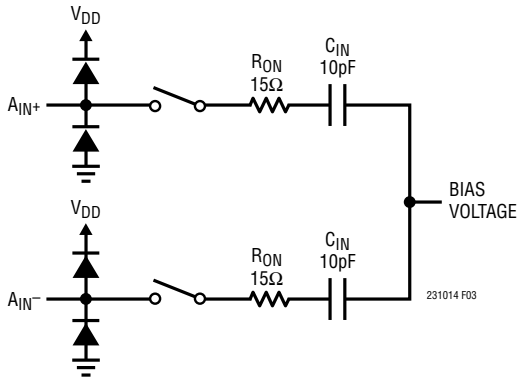


Figure 3. The Equivalent Circuit for the Differential Analog Input of the LTC2310-14

APPLICATIONS INFORMATION

protection. In the acquisition phase, 10pF (C_{IN}) from the sampling capacitor in series with approximately 15Ω (R_{ON}) from the on-resistance of the sampling switch is connected to the input. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the ADC sampler. The inputs of the ADC core draw a small current spike while charging the C_{IN} capacitors during acquisition.

Single-Ended Signals

Single-ended signals can be directly digitized by the LTC2310-14. These signals should be sensed pseudo-differentially for improved common mode rejection. By connecting the reference signal (e.g., ground sense) of the main analog signal to the other A_{IN} pin, any noise or disturbance common to the two signals will be rejected by the high CMRR of the ADC. The LTC2310-14 flexibility handles both pseudo-differential unipolar and bipolar signals, with no configuration required. The wide common mode input range relaxes the accuracy requirements of any signal conditioning circuits prior to the analog inputs.

Pseudo-Differential Bipolar Input Range

The pseudo-differential bipolar configuration represents driving one of the analog inputs at a fixed voltage, typically $V_{REF}/2$, and applying a signal to the other A_{IN} pin. In this case the analog input swings symmetrically around the fixed input yielding bipolar two's complement output codes with an ADC span of half of full-scale. This configuration is illustrated in Figure 4, and the corresponding transfer function in Figure 5. The fixed analog input pin need not be set at $V_{REF}/2$, but at some point within the V_{DD} rails allowing the alternate input to swing symmetrically around this voltage. If the input signal ($A_{IN+} - A_{IN-}$) swings beyond ±REFOUT/2, valid codes will be generated by the ADC and must be clamped by the user, if necessary.

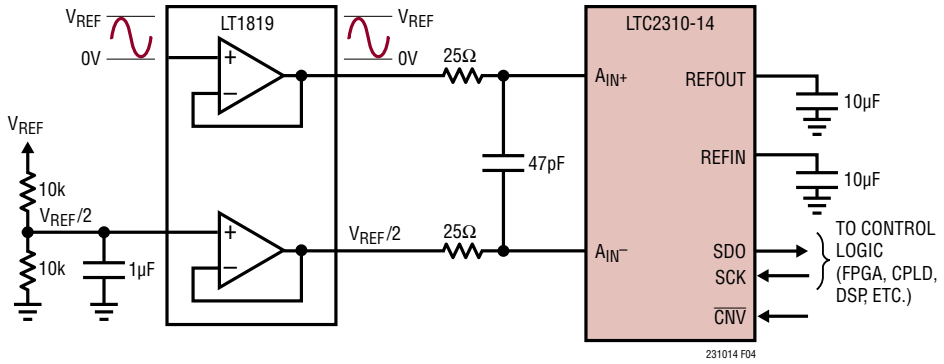


Figure 4. Pseudo-Differential Bipolar Application Circuit

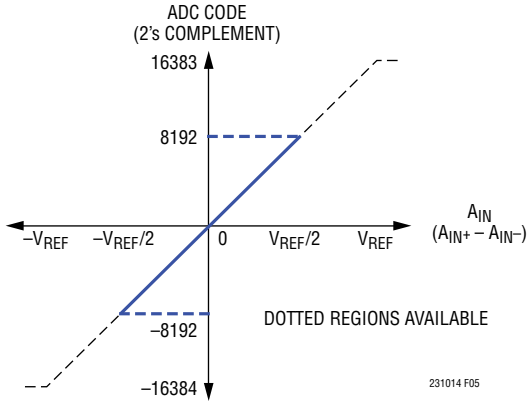


Figure 5. Pseudo-Differential Bipolar Transfer Function

APPLICATIONS INFORMATION

Pseudo-Differential Unipolar Input Range

The pseudo-differential unipolar configuration represents driving one of the analog inputs at ground and applying a signal to the other A_{IN} pin. In this case, the analog input swings between ground and V_{REF} yielding unipolar two's complement output codes with an ADC span of half of full-scale. This configuration is illustrated in Figure 6, and the corresponding transfer function in Figure 7. If the input signal ($A_{IN+} – A_{IN–}$) swings negative, valid codes will be generated by the ADC and must be clamped by the user, if necessary.

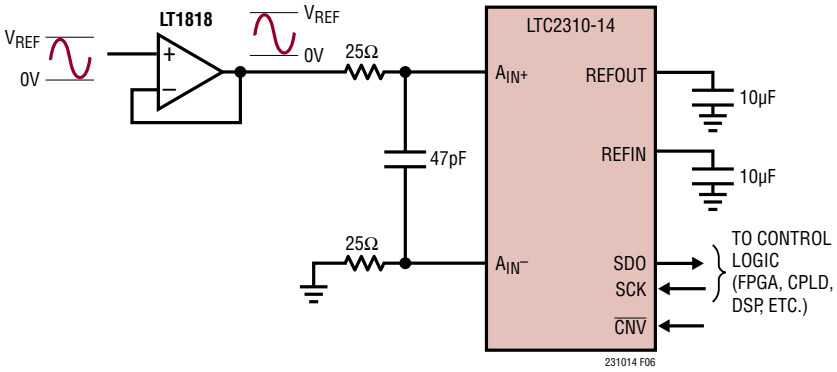


Figure 6. Pseudo-Differential Unipolar Application Circuit

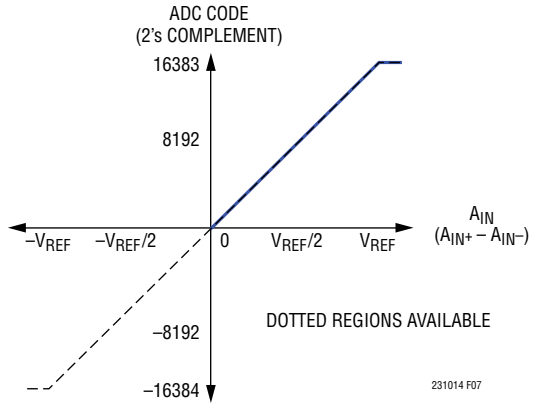


Figure 7. Pseudo-Differential Unipolar Transfer Function

APPLICATIONS INFORMATION

Single-Ended-to-Differential Conversion

While single-ended signals can be directly digitized as previously discussed, single-ended to differential conversion circuits may also be used when higher dynamic range is desired. By producing a differential signal at the inputs of the LTC2310-14, the signal swing presented to the ADC is maximized, thus increasing the achievable SNR.

The LT®1819 high speed dual operational amplifier is recommended for performing single-ended-to-differential conversions, as shown in Figure 8. In this case, the first amplifier is configured as a unity-gain buffer and the single-ended input signal directly drives the high impedance input of this amplifier.

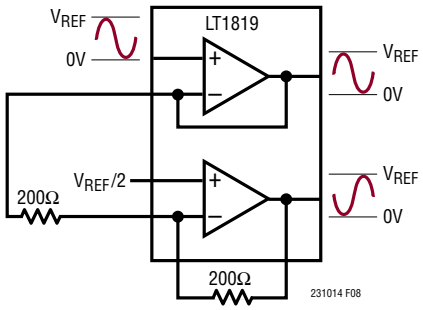


Figure 8. Single-Ended to Differential Driver

Fully-Differential Inputs

To achieve the best distortion performance of the LTC2310-14, we recommend driving a fully differential signal through LT1819 amplifiers configured as two unity-gain buffers, as shown in Figure 9. This circuit achieves the full data sheet THD specification of –90dB at input frequencies up to 500kHz. A full-differential input signal can span the maximum full-scale of the ADC, up to ±REFOUT. The common mode input voltage can span the entire supply range up to V_{DD} limited by the input signal swing. The fully-differential configuration is illustrated in Figure 10, with the corresponding transfer function illustrated in Figure 11.

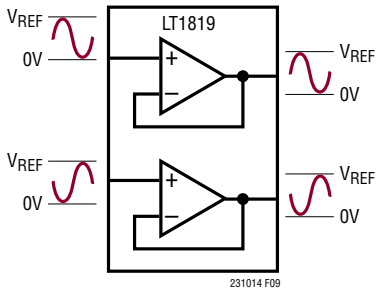


Figure 9. LT1819 Buffering a Fully-Differential Signal Source

APPLICATIONS INFORMATION

INPUT DRIVE CIRCUITS

A low impedance source can directly drive the high impedance inputs of the LTC2310-14 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize the distortion performance of the ADC. Minimizing settling time is important even for DC inputs, because the ADC inputs draw a current spike at the start of the acquisition phase.

For best performance, a buffer amplifier should be used to drive the analog inputs of the LTC2310-14. The amplifier provides low output impedance to minimize gain error and allow for fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the ADC inputs, which draw a small current spike during acquisition.

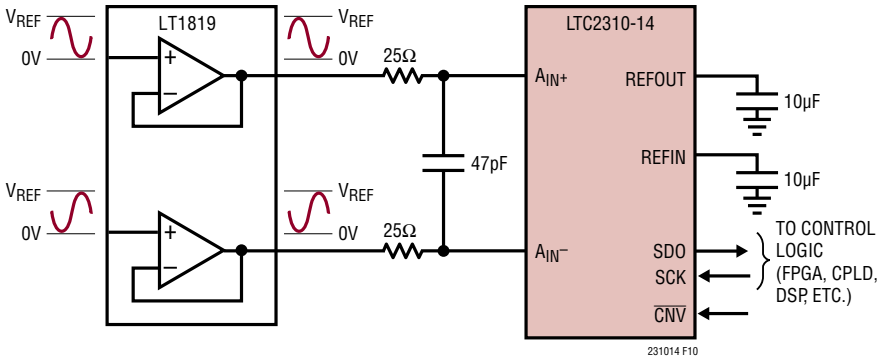


Figure 10. Fully-Differential Application Circuit

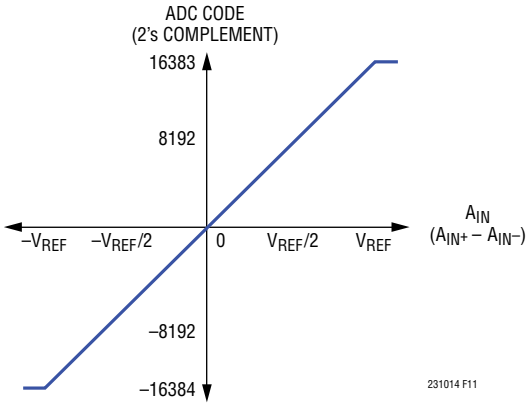


Figure 11. Fully-Differential Transfer Function

APPLICATIONS INFORMATION

Input Filtering

The noise and distortion of the buffer amplifier and signal source must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the buffer amplifier input with a low bandwidth filter to minimize noise. The simple 1-pole RC lowpass filter shown in Figure 12 is sufficient for many applications.

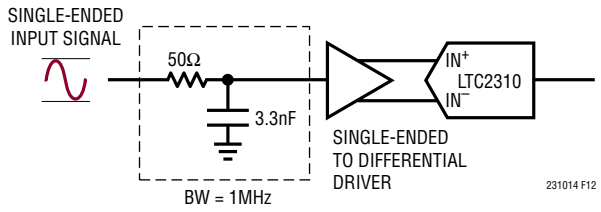


Figure 12. Input Signal Chain

The sampling switch on-resistance (R_{ON}) and the sample capacitor (C_{IN}) form a second lowpass filter that limits the input bandwidth to the ADC core to 110MHz. A buffer amplifier with a low noise density must be selected to minimize the degradation of the SNR over this bandwidth.

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

ADC REFERENCE

Internal Reference

The LTC2310-14 has an on-chip, low noise, low drift (20ppm/°C max), temperature compensated bandgap reference that is internally buffered and is available at REFIN (Pin 2). The internal reference buffer gains the REFIN pin voltage (1.25V) to REFOUT (pin 3) and is 4.096V for a 5V supply and 2.048V for 3.3V supply. Bypass REFOUT to GND with a 10µF (X5R, 0805 size) ceramic capacitor. The 10µF capacitor should be soldered as close as possible to the REFOUT pin to minimize wiring inductance. The REFIN pin produces a 1.25V precision reference which should also be bypassed with a 10µF (X5R, 0805 size) ceramic capacitor. The REFIN pin may be overdriven with an external precision reference as shown in Figure 13a.

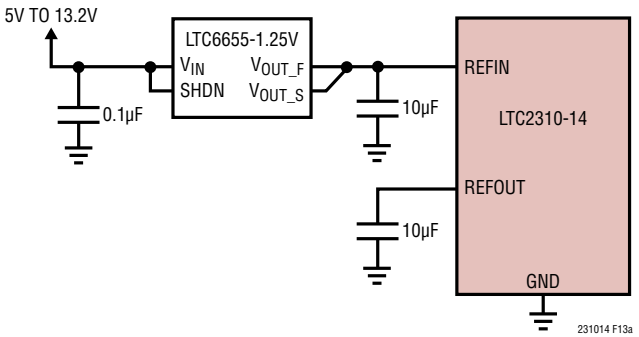


Figure 13a. LTC2310-14 with an External REFIN Voltage

Table 1. Internal Reference with Internal Buffer

V_{DD}	REFIN	REFOUT	FULLY DIFFERENTIAL INPUT RANGE	UNIPOLAR INPUT RANGE	BIPOLAR INPUT RANGE
5V	1.25V	4.096V	±4.096V	0V to 4.096V	±2.048V
3.3V	1.25V	2.048V	±2.048V	0V to 2.048V	±1.024V

Table 2. External Reference with Internal Buffer

V_{DD}	REFIN (OVER-DRIVEN)	REFOUT	FULLY DIFFERENTIAL INPUT RANGE	UNIPOLAR INPUT RANGE	BIPOLAR INPUT RANGE
5V	1V	3.3V	±3.3V	0V to 3.3V	±1.65V
	1.25V	4.096V	±4.096V	0V to 4.096V	±2.048V
	1.45V	4.7V	±4.7V	0V to 4.7V	±2.35V
3.3V	1V	1.65V	±1.65V	0V to 1.65V	±0.825V
	1.25V	2.048V	±2.048V	0V to 2.048V	±1.024V
	1.85	3V	±3V	0V to 3V	±1.5V

Table 3. External Reference Unbuffered

V_{DD}	REFIN	REFOUT	FULLY DIFFERENTIAL INPUT RANGE	UNIPOLAR INPUT RANGE	BIPOLAR INPUT RANGE
5V	0V	0.5V	±0.5V	0V to 0.5V	±0.25V
	0V	5V	±5V	0V to 5V	±2.5V
3.3V	0V	0.5V	±0.5V	0V to 0.5V	±0.25V
	0V	3.3V	±3.3V	0V to 3.3V	±1.65V

APPLICATIONS INFORMATION

External Reference

The internal reference buffer can also be overdriven from 1.25V to 5V with an external reference at REFOUT as shown in Figure 13b. In this configuration, REFIN must be grounded to disable the internal reference buffer. A 55kΩ internal resistance loads the REFOUT pin when the reference buffer is disabled. To maximize the input signal swing and corresponding SNR, the LTC6655-5 is recommended when overdriving REFOUT. The LTC6655-5 offers the same small size, accuracy, drift and extended temperature range as the LTC6655-4.096. By using a 5V reference, a higher SNR can be achieved. We recommend bypassing the LTC6655-5 with a 10µF ceramic capacitor (X5R, 0805 size) as close as possible to the REFOUT pin.

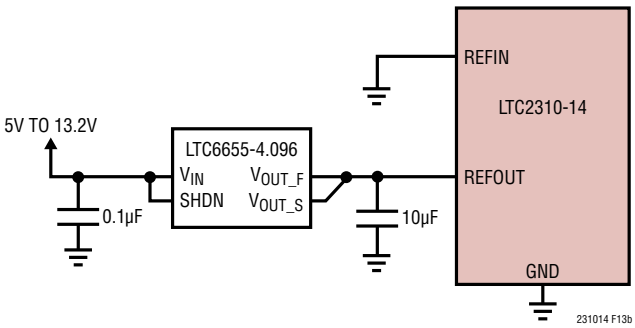


Figure 13b. LTC2310-14 with an External REFOUT Voltage

Internal Reference Buffer Transient Response

The REFOUT pin of the LTC2310-14 draws charge (Q_{CONV}) from the external bypass capacitors during each conversion cycle. If the internal reference buffer is overdriven, the external reference must provide all of this charge with a DC current equivalent to $I_{REFOUT} = Q_{CONV}/t_{CYC}$. Thus, the DC current draw of REFOUT depends on the sampling rate and output code. In applications where a burst of samples is taken after idling for long periods, as shown in Figure 14 , I_{REFOUT} quickly goes from approximately ~75µA to a maximum of 350µA for REFOUT = 5V at 2Msps. This step in DC current draw triggers a transient response in the external reference that must be considered since any deviation in the voltage at REFOUT will affect the accuracy of the output code. If an external reference is used to buffer/drive the REFOUT pin, the fast settling LTC6655 reference is recommended.

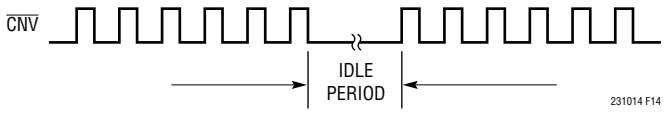


Figure 14. $\overline{CNV}$ Waveform Showing Burst Sampling

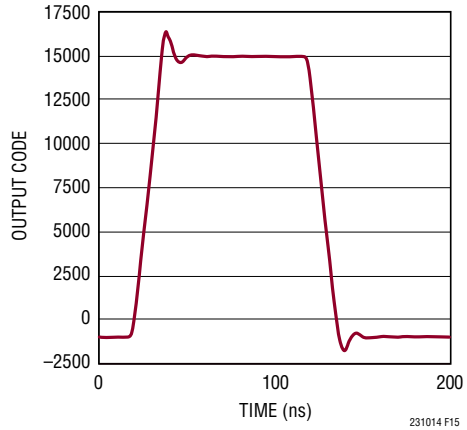


Figure 15. Transient Response of the LTC2310-14

DYNAMIC PERFORMANCE

Fast Fourier transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2310-14 provides guaranteed tested limits for both AC distortion and noise measurements.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the A/D output. The output is bandlimited to frequencies from above DC and below half the sampling

APPLICATIONS INFORMATION

frequency. Figure 16 shows that the LTC2310-14 achieves a typical SINAD of 81.7dB at a 2MHz sampling rate with a 500kHz input.

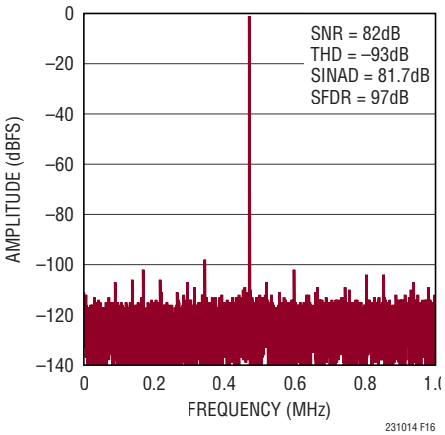


Figure 16. 32k Point FFT of the LTC2310-14

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 16 shows that the LTC2310-14 achieves a typical SNR of 82dB at a 2MHz sampling rate with a 500kHz input.

Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots + VN^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through VN are the amplitudes of the second through Nth harmonics. The THD specifications for the LTC2310-14 consider the first seven harmonics (i.e. N=7). Figure 16 shows that the LTC2310-14 achieves a typical THD of –93dB at a 2MHz sampling rate with a 500kHz input.

POWER CONSIDERATIONS

The LTC2310-14 requires two power supplies: the 5V power supply (V_{DD}), and the digital input/output interface power supply (OV_{DD}). The flexible OV_{DD} supply allows the LTC2310-14 to communicate with any digital logic operating between 1.8V and 2.5V. When using LVDS I/O, the OV_{DD} supply must be set to 2.5V.

Power Supply Sequencing

The LTC2310-14 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2310-14 has a power-on-reset (POR) circuit that will reset the LTC2310-14 at initial power-up or whenever the power supply voltage drops below 2V. Once the supply voltage re-enters the nominal supply voltage range, the POR will reinitialize the ADC. No conversions should be initiated until 10ms after a POR event to ensure the reinitialization period has ended. Any conversions initiated before this time will produce invalid results.

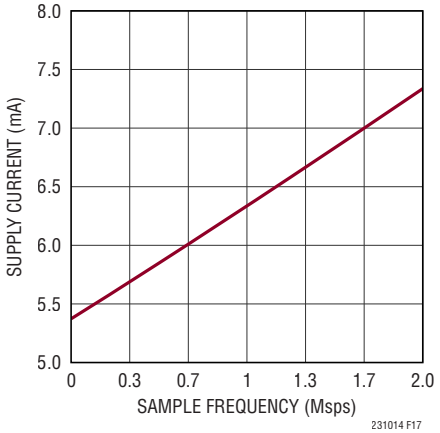


Figure 17. Power Supply Current of the LTC2310-14 Versus Sampling Rate

APPLICATIONS INFORMATION

TIMING AND CONTROL

$\overline{CNV}$ Timing

The LTC2310-14 conversion is controlled by $\overline{CNV}$. A falling edge on $\overline{CNV}$ will start the conversion process. The conversion process is internally timed. For optimum performance, $\overline{CNV}$ should be driven by a clean low jitter signal. The Typical Application at the back of the data sheet illustrates a recommended implementation to reduce the relatively large jitter from an FPGA $\overline{CNV}$ pulse source. Note the low jitter input clock times the falling edge of the $\overline{CNV}$ signal. The rising edge jitter of $\overline{CNV}$ is much less critical to performance. The minimum pulse width of the $\overline{CNV}$ signal is 30ns at a 2Msps conversion rate.

SCK Serial Data Clock Input

The falling edge of this clock shifts the conversion result MSB first onto the SDO pins. A 64MHz external clock must be applied at the SCK pin to achieve 2Msps throughput.

Nap/Sleep Modes

Nap mode is a method to save power without sacrificing power-up delays for subsequent conversions. Sleep mode has substantial power savings, but a power-up delay is incurred to allow the reference and power systems to become valid. To enter nap mode on the LTC2310-14, the SCK signal must be held high or low and a series of two $\overline{CNV}$ pulses must be applied. This is the case for both CMOS and LVDS modes. The second rising edge of $\overline{CNV}$ initiates the nap state. The nap state will persist until either a single rising edge of SCK is applied, or further $\overline{CNV}$ pulses are applied. The SCK rising edge will put the LTC2310-14 back into the operational (full-power) state. When in nap mode, two additional pulses will put the LTC2310-14 in sleep mode. When configured for CMOS I/O operation, a single rising edge of SCK can return the LTC2310-14 into operational mode. A 10ms delay is necessary after exiting sleep mode to allow the reference buffer to recharge the external filter capacitor. In LVDS mode, exit sleep mode by supplying a fifth $\overline{CNV}$ pulse. The fifth pulse will return the LTC2310-14 to operational mode, and further SCK pulses will keep the part from re-entering nap and sleep modes. The fifth SCK pulse also works in CMOS mode as a method to exit sleep. In the absence of SCK pulses, repetitive $\overline{CNV}$ pulses will cycle the LTC2310-14 between operational, nap and sleep modes indefinitely.

Refer to the timing diagrams in Figure 18, Figure 19, Figure 20 and Figure 21 for more detailed timing information about sleep and nap modes.

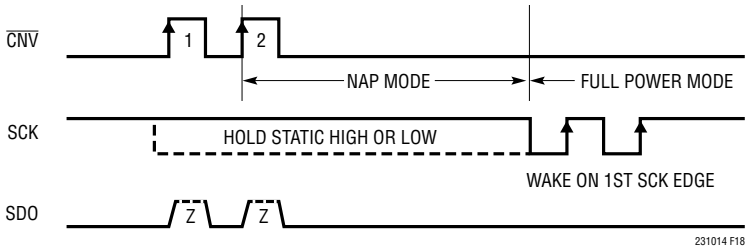


Figure 18. CMOS and LVDS Mode NAP and WAKE Using SCK

APPLICATIONS INFORMATION

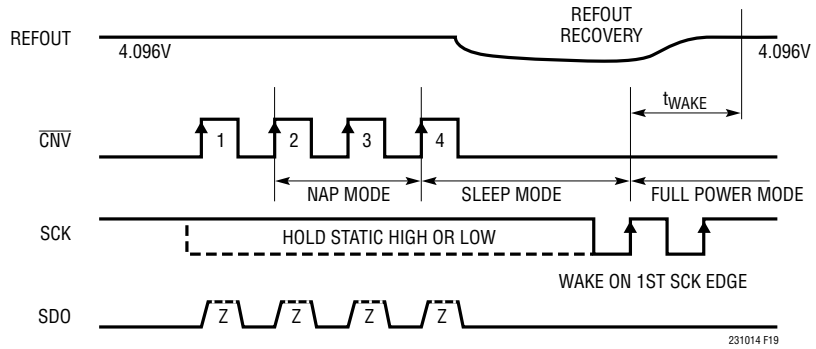


Figure 19. CMOS Mode SLEEP and WAKE Using SCK

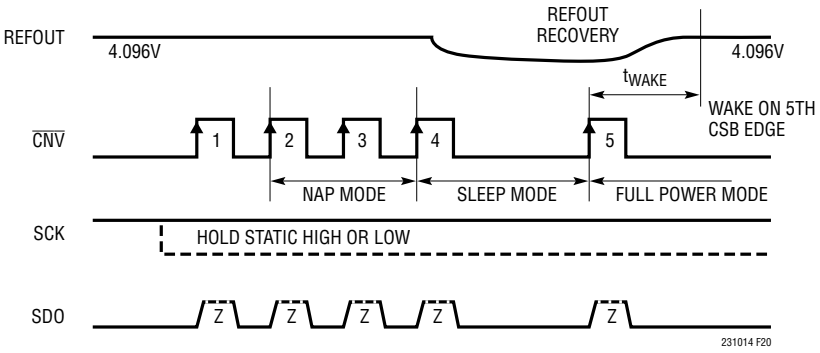
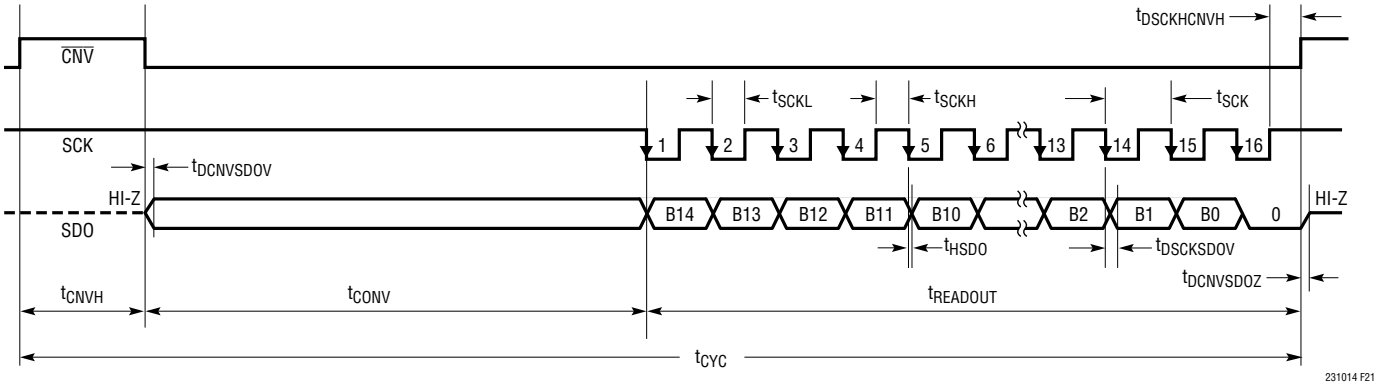


Figure 20. LVDS and CMOS Mode SLEEP and WAKE Using $\overline{CNV}$



SERIAL DATA BITS B[14:0] CORRESPOND TO CURRENT CONVERSION

Figure 21. LTC2310-14 Timing Diagram, CMOS, LVDS I/O Modes

APPLICATIONS INFORMATION

DIGITAL INTERFACE

The LTC2310-14 features a serial digital interface that is simple and straightforward to use. The flexible OV_{DD} supply allows the LTC2310-14 to communicate with any digital logic operating between 1.8V and 2.5V. A 64MHz external clock must be applied at the SCK pin to achieve 2Msps throughput.

In addition to a standard CMOS SPI interface, the LTC2310-14 provides an optional LVDS SPI interface to support low noise digital design. The $\overline{CMOS}$/LVDS pin is used to select the digital interface mode.

The falling edge of SCK outputs the conversion result MSB first on the SDO pins. In CMOS mode, use the SDO^+ pin as the serial data output and the SCK^+ pin as the serial clock input. Do not connect the SDO^- and SCK^- pins as they have internal pull-downs to GND.

In LVDS mode, use the SDO^+/SDO^- pins as a differential output. These pins must be differentially terminated by an external 100Ω resistor at the receiver (FPGA). The SCK^+/SCK^- pins are a differential input and must be terminated differentially by an external 100Ω resistor at the receiver (ADC), see Figure 22.

BOARD LAYOUT

To obtain the best performance from the LTC2310-14, a four layer printed circuit board is recommended. Layout for the printed circuit board (PCB) should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals adjacent to analog signals or underneath the ADC.

A single solid ground plane is used. Bypass capacitors to the supplies are placed as close as possible to the supply pins. Low impedance common returns for these bypass capacitors are essential to the low noise operation of the ADC. The analog input traces are screened by ground.

Reference Design

For a detailed look at the reference design for this converter, including schematics and PCB layout, please refer to the DC2425, the evaluation kit for the LTC2310-14.

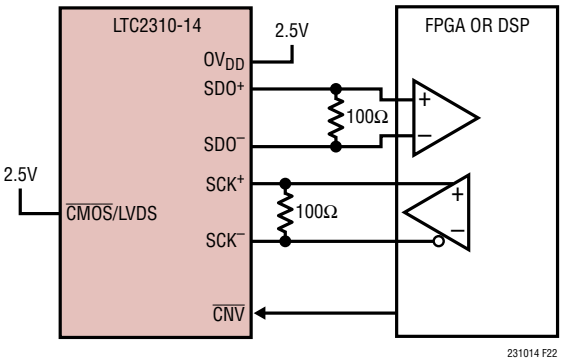
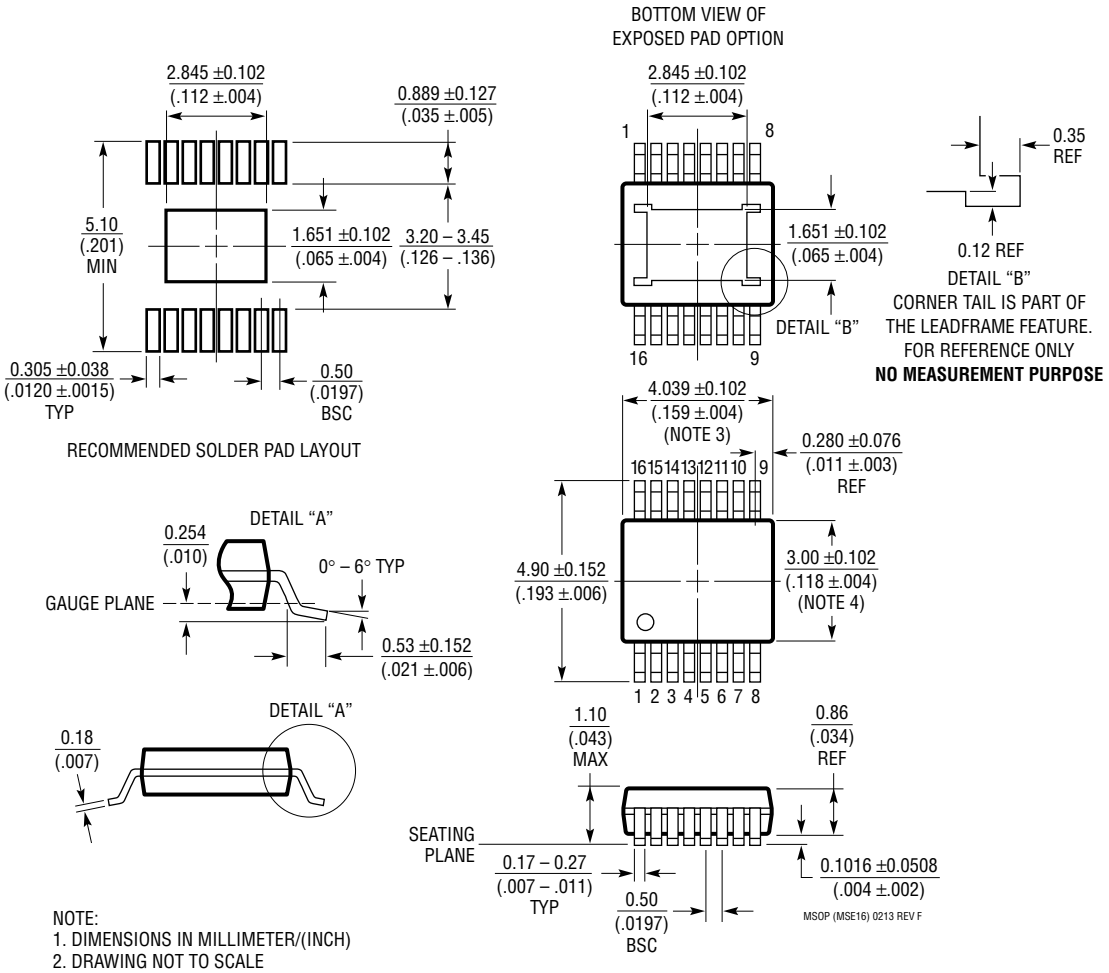


Figure 22. LTC2310-14 Using the LVDS Interface

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2310-14#packaging for the most recent package drawings.

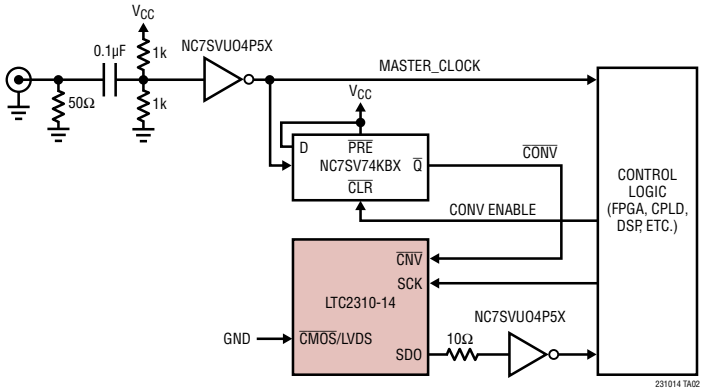
MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

TYPICAL APPLICATION

Low Jitter Clock Timing with RF Sine Generator Using Clock Squaring/Level-Shifting Circuit and Retiming Flip-Flop



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC2310-16	16-Bit, 2Msps, Differential Input ADC	3.3V/5V Supply, 35mW, 20ppm/°C Max Internal Reference, Flexible Inputs, 4mm × 5mm 16-Lead MSOP Package
LTC2311-16/LTC2311-14/ LTC2311-12	16-/14-/12-Bit, 5Msps, Differential Input ADC	3.3V/5V Supply, 50mW, 20ppm/°C Max Internal Reference, Flexible Inputs, 4mm × 5mm 16-Lead MSOP Package
LTC2323-16/LTC2323-14/ LTC2323-12	16-/14-/12-Bit, 5Msps, Simultaneous Sampling Dual ADCs	3.3V/5V Supply, 40mW/Ch, 20ppm/°C Max Internal Reference, Flexible Inputs, 4mm × 5mm QFN-28 Package
LTC1407/LTC1407-1	12-/14-Bit, 3Msps Simultaneous Sampling ADC	3V Supply, 2-Channel Differential, 1.5Msps per Channel Throughput, Unipolar/Bipolar Inputs, 14mW, MSOP Package
LTC2314-14	14-Bit, 4.5Msps Serial ADC	3V/5V Supply, 18mW/31mW, 20ppm/°C Max Internal Reference, Unipolar Inputs, 8-Lead TSOT-23 Package
LTC2321-16/LTC2321-14/ LTC2321-12	16-/14-/12-Bit, 2Msps, Simultaneous Sampling Dual ADCs	3.3V/5V Supply, 33mW/Ch, 10ppm°C Max Internal Reference, Flexible Inputs, 4mm × 5mm QFN-28 Package
LTC2370-16/LTC2368-16/ LTC2367-16/LTC2364-16	16-Bit, 2Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Pseudo-Differential Unipolar Input, 94dB SNR, 5V Input Range, DGC, Pin-Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2380-16/LTC2378-16/ LTC2377-16/LTC2376-16	16-Bit, 2Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 96.2dB SNR, ±5V Input Range, DGC, Pin-Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
DACs		
LTC2632	Dual 12-/10-/8-Bit, SPI V_{OUT} DACs with Internal Reference	2.7V to 5.5V Supply Range, 10ppm/°C Reference, External REF Mode, Rail-to-Rail Output, 8-Pin ThinSOT™ Package
LTC2602/LTC2612/ LTC2622	Dual 16-/14-/12-Bit SPI V_{OUT} DACs with External Reference	300µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, 8-Lead MSOP Package
References		
LTC6655	Precision Low Drift, Low Noise Buffered Reference	5V/4.096V/3.3V/3V/2.5V/2.048V/1.25V, 2ppm/°C, 0.25ppm Peak-to-Peak Noise, MSOP-8 Package
LTC6652	Precision Low Drift, Low Power Buffered Reference	5V/4.096V/3.3V/3V/2.5V/2.048V/1.25V, 5ppm/°C, 2.1ppm Peak-to-Peak Noise, MSOP-8 Package
Amplifiers		
LT1818/LT1819	400MHz, 2500V/µs, 9mA Single/Dual Operational Amplifiers	–85dBc Distortion at 5MHz, 6nV/√Hz Input Noise Voltage, 9mA Supply Current, Unity-Gain Stable
LT1806	325MHz, Single, Rail-to-Rail Input and Output, Low Distortion, Low Noise Precision Op Amps	–80dBc Distortion at 5MHz, 3.5nV/√Hz Input Noise Voltage, 9mA Supply Current, Unity-Gain Stable
LT6200	165MHz, Rail-to-Rail Input and Output, 0.95nV/√Hz Low Noise, Op Amp Family	Low Noise, Low Distortion, Unity-Gain Stable