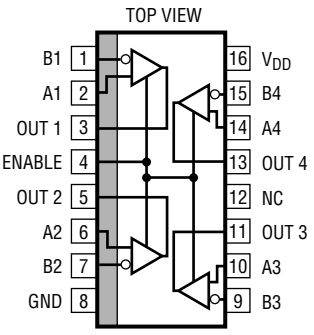
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 10V
Digital Input Currents ..... –100mA to 100mA
Digital Input Voltages ..... –0.5V to 10V
Receiver Input Voltages ..... ±10V
Receiver Output Voltages ..... –0.5V to V_{DD} + 0.5V
Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 90°C/W

ORDER PART NUMBER
LTC1520CS

Consult factory for Industrial and Military grade parts.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ±5% (Notes 2, 3) per receiver, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CM}	Input Common Mode Voltage	A, B Inputs	●	–0.2		V_{DD} + 0.2	V
V_{IH}	Input High Voltage	Enable Input	●	2			V
V_{IL}	Input Low Voltage	Enable Input	●			0.8	V
I_{IN1}	Input Current	Enable Input	●	–1		1	µA
I_{IN2}	Input Current (A, B)	V_A, V_B = 5V V_A, V_B = 0	● ●	 –250		250	µA µA
R_{IN}	Input Resistance (Figure 5)	–0.2V ≤ V_{CM} ≤ V_{DD} + 0.2V	●	18			kΩ
C_{IN}	A, B Input Capacitance	(Note 4)			3		pF
V_{OC}	Open-Circuit Input Voltage (Figure 5)	V_{DD} = 5V (Note 4)	●	3.2	3.3	3.4	V
$V_{ID(MIN)}$	Differential Input Threshold Voltage	–0.2V < V_{CM} < V_{DD} + 0.2V	●	–0.1		0.1	V
dV_{ID}	Input Hysteresis	V_{CM} = 2.5V	●		20		mV
V_{OH}	Output High Voltage	I_{OUT} = –4mA, V_{ID} = 0.1V, V_{DD} = 5V	●	4.6			V
V_{OL}	Output Low Voltage	I_{OUT} = 4mA, V_{ID} = 0.1V, V_{DD} = 5V	●			0.4	V
I_{OZR}	Three-State Output Current	0V ≤ V_{OUT} ≤ V_{DD}	●	–10		10	µA
I_{DD}	Total Supply Current All 4 Receivers	V_{ID} ≥ 0.1V, No Load, Enable = 5V	●		12	20	mA
I_{OSR}	Short-Circuit Current	V_{OUT} = 0V, V_{OUT} = V_{DD}	●	–50		50	mA
CMRR	Common Mode Rejection Ratio	V_{CM} = 2.5V, f = 25MHz			45		dB

SWITCHING TIME CHARACTERISTICS

V_{DD} = 5V ±5% (Notes 2, 3) V_{ID} = 500mV, V_{CM} = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}, t_{PHL}	Input-to-Output Propagation Delay	C_L = 15pF (Figure 1)	●	15	18	21	ns
t_r, t_f	Rise/Fall Times	C_L = 15pF			2.5		ns
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Skew	C_L = 15pF, Same Receiver (Note 5)	●		500		ps
t_{ZL}	Enable to Output Low	C_L = 15pF (Figure 2)	●		10	35	ns
t_{ZH}	Enable to Output High	C_L = 15pF (Figure 2)	●		10	35	ns
t_{LZ}	Disable from Output Low	C_L = 15pF (Figure 2)	●		20	35	ns
t_{HZ}	Disable from Output High	C_L = 15pF (Figure 2)	●		20	35	ns
t_{CH-CH}	Channel-to-Channel Skew	C_L = 15pF (Figure 3) (Note 6)	●		400		ps
$t_{PKG-PKG}$	Package-to-Package Skew	C_L = 15pF, Same Temperature (Figure 4, Note 4)			1.5		ns
	Minimum Input Pulse Width	(Note 4)			12		ns
f_{IN}	Maximum Input Frequency	(Note 4)			40		MHz

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. Recommended: V_{DD} = 5V ±5%.

Note 2: All currents into the device pins are positive; all currents out of the device pins are negative.

Note 3: All typicals are given for V_{DD} = 5V, T_A = 25°C.

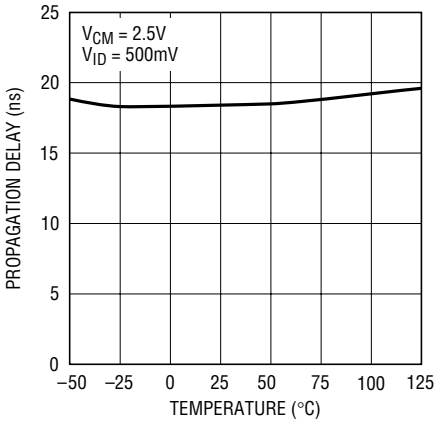
Note 4: Guaranteed by design, but not tested.

Note 5: Worst-case $\lvert t_{PLH} - t_{PHL} \rvert$ skew for a single receiver in a package over the full operating temperature range.

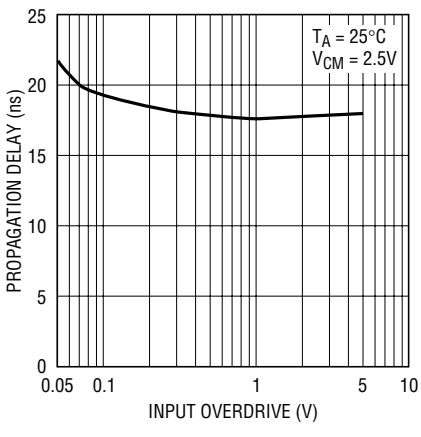
Note 6: Maximum difference between any two t_{PLH} or t_{PHL} transitions in a single package over the full operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

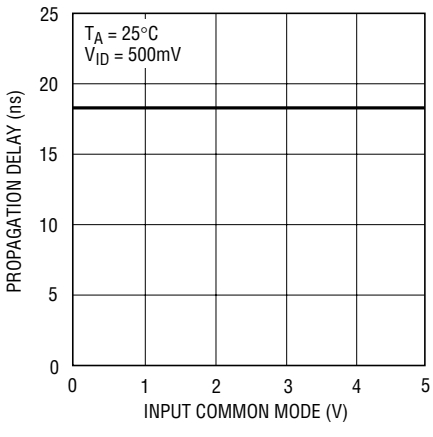
Propagation Delay (t_{PLH}/t_{PHL}) vs Temperature



Propagation Delay (t_{PLH}/t_{PHL}) vs Input Overdrive

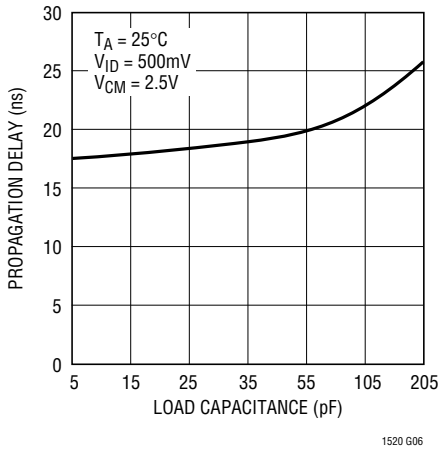


Propagation Delay (t_{PLH}/t_{PHL}) vs Input Common Mode



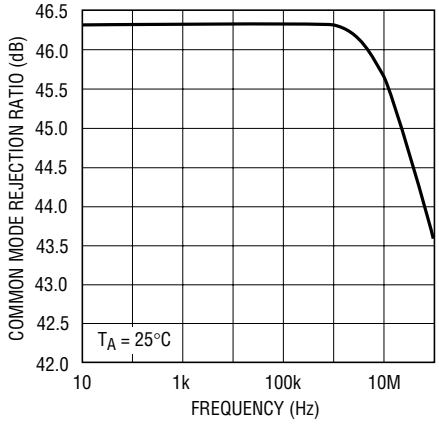
TYPICAL PERFORMANCE CHARACTERISTICS

Propagation Delay vs Load Capacitance (t_{PLH}/t_{PHL})



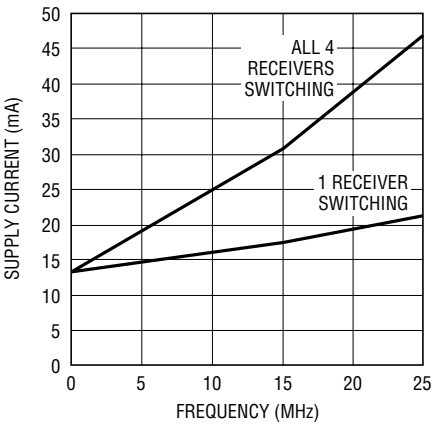
1520 G06

CMRR vs Frequency



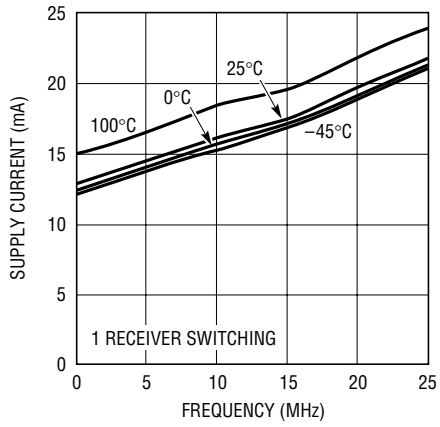
LTC1520 G04

Supply Current vs Frequency



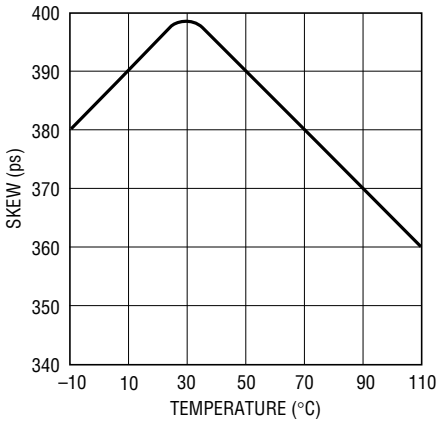
1520 G05

Supply Current vs Temperature and Frequency



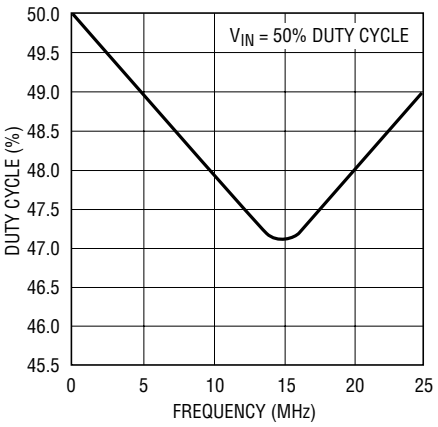
1520 G07

Skew vs Temperature (t_{SKD})



1520 G08

Output Duty Cycle vs Frequency



1520 G09

PIN FUNCTIONS

B1 (Pin 1): Receiver 1 Inverting Input.

A1 (Pin 2): Receiver 1 Noninverting Input.

RO1 (Pin 3): Receiver 1 Output.

Enable (Pin 4): Receiver Output Enable Pin. A logic high input enables the receiver outputs. A logic low input forces the receiver outputs into a high impedance state. Do not float.

RO2 (Pin 5): Receiver 2 Output.

A2 (Pin 6): Receiver 2 Noninverting Input.

B2 (Pin 7): Receiver 2 Inverting Input.

GND (Pin 8): Ground Pin. A ground plane is recommended for all LTC1520 applications.

B3 (Pin 9): Receiver 3 Inverting Input.

A3 (Pin 10): Receiver 3 Noninverting Input.

RO3 (Pin 11): Receiver 3 Output.

NC (Pin 12): No Connection.

RO4 (Pin 13): Receiver 4 Output.

A4 (Pin 14): Receiver 4 Noninverting Input.

B4 (Pin 15): Receiver 4 Inverting Input.

V_{DD} (Pin 16): 5V Supply Pin. This pin should be decoupled with a 0.1µF ceramic capacitor as close as possible to the pin. Recommended: V_{DD} = 5V ±5%.

SWITCHING TIME WAVEFORMS

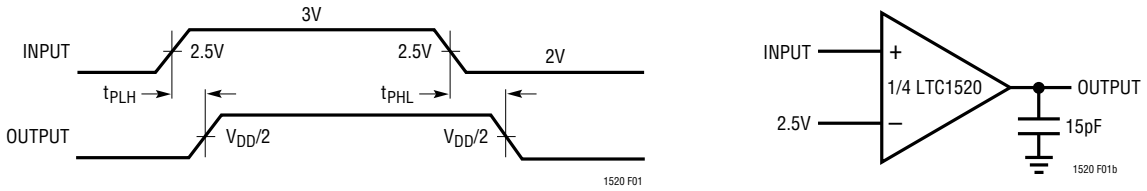


Figure 1. Propagation Delay Test Circuit and Waveforms

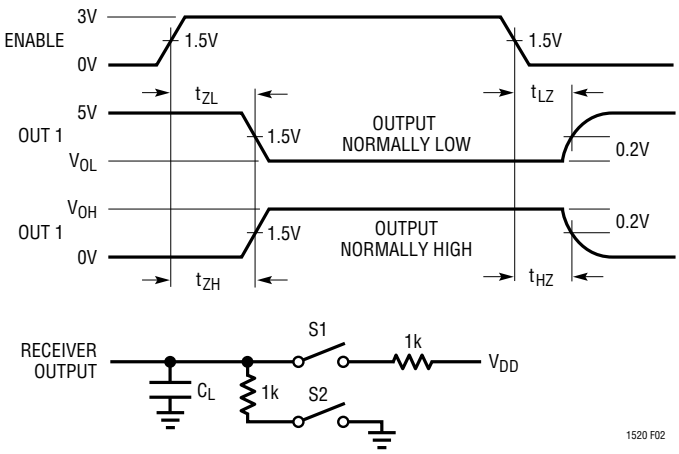


Figure 2. Receiver Enable and Disable Timing Test Circuit and Waveforms

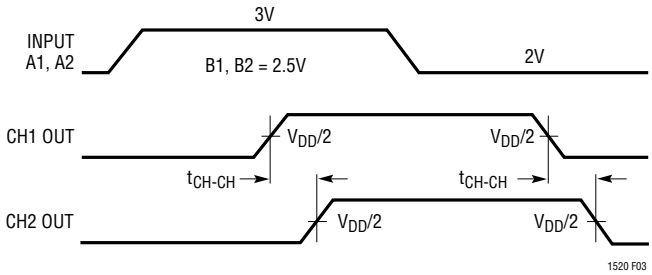


Figure 3. Any Channel to Any Channel Skew, Same Package

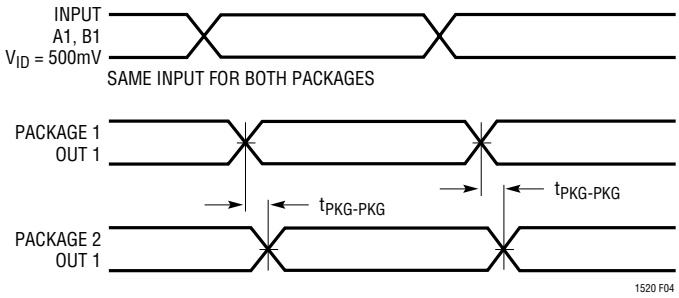


Figure 4. Package-to-Package Propagation Delay Skew

EQUIVALENT INPUT NETWORKS

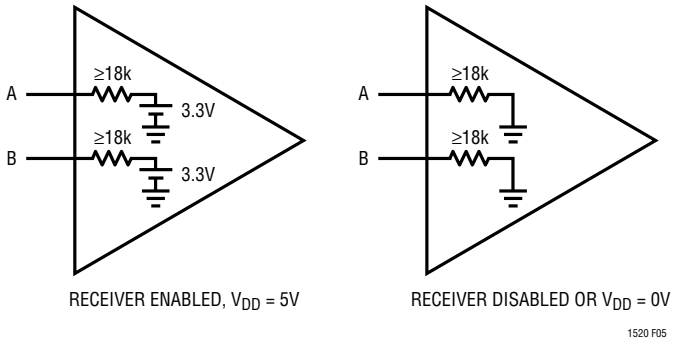


Figure 5. Input Thevenin Equivalent

APPLICATIONS INFORMATION

Theory of Operation

Unlike typical line receivers whose propagation delay can vary by as much as 500% from package to package and show significant temperature drift, the LTC1520 employs a novel architecture that produces a tightly controlled and temperature compensated propagation delay. The differential timing skew is also minimized between rising and falling output edges, and the propagation delays of any two receivers within a package are very tightly matched.

The precision timing features of the LTC1520 reduce overall system timing constraints by providing a narrow 6ns window during which valid data appears at the receiver output. This output timing window applies to all receivers in separate packages over all operating temperatures thereby making the LTC1520 well suited for high speed parallel data transmission applications such as backplanes.

In clocked data systems, the low skew minimizes duty cycle distortion of the clock signal. The LTC1520 can propagate signals at frequencies up to 25MHz (50Mbps) with less than 5% duty cycle distortion. When a clock signal is used to retime parallel data, the maximum recommended data transmission rate is 25Mbps to avoid timing errors due to clock distortion.

Rail-to-rail input common mode range enables the LTC1520 to be used in both single-ended and differential applications with transmission distances up to 100 feet. Thermal shutdown and short-circuit protection prevent latchup damage to the LTC1520 during fault conditions.

Single-Ended Applications

Over short distances, the LTC1520 can be configured to receive single-ended data by tying one input to a fixed bias voltage and connecting the other input to the driver output. In such applications, standard high speed CMOS logic may be used as a driver for the LTC1520. The receiver trip points may be easily adjusted to accommodate different driver output swings by changing the resistor divider at the fixed input. Figure 6a shows a single-ended receiver configuration with the driver and receiver connected via PC traces. Note that at very high speeds, transmission line and driver ringing effects have to be considered. Motorola's *MECL System Design Handbook* serves as an excellent reference for transmission line and termination effects. To mitigate transmission errors and duty cycle distortion due to driver ringing, a small output filter or a dampening resistor on V_{DD} may be needed as shown in Figure 6b. To transmit single-ended data over distances up to 10 feet, twisted pair is recommended with the unused wire grounded at both ends (Figure 7).

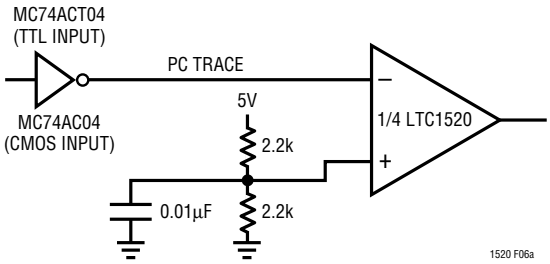


Figure 6a. Single-Ended Receiver

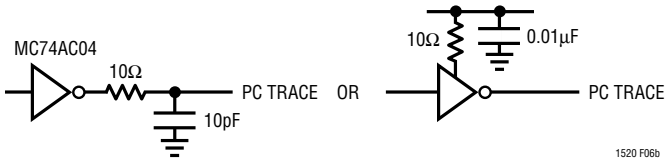


Figure 6b. Techniques to Minimize Driver Ringing

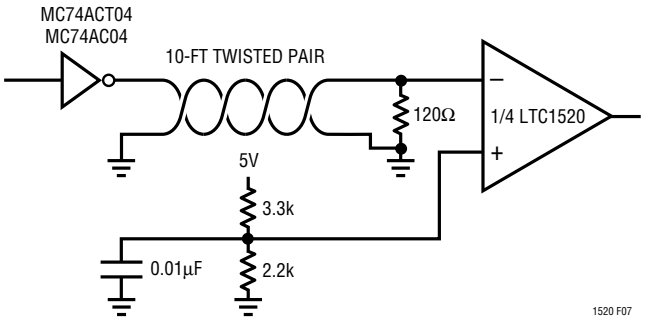


Figure 7. Medium Distance Single-Ended Transmission Using a CMOS Driver

Differential Transmission

The LTC1520 is well suited for medium distance differential transmission due to its rail-to-rail input common mode range. Clock rates up to 25MHz can be transmitted over 100 feet of high quality twisted pair. Figure 8 shows the

APPLICATIONS INFORMATION

LTC1520 receiving differential data from a PECL driver. As in the single-ended configurations, care must be taken to properly terminate the differential data lines to avoid unwanted reflections, etc.

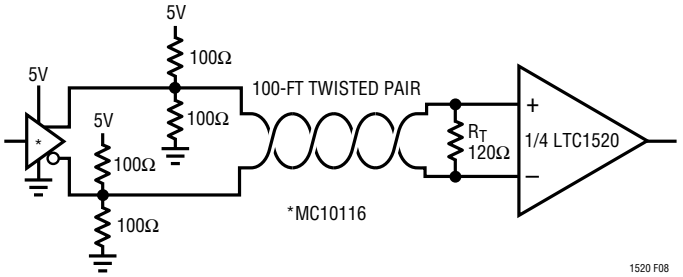


Figure 8. Differential Transmission Over Long Distances

Alternate Uses

The tightly controlled propagation delay of the LTC1520 allows the part to serve as a fixed delay element. Figure 9 shows the LTC1520 used as a tapped delay line with 18ns ±3ns steps. Several LTC1520s may be connected in series to form longer delay lines. Each tap in the delay line is accurate to within ±17% over temperature.

As shown in Figure 10, the LTC1520 can be used to create a temperature stable ring oscillator with period increments of 36ns. Low skew and good channel-to-channel matching enable this oscillator to achieve better than a 45/55 duty cycle (the duty cycle approaches 50/50 as more LTC1520s are used for lower frequencies). Note that the fixed voltage bias may either be created externally with a resistor divider or generated internally using a bypass capacitor and the internal open circuit bias point (approximately 3.3V). The use of the internal bias point will result in a 1% to 2% distortion of the duty cycle.

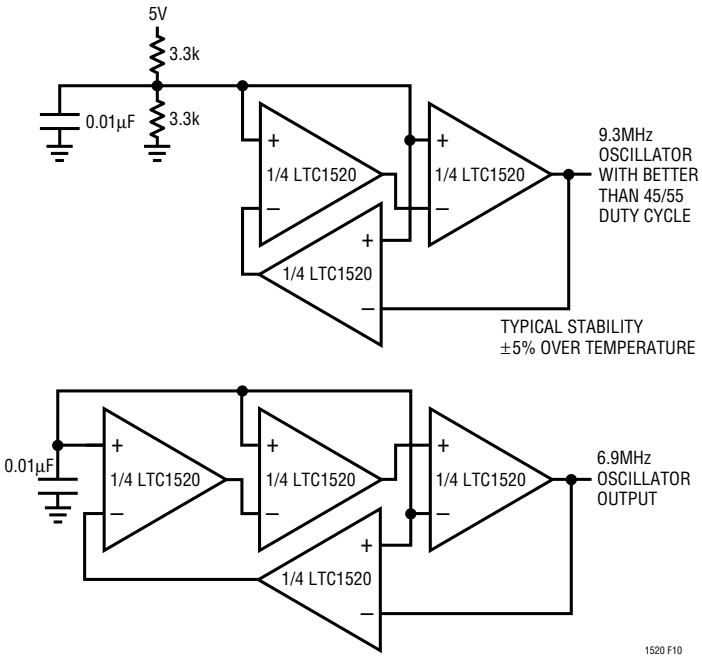


Figure 10. Temperature Stable Ring Oscillators

Layout Considerations

A ground plane is recommended when using a high frequency device like the LTC1520. A 0.1µF ceramic bypass capacitor less than 1/4 inch away from the V_{DD} pin is also recommended. Good bypassing is especially needed when all four channels are driven simultaneously by the same input. Under these conditions, and with a bypass capacitor more than 1 1/4 inches away from the V_{DD} pin, the parasitic inductances will cause ringing in the V_{DD} and output pins. This in turn can cause false triggering of the output short-circuit detector (Figure 11). When the bypass capacitor is placed close to the V_{DD} pin, however, the LTC1520 operates normally (Figure 12).

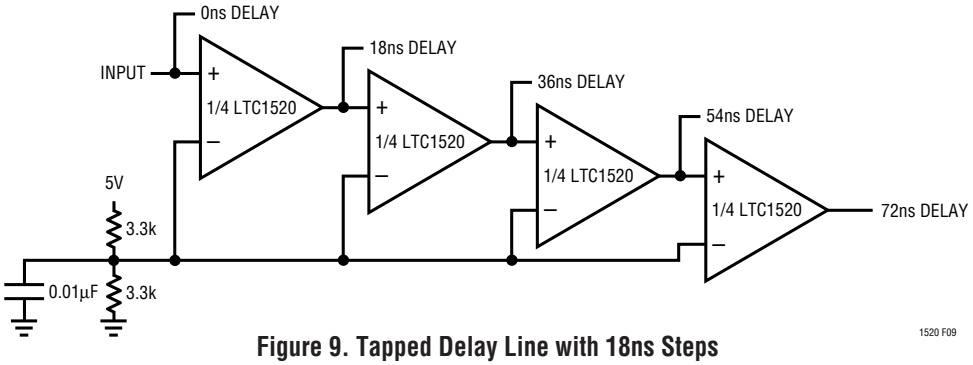


Figure 9. Tapped Delay Line with 18ns Steps

APPLICATIONS INFORMATION

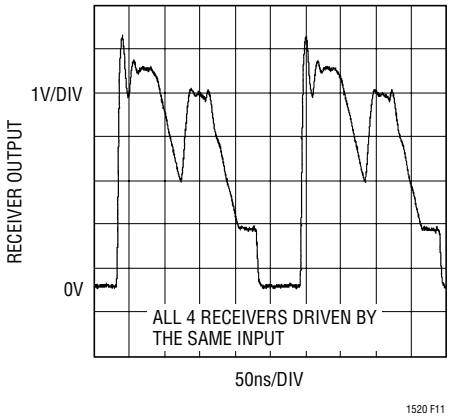


Figure 11. V_{DD} Bypassing > 1 1/4″ Away

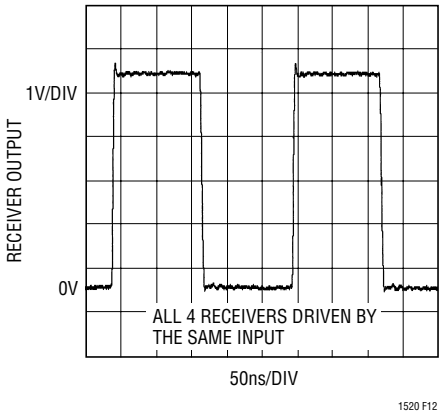
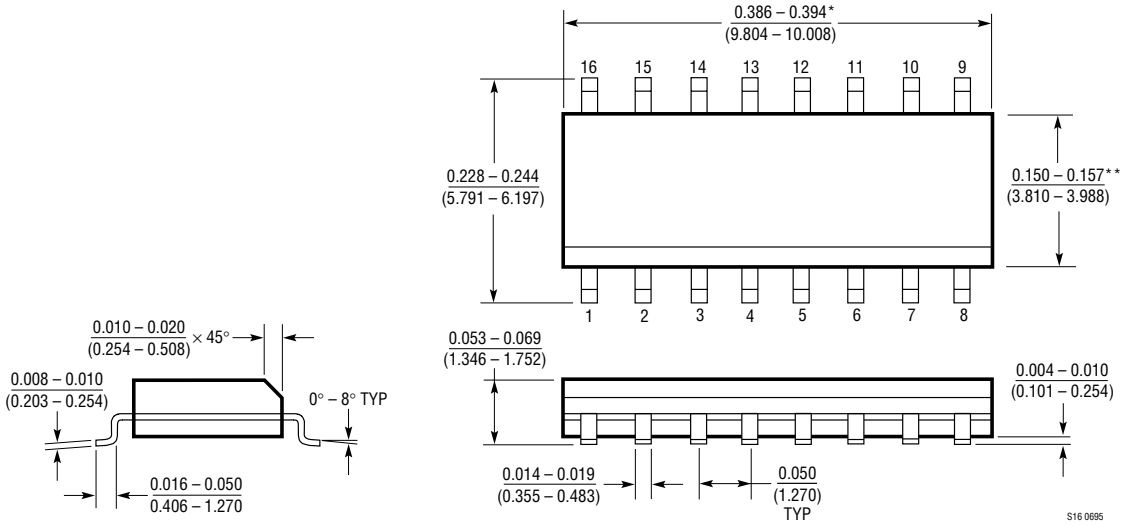


Figure 12. V_{DD} Bypassing < 3/8″ Away

PACKAGE DESCRIPTION

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC486/487	Low Power Quad RS485 Drivers	10Mbps, –7V to 12V Common Mode Range
LTC488/489	Low Power Quad RS485 Receivers	10Mbps, –7V to 12V Common Mode Range
LT®1016	Ultrafast Precision Comparator	Single 5V Supply, 10ns Propagation Delay
LTC1518	High Speed Quad RS485 Receiver	50Mbps, –7V to 12V Common Mode Range
LTC1519	High Speed Quad RS485 Receiver	50Mbps, –7V to 12V Common Mode Range

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977
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