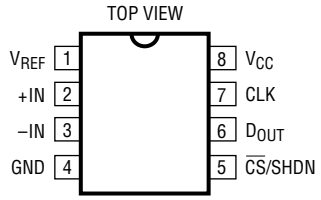
ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Supply Voltage (V_{CC}) to GND 12V
Voltage
  Analog and Reference ..... –0.3V to V_{CC} + 0.3V
  Digital Inputs ..... –0.3V to 12V
  Digital Output ..... –0.3V to V_{CC} + 0.3V

Power Dissipation 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

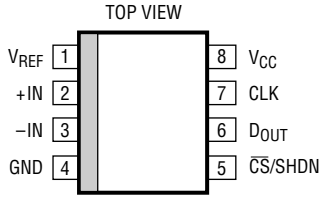
PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

T_{JMAX} = 150°C, θ_{JA} = 130°C/W

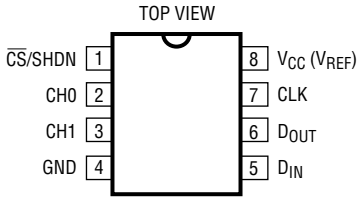
ORDER PART NUMBER
LTC1285CN8



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 175°C/W

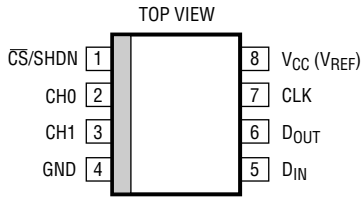
ORDER PART NUMBER	PART MARKING
LTC1285CS8	1285C



N8 PACKAGE
8-LEAD PDIP

T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1288CN8



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 175°C/W

ORDER PART NUMBER	PART MARKING
LTC1288CS8	1288C

Consult factory for Industrial and Military grade parts.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage (Note 3)	LTC1285 LTC1288	2.7 2.7		6 6	V V
f_{CLK}	Clock Frequency	V_{CC} = 2.7V	(Note 4)		120	kHz
t_{CYC}	Total Cycle Time	LTC1285, f_{CLK} = 120kHz LTC1288, f_{CLK} = 120kHz	125.0 141.5			µs µs
t_{hDI}	Hold Time, D_{IN} After CLK↑	V_{CC} = 2.7V	450			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Operating Sequence)	LTC1285, V_{CC} = 2.7V LTC1288, V_{CC} = 2.7V	2 2			µs µs
t_{suDI}	Setup Time, D_{IN} Stable Before CLK↑	V_{CC} = 2.7V	600			ns
t_{WHCLK}	CLK High Time	V_{CC} = 2.7V	3.5			µs
t_{WLCLK}	CLK Low Time	V_{CC} = 2.7V	3.5			µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	V_{CC} = 2.7V	2			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	LTC1285, f_{CLK} = 120kHz LTC1288, f_{CLK} = 120kHz	123.0 139.5			µs µs

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		LTC1285 MIN	LTC1285 TYP	LTC1285 MAX	LTC1288 MIN	LTC1288 TYP	LTC1288 MAX	UNITS
Resolution (No Missing Codes)		●	12			12			Bits
Integral Linearity Error	(Note 6)	●		±3/4	±2		±3/4	±2	LSB
Differential Linearity Error		●		±1/4	±3/4		±1/4	±3/4	LSB
Offset Error		●		±3/4	±3		±3/4	±3	LSB
Gain Error		●		±2	±8		±2	±8	LSB
Analog Input Range	(Note 7 and 8)	●		−0.05V to V_{CC} + 0.05V					V
REF Input Range (LTC1285) (Notes 7, 8, and 9)	$2.7 \le V_{CC} \le 6V$			1.5V to V_{CC} + 0.05V					V V
Analog Input Leakage Current (Note 10)		●		±1				±1	µA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	2			V
V_{IL}	Low Level Input Voltage	V_{CC} = 2.7V	●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			−2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 2.7V, I_O = 10µA V_{CC} = 2.7V, I_O = 360µA	● ●	2.4 2.1	2.64 2.30		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 2.7V, I_O = 400µA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS}$ = High	●			±3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			15		mA
R_{REF}	Reference Input Resistance (LTC1285)	$\overline{CS} = V_{IH}$ $\overline{CS} = V_{IL}$			2700 54		MΩ kΩ
I_{REF}	Reference Current (LTC1285)	$\overline{CS} = V_{CC}$ $t_{CYC} \ge 640µs$, $f_{CLK} \le 25kHz$ t_{CYC} = 134µs, f_{CLK} = 120kHz	● ●		0.001 50 50	2.5 70	µA µA µA
I_{CC}	Supply Current	$\overline{CS} = V_{CC}$	●		0.001	±3.0	µA
		LTC1285, $t_{CYC} \ge 640µs$, $f_{CLK} \le 25kHz$ LTC1285, t_{CYC} = 134µs, f_{CLK} = 120kHz	 ●		150 160	 320	µA µA
		LTC1288, $t_{CYC} \ge 720µs$, $f_{CLK} \le 25kHz$ LTC1288, t_{CYC} = 150µs, f_{CLK} = 120kHz	 ●		200 210	 390	µA µA

DYNAMIC ACCURACY f_{SMPL} = 7.5kHz (LTC1285), f_{SMPL} = 6.6kHz (LTC1288) (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
S/(N +D)	Signal-to-Noise Plus Distortion Ratio	1kHz Input Signal		67		dB
THD	Total Harmonic Distortion (Up to 5th Harmonic)	1kHz Input Signal		−80		dB
SFDR	Spurious-Free Dynamic Range	1kHz Input Signal		88		dB
	Peak Harmonic or Spurious Noise	1kHz Input Signal		−88		dB

AC CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			1.5		CLK Cycles
$f_{SMPL\,(MAX)}$	Maximum Sampling Frequency	LTC1285 LTC1288	● ●	7.5 6.6			kHz kHz
t_{CONV}	Conversion Time	See Operating Sequence			12		CLK Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		600	1500	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		220	660	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enable	See Test Circuits	●		180	500	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓	C_{LOAD} = 100pF			520		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		60	180	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		80	180	ns
C_{IN}	Input Capacitance	Analog Inputs, On Channel Analog Inputs, Off Channel Digital Input			20 5 5		pF pF pF

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: These devices are specified at 3V. For 5V specified devices, see LTC1286 and LTC1298.

Note 4: Increased leakage currents at elevated temperatures cause the sample-and-hold to droop, therefore it is recommended that $f_{CLK} \geq 75kHz$ at 70° and $f_{CLK} \geq 1kHz$ at 25°C.

Note 5: V_{CC} = 2.7V, V_{REF} = 2.5V and CLK = 120kHz unless otherwise specified.

Note 6: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below GND or one diode drop above V_{CC}. This spec allows 50mV forward bias of either diode for $2.7V \leq V_{CC} \leq 6V$. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV the output code will be correct. To achieve an absolute 0V to 2.7V input voltage range will therefore require a minimum supply voltage of 2.650V over initial tolerance, temperature variations and loading. For $2.7V < V_{CC} \leq 6V$, reference and analog input range cannot exceed 6.05V. If reference and analog input range are greater than 6.05V, the output code will not be guaranteed to be correct.

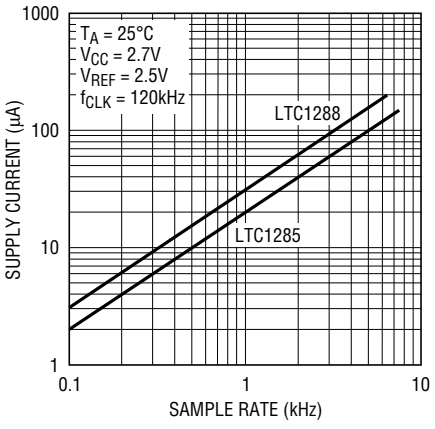
Note 8: The supply voltage range for the LTC1285 and the LTC1288 is from 2.7V to 6V.

Note 9: Recommended operating conditions

Note 10: Channel leakage current is measured after the channel selection.

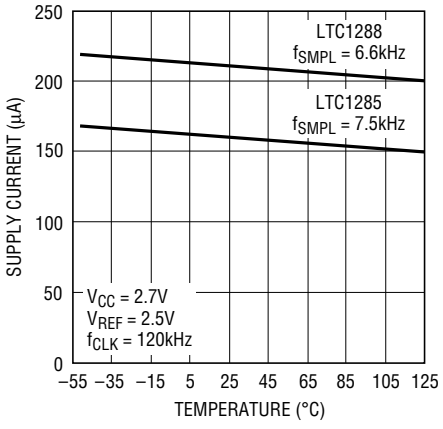
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Sample Rate



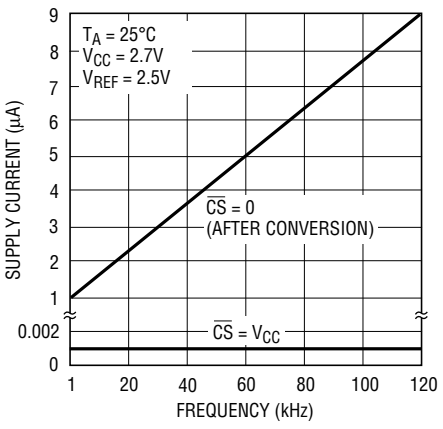
LTC1285/88 • TPC01

Supply Current vs Temperature



LTC1285/88 • TPC02

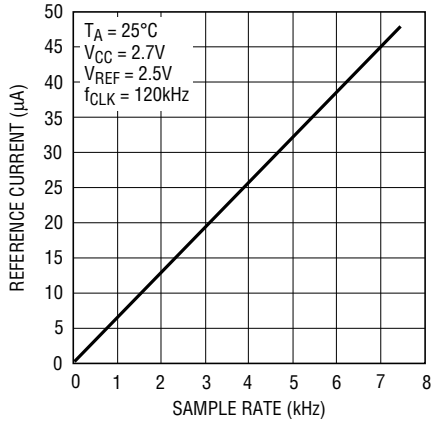
Shutdown Supply Current vs Clock Rate with $\overline{CS}$ High and $\overline{CS}$ Low



LTC1285/88 • TPC03

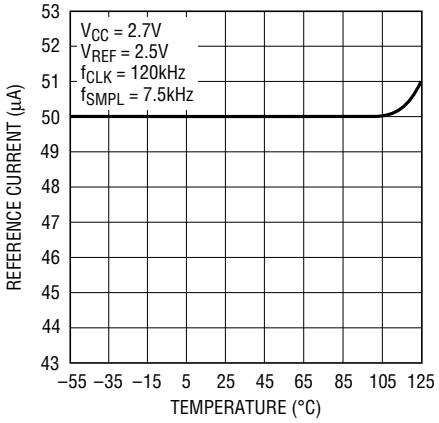
TYPICAL PERFORMANCE CHARACTERISTICS

Reference Current vs Sample Rate (LTC1285)



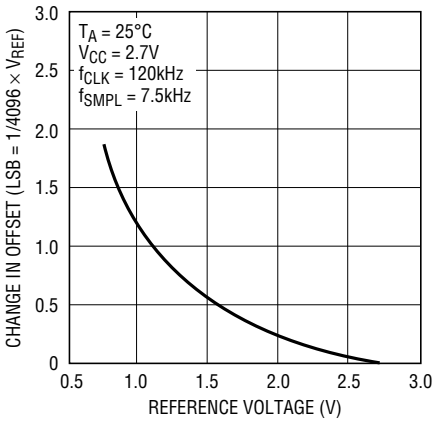
LTC1285/88 • TPC04

Reference Current vs Temperature



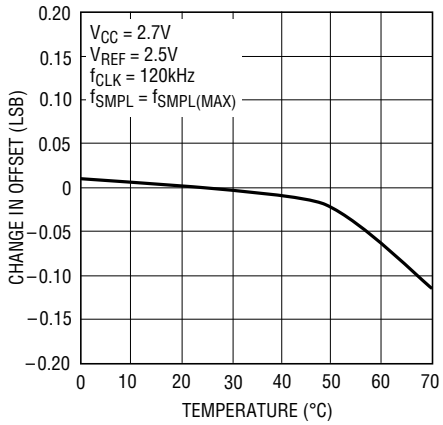
LTC1285/88 • TPC05

Change in Offset vs Reference Voltage



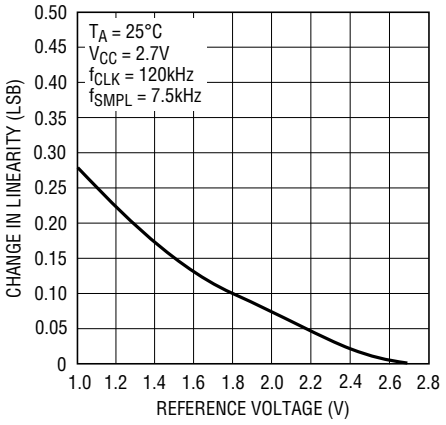
LTC1285/88 • TPC06

Change in Offset vs Temperature



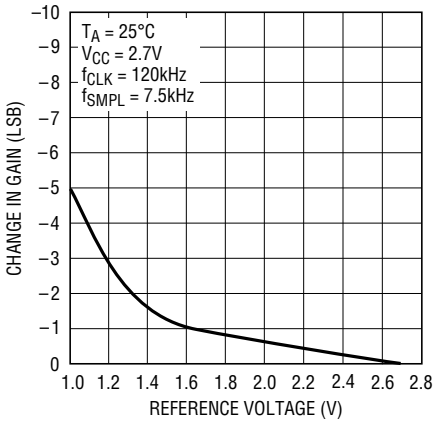
LTC1285/88 • TPC07

Change in Linearity vs Reference Voltage



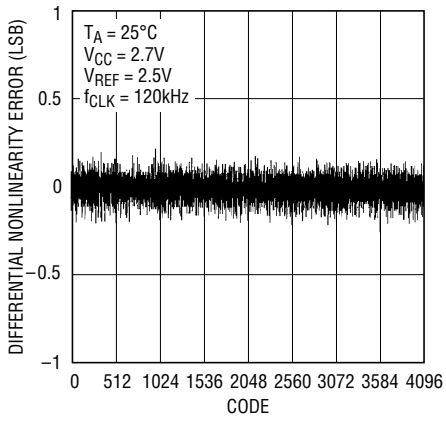
LTC1285/88 • TPC08

Change in Gain vs Reference Voltage



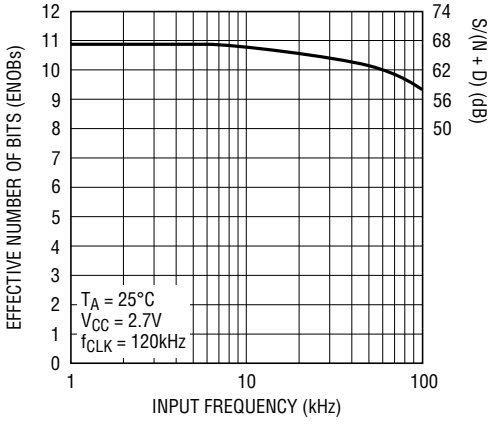
LTC1285/88 • TPC09

Differential Nonlinearity vs Code



LTC1285/88 • TPC11

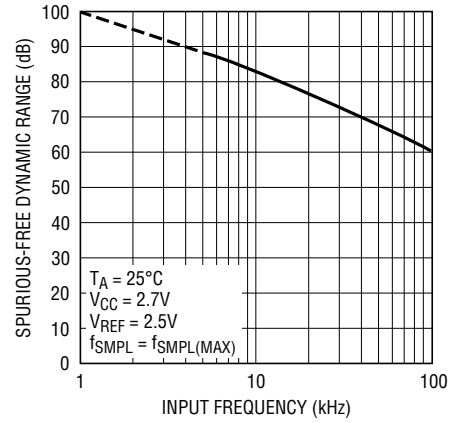
Effective Bits and S/(N + D) vs Input Frequency



LTC1285/88 • TPC12

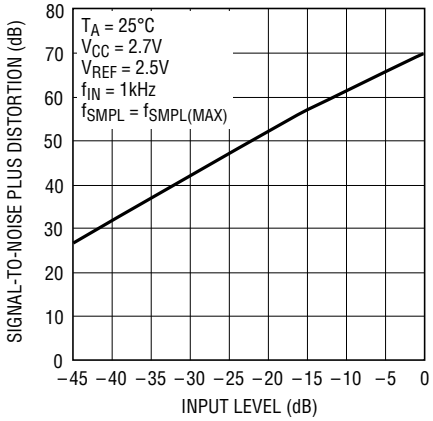
TYPICAL PERFORMANCE CHARACTERISTICS

Spurious-Free Dynamic Range vs Input Frequency



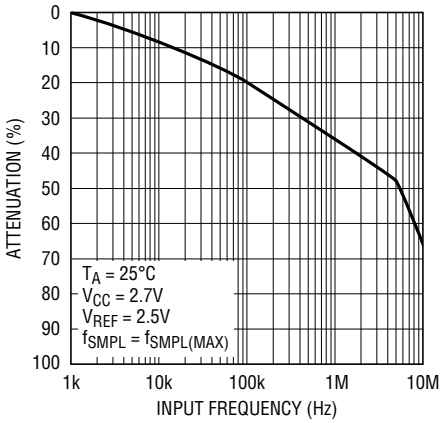
LTC1285/88 • G13

S/(N + D) vs Input Level



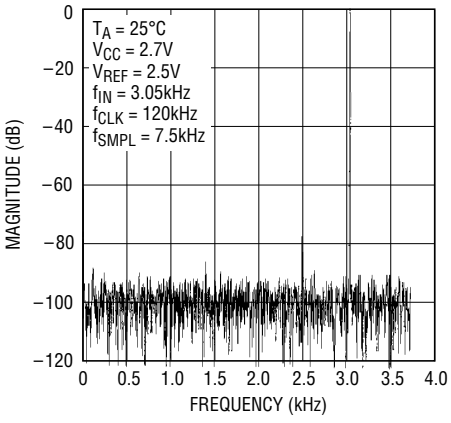
LTC1285/88 • TPC14

Attenuation vs Input Frequency



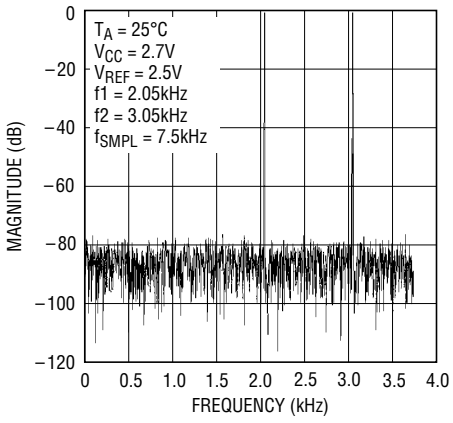
LTC1285/86 • TPC15

4096 Point FFT Plot



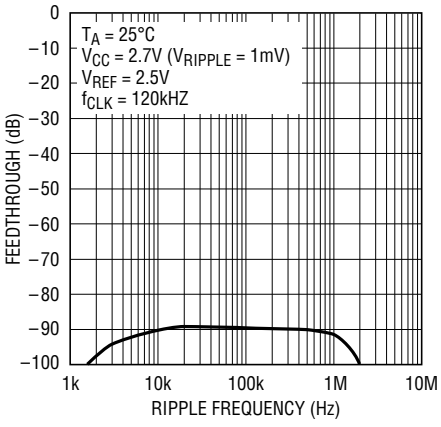
LTC1285/88 • TPC16

Intermodulation Distortion



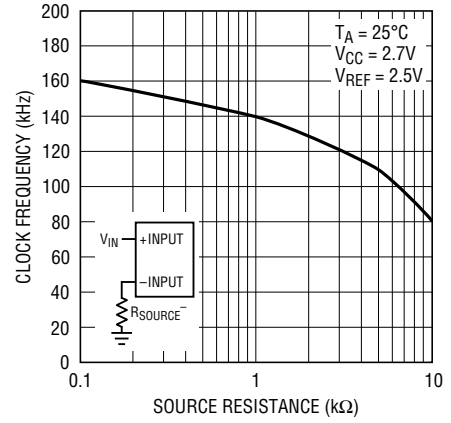
LTC1285/88 • TPC17

Power Supply Feedthrough vs Ripple Frequency



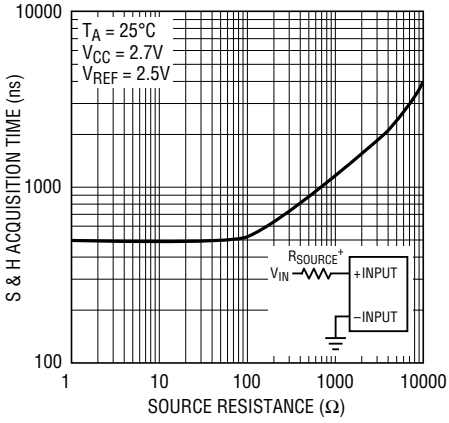
LTC1285/86 • TPC18

Maximum Clock Frequency vs Source Resistance



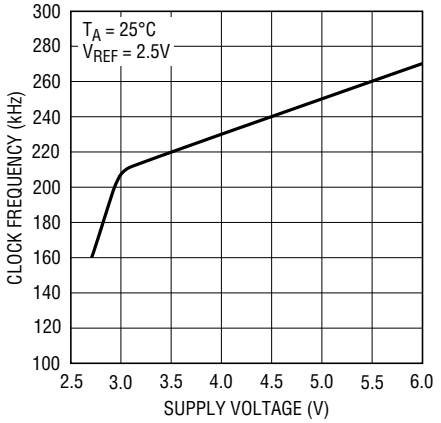
LTC1285/88 • G19

Sample-and-Hold Acquisition Time vs Source Resistance



LTC1285/88 • TPC20

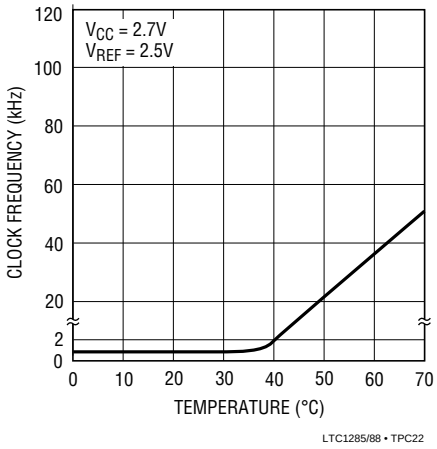
Maximum Clock Frequency vs Supply Voltage



LTC1285/88 • TPC21

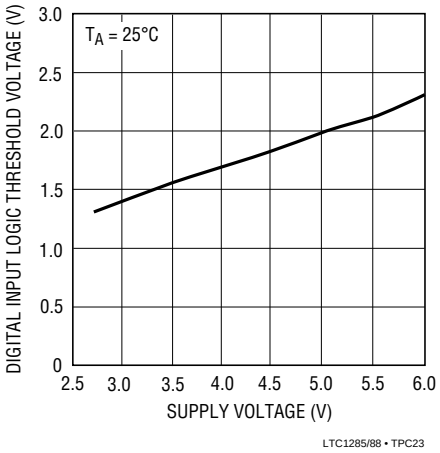
TYPICAL PERFORMANCE CHARACTERISTICS

Minimum Clock Frequency for 0.1 LSB Error vs Temperature



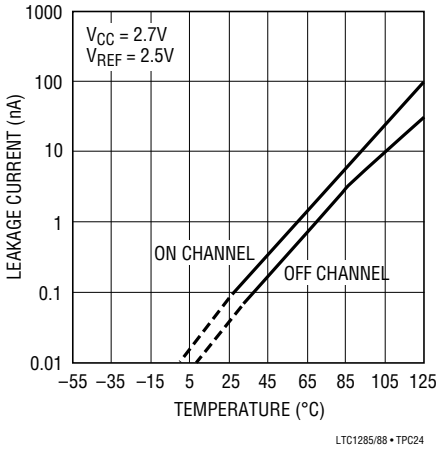
LTC1285/88 • TPC22

Digital Input Logic Threshold vs Supply Voltage



LTC1285/88 • TPC23

Input Channel Leakage Current vs Temperature



LTC1285/88 • TPC24

PIN FUNCTIONS

LTC1285

V_{REF} (Pin 1): Reference Input. The reference input defines the span of the A/D converter.

IN^+ (Pin 2): Positive Analog Input.

IN^- (Pin 3): Negative Analog Input.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

$\overline{CS}$/SHDN (Pin 5): Chip Select Input. A logic low on this input enables the LTC1285. A logic high on this input disables and powers down the LTC1285.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer and determines conversion speed.

V_{CC} (Pin 8): Power Supply Voltage. This pin provides power to the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

LTC1288

$\overline{CS}$/SHDN (Pin 1): Chip Select Input. A logic low on this input enables the LTC1288. A logic high on this input disables and powers down the LTC1288.

CH0 (Pin 2): Analog Input.

CH1 (Pin 3): Analog Input.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

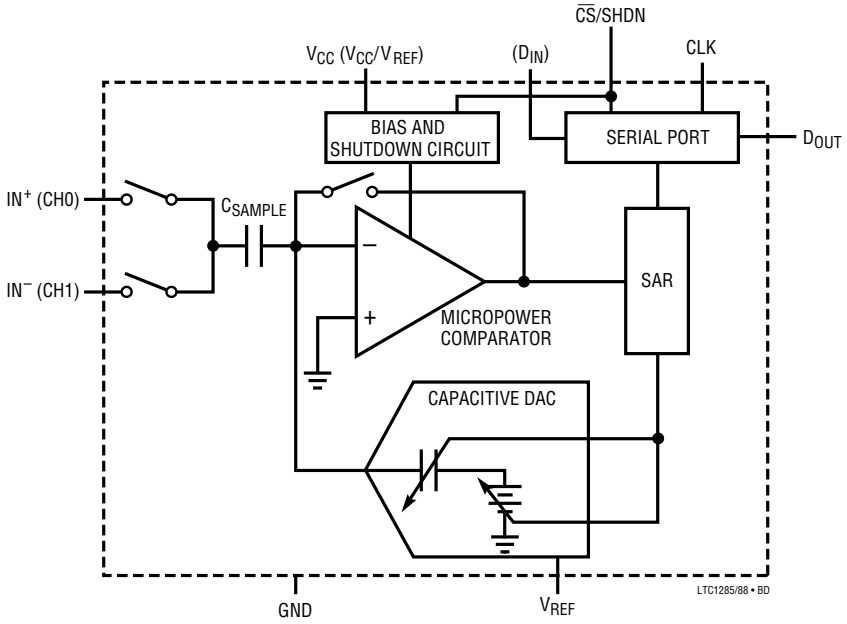
D_{IN} (Pin 5): Digital Data Input. The multiplexer address is shifted into this input.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer and determines conversion speed.

V_{CC}/V_{REF} (Pin 8): Power Supply and Reference Voltage. This pin provides power and defines the span of the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

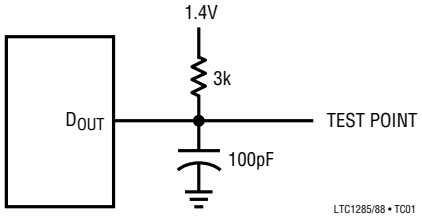
BLOCK DIAGRAM



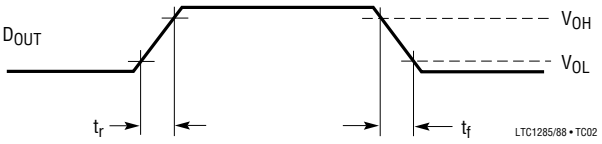
PIN NAMES IN PARENTHESES REFER TO THE LTC1288

TEST CIRCUITS

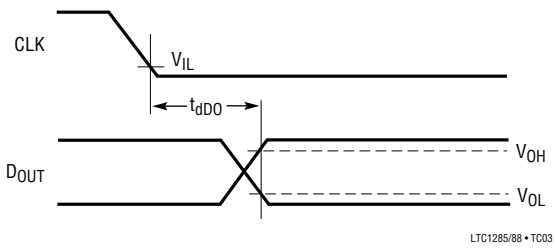
Load Circuit for t_{dDO}, t_r and t_f



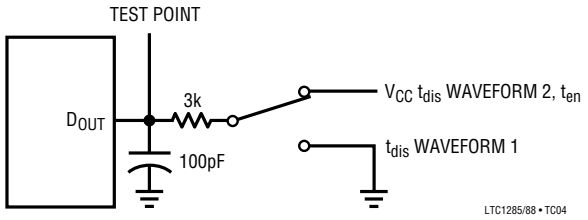
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



Voltage Waveforms for D_{OUT} Delay Times, t_{dDO}

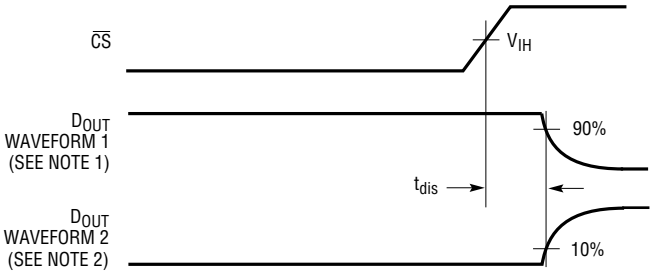


Load Circuit for t_{dis} and t_{en}



TEST CIRCUITS

Voltage Waveforms for t_{dis}

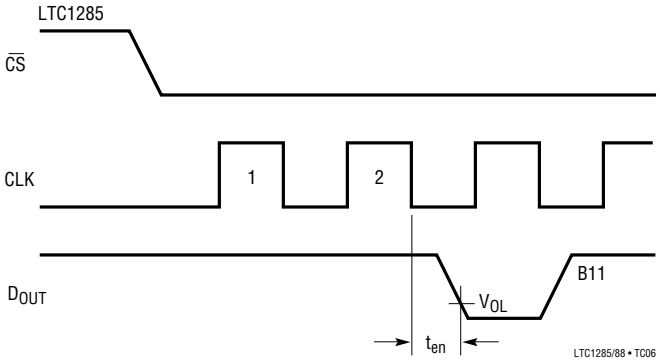


NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

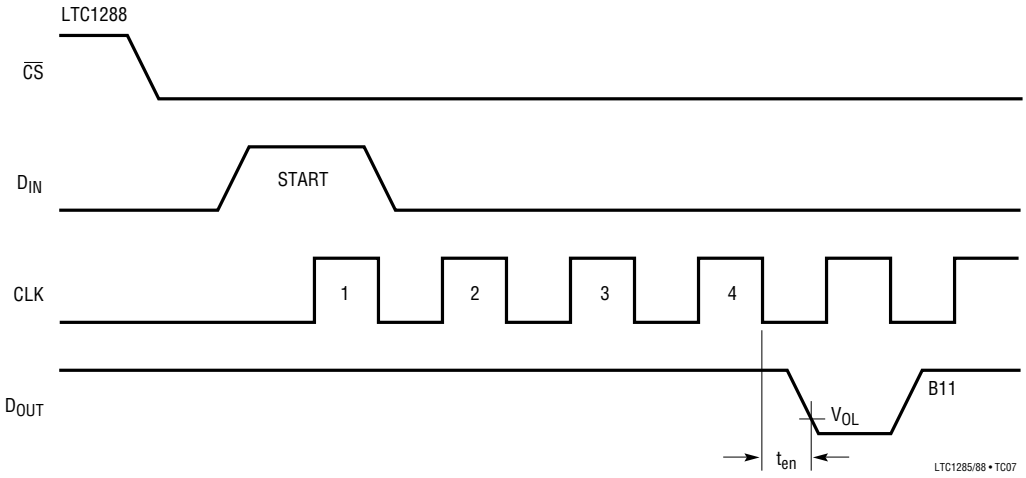
LTC1285/88 • TC05

Voltage Waveforms for t_{en}



LTC1285/88 • TC06

Voltage Waveforms for t_{en}



LTC1285/88 • TC07

APPLICATION INFORMATION

OVERVIEW

The LTC1285 and LTC1288 are 3V micropower, 12-bit, successive approximation sampling A/D converters. The LTC1285 typically draws 160µA of supply current when sampling at 7.5kHz while the LTC1288 nominally consumes 210µA of supply current when sampling at 6.6 kHz. The extra 50µA of supply current on the LTC1288 comes from the reference input which is intentionally tied to the supply. Supply current drops linearly as the sample rate is reduced (see Supply Current vs Sample Rate). The ADCs automatically power down when not performing conversions, drawing only leakage current. They are packaged in 8-pin SO and DIP packages. The LTC1285 and LTC1288 operate on a single supply from 2.7V to 6V.

Both the LTC1285 and the LTC1288 contain a 12-bit, switched-capacitor ADC, a sample-and-hold, and a serial port (see Block Diagram). Although they share the same basic design, the LTC1285 and LTC1288 differ in some respects. The LTC1285 has a differential input and has an external reference input pin. It can measure signals floating on a DC common-mode voltage and can operate with reduced spans to 1.5V. Reducing the spans allows it to achieve 366µV resolution. The LTC1288 has a two-channel input multiplexer and can convert either channel with respect to ground or the difference between the two. The reference input is tied to the supply pin.

SERIAL INTERFACE

The 2-channel LTC1288 communicates with microprocessors and other external circuitry via a synchronous, half duplex, 4-wire serial interface. The single channel LTC1285 uses a 3-wire interface (see Operating Sequence in Figures 1 and 2).

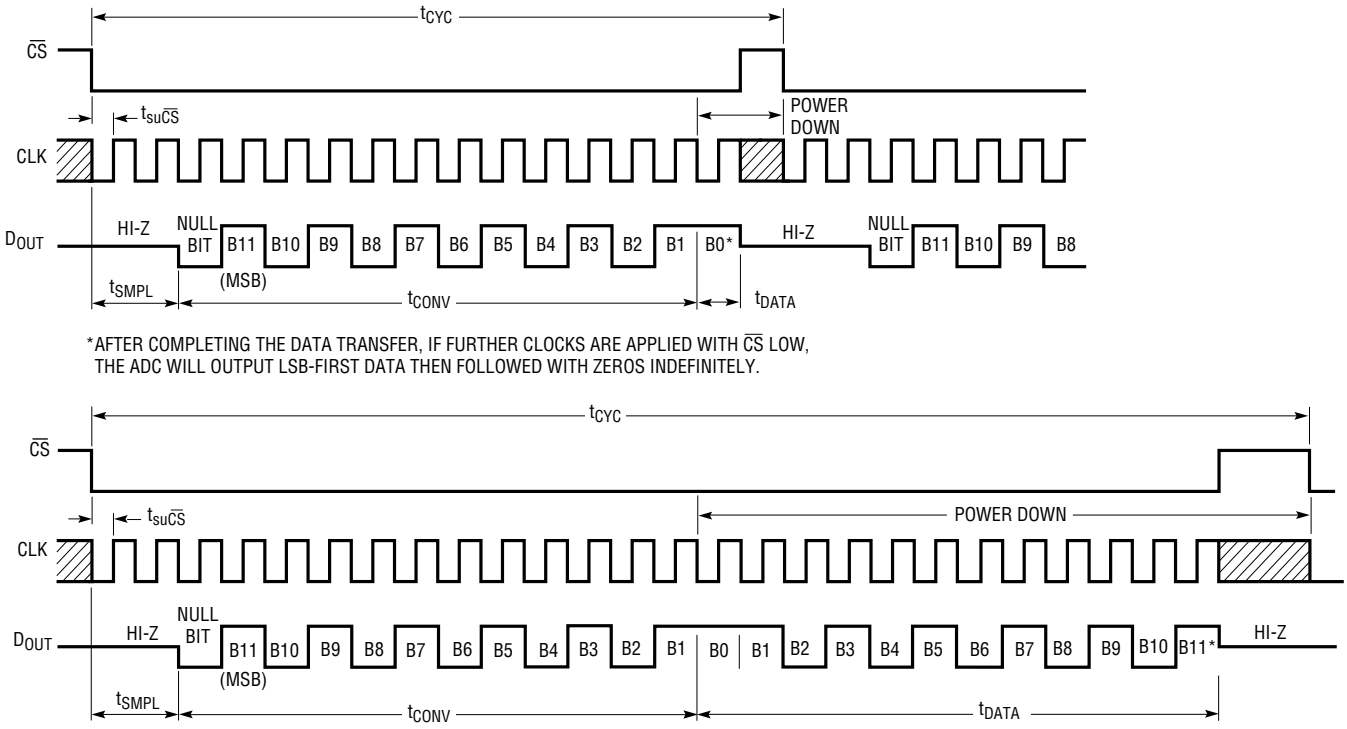
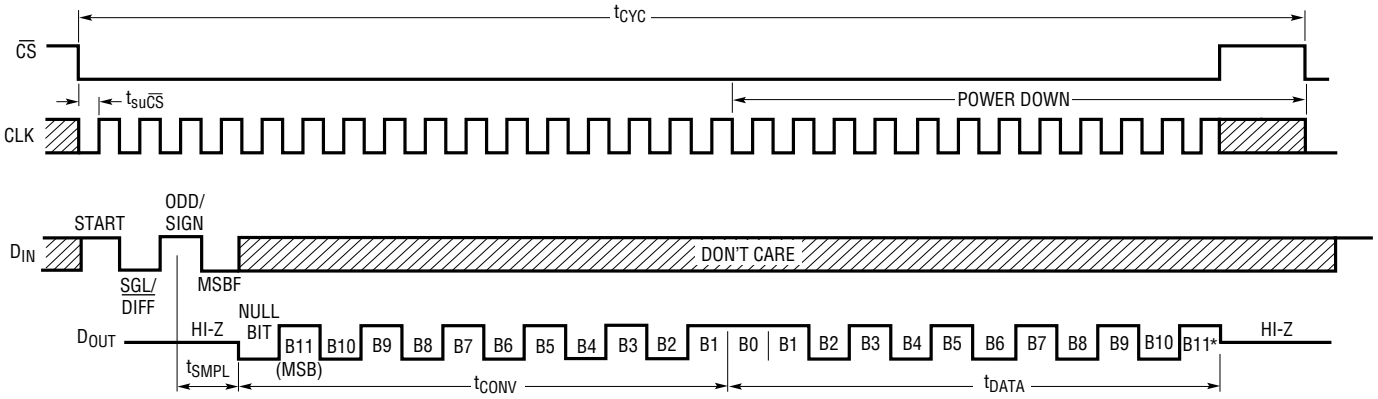


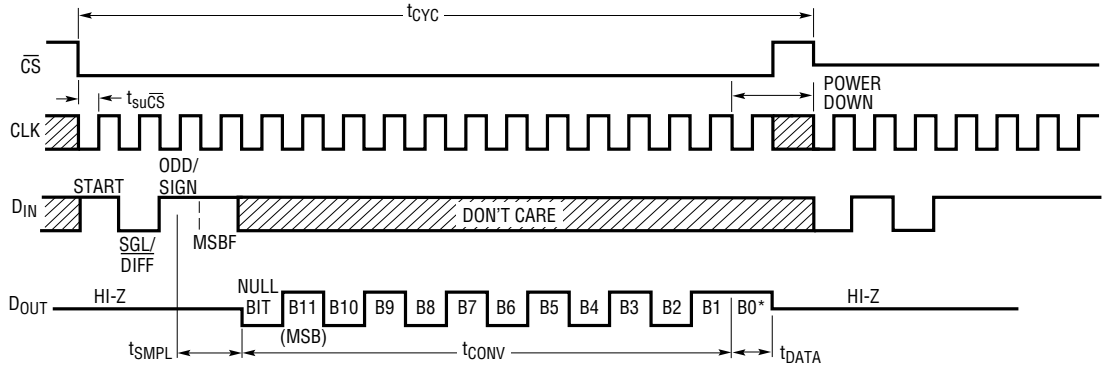
Figure 1. LTC1285 Operating Sequence

APPLICATION INFORMATION

MSB-First Data (MSBF = 0)



MSB-First Data (MSBF = 1)



*AFTER COMPLETING THE DATA TRANSFER, IF FURTHER CLOCKS ARE APPLIED WITH $\overline{CS}$ LOW, THE ADC WILL OUTPUT ZEROS INDEFINITELY.

t_{DATA}: DURING THIS TIME, THE BIAS CIRCUIT AND THE COMPARATOR POWER DOWN AND THE REFERENCE INPUT BECOMES A HIGH IMPEDANCE NODE, LEAVING THE CLK RUNNING TO CLOCK OUT LSB-FIRST DATA OR ZEROES.

LTC1285/88 • F02

Figure 2. LTC1288 Operating Sequence Example: Differential Inputs (CH^+, CH^-)

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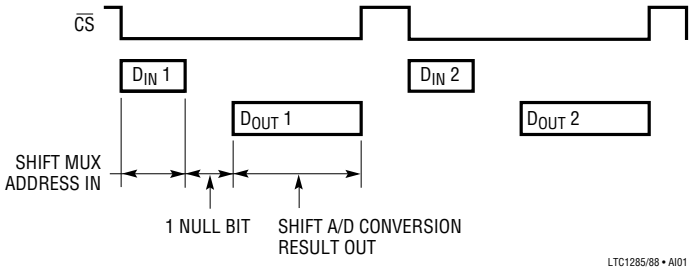
Data Transfer

The CLK synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems.

The LTC1285 does not require a configuration input word and has no D_{IN} pin. A falling $\overline{CS}$ initiates data transfer as shown in the LTC1285 operating sequence. After $\overline{CS}$ falls the second CLK pulse enables D_{OUT}. After one null bit the A/D conversion result is output on the D_{OUT} line. Bringing $\overline{CS}$ high resets the LTC1285 for the next data exchange.

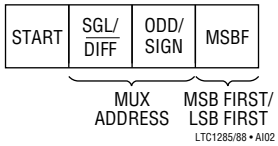
The LTC1288 first receives input data and then transmits back the A/D conversion result (half duplex). Because of the half duplex operation, D_{IN} and D_{OUT} may be tied together allowing transmission over just 3 wires: $\overline{CS}$, CLK and DATA (D_{IN}/D_{OUT}).

Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After $\overline{CS}$ falls the LTC1288 looks for a start bit. After the start bit is received, the 3-bit input word is shifted into the D_{IN} input which configures the LTC1288 and starts the conversion. After one null bit, the result of the conversion is output on the D_{OUT} line. At the end of the data exchange $\overline{CS}$ should be brought high. This resets the LTC1288 in preparation for the next data exchange.



Input Data Word

The LTC1285 requires no D_{IN} word. It is permanently configured to have a single differential input. The conversion result appears on the D_{OUT} line. The data format is MSB first followed by the LSB sequence. This provides easy interface to MSB or LSB first serial ports. For MSB first data the $\overline{CS}$ signal can be taken high after B0 (see Figure 1). The LTC1288 clocks data into the D_{IN} input on the rising edge of the clock. The input data words are defined as follows:



Start Bit

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer. The LTC1288 will ignore all leading zeros which precede this logical one. After the start bit is received, the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.

Multiplexer (MUX) Address

The bits of the input word following the START bit assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "–" signs in the selected row of the following tables. In single-ended mode, all input channels are measured with respect to GND.

LTC1288 Channel Selection

	MUX ADDRESS		CHANNEL #		
	SGL/DIFF	ODD/SIGN	0	1	GND
SINGLE-ENDED MUX MODE	1	0	+		–
	1	1		+	–
DIFFERENTIAL MUX MODE	0	0	+	–	
	0	1	–	+	

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MSB First/LSB First (MSBF)

The output data of the LTC1288 is programmed for MSB first or LSB first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB first format. Logical zeros will be filled in indefinitely following the last data bit. When the MSBF bit is a logical zero, LSB first data will follow the normal MSB first data on the D_{OUT} line (see Operating Sequence).

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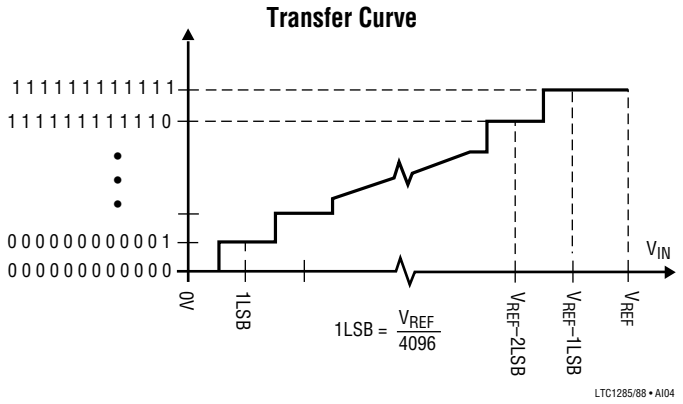
Transfer Curve

The LTC1285/LTC1288 are permanently configured for unipolar only. The input span and code assignment for this conversion type are shown in the following figures.



Output Code

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5.000V)
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	V_{REF} – 1LSB	4.99878V
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	V_{REF} – 2LSB	4.99756V
•	•	•
•	•	•
•	•	•
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	1LSB	0.00122V
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0V	0V

LTC1285/88 • AI05

Operation with D_{IN} and D_{OUT} Tied Together

The LTC1288 can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to communicate to the microprocessor (MPU). Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1288 will take control of the data line and drive it low on the 4th falling CLK edge after the start bit is received (see Figure 3). Therefore the processor port line must be switched to an input before this happens to avoid a conflict.

In the Typical Applications section, there is an example of interfacing the LTC1288 with D_{IN} and D_{OUT} tied together to the Intel 8051 MPU.

ACHIEVING MICROPOWER PERFORMANCE

With typical operating currents of 160µA and automatic shutdown between conversions, the LTC1285/LTC1288 achieves extremely low power consumption over a wide range of sample rates (see Figure 4). The auto-shutdown allows the supply curve to drop with reduced sample rate.

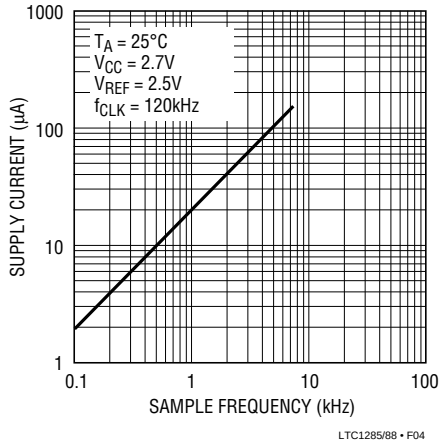


Figure 4. Automatic Power Shutdown Between Conversions Allows Power Consumption to Drop with Sample Rate

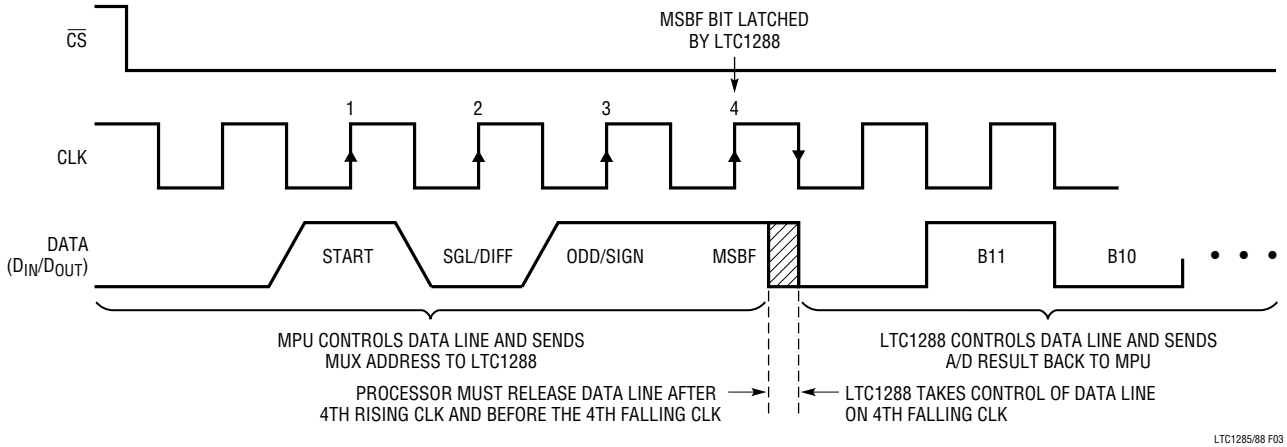


Figure 3. LTC1288 Operation with D_{IN} and D_{OUT} Tied Together

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Several things must be taken into account to achieve such a low power consumption.

Shutdown

The LTC1285/LTC1288 are equipped with automatic shutdown features. They draw power when the $\overline{CS}$ pin is low and shut down completely when that pin is high. The bias circuit and comparator powers down and the reference input becomes high impedance at the end of each conversion leaving the CLK running to clock out the LSB first data or zeroes (see Figures 1 and 2). If the $\overline{CS}$ is not running rail-to-rail, the input logic buffer will draw current. This current may be large compared to the typical supply current. To obtain the lowest supply current, bring the $\overline{CS}$ pin to ground when it is low and to supply voltage when it is high.

When the $\overline{CS}$ pin is high (= supply voltage), the converter is in shutdown mode and draws only leakage current. The status of the D_{IN} and CLK input have no effect on supply current during this time. There is no need to stop D_{IN} and CLK with $\overline{CS}$ = high; they can continue to run without drawing current.

Minimize $\overline{CS}$ Low Time

In systems that have significant time between conversions, lowest power drain will occur with the minimum $\overline{CS}$ low time. Bringing $\overline{CS}$ low, transferring data as quickly as possible, and then bringing it back high will result in the lowest current drain. This minimizes the amount of time the device draws power. After a conversion the ADC automatically shuts down even if $\overline{CS}$ is held low (see Figures 1 and 2). If the clock is left running to clock out LSB-data or zero, the logic will draw a small current. Figure 5 shows that the typical supply current with $\overline{CS}$ = ground varies from 1μA at 1kHz to 9μA at 120kHz. When $\overline{CS}$ = V_{CC}, the logic is gated off and no supply current is drawn regardless of the clock frequency.

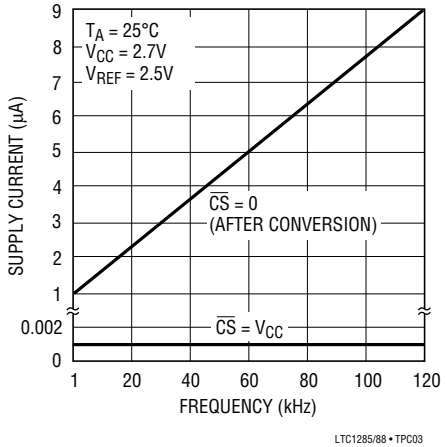

Figure 5. Shutdown Current with $\overline{CS}$ High is 1nA Typically, Regardless of the Clock. Shutdown Current with $\overline{CS}$ = Ground Varies From 1μA at 1kHz to 9μA at 120kHz

D_{OUT} Loading

Capacitive loading on the digital output can increase power consumption. A 100pF capacitor on the D_{OUT} pin can add more than 16.2μA to the supply current at a 120kHz clock frequency. An extra 16.2μA or so of current goes into charging and discharging the load capacitor. The same goes for digital lines driven at a high frequency by any logic. The $C \times V \times f$ currents must be evaluated and the troublesome ones minimized.

OPERATING ON OTHER THAN 3V SUPPLIES

Both the LTC1285 and the LTC1288 operate from a 2.7V to 6V supply. To operate the LTC1285/LTC1288 on other than 3V supplies a few things must be kept in mind.

Input Logic Levels

The input logic levels of $\overline{CS}$, CLK and D_{IN} are made to meet TTL on a 3V supply. When the supply voltage varies, the input logic levels also change. For the LTC1285/LTC1288 to sample and convert correctly, the digital inputs have to be in the proper logical low and high levels relative to the operating supply voltage (see typical curve of Digital Input Logic Threshold vs Supply Voltage). If achieving micropower consumption is desirable, the digital inputs must go rail-to-rail between supply voltage and ground (see ACHIEVING MICROPOWER PERFORMANCE section).

Clock Frequency

The maximum recommended clock frequency is 120kHz for the LTC1285/LTC1288 running off a 3V supply. With the supply voltage changing, the maximum clock frequency for the devices also changes (see the typical curve

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of Maximum Clock Rate vs Supply Voltage). If the maximum clock frequency is used, care must be taken to ensure that the device converts correctly.

Mixed Supplies

It is possible to have a microprocessor running off a 5V supply and communicate with the LTC1285/LTC1288 operating on a 3V supply. The inputs of $\overline{CS}$, CLK and D_{IN} of the LTC1285/LTC1288 have no problem to take a voltage swing from 0V to 5V. With the LTC1285 operating on a 3V supply, the output of D_{OUT} may only go between 0V and 3V. The 3V output level is higher enough to trip a TTL input of the MPU. Figure 6 shows a 3V powered LTC1285 interfacing a 5V system.

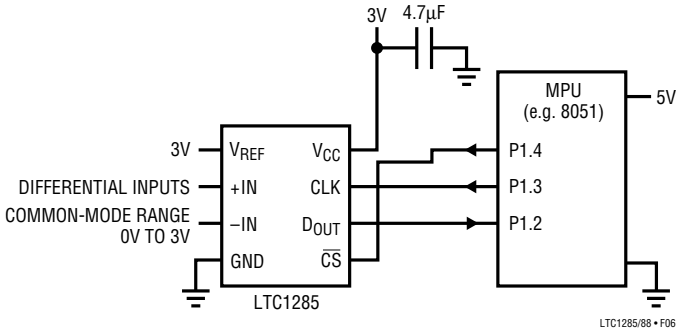

Figure 6. Interfacing a 3V Powered LTC1285 to a 5V System

BOARD LAYOUT CONSIDERATIONS

Grounding and Bypassing

The LTC1285/LTC1288 are easy to use if some care is taken. They should be used with an analog ground plane and single point grounding techniques. The GND pin should be tied directly to the ground plane.

The V_{CC} pin should be bypassed to the ground plane with a 10µF tantalum capacitor with leads as short as possible. If the power supply is clean, the LTC1285/LTC1288 can also operate with smaller 1µF or less surface mount or ceramic bypass capacitors. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

SAMPLE-AND-HOLD

Both the LTC1285 and the LTC1288 provide a built-in sample-and-hold (S&H) function to acquire signals. The S&H of the LTC1285 acquires input signals from "+" input relative to "–" input during the t_{SMPL} time (see Figure 1). However, the S&H of the LTC1288 can sample input signals in the single-ended mode or in the differential inputs during the t_{SMPL} time (see Figure 7).

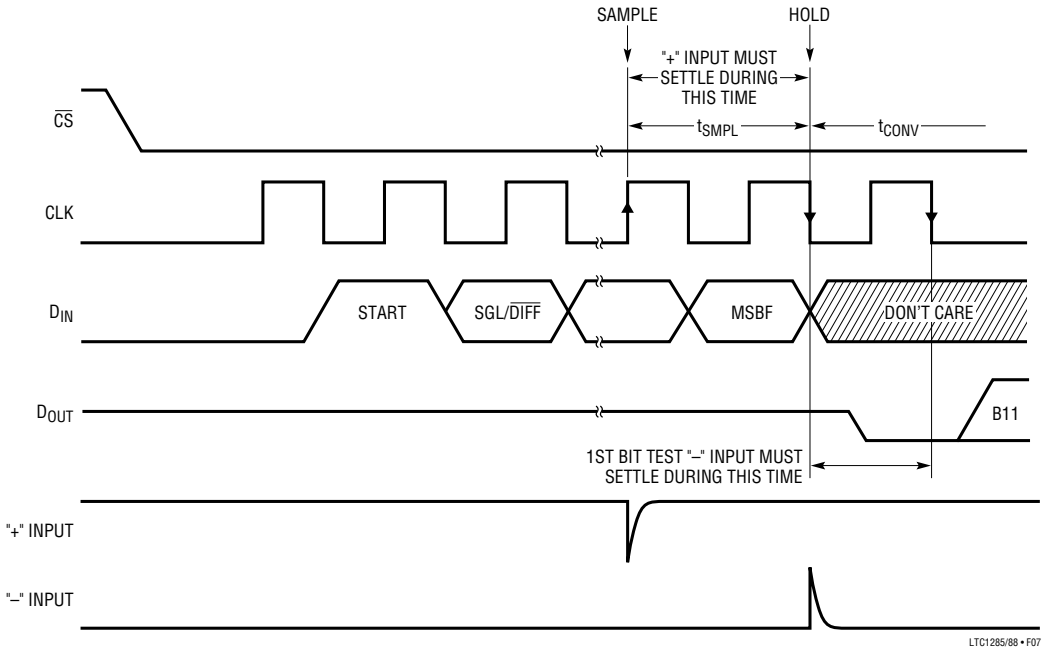

Figure 7. LTC1288 "+" and "–" Input Settling Windows

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Single-Ended Inputs

The sample-and-hold of the LTC1288 allows conversion of rapidly varying signals. The input voltage is sampled during the t_{SMPL} time as shown in Figure 7. The sampling interval begins as the bit preceding the MSBF bit is shifted in and continues until the falling CLK edge after the MSBF bit is received. On this falling edge, the S&H goes into hold mode and the conversion begins.

Differential Inputs

With differential inputs, the ADC no longer converts just a single voltage but rather the difference between two voltages. In this case, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single-ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 12 CLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input this error would be:

$$V_{ERROR\ (MAX)} = V_{PEAK} \times 2 \times \pi \times f(\text{"}-\text{"}) \times 12/f_{CLK}$$

Where f("–") is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. In most cases V_{ERROR} will not be significant. For a 60Hz signal on the "–" input to generate a 1/4LSB error (152µV) with the converter running at CLK = 120kHz, its peak value would have to be 4.03mV.

ANALOG INPUTS

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1285/LTC1288 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

"+" Input Settling

The input capacitor of the LTC1285 is switched onto "+" input during the t_{SMPL} time (see Figure 1) and samples the input signal within that time. However, the input capacitor of the LTC1288 is switched onto "+" input during the sample phase (t_{SMPL}, see Figure 7). The sample phase is 1 1/2 CLK cycles before conversion starts. The voltage on the "+" input must settle completely within t_{SMPLE} for the LTC1285 and the LTC1288 respectively. Minimizing R_{SOURCE}^+ and C1 will improve the input settling time. If a large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency.

"–" Input Settling

At the end of the t_{SMPL}, the input capacitor switches to the "–" input and conversion starts (see Figures 1 and 7). During the conversion, the "+" input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. However, it is critical that the "–" input voltage settles completely during the first CLK cycle of the conversion time and be free of noise. Minimizing R_{SOURCE}^- and C2 will improve settling time. If a large "–" input source resistance must be used, the time allowed for settling can be extended by using a slower CLK frequency.

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 7). Again, the"+" and "–" input sampling times can be extended as described above to accommodate slower op amps. Most op amps, including the LT1006 and LT1413 single supply op amps, can be made to settle well even with the minimum settling windows of 12.5µs ("+" input) which occur at the maximum clock rate of 120kHz.

Source Resistance

The analog inputs of the LTC1285/LTC1288 look like a 20pF capacitor (C_{IN}) in series with a 500Ω resistor (R_{ON}) as shown in Figure 8. C_{IN} gets switched between the

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selected "+" and "–" inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

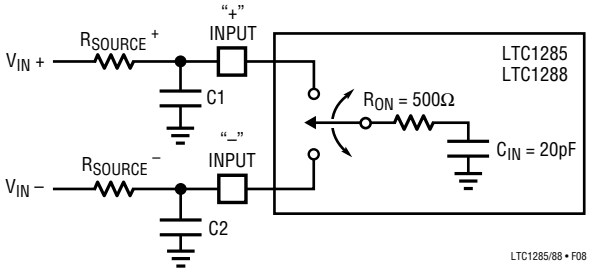

Figure 8. Analog Input Equivalent Circuit

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 9. For large values of C_F (e.g., 1µF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 20pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 133.3µs, the input current equals 0.375µA at V_{IN} = 2.5V. In this case, a filter resistor of 160Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time.

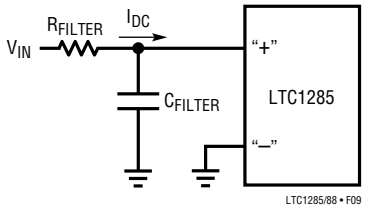

Figure 9. RC Input Filtering

Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 1µA (at 125°C) flowing through a source resistance of 240Ω will cause a voltage drop of 240µV or 0.4LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

REFERENCE INPUTS

The reference input of the LTC1285 is effectively a 50kΩ resistor from the time $\overline{CS}$ goes low to the end of the conversion. The reference input becomes a high impedence node at any other time (see Figure 10). Since the voltage on the reference input defines the voltage span of the A/D converter, the reference input should be driven by a reference with low R_{OUT} (ex. LT1004, LT1019 and LT1021) or a voltage source with low R_{OUT}.

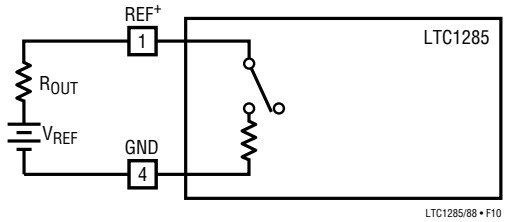

Figure 10. Reference Input Equivalent Circuit

Reduced Reference Operation

The minimum reference voltage of the LTC1288 is limited to 2.7V because the V_{CC} supply and reference are internally tied together. However, the LTC1285 can operate with reference voltages below 1.5V.

The effective resolution of the LTC1285 can be increased by reducing the input span of the converter. The LTC1285 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Change in Linearity vs Reference Voltage and Change in Gain vs Reference

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Voltage). However, care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low V_{REF} values:

1. Offset
2. Noise
3. Conversion speed (CLK frequency)

Offset with Reduced V_{REF}

The offset of the LTC1285 has a larger effect on the output code. When the ADC is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Change in Offset vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example, a V_{OS} of 122µV which is 0.2LSB with a 2.5V reference becomes 1LSB with a 1V reference and 5LSBs with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input of the LTC1285.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1285 can be reduced to approximately 400µV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 2.5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced.

For operation with a 2.5V reference, the 400µV noise is only 0.66LSB peak-to-peak. In this case, the LTC1285 noise will contribute a little bit of uncertainty to the output code. However, for reduced references the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1.25V reference this same 400µV noise is 1.32LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 1LSB. If the reference is further reduced to 1V, the 400µV noise becomes equal to 3.3LSBs and a stable code may be difficult to achieve. In this case averaging multiple readings may be necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on V_{CC}, V_{REF} or V_{IN}) will add to the internal noise. The lower the reference voltage to be used the more critical it becomes to have a clean, noise free setup.

Conversion Speed with Reduced V_{REF}

With reduced reference voltages, the LSB step size is reduced and the LTC1285 internal comparator overdrive is reduced. Therefore, it may be necessary to reduce the maximum CLK frequency when low values of V_{REF} are used.

DYNAMIC PERFORMANCE

The LTC1285/LTC1288 have exceptional sampling capability. Fast Fourier Transform (FFT) test techniques are used to characterize the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 11 shows a typical LTC1285 plot.

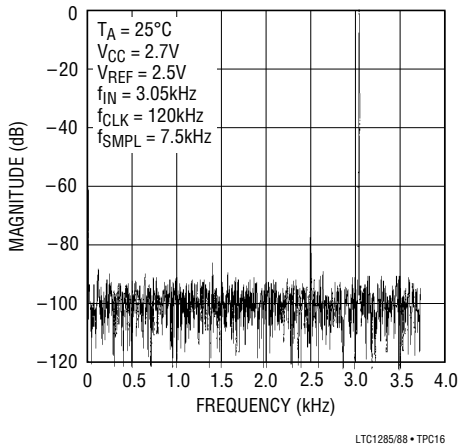


Figure 11. LTC1285 Non-Averaged, 4096 Point FFT Plot

APPLICATION INFORMATION

Signal-to-Noise Ratio

The Signal-to-Noise plus Distortion Ratio (S/N + D) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the ADC's output. The output is band limited to frequencies above DC and below one half the sampling frequency. Figure 12 shows a typical spectral content with a 7.5kHz sampling rate.

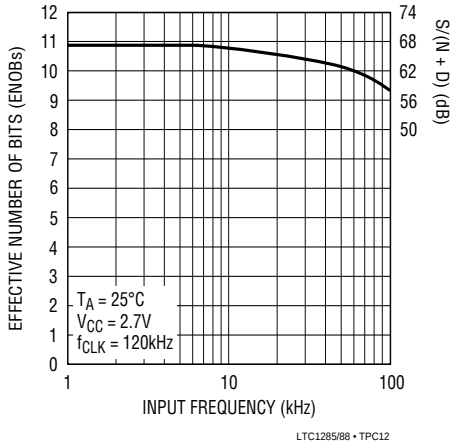


Figure 12. Effective Bits and S/(N + D) vs Input Frequency

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to S/(N+D) by the equation:

$$ENOB = [S/(N + D) - 1.76]/6.02$$

where S/(N + D) is expressed in dB. At the maximum sampling rate of 7.5kHz with a 2.7V supply, the LTC1285 maintains above 10.7 ENOBs at 10kHz input frequency. Above 10kHz the ENOBs gradually decline, as shown in Figure 12, due to increasing second harmonic distortion. The noise floor remains low.

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half of the sampling frequency. THD is defined as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + ... + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through the N^{th} harmonics. The typical THD specification in the Dynamic Accuracy table includes the 2nd through 5th harmonics. With a 1kHz input signal, the LTC1285/LTC1288 have typical THD of 80dB with V_{CC} = 2.7V.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies f_a and f_b are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of $mf_a \pm nf_b$, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include $(f_a + f_b)$ and $(f_a - f_b)$ while 3rd order IMD terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$, and $(f_a - 2f_b)$. If the two input sine waves are equal in magnitudes, the value (in dB) of the 2nd order IMD products can be expressed by the following formula:

$$IMD\left(f_a \pm f_b\right) = 20\log\left[\frac{\text{amplitude}\left(f_a \pm f_b\right)}{\text{amplitude at } f_a}\right]$$

For input frequencies of 2.05kHz and 3.05kHz, the IMD of the LTC1285/LTC1288 is 72dB with a 2.7V supply.

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in dBs relative to the RMS value of a full-scale input signal.

TYPICAL APPLICATIONS

MICROPROCESSOR INTERFACES

The LTC1285/LTC1288 can interface directly without external hardware to most popular microprocessor (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then 3 or 4 of the MPU's parallel port lines can be programmed to form the serial link to the LTC1285/LTC1288. Included here is one serial interface example and one example showing a parallel port programmed to form the serial interface.

Motorola SPI (MC68HC11)

The MC68HC11 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB-first and in 8-bit increments. The D_{IN} word sent to the data register starts with the SPI process. With three 8-bit transfers, the A/D result is read into the MPU. The second 8-bit transfer clocks B11 through B8 of the A/D conversion result into the processor. The third 8-bit transfer clocks the remaining bits, B7 through B0, into the MPU. The data is right justified into two memory locations. ANDing the second byte with OF_{HEX} clears the four most significant bits. This operation was not included in the code. It can be inserted in the data gathering loop or outside the loop when the data is processed.

MC68HC11 Code

In this example the D_{IN} word configures the input MUX for a single-ended input to be applied to CH0. The conversion result is output MSB-first.

Table 1. Microprocessor with Hardware Serial Interfaces Compatible with the LTC1286/LTC1298

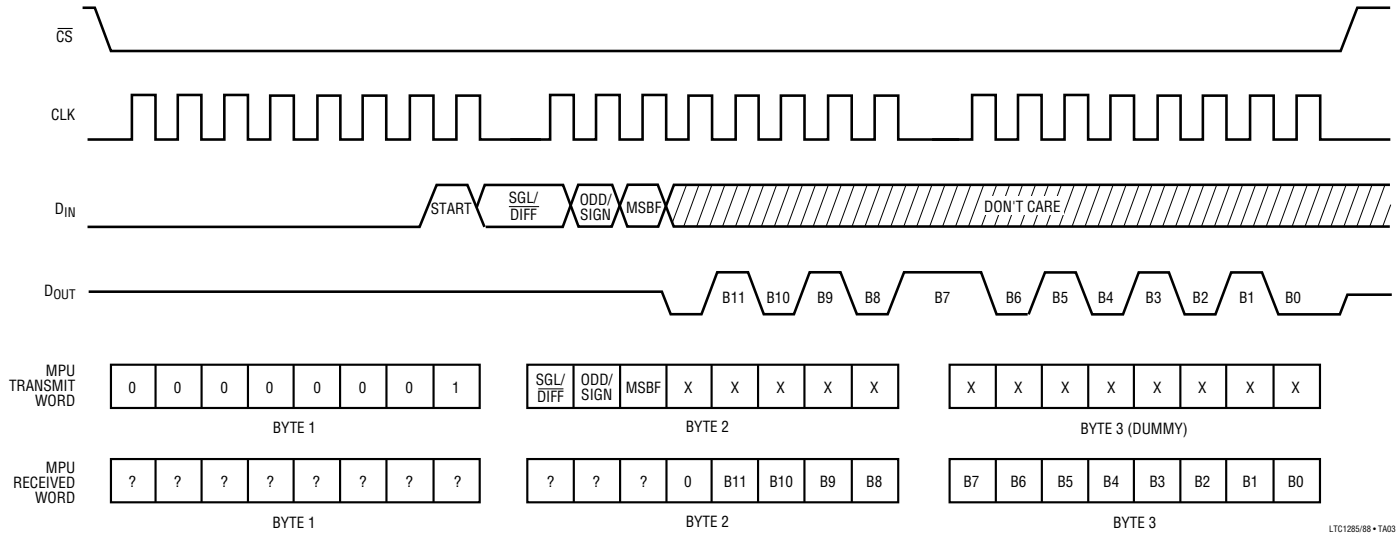
PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2,S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD63705	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	CSI/O
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MICROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS†
HPC16000 Family	MICROWIRE/PLUS†
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020	Serial Port
Intel	
8051	Bit Manipulation on Parallel Port

* Requires external hardware

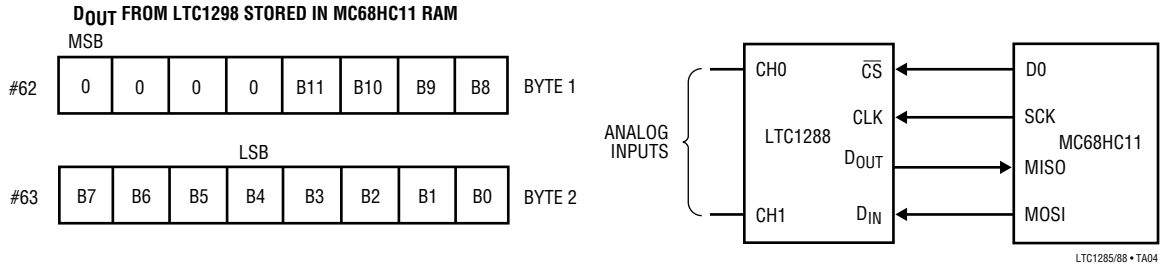
† MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

TYPICAL APPLICATIONS

Timing Diagram for Interface to the MC68HC11



Hardware and Software Interface to the MC68HC11



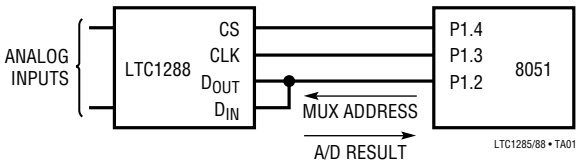
LABEL	MNEMONIC	OPERAND	COMMENTS	LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	#$50	CONFIGURATION DATA FOR SPCR	WAIT1	BPL	WAIT1	CHECK IF TRANSFER IS DONE
	STAA	$1028	LOAD DATA INTO SPCR ($1028)		LDAA	$51	LOAD DIN INTO ACC A FROM $51
	LDAA	#$1B	CONFIG. DATA FOR PORT D DDR		STAA	$102A	LOAD DIN INTO SPI, START SCK
	STAA	$1009	LOAD DATA INTO PORT D DDR	WAIT2	LDAA	$1029	CHECK SPI STATUS REG
	LDAA	#$01	LOAD DIN WORD INTO ACC A		BPL	WAIT2	CHECK IF TRANSFER IS DONE
	STAA	$50	LOAD DIN DATA INTO $50		LDAA	$102A	LOAD LTC1288 MSBs INTO ACC A
	LDAA	#$A0	LOAD DIN WORD INTO ACC A		STAA	$62	STORE MSBs IN $62
	STAA	$51	LOAD DIN DATA INTO $51		LDAA	$52	LOAD DUMMY INTO ACC A FROM $52
	LDAA	#$00	LOAD DUMMY DIN WORD INTO ACC A		STAA	$102A	LOAD DUMMY DIN INTO SPI, START SCK
	STAA	$52	LOAD DUMMY DIN DATA INTO $52				
	LDX	#$1000	LOAD INDEX REGISTER X WITH $1000	WAIT3	LDAA	$1029	CHECK SPI STATUS REG
					BPL	WAIT3	CHECK IF TRANSFER IS DONE
LOOP	BCLR	$08,X,#$01	D0 GOES LOW (CS GOES LOW)		BSET	$08,X#$01	DO GOES HIGH (CS GOES HIGH)
	LDAA	$50	LOAD DIN INTO ACC A FROM $50		LDAA	$102A	LOAD LTC1288 LSBs IN ACC
	STAA	$102A	LOAD DIN INTO SPI, START SCK		STAA	$63	STORE LSBs IN $63
	LDAA	$1029	CHECK SPI STATUS REG		JMP	LOOP	START NEXT CONVERSION

TYPICAL APPLICATIONS

Interfacing to the Parallel Port of the INTEL 8051 Family

The Intel 8051 has been chosen to demonstrate the interface between the LTC1288 and parallel port microprocessors. Normally the $\overline{CS}$, CLK and D_{IN} signals would be generated on 3 port lines and the D_{OUT} signal read on a 4th port line. This works very well. However, we will demonstrate here an interface with the D_{IN} and D_{OUT} of the LTC1288 tied together as described in the SERIAL INTERFACE section. This saves one wire.

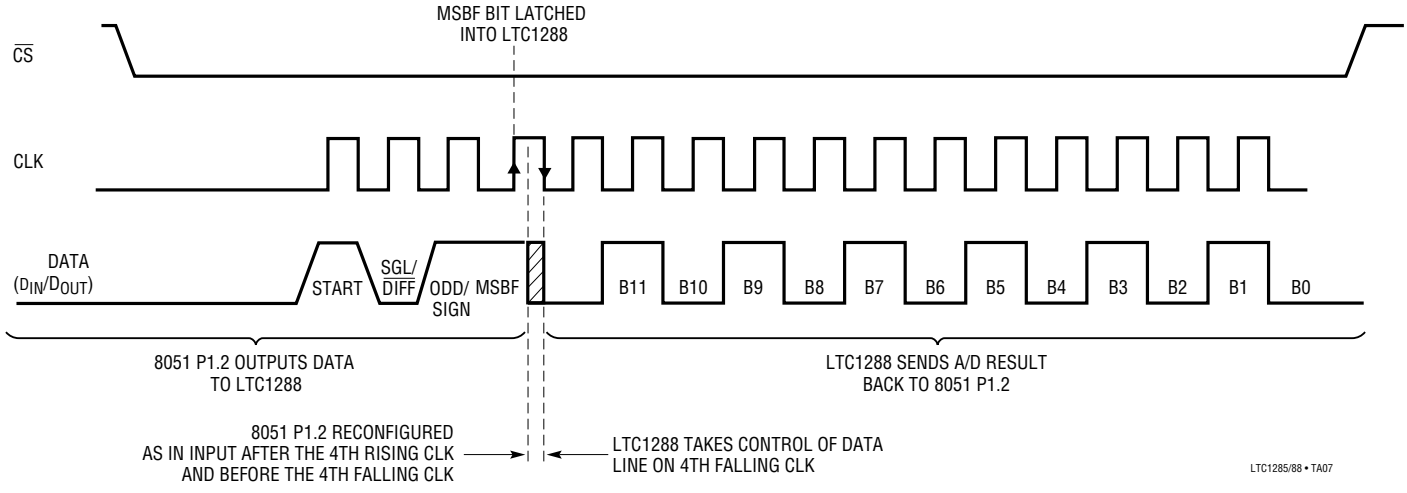
The 8051 first sends the start bit and MUX address to the LTC1288 over the data line connected to P1.2. Then P1.2 is reconfigured as an input (by writing to it a one) and the 8051 reads back the 12-bit A/D result over the same data line.



LABEL	MNEMONIC	OPERAND	COMMENTS
	MOV	A, #FFH	D_{IN} word for LTC1288
	SETB	P1.4	Make sure $\overline{CS}$ is high
	CLR	P1.4	$\overline{CS}$ goes low
	MOV	R4, #04	Load counter
LOOP 1	RLC	A	Rotate D_{IN} bit into Carry
	CLR	P1.3	SCLK goes low
	MOV	P1.2, C	Output D_{IN} bit to LTC1288
	SETB	P1.3	SCLK goes high
	DJNZ	R4, LOOP 1	Next bit
	MOV	P1, #04	Bit 2 becomes an input
	CLR	P1.3	SCLK goes low
	MOV	R4, #09	Load counter
LOOP 2	MOV	C, P1.2	Read data bit into Carry
	RLC	A	Rotate data bit into Acc.
	SETB	P1.3	SCLK goes high
	CLR	P1.3	SCLK goes low
	DJNZ	R4, LOOP 2	Next bit
	MOV	R2, A	Store MSBs in R2
	CLR	A	Clear Acc.
	MOV	R4, #04	Load counter
LOOP 3	MOV	C, P1.2	Read data bit into Carry
	RLC	A	Rotate data bit into Acc.
	SETB	P1.3	SCLK goes high
	CLR	P1.3	SCLK goes low
	DJNZ	R4, LOOP 3	Next bit
	MOV	R4, #04	Load counter
LOOP 4	RRC	A	Rotate right into Acc.
	DJNZ	R4, LOOP 4	Next Rotate
	MOV	R3, A	Store LSBs in R3
	SETB	P1.4	$\overline{CS}$ goes high

D_{OUT} FROM 1288 STORED IN 8501 RAM

	MSB							
R2	B11	B10	B9	B8	B7	B6	B5	B4
	LSB							
R3	B3	B2	B1	B0	0	0	0	0



TYPICAL APPLICATIONS

A "Quick Look" Circuit for the LTC1285

Users can get a quick look at the function and timing of the LT1285 by using the following simple circuit (Figure 13). V_{REF} is tied to V_{CC}. V_{IN} is applied to the +IN input and the –IN input is tied to the ground. $\overline{CS}$ is driven at 1/16 the clock rate by the 74C161 and D_{OUT} outputs the data. The output data from the D_{OUT} pin can be viewed on an oscilloscope that is set up to trigger on the falling edge of $\overline{CS}$ (Figure 14). Note the LSB data is partially clocked out before $\overline{CS}$ goes high.

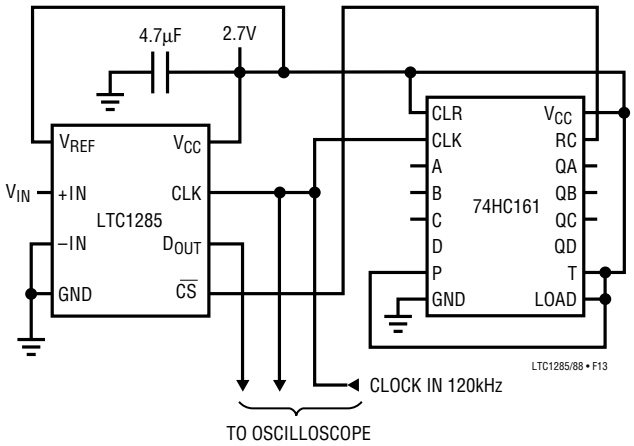


Figure 13. "Quick Look" Circuit for the LTC1285

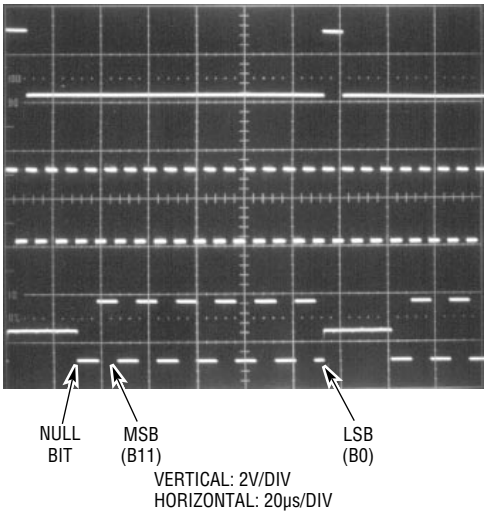


Figure 14. Scope Trace the LTC1285 "Quick Look" Circuit Showing A/D Output 101010101010 (AAA_{HEX})

Micropower Battery Voltage Monitor

A common problem in battery systems is battery voltage monitoring. This circuit monitors the 10 cell stack of NiCad or NiMH batteries found in laptop computers. It draws only 40µA from the 2.7V supply at f_{SMPL} = 0.1kHz and 30µA to 62µA from the battery. The 12-bits of resolution of the LTC1285 are positioned over the desired range of 8V to 16V. This is easily accomplished by using the ADC's differential inputs. Tying the –input to the reference gives an ADC input span of V_{REF} to $2V_{REF}$ (1.2V to 2.4V). The resistor divider then scales the input voltage for 8V to 16V.

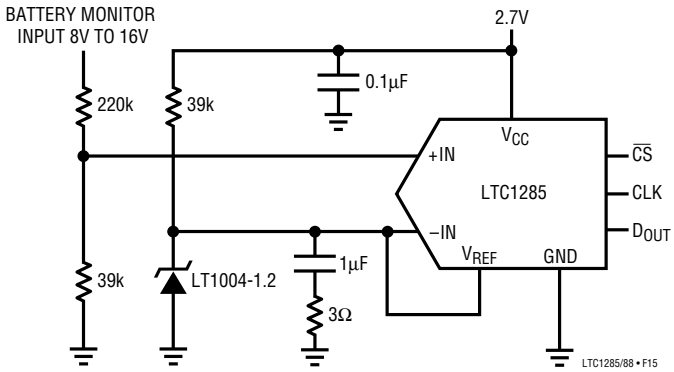
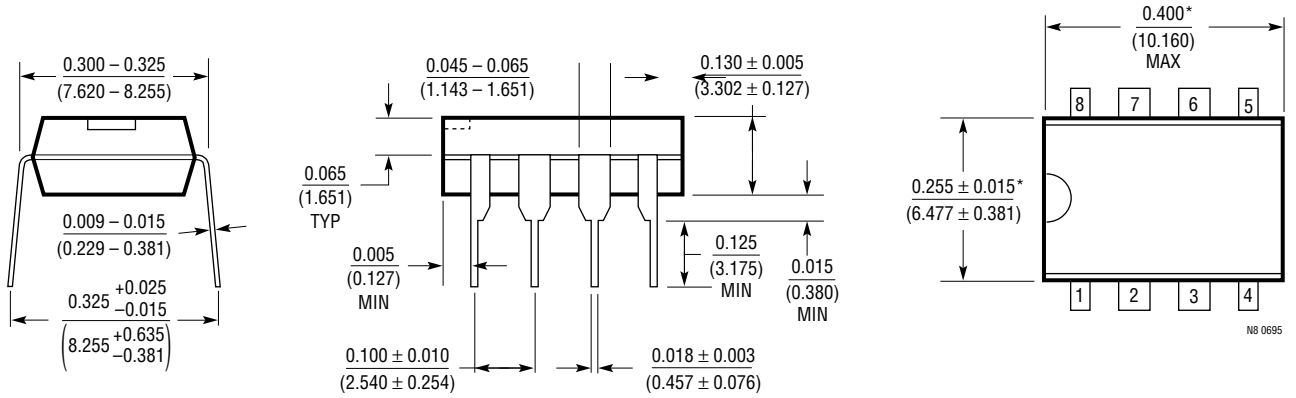


Figure 15. Micropower Battery Voltage Monitor

PACKAGE DESCRIPTION

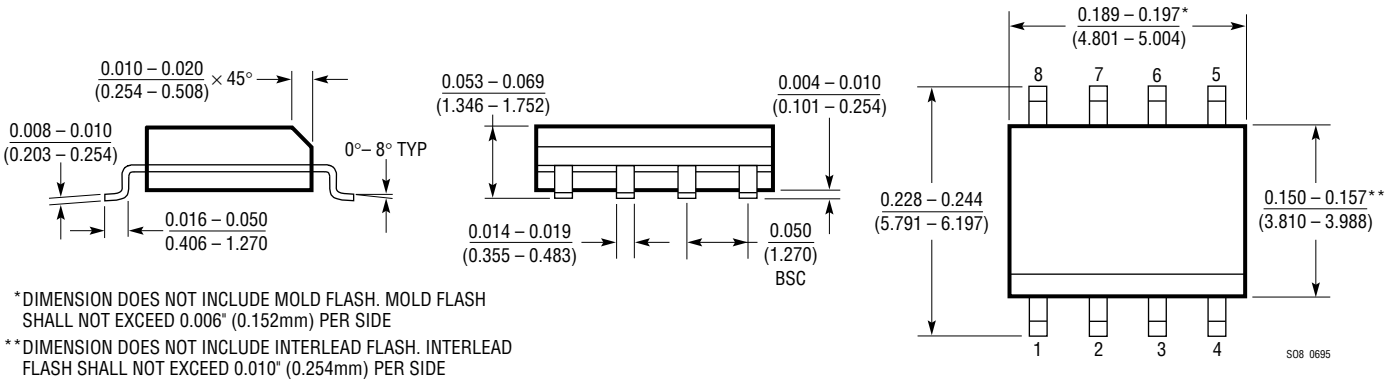
Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead Plastic DIP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S8 Package
8-Lead Plastic SOIC



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1096/LTC1098	8-Pin SOIC, Micropower 8-Bit ADC	Low Power, Small Size, Low Cost
LTC1196/LTC1198	8-Pin SOIC, 1Msps 8-bit ADC	Low Power, Small Size, Low Cost
LTC1282	3V High Speed Parallel 12-Bit ADC	Complete, V_{REF}, CLK, Sample-and-Hold, 140ksps
LTC1289	Multiplexed 3V, 1A 12-Bit ADC	8-Channel, 12-Bit Serial I/O
LTC1522	16-Pin SOIC, 3V Micropower 12-Bit ADC	4-Channel, 12-Bit Serial I/O

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