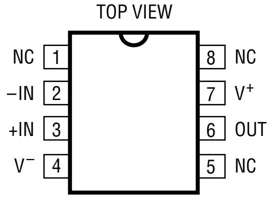
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage .... (V^+ + 0.3V) to (V^- – 0.3V)
Output Short Circuit Duration .... Indefinite
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.)................ 300°C

Operating Temperature Range
LTC1250M **(OBSOLETE)** .... –55°C to 125°C
LTC1250C .... 0°C TO 70°C

PACKAGE/ORDER INFORMATION

TOP VIEW



N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 110°C, θ_{JA} = 130°CW

ORDER PART NUMBER

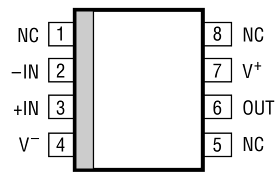
LTC1250CN8

J8 PACKAGE
8-LEAD CERAMIC DIP
T_{JMAX} = 150°C, θ_{JA} = 100°CW (J8)

LTC1250MJ8
LTC1250CJ8

OBSOLETE PACKAGE
Consider the N8 or S8 for Alternative Source

TOP VIEW



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 110°C, θ_{JA} = 200°CW

ORDER PART NUMBER

LTC1250CS8

S8 PART MARKING

1250

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, V_{IN} = ±5V, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		LTC1250M MIN	LTC1250M TYP	LTC1250M MAX	LTC1250C MIN	LTC1250C TYP	LTC1250C MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C (Note 2)			±5	±10		±5	±10	µV
ΔV_{OS}	Average Input Offset Drift	(Note 2)	●		±0.01	±0.05		±0.01	±0.05	µV/°C
	Long Term Offset Drift				50			50		nV/√Mo
e_n	Input Noise Voltage (Note 3)	T_A = 25°C, 0.1Hz to 10Hz T_A = 25°C, 0.1Hz to 1Hz			0.75 0.2	1.0		0.75 0.2	1.0	μV_{P-P} μV_{P-P}
i_n	Input Noise Current	f = 10Hz			4.0			4.0		fA/√Hz
I_B	Input Bias Current	T_A = 25°C (Note 4)	 ●		±50	±150 ±950		±50	±200 ±450	pA pA
I_{OS}	Input Offset Current	T_A = 25°C (Note 4)	 ●		±100	±300 ±500		±100	±400 ±500	pA pA
CMRR	Common Mode Rejection Ratio	V_{CM} = –4V to 3V	●	110	130		110	130		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.375V to ±8V	●	115	130		115	130		dB
A_{VOL}	Large-Signal Voltage Gain	R_L = 10k, V_{OUT} = ±4V	●	125	170		125	170		dB
	Maximum Output Voltage Swing	R_L = 1k R_L = 100k	●	±4.0	4.3/–4.7 ±4.92		±4.0	4.3/–4.7 ±4.95		V V
SR	Slew Rate	R_L = 10k, C_L = 50pF			10			10		V/µs
GBW	Gain-Bandwidth Product				1.5			1.5		MHz
I_S	Supply Current	No Load, T_A = 25°C	 ●		3.0	4.0 7.0		3.0	4.0 5.0	mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, V_{IN} = ±5V, otherwise specifications are at T_A

SYMBOL	PARAMETER	CONDITIONS		LTC1250M MIN	LTC1250M TYP	LTC1250M MAX	LTC1250C MIN	LTC1250C TYP	LTC1250C MAX	UNITS
f_S	Internal Sampling Frequency	T_A = 25°C			4.75			4.75		kHz
V_{OS}	Input Offset Voltage	T_A = 25°C (Note 2)			±2	±5		±2	±5	µV
ΔV_{OS}	Average Input Offset Drift	(Note 2)	●		±0.01	±0.05		±0.01	±0.05	µV/°C
e_n	Input Noise Voltage (Note 3)	T_A = 25°C, 0.1Hz to 10Hz T_A = 25°C, 0.1Hz to 1Hz			1.0 0.3			1.0 0.3		μV_{P-P} μV_{P-P}
I_B	Input Bias Current	T_A = 25°C (Note 4)			±20	±100		±20	±100	pA
I_{OS}	Input Offset Current Maximum Output Voltage Swing	T_A = 25°C (Note 4) R_L = 1k R_L = 100k		 4.0 	±40 4.3 4.95	±200 	 4.0 	±40 4.3 4.95	±200 	pA V V
I_S	Supply Current	T_A = 25°C			1.8	2.5		1.8	2.5	mA
f_S	Sampling Frequency	T_A = 25°C			3			3		kHz

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

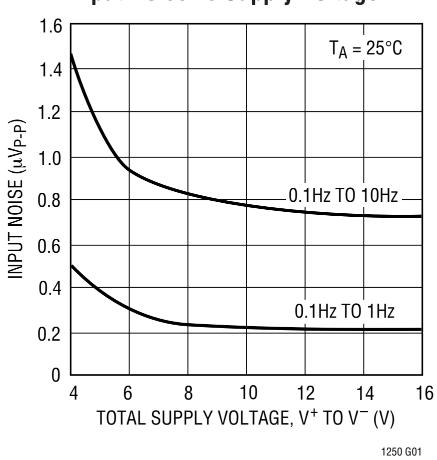
Note 2: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels during automated testing.

Note 3: 0.1Hz to 10Hz noise is specified DC coupled in a 10s window; 0.1Hz to 1Hz noise is specified in a 100s window with an RC high-pass filter at 0.1Hz. The LTC1250 is sample tested for noise; for 100% tested parts contact LTC Marketing Dept.

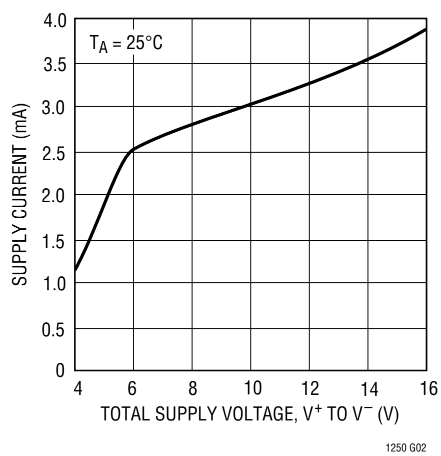
Note 4: At T ≤ 0°C these parameters are guaranteed by design and not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

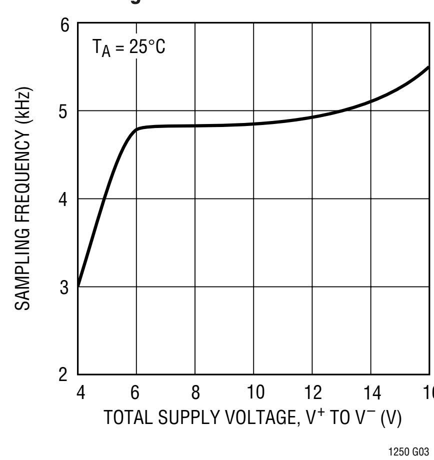
Input Noise vs Supply Voltage



Supply Current vs Supply Voltage

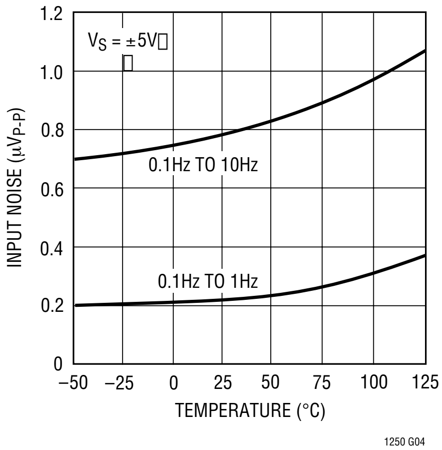


Sampling Frequency vs Supply Voltage

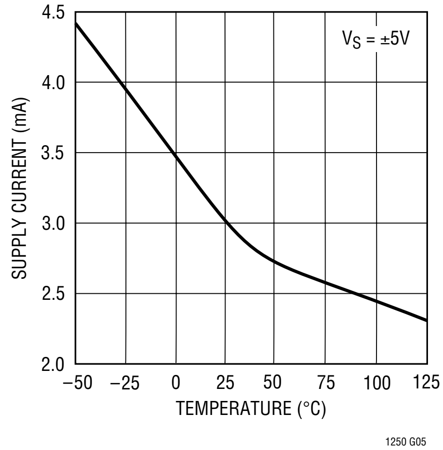


TYPICAL PERFORMANCE CHARACTERISTICS

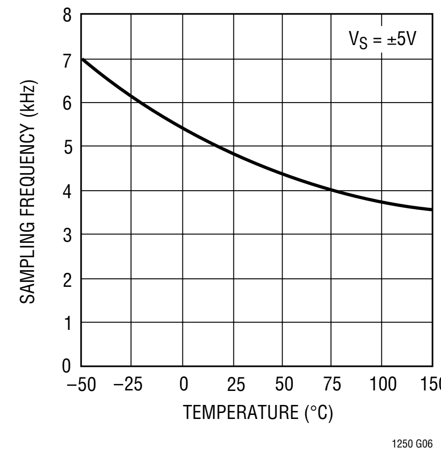
Input Noise vs Temperature



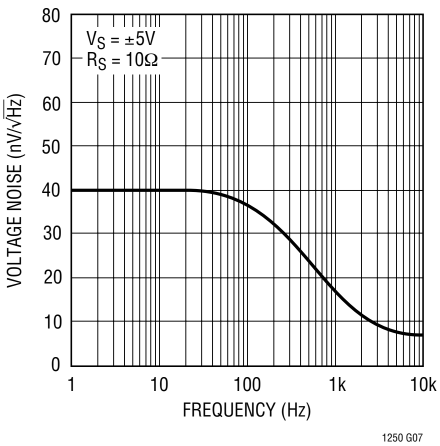
Supply Current vs Temperature



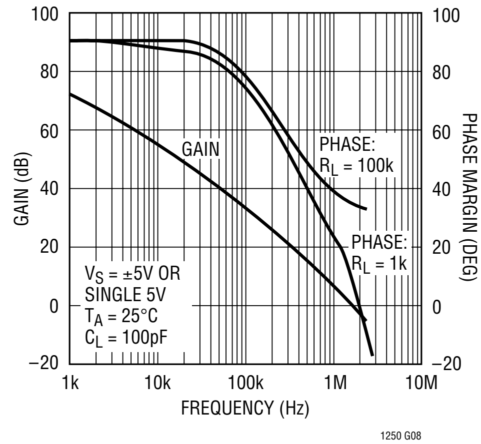
Sampling Frequency vs Temperature



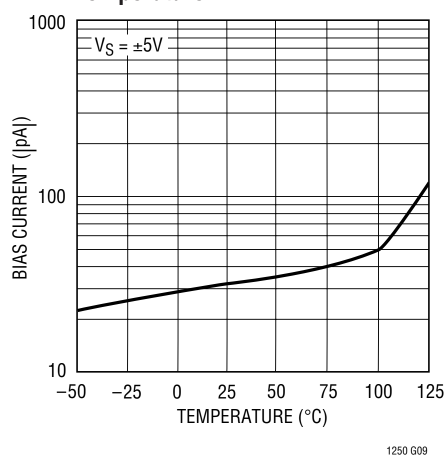
Voltage Noise vs Frequency



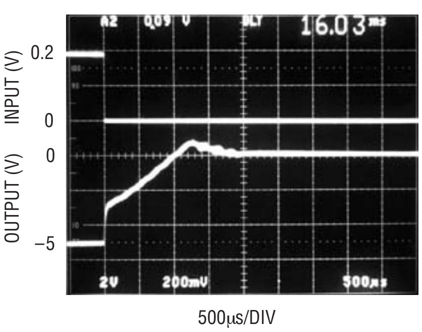
Gain/Phase vs Frequency



Bias Current (Magnitude) vs Temperature

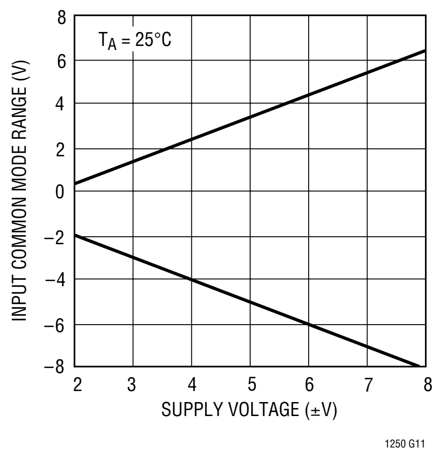


Overload Recovery

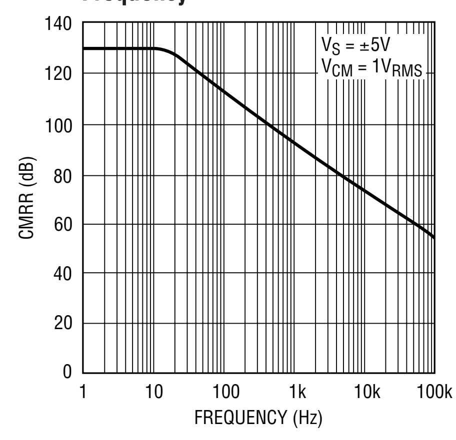


$A_V = 100$, $R_L = 100k$, $C_L = 50pF$, $V_S = \pm 5V$

Common Mode Input Range vs Supply Voltage

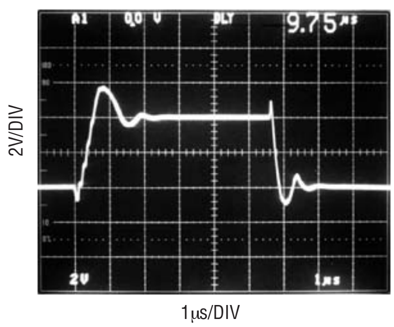


Common Mode Rejection Ratio vs Frequency



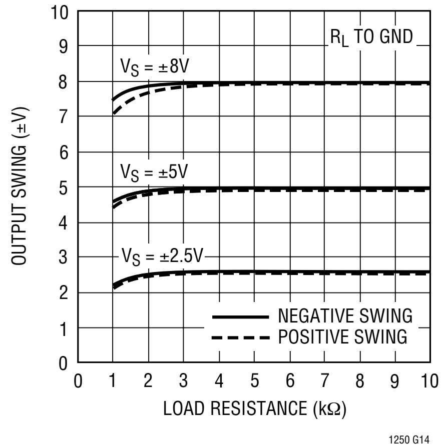
TYPICAL PERFORMANCE CHARACTERISTICS

Transient Response

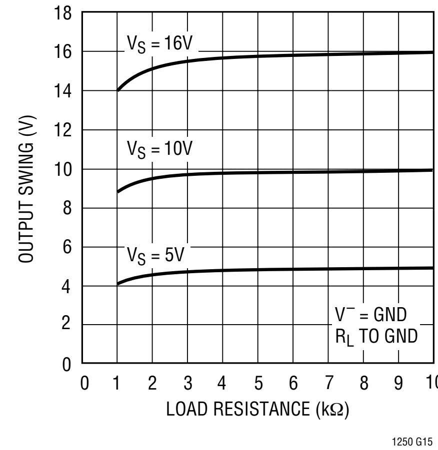


A_V = 1, R_L = 100k, C_L = 50pF, V_S = ±5V

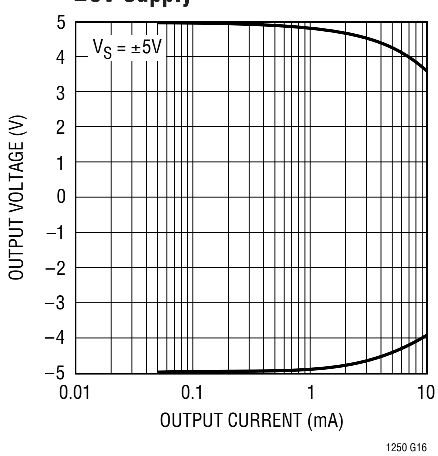
Output Swing vs Load Resistance, Dual Supplies



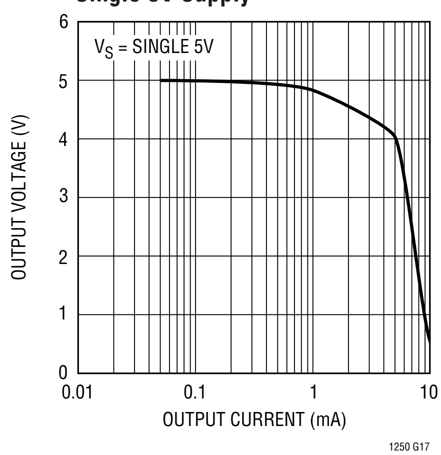
Output Voltage Swing vs Load Resistance, Single Supply



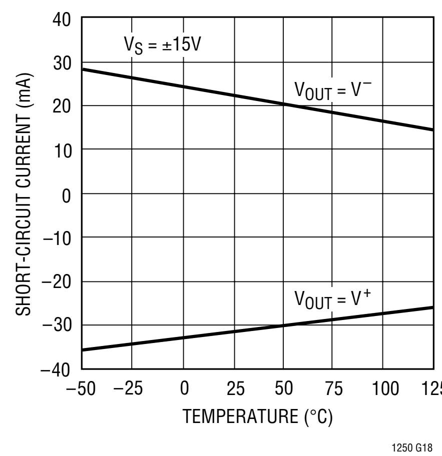
Output Swing vs Output Current, ±5V Supply



Output Swing vs Output Current, Single 5V Supply

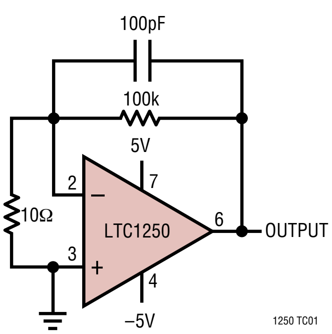


Short-Circuit Current vs Temperature

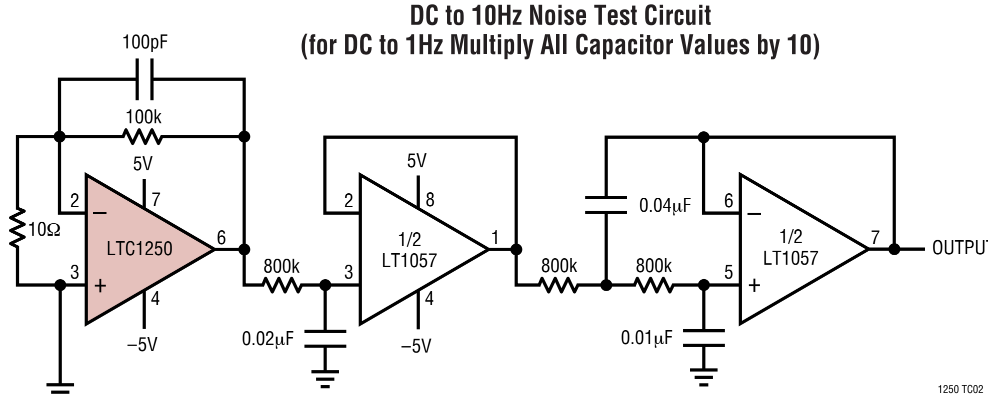


TEST CIRCUITS

Offset Test Circuit



DC to 10Hz Noise Test Circuit (for DC to 1Hz Multiply All Capacitor Values by 10)



APPLICATIONS INFORMATION

Input Noise

The LTC1250, like all CMOS amplifiers, exhibits two types of low frequency noise: thermal noise and 1/f noise. The LTC1250 uses several design modifications to minimize these noise sources. Thermal noise is minimized by raising the g_M of the front-end transistors by running them at high bias levels and using large transistor geometries. 1/f noise is combated by optimizing the zero-drift nulling loop to run at twice the 1/f corner frequency, allowing it to reduce the inherently high CMOS 1/f noise to near thermal levels at low frequencies. The resultant noise spectrum is quite low at frequencies below the internal 5kHz clock frequency, approaching the best bipolar op amps at 10Hz and surpassing them below 1Hz (Figure 1). All this is accomplished in an industry-standard pinout; the LTC1250 requires no external capacitors, no nulling or clock signals, and conforms to industry-standard 8-pin DIP and 8-pin SO packages.

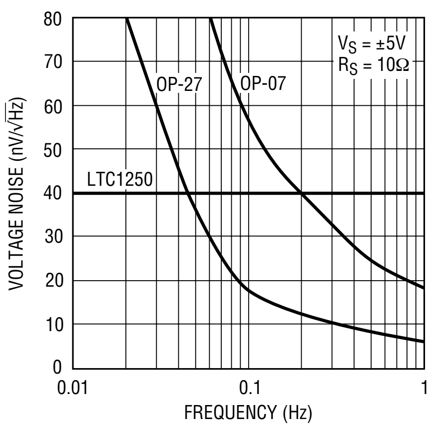


Figure 1. Voltage Noise vs Frequency

Input Capacitance and Compensation

The large input transistors create a parasitic 55pF capacitance from each input to V+. This input capacitance will react with the external feedback resistors to form a pole which can affect amplifier stability. In low gain, high impedance configurations, the pole can land below the unity-gain frequency of the feedback network and degrade phase margin, causing ringing, oscillation, and other unpleasantness. This is true of any op amp, however, the 55pF capacitance at the LTC1250's inputs can affect stability with a feedback network impedance as low as 1.9k. This effect can be eliminated by adding a capacitor across the feedback resistor, adding a zero which cancels the input pole (Figure 2). The value of this capacitor should be:

$$C_F \geq \frac{55pF}{A_V}$$

where A_V = closed-loop gain. Note that C_F is not dependent on the value of R_F. Circuits with higher gain ($A_V > 50$) or low loop impedance should not require C_F for stability.

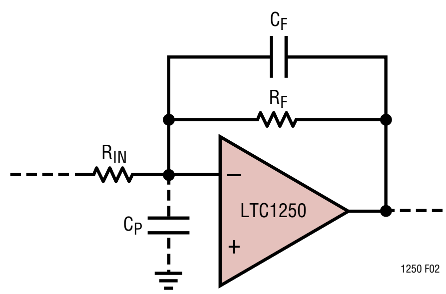


Figure 2. C_F Cancels Phase Shift Due to Parasitic C_P

Larger values of C_F, commonly used in band-limited DC circuits, may actually increase low frequency noise. The nulling circuitry in the LTC1250 closes a loop that includes the external feedback network during part of its cycle. This loop must settle to its final value within 150μs or it will not fully cancel the 1/f noise spectrum and the low frequency noise of the part will rise. If the loop is underdamped (large R_F, no C_F) it will ring for more than 150μs and the noise and offset will suffer.

The solution is to add C_F as above but beware! Too large a value of C_F will overdamp the loop, again preventing it from reaching a final value by the 150μs deadline. This condition doesn't affect the LTC1250's offset or output stability, but 1/f noise begins to rise. As a rule of thumb, the R_FC_F feedback pole should be ≥ 7kHz (1/150μs, the frequency at which the loop settles) for best 1/f performance; values between 100pF and 500pF work well with feedback resistors below 100k. This ensures adequate gain at 7kHz for the LTC1250 to properly null. High value feedback resistors (above 1M) may require experimentation to find the correct value because parasitics, both in the

APPLICATIONS INFORMATION

LTC1250 and on the PC board, play an increasing role. Low value resistors (below 5k) may not require a capacitor at all.

Input Bias Current

The inputs of the LTC1250, like all zero-drift op amps, draw only small switching spikes of AC bias current; DC leakage current is negligible except at very high temperatures. The large front-end transistors cause switching spikes 3 to 4 times greater than standard zero-drift op amps: the ±50pA bias current spec is still many times better than most bipolar parts. The spikes don't match from one input pin to the other, and are sometimes (but not always) of opposite polarity. As a result, matching the impedances at the inputs (Figure 3) will not cancel the bias current, and may cause additional errors. Don't do it.

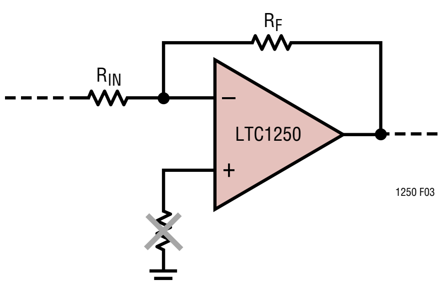


Figure 3. Extra Resistor Will *Not* Cancel Bias Current Errors

Output Drive

The LTC1250 includes an enhanced output stage which provides nearly symmetrical output source/sink currents. This output is capable of swinging a minimum of ±4V into a 1k load with ±5V supplies, and can sink or source >20mA into low impedance loads. Lightly loaded ($R_L \geq 100k$), the LTC1250 will swing to within millivolts of either rail. In single supply applications, it will typically swing 4.3V into a 1k load with a 5V supply.

Minimizing External Errors

The input noise, offset voltage, and bias current specs for the LTC1250 are all well below the levels of circuit board parasitics. Thermocouples between the copper pins of the LTC1250 and the tin/lead solder used to connect them can overwhelm the offset voltage of the LTC1250, especially if a soldering iron has been around recently. Note also that when the LTC1250's output is heavily loaded, the chip may dissipate substantial power, raising the temperature of the package and aggravating thermocouples at the inputs. Although the LTC1250 will maintain its specified accuracy under these conditions, care must be taken in the layout to prevent or compensate circuit errors. Be especially careful of air currents when measuring low frequency noise; nearby moving objects (like people) can create very large noise peaks with an unshielded circuit board. For more detailed explanations and advice on how to avoid these errors, see the LTC1051/LTC1053 data sheet.

Sampling Behavior

The LTC1250's zero-drift nulling loop samples the input at ≈ 5kHz, allowing it to process signals below 2kHz with no aliasing. Signals above this frequency may show aliasing behavior, although wideband internal circuitry generally keeps errors to a minimum. The output of the LTC1250 will have small spikes at the clock frequency and its harmonics; these will vary in amplitude with different feedback configurations. Low frequency or band-limited systems should not be affected, but systems with higher bandwidth (oversampling A/Ds, for example) may need to filter out these clock artifacts. Output spikes can be minimized with a large feedback capacitor, but this will adversely affect noise performance (see Input Capacitance and Compensation on the previous page). Applications which require spike-free output in addition to minimum noise will need a low-pass filter after the LTC1250; a simple RC will usually do the job (Figure 4). The LTC1051/LTC1053 data sheet includes more information about zero-drift amplifier sampling behavior.

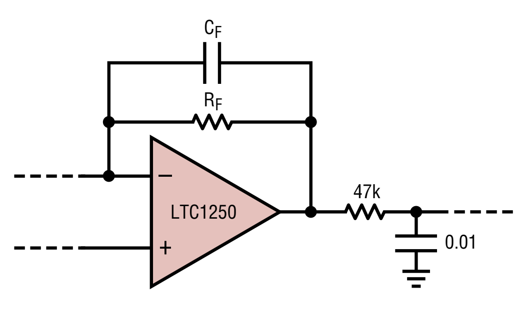


Figure 4. RC Output Pole Limits Bandwidth to 330Hz

APPLICATIONS INFORMATION

Single Supply Operation

The LTC1250 will operate with single supply voltages as low as 4.5V, and the output swings to within millivolts of either supply when lightly loaded. The input stage will common mode to within 250mV of ground with a single 5V supply, and will common mode to ground with single supplies above 11V. Most bridge transducers bias their inputs above ground when powered from single supplies, allowing them to interface directly to the LTC1250 in single supply applications. Single-ended, ground-referenced signals will need to be level shifted slightly to interface to the LTC1250's inputs.

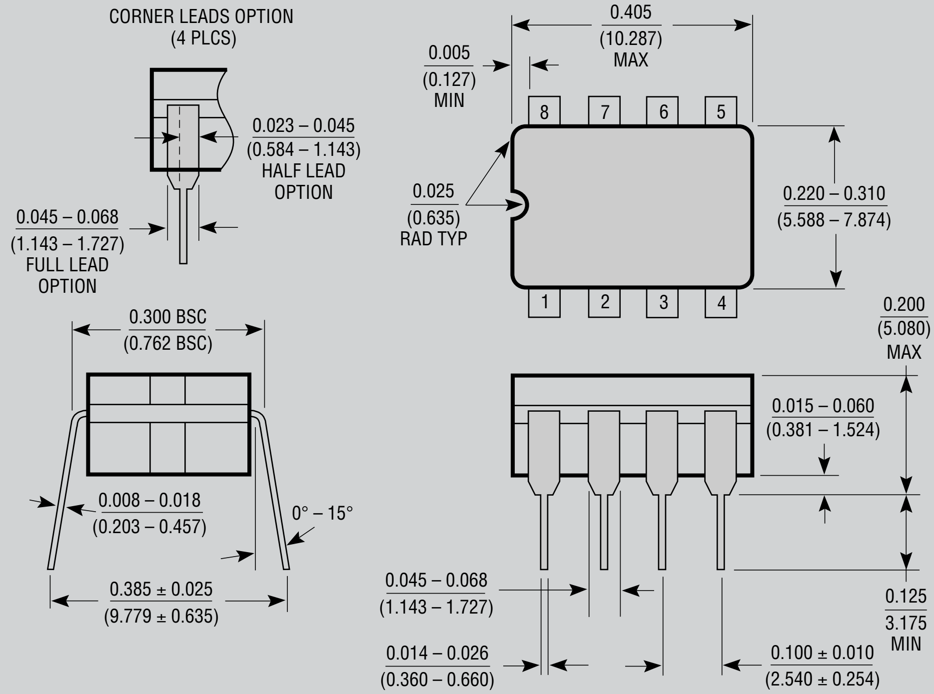
Fault Conditions

The LTC1250 is designed to withstand most external fault conditions without latch-up or damage. However, unusually severe fault conditions can destroy the part. All pins are protected against faults of ±25mA or 5V beyond either supply, whichever comes first. If the external circuitry can exceed these limits, series resistors or voltage clamp diodes should be included to prevent damage.

The LTC1250 includes internal protection against ESD damage. All data sheet parameters are maintained to 1kV ESD on any pin; beyond 1kV, the input bias and offset currents will increase, but the remaining specs are unaffected and the part remains functional to 5kV at the input pins and 8kV at the output pin. Extreme ESD conditions should be guarded against by using standard antistatic precautions.

PACKAGE DESCRIPTION

J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



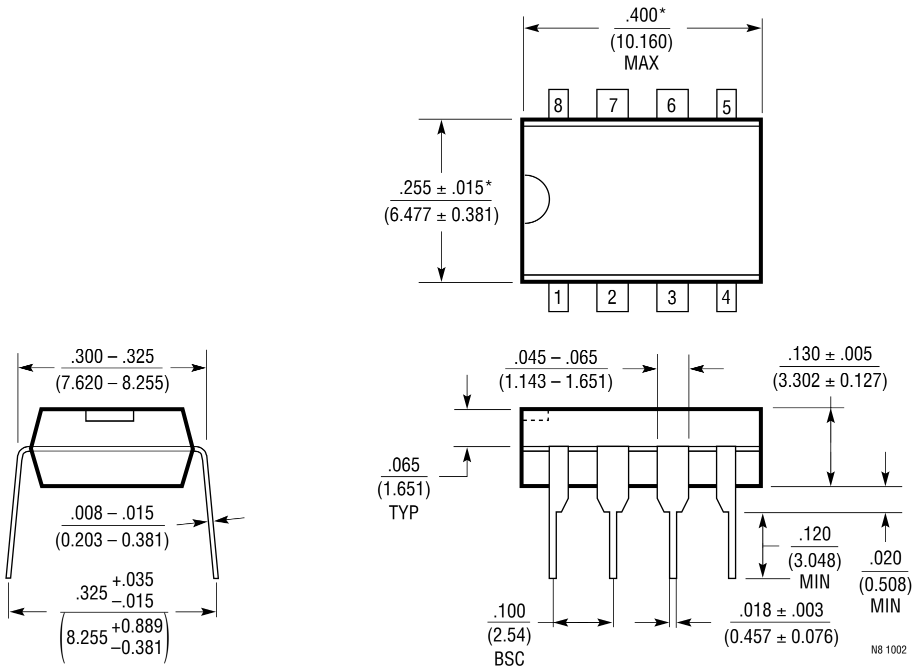
NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

J8 0694

OBSOLETE PACKAGE

PACKAGE DESCRIPTION

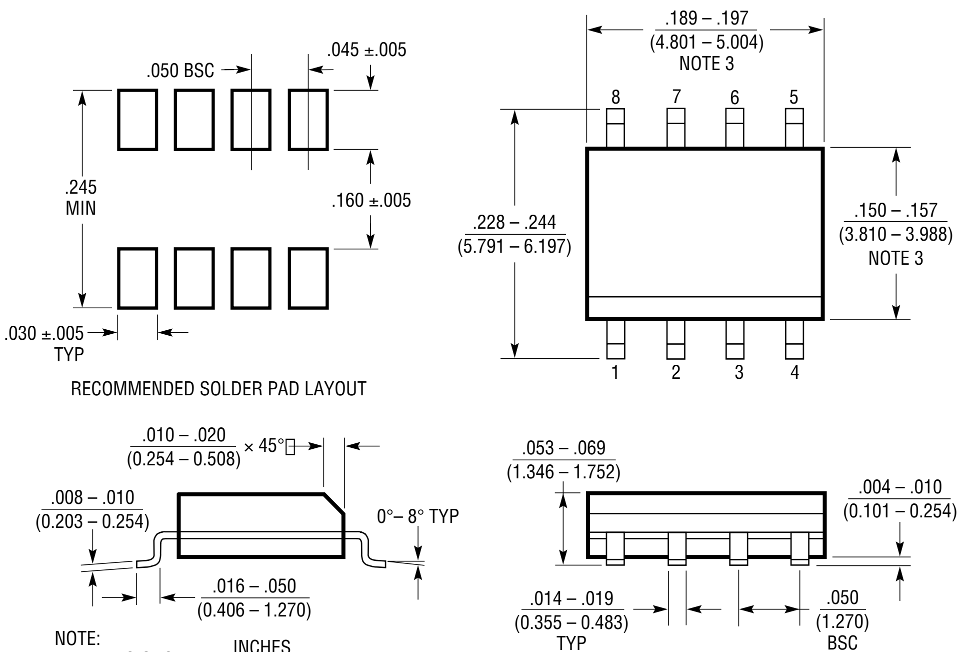
N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

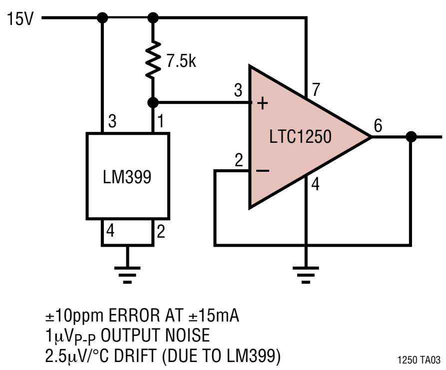


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

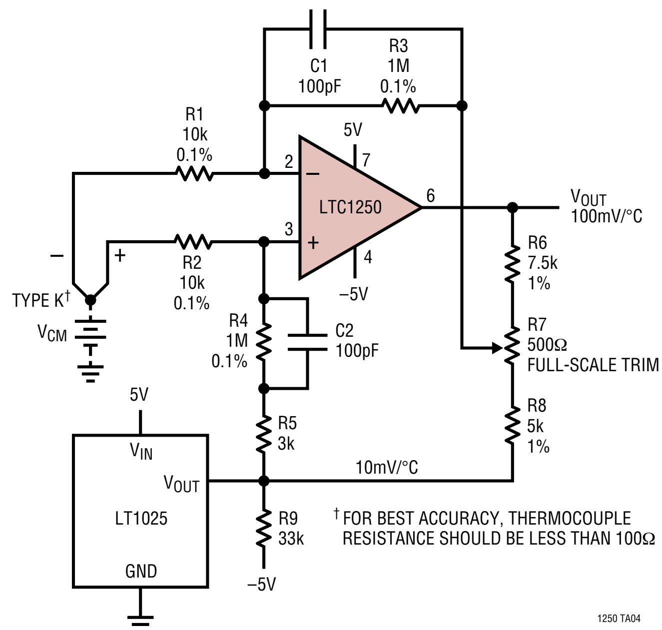
SO8 0303

TYPICAL APPLICATIONS

Reference Buffer



Differential Thermocouple Amplifier



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1050/LTC1051/ LTC1053	Single/Dual/Quad Precision Zero-Drift Op Amp	V_{OS} Max = 5µV, V_{SUPPLY} Max = 16.5V
LTC1150/LTC1151	Single/Dual ±15V Zero-Drift Op Amp	High Voltage Operation
LTC2050/LTC2051/ LTC2052	Single/Dual/Quad Zero-Drift Op Amp	Single Supply 2.7V to =/–5V, SOT-23/MS8/GN16 Package
LTC2053	Zero-Drift Instrumentation Amp	Rail-Rail, MS8, 116dB, Two Resistors Set Gain
LTC2054/LTC2055	Single/Dual Zero-Drift Op Amp	150µA per Amplifier (Max), SOT-23/MS8 Package
LTC6800	Rail-to-Rail Input/Output Instrumentation Amp	Low Cost, Single Supply, MS8, Two Resistors Set Gain

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