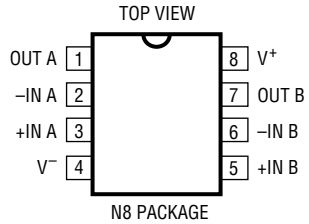
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 36V
Input Voltage (Note 2) ..... (V^+ + 0.3V) to (V^- – 0.3V)
Output Short Circuit Duration ..... Indefinite
Burn-In Voltage 36V

Operating Temperature Range
LTC1151C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION

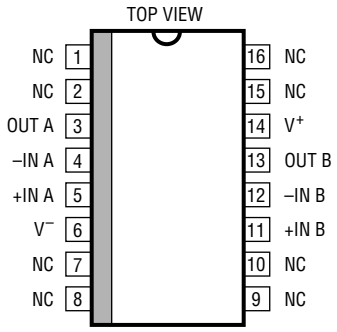


N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LTC1151CN8



SW PACKAGE
16-LEAD PLASTIC SO (WIDE)

T_{JMAX} = 110°C, θ_{JA} = 200°C/W

ORDER PART NUMBER

LTC1151CSW

Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±15V, unless otherwise specified.

PARAMETER	CONDITIONS		LTC1151C MIN	LTC1151C TYP	LTC1151C MAX	UNITS
Input Offset Voltage	T_A = 25°C (Note 3)			±0.5	±5	µV
Average Input Offset Drift	(Note 3)	●		±0.01	±0.05	µV/°C
Long Term Offset Voltage Drift				50		nV/√mo
Input Offset Current	T_A = 25°C	 ●		±20	±200 ±0.5	pA nA
Input Bias Current	T_A = 25°C	 ●		±15	±100 ±0.5	pA nA
Input Noise Voltage	R_S = 100Ω, 0.1Hz to 10Hz R_S = 100Ω, 0.1Hz to 1Hz			1.5 0.5		μV_{P-P} μV_{P-P}
Input Noise Current	f = 10Hz (Note 4)			2.2		fA/√Hz
Input Voltage Range	Positive Negative	● ●	12 –15	13.2 –15.3		V V
Common Mode Rejection Ratio	V_{CM} = V^- to 12V	●	106	130		dB
Power Supply Rejection Ratio	V_S = ±2.375V to ±16V	●	110	130		dB
Large-Signal Voltage Gain	R_L = 10k, V_{OUT} = ±10V	●	125	140		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±15V, unless otherwise specified.

PARAMETER	CONDITIONS		LTC1151C MIN	LTC1151C TYP	LTC1151C MAX	UNITS
Maximum Output Voltage Swing	R_L = 10k, T_A = 25°C R_L = 10k R_L = 100k	 ● 	±13.5 +10.5/–13.5 	±14.50 ±14.95	 	V V V
Slew Rate	R_L = 10k, C_L = 50pF			2.5		V/µs
Gain-Bandwidth Product				2		MHz
Supply Current per Amplifier	No Load, T_A = 25°C No Load	 ●		0.9 	1.5 2.0	mA mA
Internal Sampling Frequency				1000		Hz

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, unless otherwise specified.

Input Offset Voltage	T_A = 25°C (Note 3)			±0.05	±5	µV
Average Input Offset Drift	(Note 3)	●		±0.01	±0.05	µV/°C
Long Term Offset Voltage Drift				50		nV/√mo
Input Offset Current	T_A = 25°C			±10	100	pA
Input Bias Current	T_A = 25°C			±5	50	pA
Input Noise Voltage	R_S = 100Ω, 0.1Hz to 10Hz R_S = 100Ω, 0.1Hz to 1Hz			2.0 0.7		μV_{P-P} μV_{P-P}
Input Noise Current	f = 10Hz (Note 4)			1.3		fA/√Hz
Input Voltage Range	Positive Negative		2.7 0	3.2 –0.3		V V
Common Mode Rejection Ratio	V_{CM} = 0V to 2.7V		110			dB
Power Supply Rejection Ratio	V_S = ±2.375V to ±16V	●	110	130		dB
Large-Signal Voltage Gain	R_L = 10k, V_{OUT} = 0.3V to 4.5V	●	115	140		dB
Maximum Output Voltage Swing	R_L = 10k to GND R_L = 100k to GND			4.85 4.97		V V
Slew Rate	R_L = 10k, C_L = 50pF			1.5		V/µs
Gain Bandwidth Product				1.5		MHz
Supply Current per Amplifier	No Load, T_A = 25°C	 ●		0.5 	1.0 1.5	mA mA
Internal Sampling Frequency				750		Hz

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1151.

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic test systems. V_{OS} is measured to a limit determined by test equipment capability.

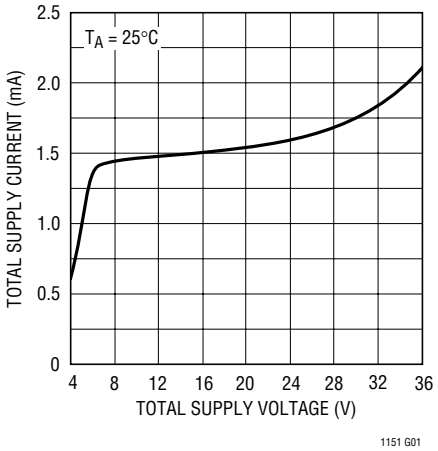
Note 4: Current Noise is calculated from the formula:

$$I_N = \sqrt{(2q \bullet I_b)}$$

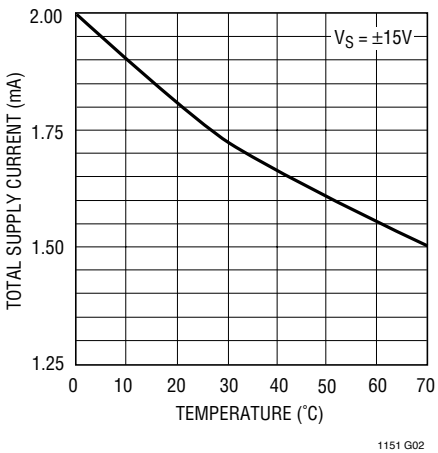
where $q = 1.6 \times 10^{-19}$ Coulomb.

TYPICAL PERFORMANCE CHARACTERISTICS

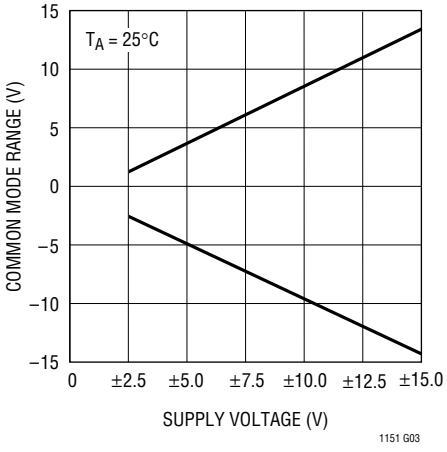
Supply Current vs Supply Voltage



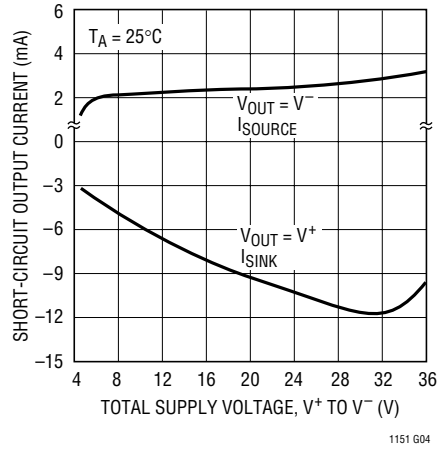
Supply Current vs Temperature



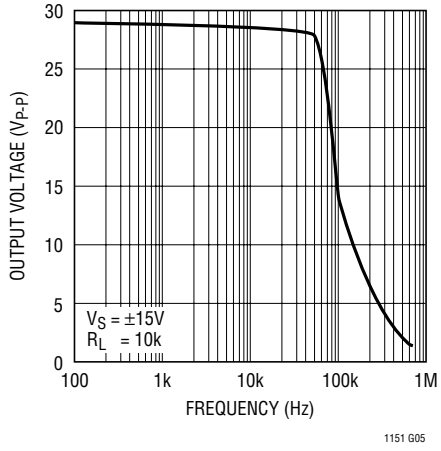
Common Mode Input Voltage Range vs Supply Voltage



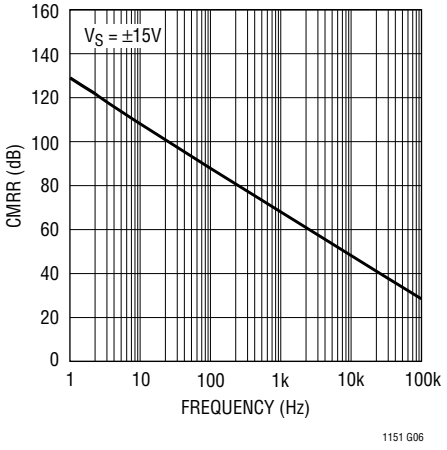
Output Short-Circuit Current vs Supply Voltage



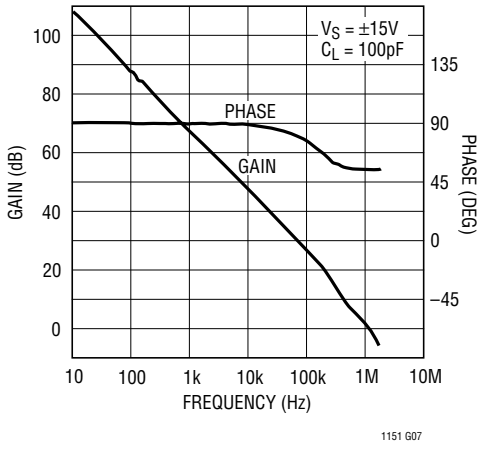
Undistorted Output Swing vs Frequency



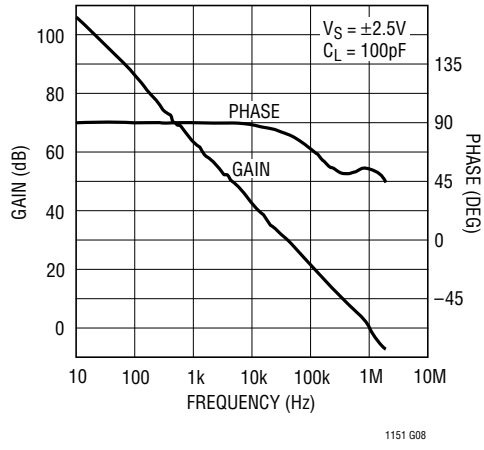
CMRR vs Frequency



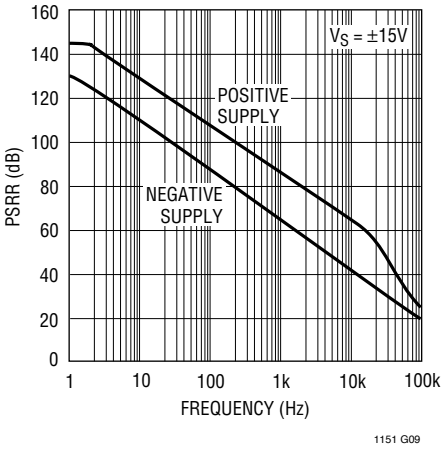
Gain and Phase vs Frequency



Gain and Phase vs Frequency

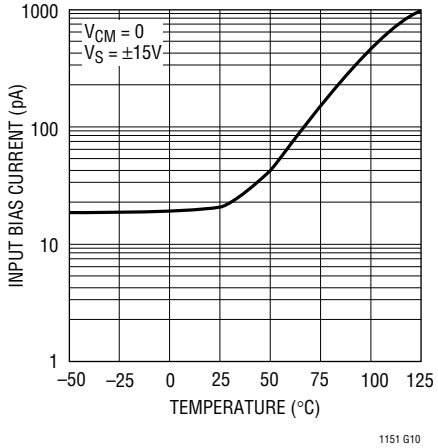


PSRR vs Frequency

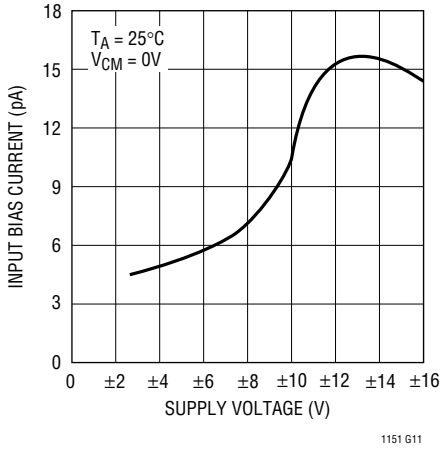


TYPICAL PERFORMANCE CHARACTERISTICS

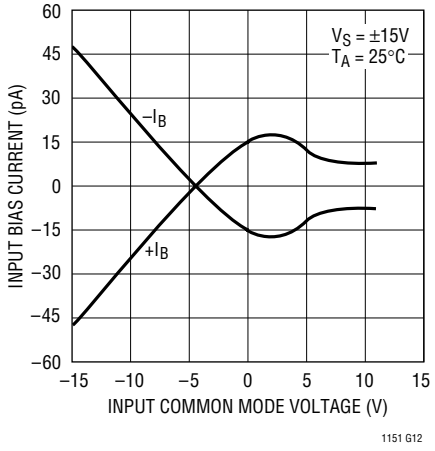
Input Bias Current Magnitude vs Temperature



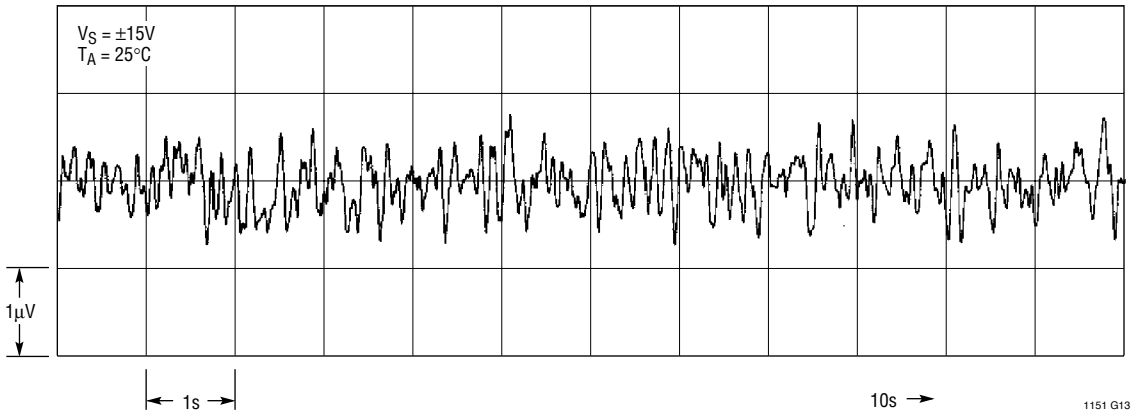
Input Bias Current Magnitude vs Supply Voltage



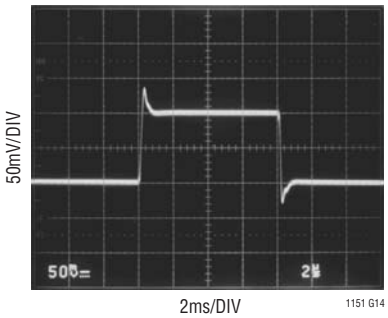
Input Bias Current vs Input Common Mode Voltage



0.1Hz to 10Hz Noise

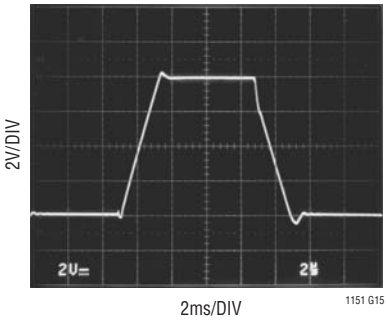


Small-Signal Transient Response



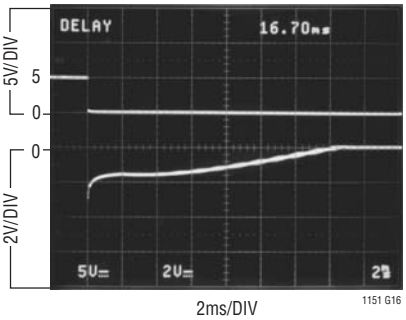
V_S = ±15V, A_V = 1
C_L = 100pF, R_L = 10k

Large-Signal Transient Response



V_S = ±15V, A_V = 1
C_L = 100pF, R_L = 10k

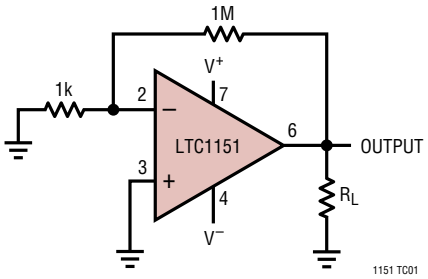
Negative Overload Recovery



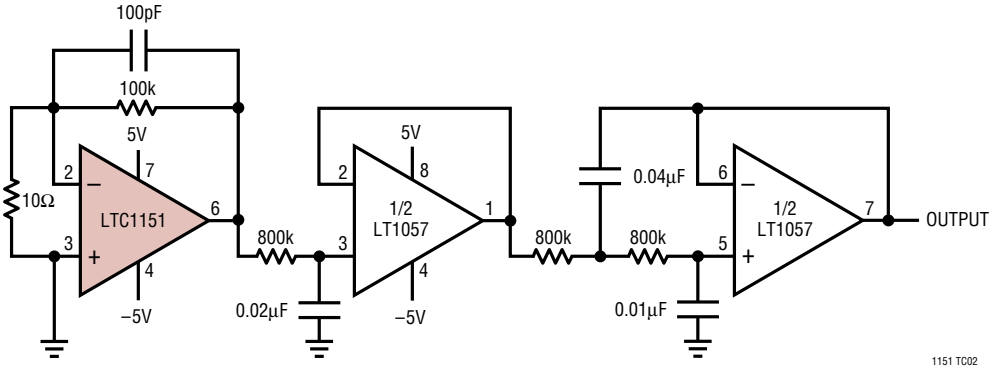
V_S = ±15V, A_V = –100
NOTE: POSITIVE OVERLOAD RECOVERY IS TYPICALLY 3ms.

TEST CIRCUITS

Offset Voltage Test Circuit



DC-10Hz Noise Test Circuit



APPLICATIONS INFORMATION

ACHIEVING PICOAMPERE/MICROVOLT PERFORMANCE

Picoamperes

In order to realize the picoampere level of accuracy of the LTC1151 proper care must be exercised. Leakage currents in circuitry external to the amplifier can significantly degrade performance. High quality insulation should be used (e.g., Teflon); cleaning of all insulating surfaces to remove fluxes and other residues will probably be necessary, particularly for high temperature performance. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground; in noninverting connections to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

Microvolts

Thermocouple effects must be considered if the LTC1151's ultra low drift is to be fully utilized. Any connection of dissimilar metals forms a thermoelectric junction producing an electric potential which varies with temperature (Seebeck effect). As temperature sensors, thermocouples exploit this phenomenon to produce useful information. In low drift amplifier circuits the effect is a primary source of error.

Connectors, switches, relay contacts, sockets, resistors, solder, and even copper wire are all candidates for thermal EMF generation. Junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C; four times the maximum drift specification of the LTC1151.

Minimizing thermal EMF-induced errors is possible if judicious attention is given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the amplifier's input signal path. Avoid connectors, sockets, switches and relays where possible. In instances where this is not possible, attempt to balance the number and type of junctions so that differential cancellation occurs. Doing this may involve deliberately introducing junctions to offset unavoidable junctions.

Figure 1 is an example of the introduction of an unnecessary resistor to promote differential thermal balance. Maintaining compensating junctions in close physical proximity will keep them at the same temperature and reduce thermal EMF errors.

When connectors, switches, relays and/or sockets are necessary they should be selected for low thermal EMF activity. The same techniques of thermally balancing and coupling the matching junctions are effective in reducing the thermal EMF errors of these components.

APPLICATIONS INFORMATION

Resistors are another source of thermal EMF errors. Table 1 shows the thermal EMF generated for different resistors. The temperature gradient across the resistor is important, not the ambient temperature. There are two junctions formed at each end of the resistor and if these junctions are at the same temperature, their thermal EMFs will cancel each other. The thermal EMF numbers are approximate and vary with resistor value. High values give higher thermal EMF.

Table 1. Resistor Thermal EMF

RESISTOR TYPE	THERMAL EMF/°C GRADIENT
Tin Oxide	>1mV/°C
Carbon Composition	~450µV/°C
Metal Film	~20µV/°C
Wire Wound Evenohm, Manganin	~2µV/°C

PACKAGE-INDUCED OFFSET VOLTAGE

Package-induced thermal EMF effects are another important source of errors. They arise at the junctions formed when wire or printed circuit traces contact a package lead. Like all the previously mentioned thermal EMF effects, they are outside the LTC1151's offset nulling loop and cannot be cancelled. The input offset voltage specification of the LTC1151 is actually set by the package-induced warm-up drift rather than by the circuit itself. The thermal time constant ranges from 0.5 to 3 minutes, depending on package type.

ALIASING

Like all sampled data systems, the LTC1151 exhibits aliasing behavior at input frequencies near the sampling frequency. The LTC1151 includes a high frequency correction loop which minimizes this effect. As a result, aliasing is not a problem for many applications.

For a complete discussion of the correction circuitry and aliasing behavior, please refer to the LTC1051/LTC1053 data sheet.

LOW SUPPLY OPERATION

The minimum supply for proper operation of the LTC1151 is typically 4.0V (±2.0V). In single supply applications, PSRR is guaranteed down to 4.7V (±2.35V) to ensure proper operation at minimum TTL supply voltage of 4.75V.

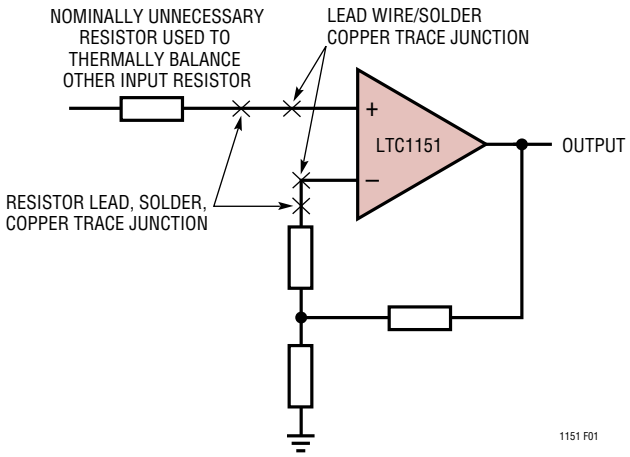
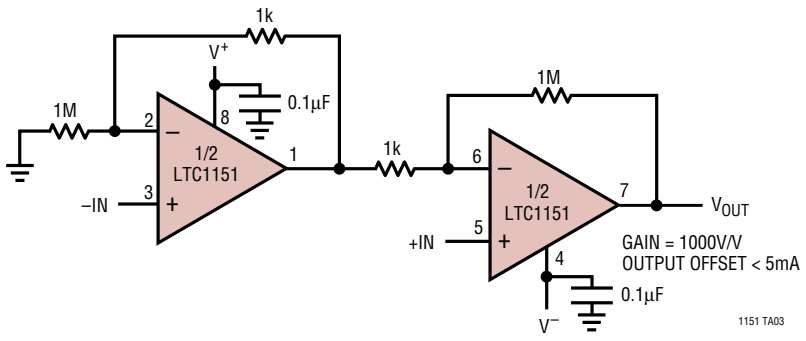


Figure 1. Extra Resistors Cancel Thermal EMF

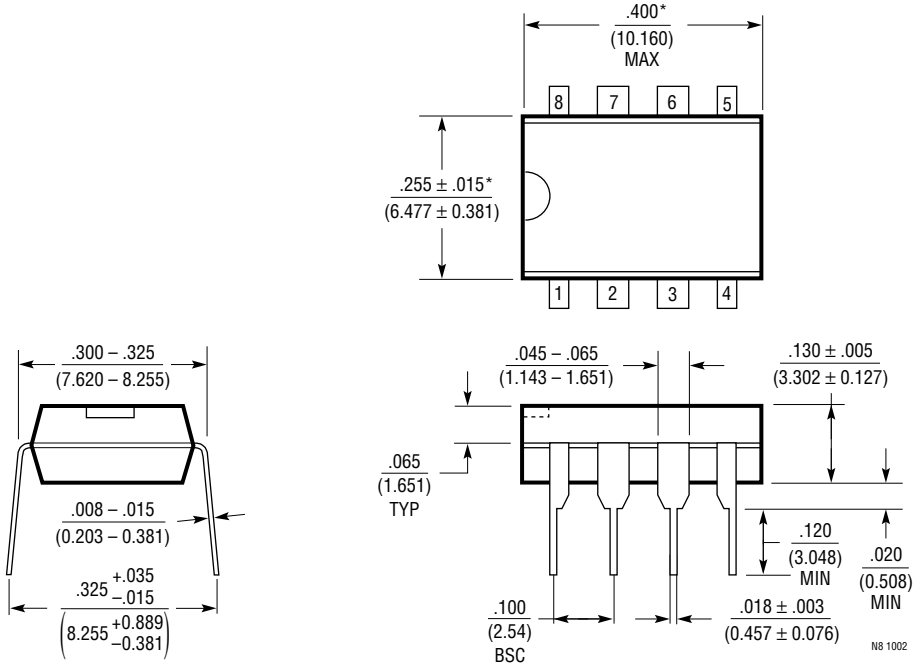
TYPICAL APPLICATIONS

High Voltage Instrumentation Amplifier



PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)

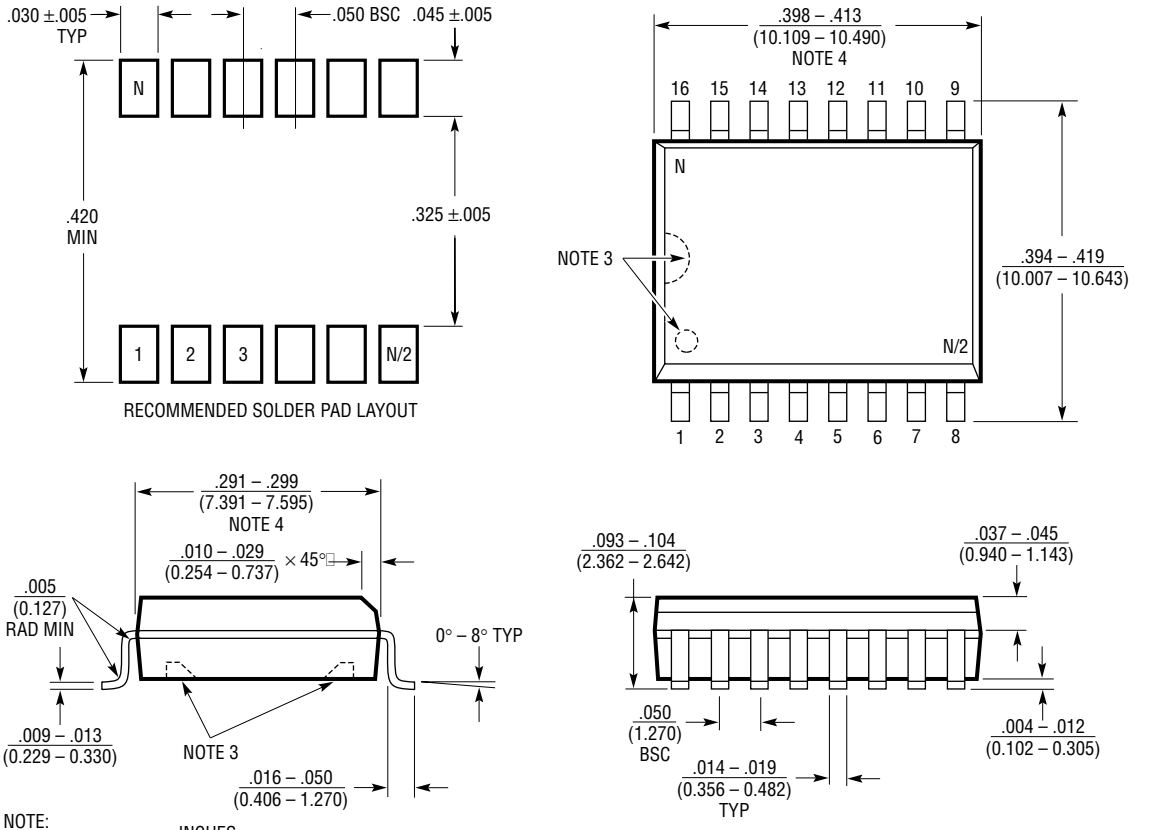


NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

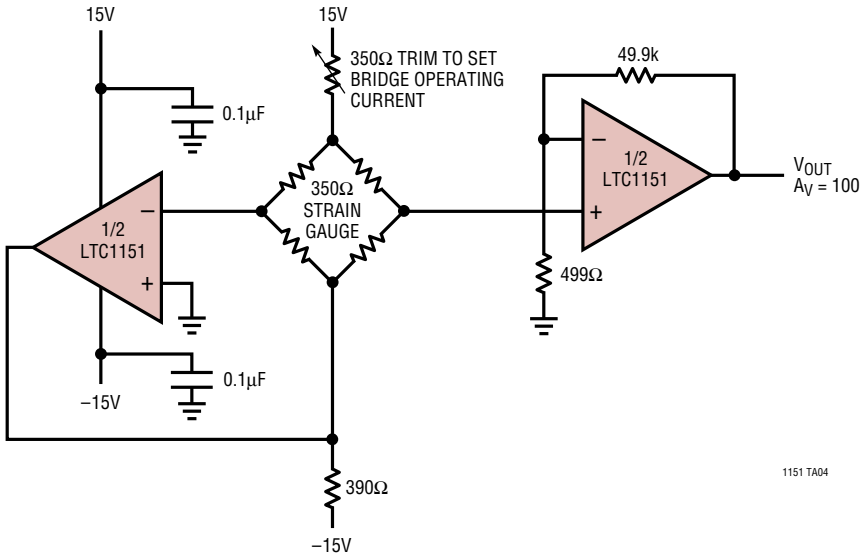
SW Package
16-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

TYPICAL APPLICATIONS

Bridge Amplifier with Active Common-Mode Suppression



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1049	Low Power Zero-Drift Op Amp	Low Supply Current 200µA
LTC1050	Precision Zero-Drift Op Amp	Single Supply Operation 4.75V to 16V, Noise Tested and Guaranteed
LTC1051/LTC1053	Precision Zero-Drift Op Amp	Dual/Quad
LTC1150	±15V Zero-Drift Op Amp	High Voltage Operation ±18V
LTC1152	Rail-to-Rail Input and Output Zero-Drift Op Amp	Single Zero-Drift Op Amp with Rail-to-Rail Input and Output and Shutdown
LT1677	Low Noise Rail-toRail Input and Output	V_{OS} = 90µV, V_S = 2.7V to 44V Precision Op Amp
LT1884/LT1885	Rail-to-Rail Output Precision Op Amp	V_{OS} = 50µV, I_B = 400pA, V_S = 2.7V to 40V
LTC2050/LTC2051/LTC2052	Single/Dual/Quad Zero-Drift Op Amp	Single Supply, 2.7V to ±5V, SOT-23/MS8/GN 16 Package
LTC2053	Zero-Drift Instrumentation Amp	Rail-to-Rail, MS8, 116dB, Two Resistors Set Gain
LTC2054/LTC2055	Single/Dual Zero-Drift Op Amp	150µA per Amplifier (Max), SOT-23/MS8 Package

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