

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} , $\overline{SHDN}$ Voltage	16V
SWP, SWN, V_{POS} Voltage	36V
DN Voltage	-36V
FBP, FBN, SSP, SSN Voltage	10V
Maximum Junction Temperature	125°C
Operating Temperature Range	
Extended Commercial	-40°C to 85°C
Storage Temperature Range	-65°C to 125°C

PACKAGE/ORDER INFORMATION

DD PACKAGE 10-LEAD (3mm × 3mm) PLASTIC DFN $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 43^{\circ}\text{C/W}$, $\theta_{JC} = 3^{\circ}\text{C/W}$ EXPOSED PAD IS GND (PIN 11) MUST BE SOLDERED TO PCB	ORDER PART NUMBER
	LT3472EDD
	DFN PART MARKING
	LBGC

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. $V_{IN} = 3\text{V}$, $\overline{SHDN} = 3\text{V}$ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Operation Voltage		2.2			V
Maximum Operation Voltage				16	V
Supply Current	$\overline{SHDN} = 3\text{V}$, Not Switching $\overline{SHDN} = 0\text{V}$		2.8 0.1	1	mA μA
$\overline{SHDN}$ Voltage High		● 0.8			V
$\overline{SHDN}$ Voltage Low		●		0.3	V
$\overline{SHDN}$ Pin Bias Current	$\overline{SHDN} = 3\text{V}$		35		μA
Positive Feedback Voltage		● 1.2	1.25	1.3	V
Negative Feedback Voltage		● -5	0	5	mV
Positive Feedback Voltage Line Regulation			0.01		%/V
Negative Feedback Voltage Line Regulation			0.008		mV/V
FBP Current	$\text{FBP} = V_{\text{FBP}}$	● 24.5	25	25.3	μA
FBN Current	$\text{FBN} = V_{\text{FBN}}$	● 24.5	25	25.3	μA
FBP to Start Negative Channel		1.02	1.1	1.18	V
Switching Frequency		0.9	1.1	1.4	MHz
Maximum Duty Cycle (Both Channels)		● 88	92		%
Positive Channel Switch Current Limit		● 250	350		mA
Negative Channel Switch Current Limit		● 300	400		mA
Positive Channel Switch V_{CESAT}	$I_{\text{SWP}} = 200\text{mA}$		245		mV
Negative Channel Switch V_{CESAT}	$I_{\text{SWN}} = 200\text{mA}$		400		mV
Switch Leakage Current (Both Channels)	$V_{\text{SW}} = 5\text{V}$		0.01	5	μA
Schottky DP Forward Drop	$I_{\text{DP}} = 150\text{mA}$		700	950	mV
Schottky DN Forward Drop	$I_{\text{DN}} = 150\text{mA}$		750	1000	mV
Schottky Leakage Current (Both Channels)	$V_R = 36\text{V}$			4	μA

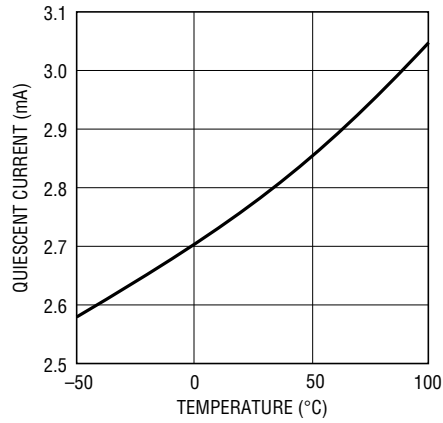
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LT3472E is guaranteed to meet specified performance from

0°C to 70°C. Specifications over the -40°C to 85°C operating range are assured by design, characterization and correlation with statistical process controls.

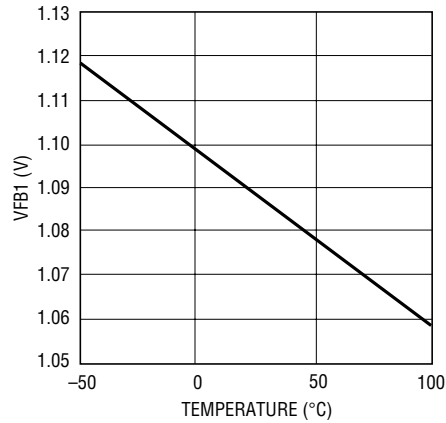
TYPICAL PERFORMANCE CHARACTERISTICS

Quiescent Current



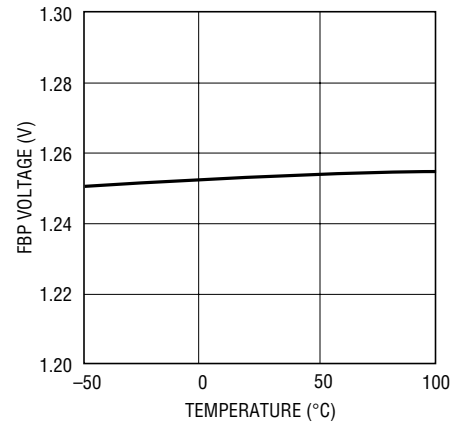
3472 G01

Minimum FBP Voltage to Enable Inverter



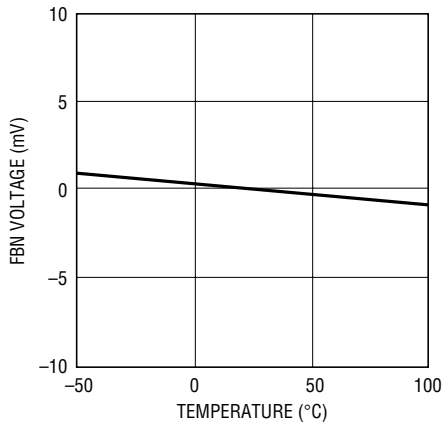
3472 G02

FBP Voltage



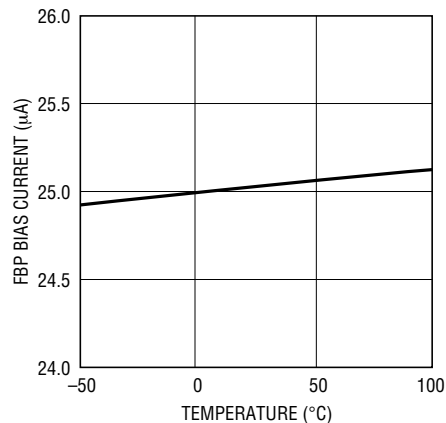
3472 G03

FBN Voltage



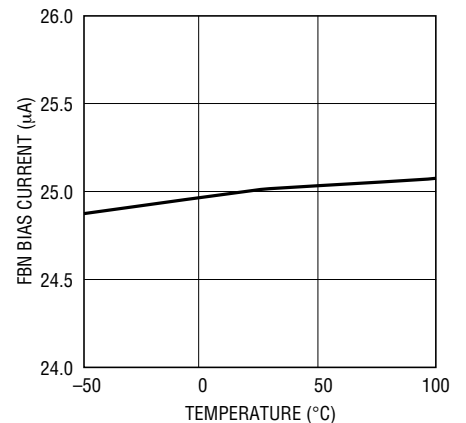
3472 G04

FBP Bias Current



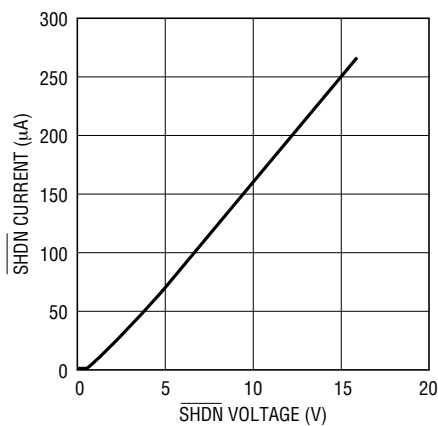
3472 G05

FBN Bias Current



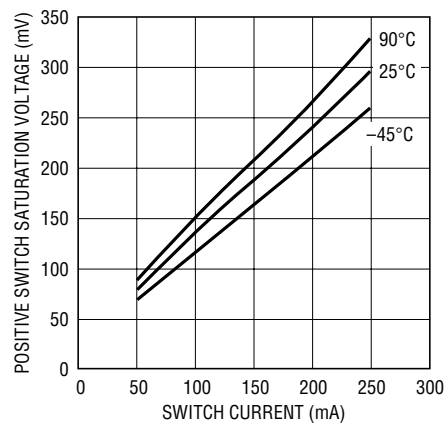
3472 G06

SHDN Pin Bias Current



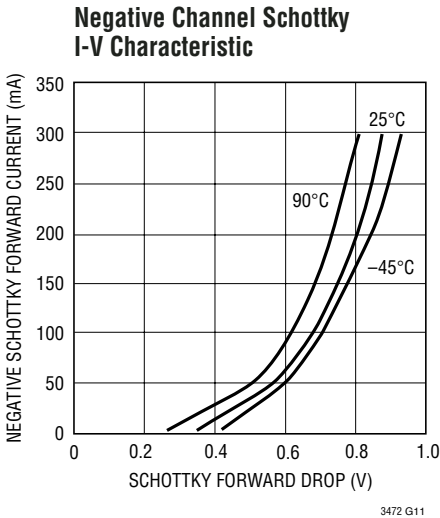
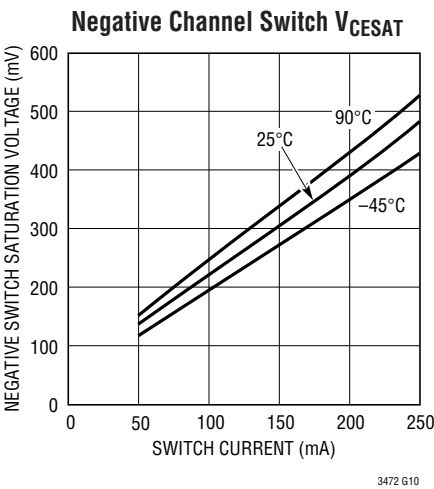
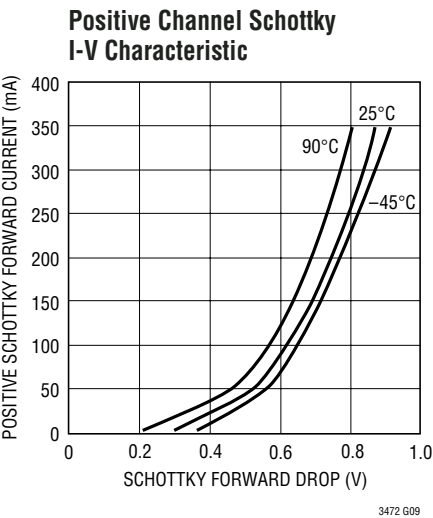
3472 G07

Positive Channel Switch V_{CESAT}



3472 G08

TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS

SWP (Pin 1): Switch Pin for Positive (Boost) Channel. Connect boost inductor here.

V_{IN} (Pin 2): Input Supply Pin. Must be locally bypassed with a X5R or X7R type ceramic capacitor.

SHDN (Pin 3): Shutdown Pin. Connect to 0.8V or higher to enable device, 0.3V or less to disable device.

SWN (Pin 4): Switch Pin for Negative (Inverter) Channel. Connect inverter input inductor and flying capacitor here.

DN (Pin 5): Anode of Internal Schottky for Inverter. Connect inverter output inductor and flying capacitor here.

FBN (Pin 6): Feedback Pin for Inverter. Connect feedback resistor R2 from this pin to V_{O2}. Choose R2 according to $V_{O2} = 1.25 \cdot R2/50k$. Pin voltage = 0V when regulated.

SSN (Pin 7): Soft Start-Up Pin for Inverter. Connect a cap here for soft start-up. Leave open for quick start-up. This pin is connected to 1.25V with a 50k resistor internally.

FBP (Pin 8): Feedback Pin for Boost. Connect boost feedback resistor R1 from this Pin to V_{O1}. Choose R1 according to $V_{O1} = 1.25 \cdot (1 + R1/50k)$. Pin voltage = 1.25V when regulated.

SSP (Pin 9): Soft Start-Up Pin for Boost. Connect a cap here for soft start-up. Leave open for quick start-up. This pin is connected to 1.25V with a 50k resistor internally.

V_{POS} (Pin 10): Output Pin for Boost. Connect boost output capacitor here.

GND (Exposed Pad) (Pin 11): GND Pin. Tie directly to ground plane through multiple vias under the package for optimum thermal performance.

BLOCK DIAGRAM

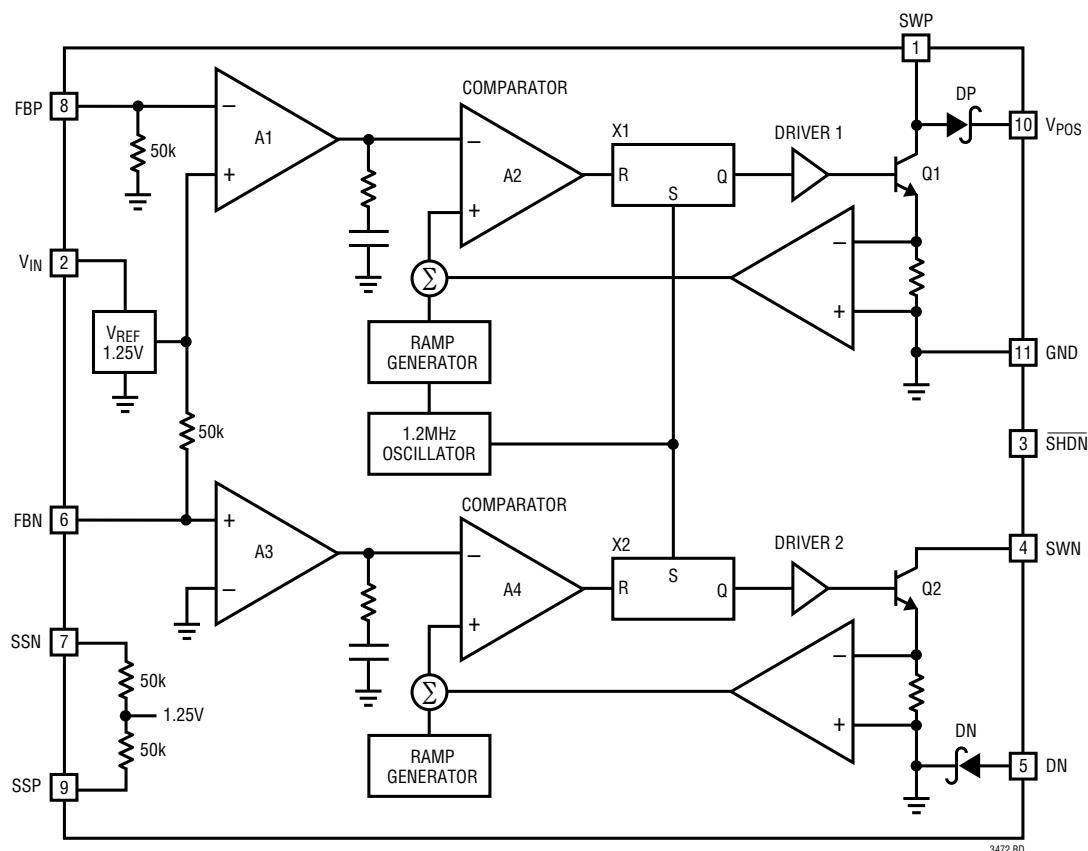


Figure 1. LT3472 Block Diagram

APPLICATIONS INFORMATION

Operation

The LT3472 uses a constant frequency, current mode control scheme to provide excellent line and load regulation. Operation can be best understood by referring to the block diagram in Figure 1. At the start of each oscillator cycle, the SR latch X1 is set, which turns on the power switch Q1. A voltage proportional to the switch current is added to a stabilizing ramp and the resulting sum is fed into the positive terminal of the PWM comparator A2. When this voltage exceeds the level at the negative input of A2, the SR latch X1 is reset turning off the power switch Q1. The level at the negative input of A2 is set by the error amplifier A1, and is simply an amplified version of the difference between the feedback voltage and the reference voltage of 1.25V. In this manner, the error amplifier sets the correct peak current level to keep the output in regulation. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered. The second channel is an inverting converter. The basic operation is the same as the positive channel. The SR latch X2 is also set at the start of each oscillator cycle. The power switch Q2 is turned on at the same time as Q1. The turn off of Q2 is determined by its own feedback loop, which consists of error amplifier A3 and PWM comparator A4. The reference voltage of this negative channel is ground.

Switching waveforms with typical load conditions are shown in Figure 2.

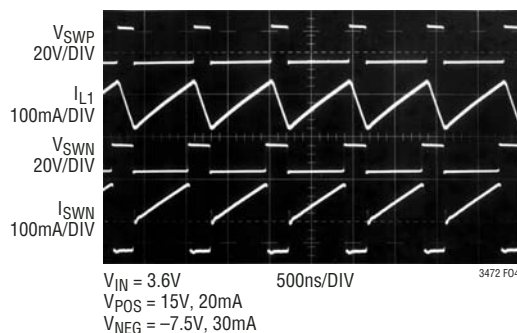


Figure 2. Switching Waveforms

Inductor Selection

A 22 μ H inductor is recommended for LT3472 step-up channel. The inverter channel can use a 22 μ H or 47 μ H inductor. 47 μ H inductors will provide slightly more current. Small size and high efficiency are the major concerns for most LT3472 applications. Inductors with low core losses and small DCR (copper wire resistance) at 1.1MHz are good choices for LT3472 applications. Some inductors in this category with small size are listed in Table 1. The efficiency comparison of different inductors is shown in Figure 3.

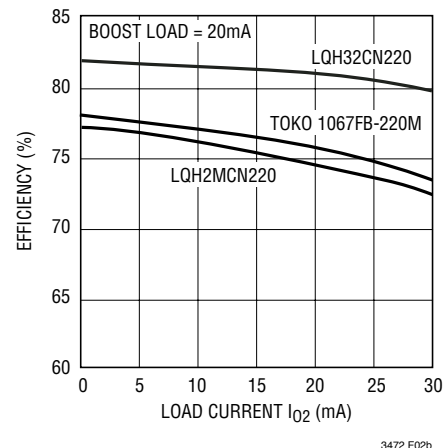
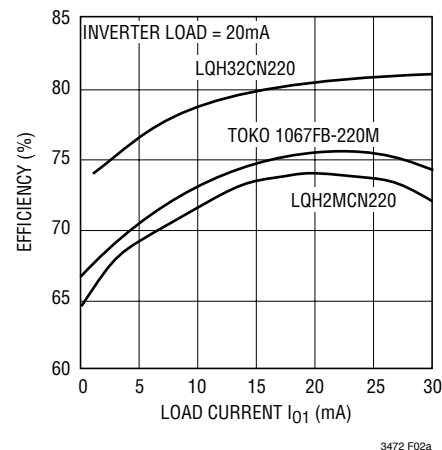


Figure 3. Efficiency Comparison of Different Inductors

APPLICATIONS INFORMATION

Table 1. Recommended Inductors

Part No.	Inductance (μH)	DCR (Ω)	Current Rating (mA)	Manufacturer
LQH32CN220	22	0.71	250	Murata (814) 237-1431 www.murata.com
LQH32CN470	47	1.3	170	
LQH2MCN220	22	2.1	185	
LQH2MCN470	47	5.1	120	
D1067FB-220M	22	2.0	270	TOKO (408) 432-8281 www.tokoam.com
ELJPC220KF	22	4.0	160	Panasonic (714) 373-7334 www.panasonic.com
CDRH3D16-220	22	0.53	350	Sumida (847) 956-0666 www.sumida.com
LB2012B220M	22	1.7	75	Taiyo Yuden (408) 573-4150 www.t-yuden.com
LEM2520-220	22	5.5	125	

Capacitor Selection

The small size of ceramic capacitors makes them suitable for LT3472 applications. X5R and X57 types of ceramic capacitors are recommended because they retain their capacitance over wider voltage and temperature ranges than other types such as Y5V or Z5U. A 2.2μF input capacitor and a 2.2μF output capacitor are sufficient for most LT3472 applications.

Table 2. Recommended Ceramic Capacitor Manufacturers

Manufacturer	Phone	URL
Taiyo Yuden	(408) 573-4150	www.t-yuden.com
Murata	(814) 237-1431	www.murata.com
Kemet	(408) 986-0424	www.kemet.com

Inrush Current

The LT3472 uses internal Schottky diodes. When supply voltage is abruptly applied to V_{IN} pin, for the positive channel, the voltage difference between V_{IN} and V_{POS} generates inrush current flowing from input through the inductor L_P and the internal Schottky diode D_P to charge the output capacitor C_{OP} . For the inverter channel, there is a similar inrush current flowing from input through the inductor L_{N1} path, charging the capacitor C_{NF} , and returning through the internal Schottky diode D_N . The maximum current the Schottky diodes in the LT3472 can sustain is

1A. The selection of inductor and capacitor value should ensure the peak of the inrush current to be below 1A. The peak inrush current can be calculated as follows:

$$I_P = \frac{V_{IN} - 0.6}{L \cdot \omega} \cdot \text{EXP} \left[-\frac{\alpha}{\omega} \cdot \arctan \left(\frac{\omega}{\alpha} \right) \right] \cdot \text{SIN} \left[\arctan \left(\frac{\omega}{\alpha} \right) \right]$$

$$\alpha = \frac{r + 1.5}{2 \cdot L}$$

$$\omega = \sqrt{\frac{1}{L \cdot C} - \frac{r}{4 \cdot L^2}}$$

where L is the inductance, r is the resistance of the inductor and C is the output capacitance. For low DCR inductors, which is usually the case for this application, the peak inrush current can be simplified as follows:

$$I_P = \frac{V_{IN} - 0.6}{L \cdot \omega} \cdot \text{EXP} \left(-\frac{\alpha}{\omega} \cdot \frac{\pi}{2} \right)$$

Table 3 gives inrush peak currents for some component selections. Note that inrush current is not a concern if the input voltage rises slowly.

Table 3. Inrush Peak Current

V_{IN} (V)	r (Ω)	L (μH)	C (μF)	I_P (A)
5	0.5	22	2.2	0.89
3.6	0.7	22	2.2	0.59
3.6	2.1	22	2.2	0.46
3.6	1.3	47	1	0.32
3.6	0.7	22	1	0.46

External Diode Selection

As stated previously the LT3472 has internal Schottky diodes. The Schottky diode D_P is sufficient for most step-up applications. However, for high current inverter applications, a properly selected external Schottky diode in parallel with D_N can improve efficiency. For external diode selection, both forward voltage drop and diode capacitance need to be considered. Schottky diodes rated for higher current usually have lower forward voltage drop

APPLICATIONS INFORMATION

and larger capacitance, which can cause significant switching losses at 1.1MHz switching frequency. Some recommended Schottky diodes are listed in Table 4.

Table 4. Recommended Schottky Diodes

Part No.	Forward Current (mA)	Forward Voltage Drop (V)	Diode Capacitance (pF)	Manufacturer
CMDSH-3	100	0.58 @100mA	7 @ 10V	Central Semiconductor (631) 435-1110 www.centalsemi.com
CMDSH2-3	200	0.49 @ 200mA	15 @ 10V	

Setting the Output Voltages

The LT3472 has an accurate feedback resistor of 50k for each channel. Only one resistor is needed to set the output voltage for each channel. The output voltage can be set according to the following formulas:

$$V_{POS} = 1.25 \cdot \left(1 + \frac{R1}{50k}\right)$$

$$V_{NEG} = -1.25 \cdot \left(\frac{R2}{50k}\right)$$

In order to maintain accuracy, high precision resistors are preferred (1% is recommended).

Soft-Start

The LT3472 has independent soft-start control for each channel. As shown in Figure 1, the SSP and SSN pins have an internal resistor of 50k pulling up to 1.25V, respectively. By connecting a capacitor from the SSP or SSN pin to ground, the ramp of each output can be programmed individually. If SSP or SSN is open or pull higher than 1.25V, the corresponding output will ramp up quickly. The waveforms with and without soft-start for the Boost channel are shown in Figure 4.

The waveforms with and without soft-start for the negative channel are shown in Figure 5.

Start Sequencing

The LT3472 has internal sequencing circuitry that inhibits the negative channel from operating until feedback voltage of the step-up channel reaches about 1.1V, ensuring that

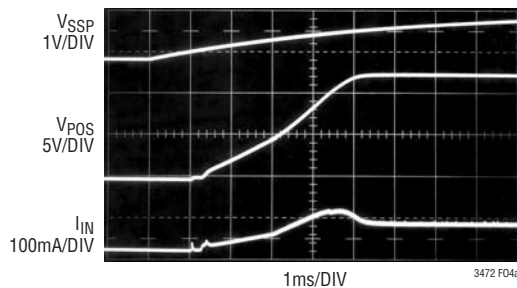


Figure 4a. V_{SSP} , V_{POS} , I_{IN} with 100nF on SSP

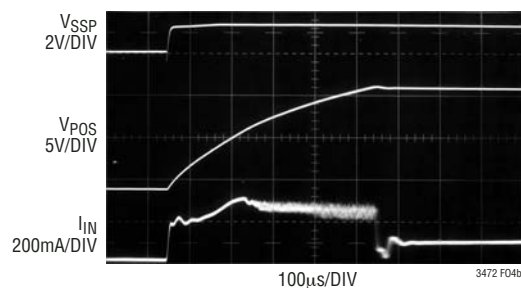


Figure 4b. V_{SSP} , V_{POS} , I_{IN} with SSP Open

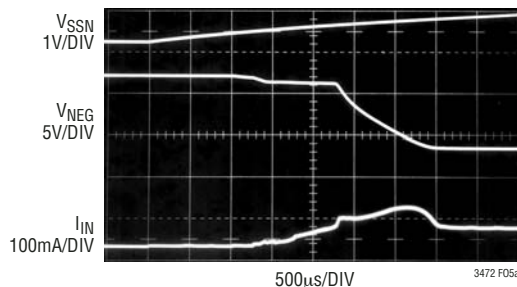


Figure 5a. V_{SSN} , V_{NEG} , I_{IN} with 100nF on SSN

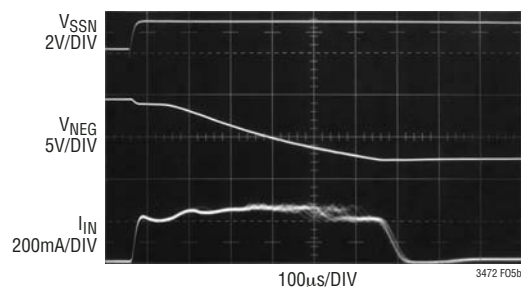


Figure 5b. V_{SSN} , V_{NEG} , I_{IN} with SSN Open

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the sum of the two outputs is always positive. The sequencing is shown in Figure 6.

Board Layout Consideration

As with all switching regulators, careful attention must be paid to the PCB board layout and component placement. To maximize efficiency, switch rise and fall times are made as short as possible. To prevent electromagnetic interfer-

ence (EMI) problems, proper layout of the high frequency switching path is essential. The voltage signals of the SWP and SWN pins have rise and fall times of a few ns. Minimize the length and area of all traces connected to the SWP and SWN pins and always use a ground plane under the switching regulator to minimize interplane coupling. Recommended component placement is shown in Figure 7.

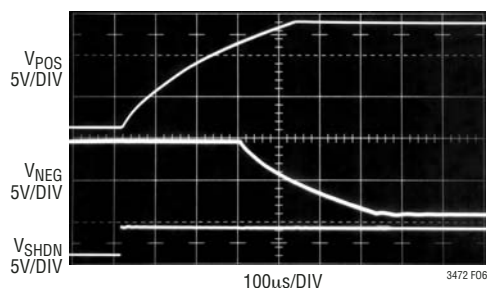


Figure 6. Start-Up Sequencing

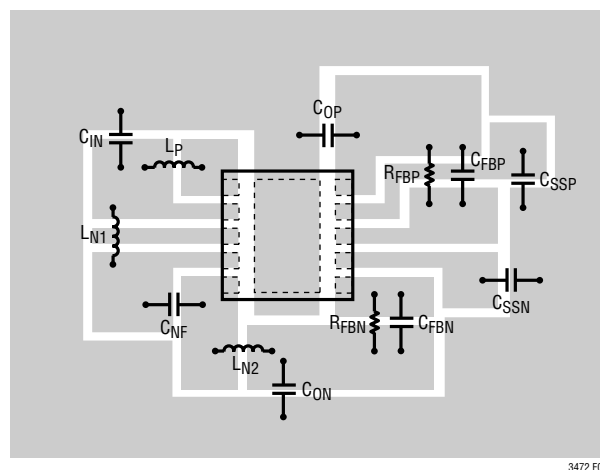
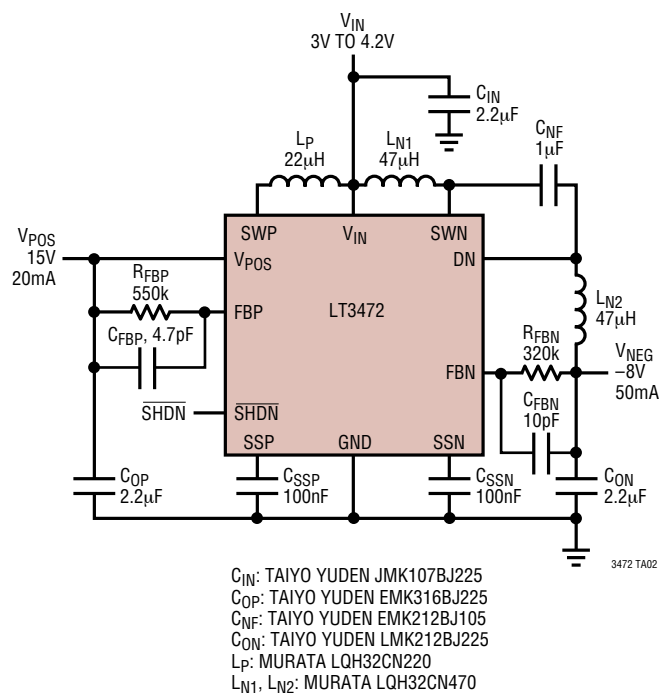
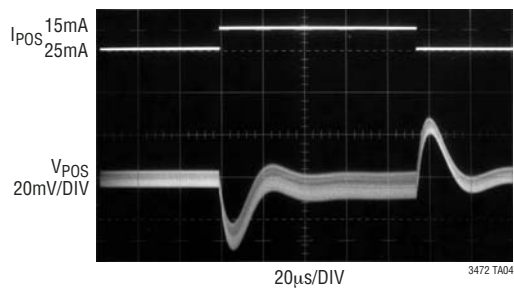


Figure 7. Recommended Component Placement

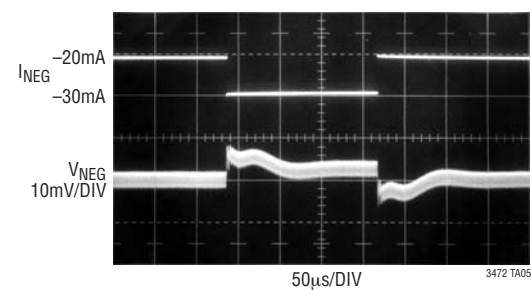
TYPICAL APPLICATIONS



V_{POS} Load Step Response

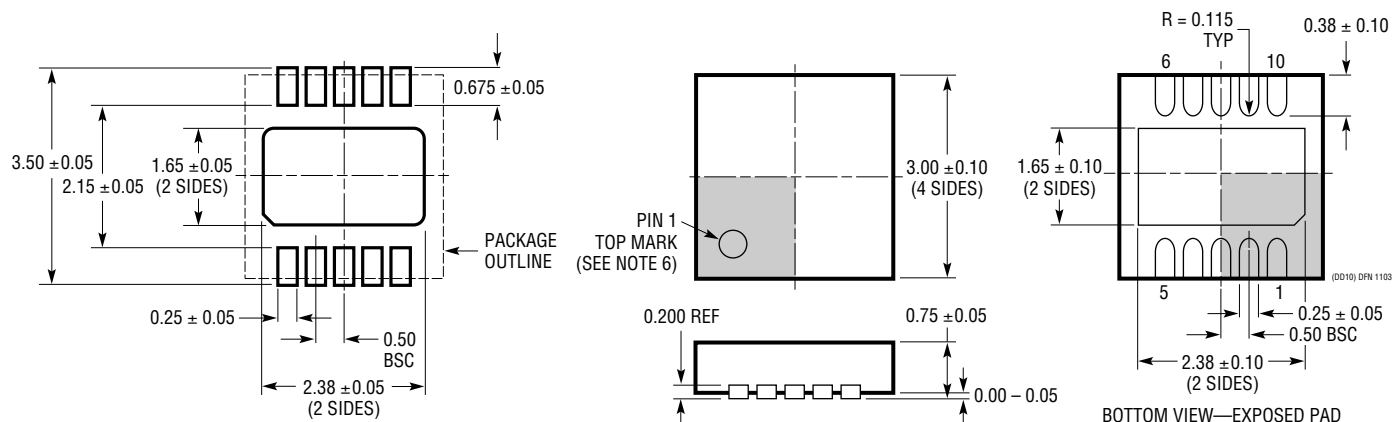


V_{NEG} Load Step Response



PACKAGE DESCRIPTION

DD Package 10-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1699)



NOTE:

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE MO-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

