ABSOLUTE MAXIMUM RATINGS (Note 1)

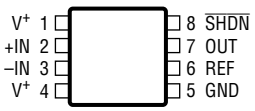
Differential Input Voltage
+IN to –IN (Notes 1, 3) ..... ±60V, 10ms
+IN to GND, –IN to GND (Note 2) ..... –5.25V to 88V
Total Supply Voltage (V^+ to GND) 6V
Input Voltage Pins 6 and 8 ..... V^+ + 0.3V, –0.3V
Output Short-Circuit Duration (Note 4) ..... Indefinite
Operating Ambient Temperature (Note 5)
LT1999C ..... –40°C to 85°C
LT1999I ..... –40°C to 85°C
LT1999H ..... –40°C to 125°C
LT1999MP ..... –55°C to 150°C

Specified Temperature Range (Note 6)
LT1999C ..... 0°C to 70°C
LT1999I ..... –40°C to 85°C
LT1999H ..... –40°C to 125°C
LT1999MP ..... –55°C to 150°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION

ORIGINAL MSOP PINOUT

TOP VIEW

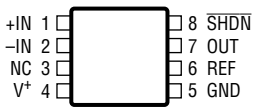


MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 300°C/W

MSOP PINOUT ENGINEERED FOR FMEA

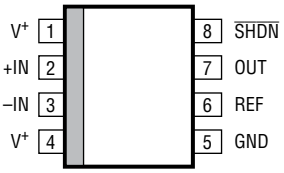
TOP VIEW



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 300°C/W

TOP VIEW



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1999CMS8-10#PBF	LT1999CMS8-10#TRPBF	LTFPB	8-Lead Plastic MSOP	0°C to 70°C
LT1999IMS8-10#PBF	LT1999IMS8-10#TRPBF	LTFPB	8-Lead Plastic MSOP	–40°C to 85°C
LT1999HMS8-10#PBF	LT1999HMS8-10#TRPBF	LTFPB	8-Lead Plastic MSOP	–40°C to 125°C
LT1999MPMS8-10#PBF	LT1999MPMS8-10#TRPBF	LTFQP	8-Lead Plastic MSOP	–55°C to 150°C
LT1999CMS8-10F#PBF	LT1999CMS8-10F#TRPBF	LTGVB	8-Lead MSOP FMEA Pinout	0°C to 70°C
LT1999IMS8-10F#PBF	LT1999IMS8-10F#TRPBF	LTGVB	8-Lead MSOP FMEA Pinout	–40°C to 85°C
LT1999HMS8-10F#PBF	LT1999HMS8-10F#TRPBF	LTGVB	8-Lead MSOP FMEA Pinout	–40°C to 125°C
LT1999MPMS8-10F#PBF	LT1999MPMS8-10F#TRPBF	LTGVB	8-Lead MSOP FMEA Pinout	–55°C to 150°C
LT1999CS8-10#PBF	LT1999CS8-10#TRPBF	199910	8-Lead Plastic SO	0°C to 70°C
LT1999IS8-10#PBF	LT1999IS8-10#TRPBF	199910	8-Lead Plastic SO	–40°C to 85°C
LT1999HS8-10#PBF	LT1999HS8-10#TRPBF	199910	8-Lead Plastic SO	–40°C to 125°C
LT1999MPS8-10#PBF	LT1999MPS8-10#TRPBF	99MP10	8-Lead Plastic SO	–55°C to 150°C
LT1999CMS8-20#PBF	LT1999CMS8-20#TRPBF	LTFNZ	8-Lead Plastic MSOP	0°C to 70°C
LT1999IMS8-20#PBF	LT1999IMS8-20#TRPBF	LTFNZ	8-Lead Plastic MSOP	–40°C to 85°C
LT1999HMS8-20#PBF	LT1999HMS8-20#TRPBF	LTFNZ	8-Lead Plastic MSOP	–40°C to 125°C

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ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1999MPMS8-20#PBF	LT1999MPMS8-20#TRPBF	LTFQQ	8-Lead Plastic MSOP	–55°C to 150°C
LT1999CMS8-20F#PBF	LT1999CMS8-20F#TRPBF	LTGVC	8-Lead MSOP FMEA Pinout	0°C to 70°C
LT1999IMS8-20F#PBF	LT1999IMS8-20F#TRPBF	LTGVC	8-Lead MSOP FMEA Pinout	–40°C to 85°C
LT1999HMS8-20F#PBF	LT1999HMS8-20F#TRPBF	LTGVC	8-Lead MSOP FMEA Pinout	–40°C to 125°C
LT1999MPMS8-20F#PBF	LT1999MPMS8-20F#TRPBF	LTGVC	8-Lead MSOP FMEA Pinout	–55°C to 150°C
LT1999CS8-20#PBF	LT1999CS8-20#TRPBF	199920	8-Lead Plastic SO	0°C to 70°C
LT1999IS8-20#PBF	LT1999IS8-20#TRPBF	199920	8-Lead Plastic SO	–40°C to 85°C
LT1999HS8-20#PBF	LT1999HS8-20#TRPBF	199920	8-Lead Plastic SO	–40°C to 125°C
LT1999MPS8-20#PBF	LT1999MPS8-20#TRPBF	99MP20	8-Lead Plastic SO	–55°C to 150°C
LT1999CMS8-50#PBF	LT1999CMS8-50#TRPBF	LTFPC	8-Lead Plastic MSOP	0°C to 70°C
LT1999IMS8-50#PBF	LT1999IMS8-50#TRPBF	LTFPC	8-Lead Plastic MSOP	–40°C to 85°C
LT1999HMS8-50#PBF	LT1999HMS8-50#TRPBF	LTFPC	8-Lead Plastic MSOP	–40°C to 125°C
LT1999MPMS8-50#PBF	LT1999MPMS8-50#TRPBF	LTFQR	8-Lead Plastic MSOP	–55°C to 150°C
LT1999CMS8-50F#PBF	LT1999CMS8-50F#TRPBF	LTGVD	8-Lead MSOP FMEA Pinout	0°C to 70°C
LT1999IMS8-50F#PBF	LT1999IMS8-50F#TRPBF	LTGVD	8-Lead MSOP FMEA Pinout	–40°C to 85°C
LT1999HMS8-50F#PBF	LT1999HMS8-50F#TRPBF	LTGVD	8-Lead MSOP FMEA Pinout	–40°C to 125°C
LT1999MPMS8-50F#PBF	LT1999MPMS8-50F#TRPBF	LTGVD	8-Lead MSOP FMEA Pinout	–55°C to 150°C
LT1999CS8-50#PBF	LT1999CS8-50#TRPBF	199950	8-Lead Plastic SO	0°C to 70°C
LT1999IS8-50#PBF	LT1999IS8-50#TRPBF	199950	8-Lead Plastic SO	–40°C to 85°C
LT1999HS8-50#PBF	LT1999HS8-50#TRPBF	199950	8-Lead Plastic SO	–40°C to 125°C
LT1999MPS8-50#PBF	LT1999MPS8-50#TRPBF	99MP50	8-Lead Plastic SO	–55°C to 150°C
AUTOMOTIVE PRODUCTS**				
LT1999HMS8-10F#WPBF	LT1999HMS8-10F#WTRPBF	LTGVB	8-Lead MSOP FMEA Pinout	–40°C to 125°C
LT1999HMS8-20F#WPBF	LT1999HMS8-20F#WTRPBF	LTGVC	8-Lead MSOP FMEA Pinout	–40°C to 125°C
LT1999HMS8-50F#WPBF	LT1999HMS8-50F#WTRPBF	LTGVD	8-Lead MSOP FMEA Pinout	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, 0°C < T_A < 70°C for C-grade parts, –40°C < T_A < 85°C for I-grade parts, and –40°C < T_A < 125°C for H-grade parts, otherwise specifications are at T_A = 25°C. V^+ = 5V, GND = 0V, V_{CM} = 12V, V_{REF} = floating, $V_{\overline{SHDN}}$ = floating, unless otherwise specified. See Figure 2.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{SENSE}	Full-Scale Input Sense Voltage (Note 7) $V_{SENSE} = V_{+IN} - V_{–IN}$	LT1999-10 LT1999-20 LT1999-50	● ● ●	–0.35 –0.2 –0.08		0.35 0.2 0.08	V V V
V_{CM}	CM Input Voltage Range		●	–5		80	V
$R_{IN(DIFF)}$	Differential Input Impedance	ΔV_{INDIFF} = ±2V/Gain	●	6.4	8	9.6	kΩ
R_{INCM}	CM Input Impedance	ΔV_{CM} = 5.5V to 80V ΔV_{CM} = –5V to 4.5V	● ●	5 3.6	20 4.8	 6	MΩ kΩ
V_{OSI}	Input Referred Voltage Offset		 ●	–750 –1500	±500	750 1500	µV µV
$\Delta V_{OSI}/\Delta T$	Input Referred Voltage Offset Drift				5		µV/°C
A_V	Gain	LT1999-10 LT1999-20 LT1999-50	● ● ●	9.95 19.9 49.75	10 20 50	10.05 20.1 50.25	V/V V/V V/V
A_V Error	Gain Error	ΔV_{OUT} = ±2V	●	–0.5	±0.2	0.5	%
I_B	Input Bias Current I(+IN) = I(–IN) (Note 8)	V_{CM} > 5.5V V_{CM} = –5V $V_{\overline{SHDN}}$ = 0.5V, 0V < V_{CM} < 80V	● ● ●	100 –2.35	137.5 –1.95 0.001	175 –1.5 2.5	µA mA µA
I_{OS}	Input Offset Current I_{OS} = I(+IN) – I(–IN) (Note 8)	V_{CM} > 5.5V V_{CM} = –5V $V_{\overline{SHDN}}$ = 0.5V, 0V < V_{CM} < 80V	● ● ●	–1 –10 –2.5		1 10 2.5	µA µA µA
PSRR	Supply Rejection Ratio	V^+ = 4.5V to 5.5V	●	68	77		dB
CMRR	Sense Input Common Mode Rejection	V_{CM} = –5V to 80V V_{CM} = –5V to 5.5V V_{CM} = 12V, $7V_{P-P}$, f = 100kHz, V_{CM} = 0V, $7V_{P-P}$, f = 100kHz	● ● ● ●	96 96 75 80	105 120 90 100		dB dB dB dB
e_n	Differential Input Referred Noise Voltage Density	f = 10kHz f = 0.1Hz to 10Hz			97 8		$nV/\sqrt{Hz}$ μV_{P-P}
REF_{RR}	REF Pin Rejection, V^+ = 5.5V ΔV_{REF} = 3.0V ΔV_{REF} = 3.25V ΔV_{REF} = 3.25V	 LT1999-10 LT1999-20 LT1999-50	 ● ● ●	 62 62 62	 70 70 70	 	 dB dB dB
R_{REF}	REF Pin Input Impedance	 $V_{\overline{SHDN}}$ = 0.5V	● ●	60 0.15	80 0.4	100 0.65	kΩ MΩ
V_{REF}	Open Circuit Voltage	 $V_{\overline{SHDN}}$ = 0.5V	● ●	2.45 1	2.5 2.5	2.55 2.75	V V
V_{REFR}	REF Pin Input Range (Note 9)	LT1999-10 LT1999-20 LT1999-50	● ● ●	1.25 1.125 1.125		V^+ – 1.25 V^+ – 1.125 V^+ – 1.125	V V V

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, 0°C < T_A < 70°C for C-grade parts, –40°C < T_A < 85°C for I-grade parts, and –40°C < T_A < 125°C for H-grade parts, otherwise specifications are at T_A = 25°C. V^+ = 5V, GND = 0V, V_{CM} = 12V, V_{REF} = floating, $V_{\overline{SHDN}}$ = floating, unless otherwise specified. See Figure 2.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{\overline{SHDN}}$	Pin Pull-Up Current	V^+ = 5.5V, $V_{\overline{SHDN}}$ = 0V	●	–6	–2		µA
V_{IH}	$\overline{SHDN}$ Pin Input High		●	V^+ – 0.5			V
V_{IL}	$\overline{SHDN}$ Pin Input Low		●			0.5	V
f_{3dB}	Small Signal Bandwidth	LT1999-10 LT1999-20 LT1999-50			2 2 1.2		MHz MHz MHz
SR	Slew Rate				3		V/µs
t_s	Settling Time due to Input Step, ΔV_{OUT} = ±2V	0.5% Settling			2.5		µs
t_r	Common Mode Step Recovery Time ΔV_{CM} = ±50V, 20ns (Note 10)	LT1999-10 LT1999-20 LT1999-50			0.8 1 1.3		µs µs µs
V_S	Supply Voltage (Note 11)		●	4.5	5	5.5	V
I_S	Supply Current	V_{CM} > 5.5V V_{CM} = –5V V^+ = 5.5V, $V_{\overline{SHDN}}$ = 0.5V, V_{CM} > 0V	● ● ●		1.55 5.8 3	1.9 7.1 10	mA mA µA
R_O	Output Impedance	ΔI_O = ±2mA			0.15		Ω
I_{SRC}	Sourcing Output Current	R_{LOAD} = 50Ω to GND	●	6	31	40	mA
I_{SNK}	Sinking Output Current	R_{LOAD} = 50Ω to V^+	●	15	26	40	mA
V_{OUT}	Swing Output High (with Respect to V^+)	R_{LOAD} = 1kΩ to Mid-Supply R_{LOAD} = Open	● ●		125 5	250 125	mV mV
	Swing Output Low (with Respect to $V^–$)	R_{LOAD} = 1kΩ to Mid-Supply R_{LOAD} = Open	● ●		250 150	400 225	mV mV
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0V to 5V			1		µs
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 5V to 0V			1		µs

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, –55°C < T_A < 150°C for MP-grade parts, otherwise specifications are at T_A = 25°C. V^+ = 5V, GND = 0V, V_{CM} = 12V, V_{REF} = floating, $V_{\overline{SHDN}}$ = floating, unless otherwise specified. See Figure 2.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{SENSE}	Full-Scale Input Sense Voltage (Note 7) $V_{SENSE} = V_{+IN} – V_{–IN}$	LT1999-10 LT1999-20 LT1999-50	● ● ●	–0.35 –0.2 –0.08		0.35 0.2 0.08	V V V
V_{CM}	CM Input Voltage Range		●	–5		80	V
$R_{IN(DIFF)}$	Differential Input Impedance	ΔV_{INDIFF} = ±2V/GAIN	●	6.4	8	9.6	kΩ
R_{INCM}	CM Input Impedance	ΔV_{CM} = 5.5V to 80V ΔV_{CM} = –5V to 4.5V	● ●	5 3.6	20 4.8	 6	MΩ kΩ
V_{OSI}	Input Referred Voltage Offset		 ●	–750 –2000	±500	750 2000	µV µV
$\Delta V_{OSI}/\Delta T$	Input Referred Voltage Offset Drift				8		µV/°C
A_V	Gain	LT1999-10 LT1999-20 LT1999-50	● ● ●	9.95 19.9 49.75	10 20 50	10.05 20.1 50.25	V/V V/V V/V
A_V Error	Gain Error	ΔV_{OUT} = ±2V	●	–0.5	±0.2	0.5	%
I_B	Input Bias Current I(+IN) = I(–IN) (Note 8)	V_{CM} > 5.5V V_{CM} = –5V $V_{\overline{SHDN}}$ = 0.5V, 0V < V_{CM} < 80V	● ● ●	100 –2.35	137.5 –1.95 0.001	180 –1.5 10	µA mA µA
I_{OS}	Input Offset Current I_{OS} = I(+IN) – I(–IN) (Note 8)	V_{CM} > 5.5V V_{CM} = –5V $V_{\overline{SHDN}}$ = 0.5V, 0V < V_{CM} < 80V	● ● ●	–1 –10 –10		1 10 10	µA µA µA
PSRR	Supply Rejection Ratio	V^+ = 4.5V to 5.5V	●	68	77		dB
CMRR	Sense Input Common Mode Rejection	V_{CM} = –5V to 80V V_{CM} = –5V to 5.5V V_{CM} = 12V, 7V_{P-P}, f = 100kHz, V_{CM} = 0V, 7V_{P-P}, f = 100kHz	● ● ● ●	96 96 75 80	105 120 90 100		dB dB dB dB
e_n	Differential Input Referred Noise Voltage Density	f= 10kHz f = 0.1Hz to 10Hz			97 8		nV/√Hz μV_{P-P}
REF_{RR}	REF Pin Rejection, V^+ = 5.5V ΔV_{REF} = 2.75V ΔV_{REF} = 3.25V ΔV_{REF} = 3.25V	 LT1999-10 LT1999-20 LT1999-50	 ● ● ●	 62 62 62	 70 70 70	 	 dB dB dB
R_{REF}	REF Pin Input Impedance $V_{\overline{SHDN}}$ = 0.5V		● ●	60 0.15	80 0.4	100 0.65	kΩ MΩ
V_{REF}	Open Circuit Voltage $V_{\overline{SHDN}}$ = 0.5V		● ●	2.45 0.25	2.5 2.5	2.55 2.75	V V
V_{REFR}	REF Pin Input Range (Note 9)	LT1999-10 LT1999-20 LT1999-50	● ● ●	1.5 1.125 1.125		V^+ – 1.25 V^+ – 1.125 V^+ – 1.125	V V V
$I_{\overline{SHDN}}$	Pin Pull-Up Current	V^+ = 5.5V, $V_{\overline{SHDN}}$ = 0V	●	–6	–2		µA
V_{IH}	$\overline{SHDN}$ Pin Input High		●	V^+ – 0.5			V
V_{IL}	$\overline{SHDN}$ Pin Input Low		●			0.5	V
f_{3dB}	Small Signal Bandwidth	LT1999-10 LT1999-20 LT1999-50			2 2 1.2		MHz MHz MHz
SR	Slew Rate				3		V/µs
t_S	Settling Time Due to Input Step, ΔV_{OUT} = ±2V	0.5% Settling			2.5		µs

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, –55°C < T_A < 150°C for MP-grade parts, otherwise specifications are at T_A = 25°C. V^+ = 5V, GND = 0V, V_{CM} = 12V, V_{REF} = floating, $V_{\overline{SHDN}}$ = floating, unless otherwise specified. See Figure 2.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_r	Common Mode Step Recovery Time ΔV_{CM} = ±50V, 20ns (Note 10)	LT1999-10 LT1999-20 LT1999-50			0.8 1 1.3		µs µs µs
V_S	Supply Voltage (Note 11)		●	4.5	5	5.5	V
I_S	Supply Current	V_{CM} > 5.5V V_{CM} = –5V V^+ = 5.5V, $V_{\overline{SHDN}}$ = 0.5V, V_{CM} > 0V	● ● ●		1.55 5.8 3	1.9 7.1 25	mA mA µA
R_O	Output Impedance	ΔI_O = ±2mA			0.15		Ω
I_{SRC}	Sourcing Output Current	R_{LOAD} = 50Ω to GND	●	3	31	40	mA
I_{SNK}	Sinking Output Current	R_{LOAD} = 50Ω to V^+	●	10	26	40	mA
V_{OUT}	Swing Output High (with Respect to V^+)	R_{LOAD} = 1kΩ to Mid-Supply R_{LOAD} = Open	● ●		125 5	250 125	mV mV
	Swing Output Low (with Respect to V^-)	R_{LOAD} = 1kΩ to Mid-Supply R_{LOAD} = Open	● ●		250 150	400 225	mV mV
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0V to 5V			1		µs
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 5V to 0V			1		µs

Note 1: Stresses beyond those listed underAbsolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Pin 2 (+IN) and Pin 3 (–IN) are protected by ESD voltage clamps which have asymmetric bidirectional breakdown characteristics with respect to the GND pin (Pin 5). These pins can safely support common mode voltages which vary from –5.25V to 88V without triggering an ESD clamp.

Note 3: Exposure to differential sense voltages exceeding the normal operating range for extended periods of time may degrade part performance. A heat sink may be required to keep the junction temperature below the Absolute Maximum Rating when the inputs are stressed differentially. The amount of power dissipated in the LT1999 due to input overdrive can be approximated by:

$$P_{DISS} = \frac{(V_{+IN} - V_{-IN})^2}{8k\Omega}$$

Note 4: A heat sink may be required to keep the junction temperature below the absolute maximum rating.

Note 5: The LT1999C/LT1999I are guaranteed functional over the operating temperature range –40°C to 85°C. The LT1999H is guaranteed functional over the operating temperature range –40°C to 125°C. The LT1999MP is guaranteed functional over the operating temperature range –55°C to 150°C. Junction temperatures greater than 125°C will promote accelerated aging. The LT1999 has a demonstrated typical life beyond 1000 hours at 150°C.

Note 6: The LT1999C is guaranteed to meet specified performance from 0°C to 70°C. The LT1999C is designed, characterized, and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LT1999I is guaranteed to meet specified performance from –40°C to 85°C. The LT1999H is guaranteed to meet specified performance from –40°C to 125°C. The LT1999MP is guaranteed to meet specified performance from –55°C to 150°C.

Note 7: Full-scale sense (V_{SENSE}) gives indication of the maximum differential input that can be applied with better than 0.5% gain accuracy. Gain accuracy is degraded when the output saturates against either power supply rail. V_{SENSE} is verified with V^+ = 5.5V, V_{CM} = 12V, with the REF pin set to it's voltage range limits. The maximum V_{SENSE} is verified with the REF pin set to it's minimum specified limit, verifying the gain error is less than 0.5% at the output. The minimum V_{SENSE} is verified with the REF pin set to its maximum specified limit, verifying the gain error at the output is less than 0.5%. See Note 9 for more information.

Note 8: I_B is defined as the average of the input bias currents to the +IN and –IN pins (Pins 2 and 3). A positive current indicates current flowing into the pin. I_{OS} is defined as the difference of the input bias currents. I_{OS} = I(+IN) – I(–IN)

Note 9: The REF pin voltage range is the minimum and maximum limits that ensures the input referred voltage offset does not exceed ±3mV over the I, C, and H temperature ranges, and ±3.5mV over the MP temperature range.

Note 10: Common mode recovery time is defined as the time it takes the output of the LT1999 to recover from a 50V, 20ns input common mode voltage transition, and settle to within the DC amplifier specifications.

Note 11: Operating the LT1999 with V^+ < 4.5V is possible, although the LT1999 is not tested or specified in this condition. See the Applications Information section.

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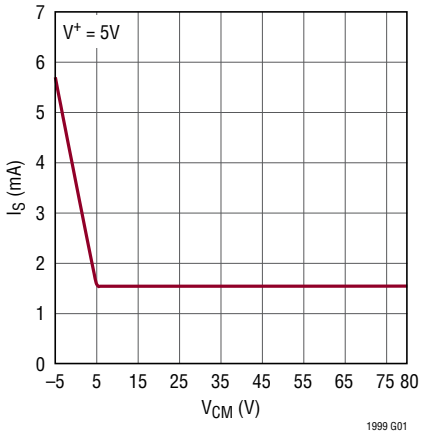
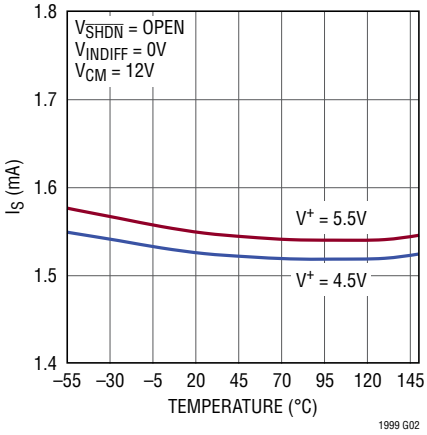
TYPICAL PERFORMANCE CHARACTERISTICS

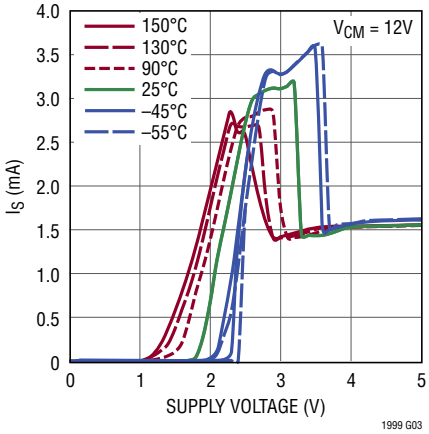
Supply Current vs Input Common Mode



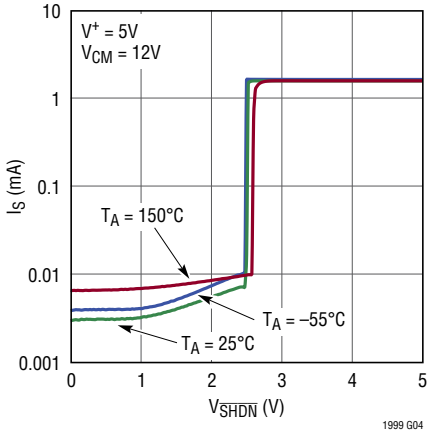
Supply Current vs Temperature



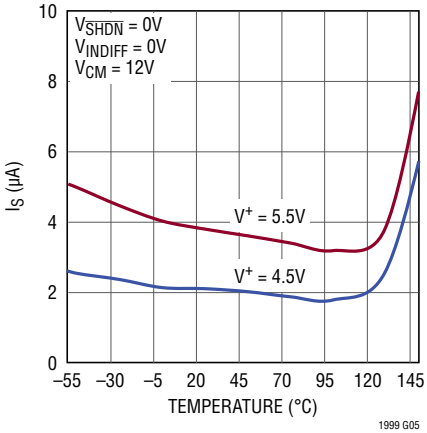
Supply Current vs Supply Voltage



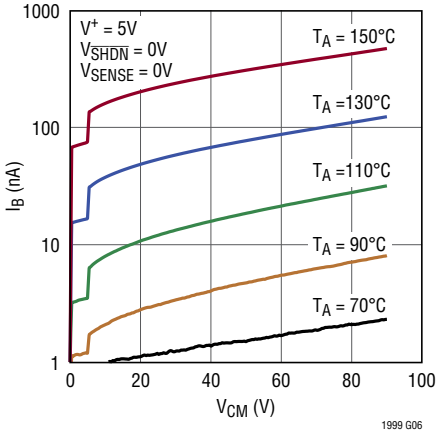
Supply Current vs SHDN Pin Voltage



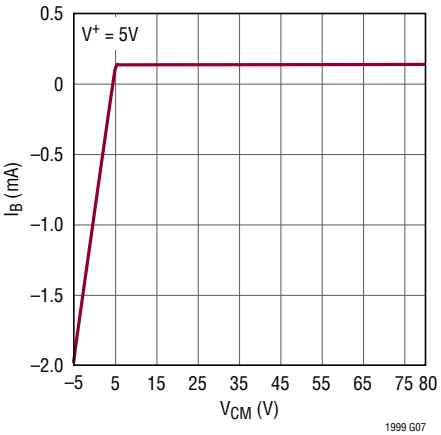
Shutdown Supply Current vs Temperature



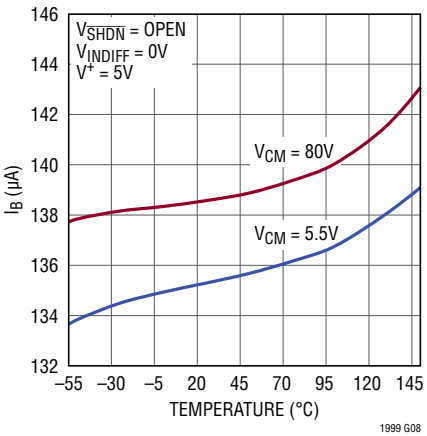
Shutdown Input Bias Current vs Input Common Mode



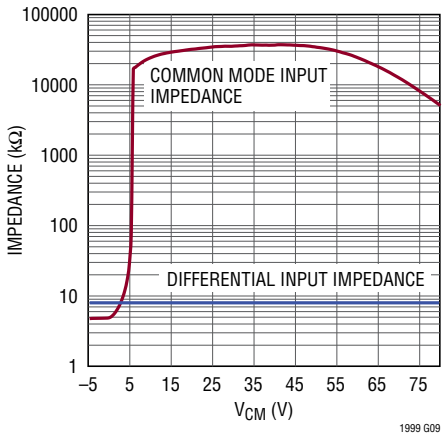
Input Bias Current vs Input Common Mode



Input Bias Current vs Temperature



Input Impedance vs Input Common Mode Voltage



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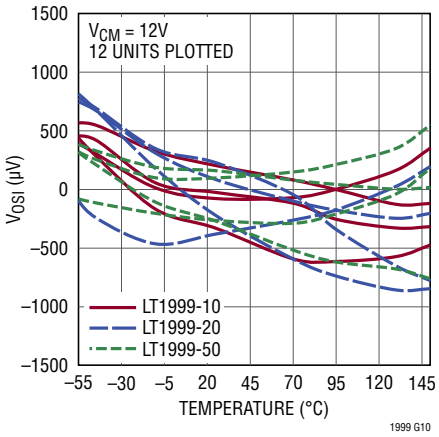
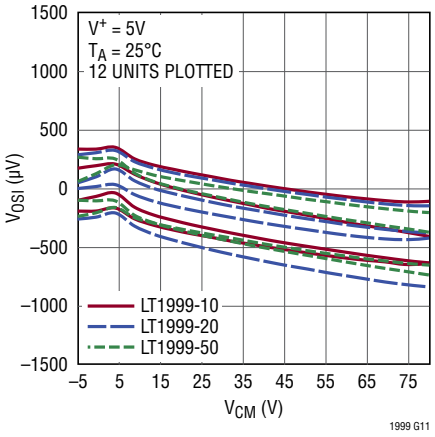
TYPICAL PERFORMANCE CHARACTERISTICS

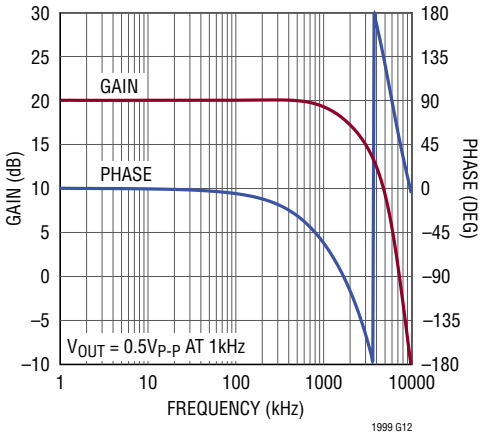
Input Referred Voltage Offset vs Temperature and Gain Option



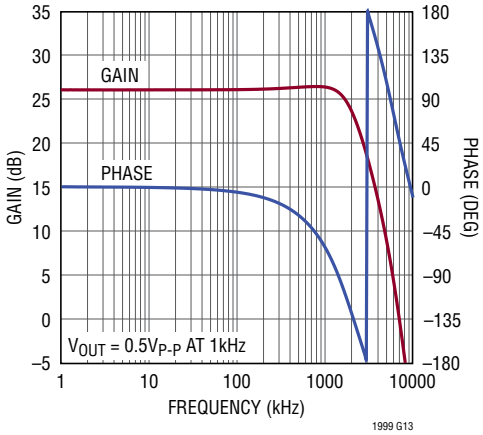
Input Referred Voltage Offset vs Input Common Mode Voltage



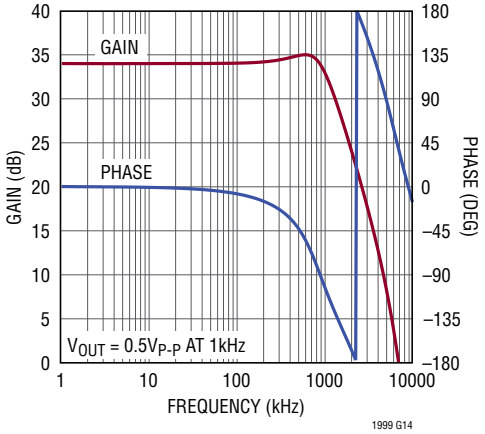
LT1999-10 Small Signal Frequency Response



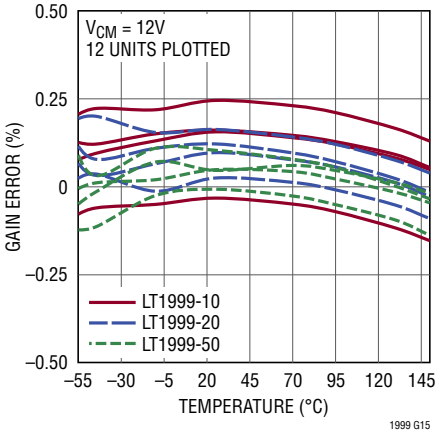
LT1999-20 Small Signal Frequency Response



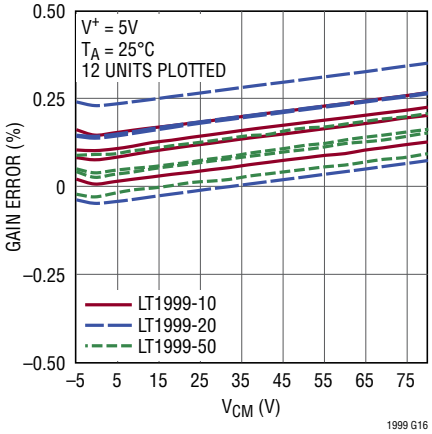
LT1999-50 Small Signal Frequency Response



Gain Error vs Temperature



Gain Error vs Input Common Mode Voltage



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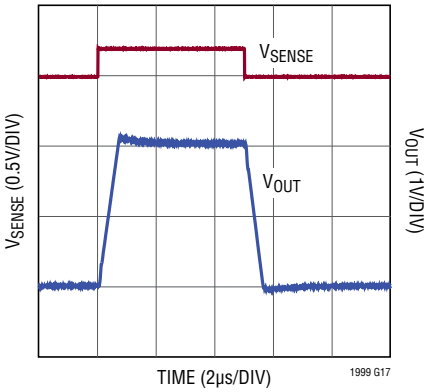
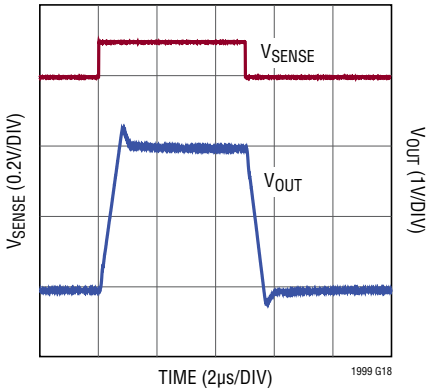
TYPICAL PERFORMANCE CHARACTERISTICS

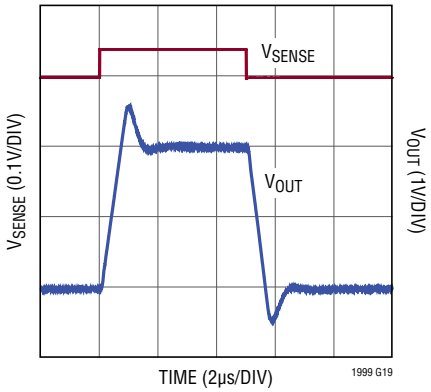
LT1999-10 Pulse Response



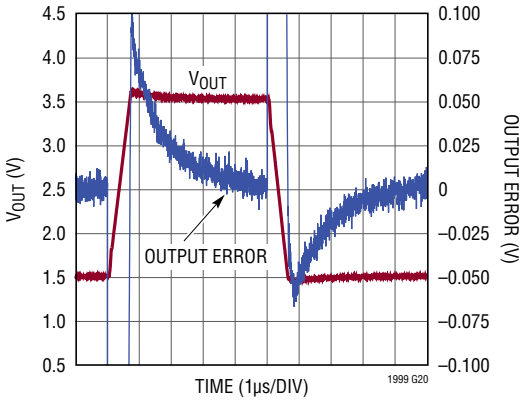
LT1999-20 Pulse Response



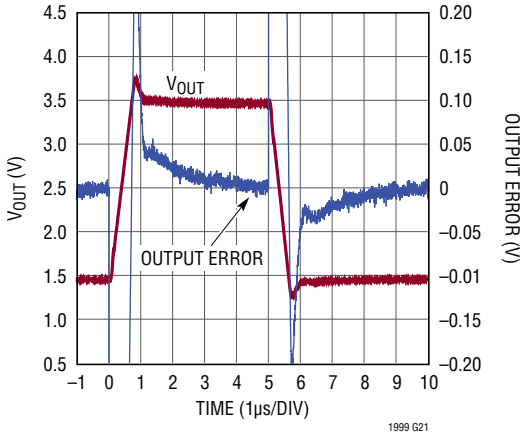
LT1999-50 Pulse Response



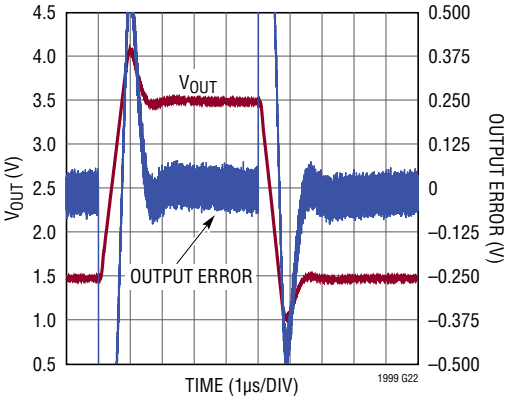
LT1999-10 2V Step Response Settling Time



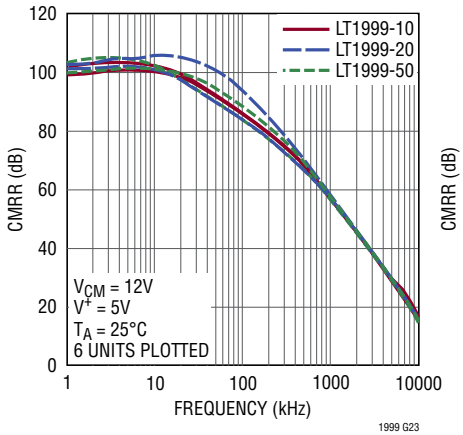
LT1999-20 2V Step Response Settling Time



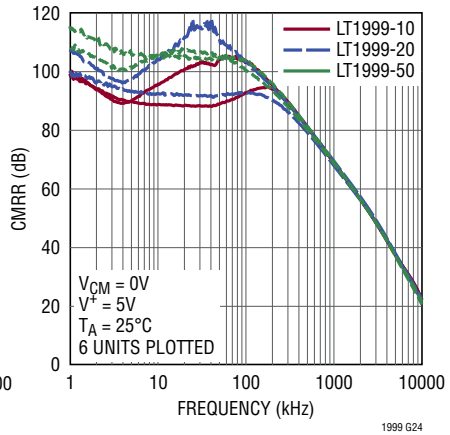
LT1999-50 2V Step Response Settling Time



CMRR vs Frequency



CMRR vs Frequency



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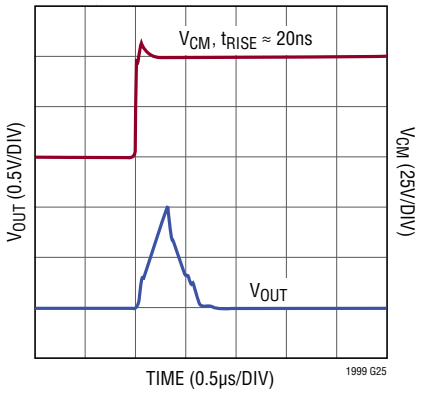
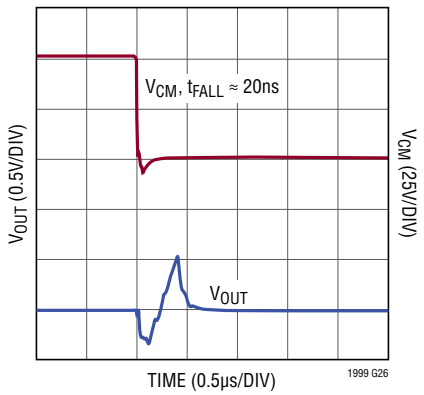
TYPICAL PERFORMANCE CHARACTERISTICS

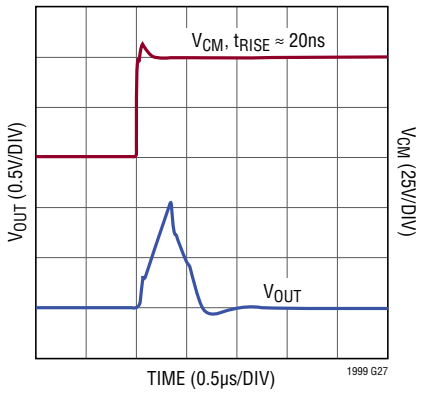
LT1999-10 Common Mode Rising Edge Step Response



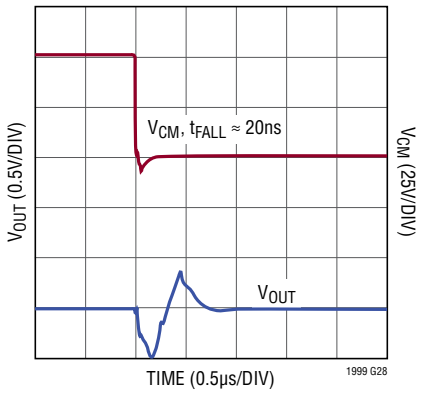
LT1999-10 Common Mode Falling Edge Step Response



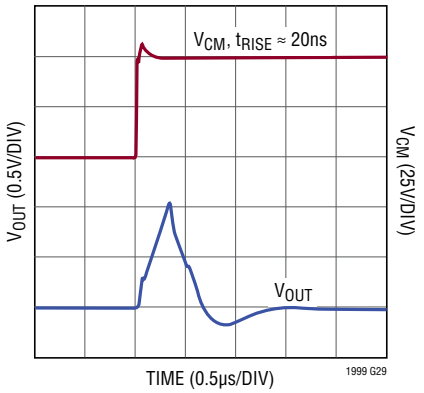
LT1999-20 Common Mode Rising Edge Step Response



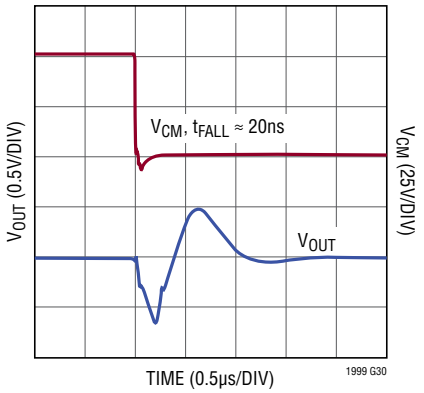
LT1999-20 Common Mode Falling Edge Step Response



LT1999-50 Common Mode Rising Edge Step Response



LT1999-50 Common Mode Falling Edge Step Response



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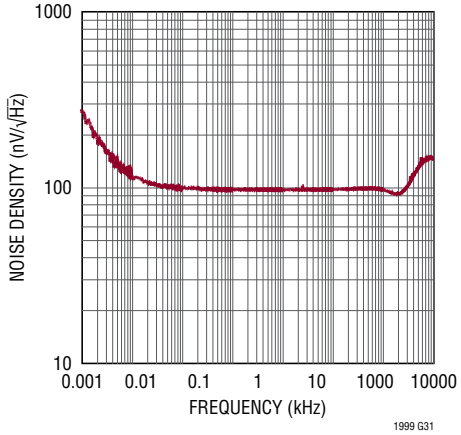
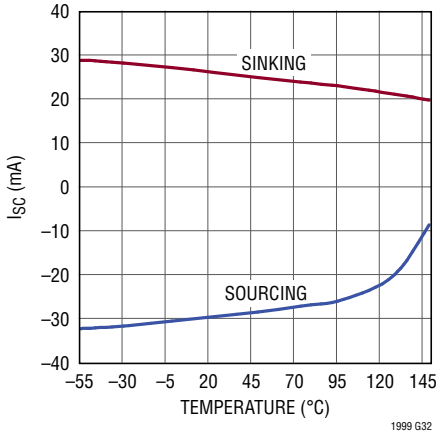
TYPICAL PERFORMANCE CHARACTERISTICS

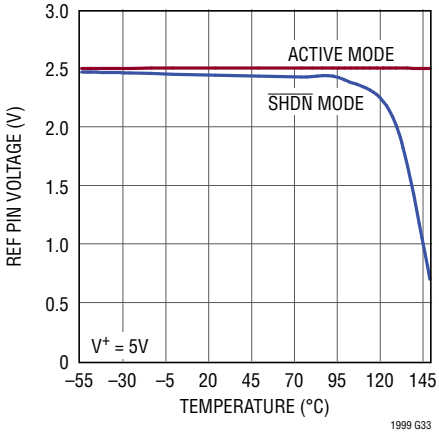
LT1999 Input Referred Noise Density vs Frequency



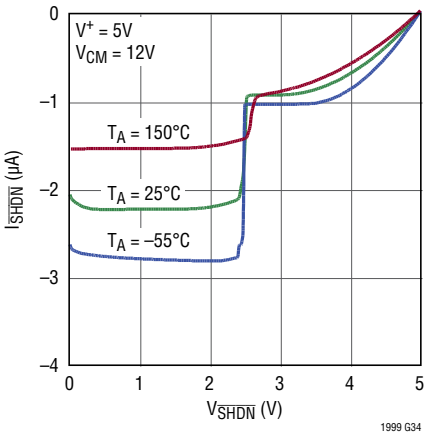
Short-Circuit Current vs Temperature



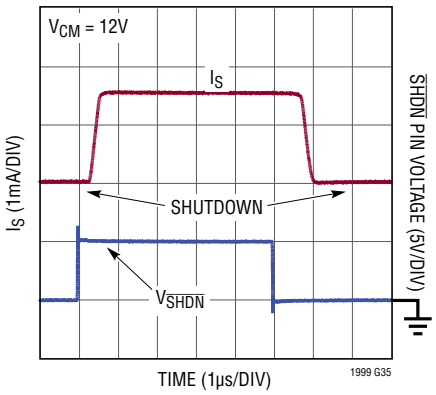
REF Open Circuit Voltage vs Temperature



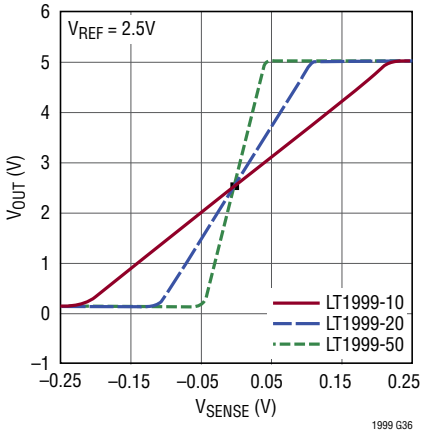
SHDN Pin Current vs SHDN Pin Voltage and Temperature



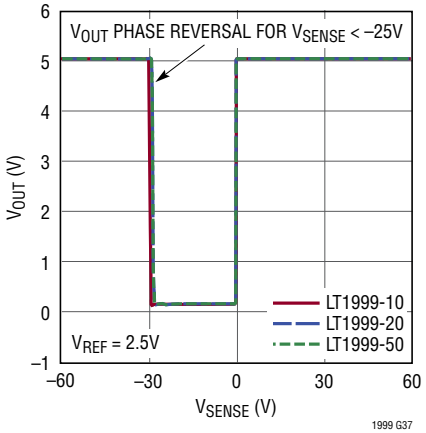
Turn-On/Turn-Off Time vs SHDN Voltage



VOUT vs VSENSE



VOUT vs VSENSE Over the Sense ABSMAX Range



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PIN FUNCTIONS (LT1999-XX/LT1999-XXF)

V^+ (Pins 1, 4/Pin 4): Power Supply Voltage. Pins 1 and 4 are tied internally together. The specified range of operation is 4.5V to 5.5V, but lower supply voltages (down to approximately 4V) is possible although the LT1999 is not tested or characterized below 4.5V. See the Applications Information section.

+IN (Pin 2/Pin 1): Positive Sense Input Pin.

–IN (Pin 3/Pin 2): Negative Sense Input Pin.

NC (NA/Pin 3)

GND (Pin 5/Pin 5): Ground Pin.

REF (Pin 6/Pin 6): Reference Pin Input. The REF pin sets the output common mode level and is set halfway between V^+ and GND using a divider made of two 160k resistors. The default open circuit potential of the REF pin is mid-supply. It can be overdriven by an external voltage source cable of driving 80k to a mid-supply potential (see the Electrical Characteristics table for its specified input voltage range).

OUT (Pin 7/Pin 7): Voltage Output. $V_{OUT} = A_V \bullet (V_{SENSE} \pm V_{OSI})$, where A_V is the gain, and V_{OSI} is the input referred offset voltage. The output amplifier has a low impedance output and is designed to drive up to 200pF capacitive loads directly. Capacitive loads exceeding 200pF should be decoupled with an external resistor of at least 100Ω.

$\overline{\text{SHDN}}$ (Pin 8/Pin 8): Shutdown Pin. When pulled to within 0.5V of GND (Pin 5), will place the LT1999 into low power shutdown. If the pin is left floating, an internal 2µA pull-up current source will place the LT1999 into the active (amplifying) state.

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BLOCK DIAGRAM

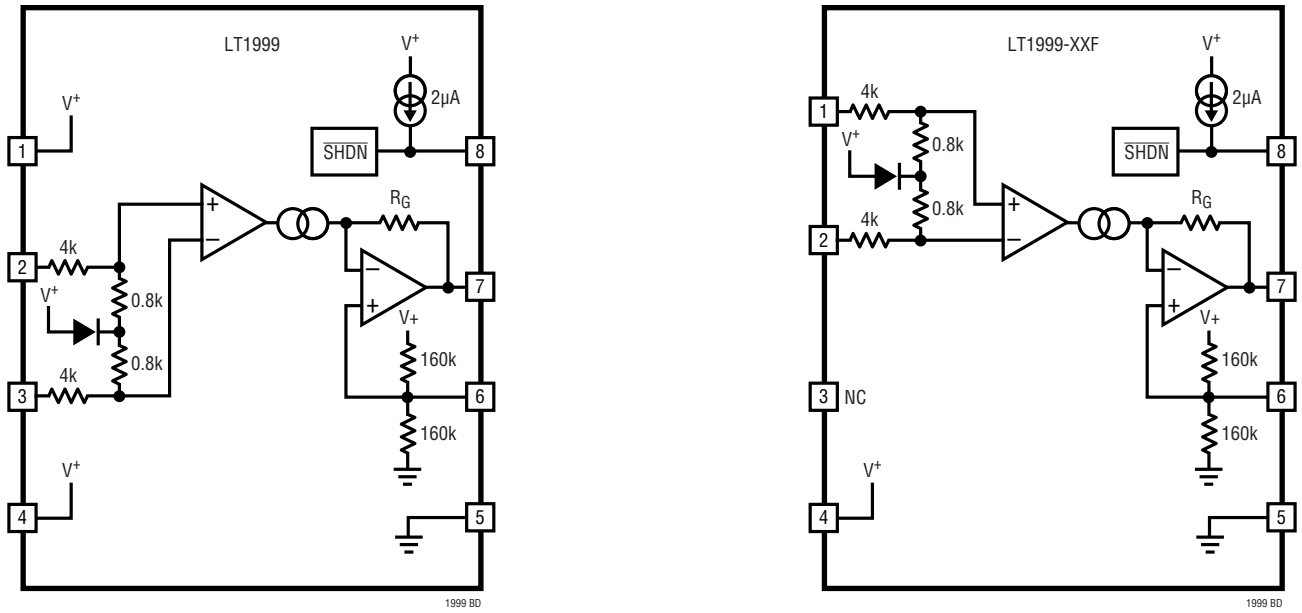

Figure 1. Simplified Block Diagram

TEST CIRCUIT

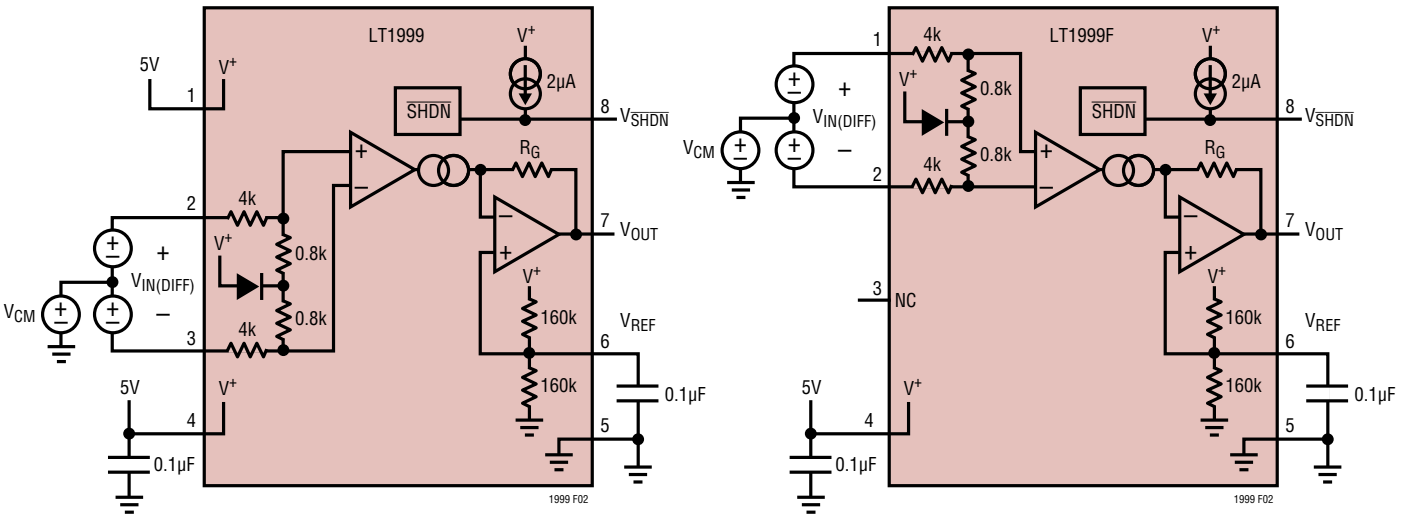

Figure 2. Test Circuit

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APPLICATIONS INFORMATION

The LT1999 current sense amplifier provides accurate bidirectional monitoring of current through a user-selected sense resistor. The voltage generated by the current flowing in the sense resistor is amplified by a fixed gain of 10V/V, 20V/V or 50V/V (LT1999-10, LT1999-20, or LT1999-50 respectively) and is level shifted to the OUT pin. The voltage difference and polarity of the OUT pin with respect to REF (Pin 6) indicates magnitude and direction of the current in the sense resistor.

THEORY OF OPERATION

Refer to the Block Diagram (Figure 1.

Case 1: $V^+ < V_{CM} < 80V$

For input common mode voltages exceeding the power supply, one can assume D1 ofFigure 1 is completely off. The sensed voltage (V_{SENSE}) is applied across Pin 2 (+IN) and Pin 3 (–IN) to matched resistors R_{+IN} and $R_{–IN}$ (nominally 4k each). The opposite ends of R_{+IN} and $R_{–IN}$ are forced to equal potentials by transconductor G_{IN}, which convert the differentially sensed voltage into a sensed current. The sensed current in R_{+IN} and $R_{–IN}$ is combined, level-shifted, and converted back into a voltage by trans-resistance amplifier A_O and resistor R_G. Amplifier A_O provides high open loop gain to accurately convert the sensed current back into a voltage and to drive external loads. The theoretical output voltage is determined by the sensed voltage (V_{SENSE}), and the ratio of two on-chip resistors:

$$V_{OUT} - V_{REF} = V_{SENSE} \bullet \frac{R_G}{R_{IN}}$$

where

$$R_{IN} = \frac{R_{+IN} + R_{–IN}}{2} \quad \text{nominally 4k}$$

For the LT1999-10, R_G is nominally 40k. For the LT1999-20, R_G is nominally 80k, and for the LT1999-50, R_G is nominally 200k.

The voltage difference between the OUT pin and the REF pin represent both polarity and magnitude of the sensed voltage. The noninverting input of amplifier A_O is biased by a resistive 160k to 160k divider tied between V^+ and GND to set the default REF pin bias to mid-supply.

Case 2: $–5V < V_{CM} < V^+$

For common mode inputs which transition or are set below the supply voltage, diode D1 will turn on and will provide a source of current through R_{+S} and $R_{–S}$ to bias the inputs of transconductance amplifier G_{IN} at least 2.25V above GND. The transition is smooth and continuous; there are negligible changes to either gain or amplifier voltage offset. The only difference in amplifier operation is the bias currents provided by D1 through R_{+S} and $R_{–S}$ are steered through the input pins, otherwise amplifier operation is identical. The inputs to transconductance amplifier G_{IN} are still forced to equal potentials forcing any differential voltages appearing at the +IN and –IN pins into a differential current. This differential current is combined, level-shifted, and converted back into a voltage by trans-resistance amplifier A_O and Resistor R_G. Resistors R_{+S} and $R_{–S}$ are trimmed to match R_{+IN} and $R_{–IN}$ respectively, to prevent common mode to differential conversion from occurring (to the extent of the matched trim) when the input common mode transitions below V^+.

As described in case 1, the output is determined by the sense voltage and the ratio of two on-chip resistors:

$$V_{OUT} - V_{REF} = V_{SENSE} \bullet \frac{R_G}{R_{IN}}$$

where

$$R_{IN} = \frac{R_{+IN} + R_{–IN}}{2}$$

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APPLICATIONS INFORMATION

Input Common Mode Range

The LT1999 was optimized for high common mode rejection. Its input stage is balanced and fully differential, designed to amplify differential signals and reject common mode signals. There is negligible crossover distortion due to sense voltage reversals. The amplifier is most linear in the zero-sense region.

With the V^+ supply configured within the specified and tested range ($4.5V < V^+ < 5.5V$), the LT1999's common mode range extends from –5V to 80V. Pushing +IN and –IN beyond the limits specified in the Absolute Maximum table can turn on the voltage clamps designed to protect the +IN and –IN pins during ESD events.

It is possible to operate the LT1999 on power supplies as low as 4V (although it is not tested or specified below 4.5V). Operating the LT1999 on supplies below 4V will produce erratic behavior. When operating the LT1999 with supplies as low as 4V, the common mode range for inputs which extend below GND is reduced. Refer to the Block Diagram (Figure 1). For inputs driven below V^+, diode D1 conducts. For proper operation, the input to the transconductor $V(G_{+IN})$ must be biased at approximately 2.25V above the GND pin. $V(G_{+IN})$ sits on the centertap of a voltage divider comprised of R_{+S} and R_{+IN} $V(G_{-IN})$ likewise sits in the middle of the voltage divider comprised of R_{-S} , and R_{-IN}). The voltage on $V(G_{+IN})$ input is given by the following equation:

$$V(G_{+IN}) = V_{+IN} \bullet \frac{R_{+S}}{R_{+S} + R_{+IN}} + \left(V^+ - V_{D1}\right) \bullet \frac{R_{+IN}}{R_{+S} + R_{+IN}}$$

Setting $V(G_{+IN})$ = 2.25V, the ratio (R_{+IN}/R_{+S}) to 5, and V_{D1} equal to 0.8V (cold temperatures), a plot of the lower input common mode range plotted against supply is shown in Figure 3.

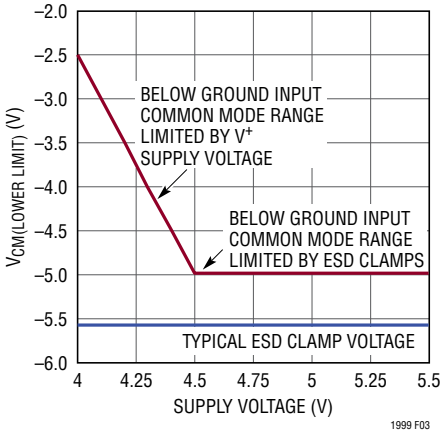

Figure 3. Lower Input Common Mode vs Supply Voltage

Output Common Mode Range

The LT1999's output common mode level is set by the voltage on the REF pin. The REF pin sits in the middle of a 160k to 160k voltage divider connected between V^+ and GND which sets the default open circuit potential of the REF pin to mid-supply. It can be overdriven by an external voltage source capable of driving 80k tied to a mid-supply potential. See the Electrical Characteristics table for the REF pin's specified input voltage range.

Differential sampling of the OUT pin with respect the REF pin provides the best noise immunity. Measurements of the output voltage made differentially with respect to the REF pin will provide the highest power supply and common mode rejection. Otherwise, power supply or GND pin disturbances are divided by the REF pin's voltage divider and appear directly at the noninverting input of the trans-resistance amplifier A_0 and are not rejected.

If not driven by a low impedance (<100Ω), the REF pin should be filtered with at least 1nF of capacitance to a low impedance, low noise ground plane. This external capacitance will also provide a charge reservoir during high frequency sampling of the REF pin by ADC inputs attached to this pin.

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APPLICATIONS INFORMATION

Shutdown Capability

If $\overline{SHDN}$ (Pin 8) is driven to within 0.5V of GND, the LT1999 is placed into a low power shutdown state in which the part will draw about 3µA from the V^+ supply. The input pins (+IN and –IN) will draw approximately 1nA if biased within the range of 0V to 80V (with no differential voltage applied). If the input pins are pulled below the GND pin, each input appears as a diode tied to GND in series with approximately 4k of resistance. The REF pin appears as approximately 0.4MΩ tied to a mid-supply potential. The output appears as reverse biased diodes tied between the output to either V^+ or GND pins.

EMI Filtering and Layout Practices

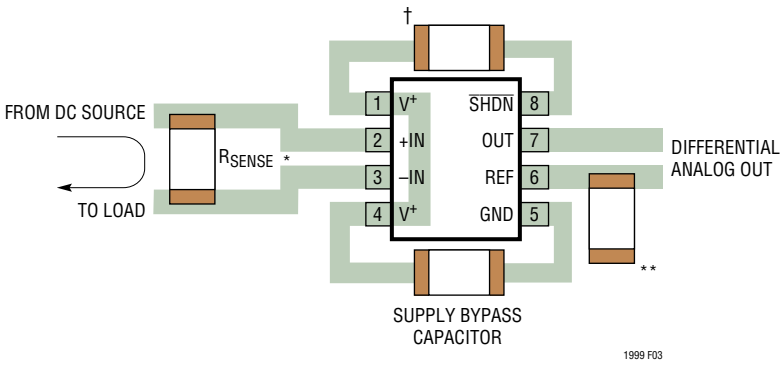
An internal 1st order differential lowpass noise/EMI suppression filter with a –3dB bandwidth of 10MHz (approximately 5× the LT1999's –3dB bandwidth) is included to help improve the LT1999's EMI susceptibility and to assist with the rejection of high frequency signals beyond the bandwidth of the LT1999 that may introduce errors. The pole is set by the following equation:

$$f_{filt} = 1/(\pi \bullet (R_{+IN} + R_{-IN}) \bullet C_F) \approx 10MHz$$

Both the resistors and capacitors have a ±15% variation so the pole can vary by approximately ±30% over manufacturing process and temperature variations.

The layout for lowest EMI/noise susceptibility is achieved by keeping short direct connections and minimizing loop areas (see Figure 4). If the user-supplied sense resistor cannot be placed in close proximity to the LT1999, the surface area of the loop comprising connections of +IN to R_{SENSE} and back to –IN should be minimized. This requires routing PCB traces connecting +IN to R_{SENSE} and –IN to R_{SENSE} adjacent with one another with minimal separation. The metal traces connecting +IN to the sense resistor and –IN to the sense resistor should match and use the same trace width.

Bypassing the V^+ pin to the GND pin with a 0.1µF capacitor with short wiring connection is recommended.



* KEEP LOOP AREA COMPRISING R_{SENSE}, +IN AND –IN PINS AS SMALL AS POSSIBLE.
** REF BYPASS TIED TO A LOW NOISE, LOW IMPEDANCE SIGNAL GROUND PLANE.
† OPTIONAL 10pF CAPACITOR TO PREVENT dV/dt EDGES ON INPUT COUPLING TO FLOATING $\overline{SHDN}$ PIN.

Figure 4. Recommended Layout

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APPLICATIONS INFORMATION

The REF pin should be either driven by a low source impedance (<100Ω) or should be bypassed with at least 1nF to a low impedance, low noise, signal ground plane (see Figure 4). Larger bypass capacitors on both V^+ pins, and the REF pin, will extend enhanced AC CMRR, and PSRR performance to lower frequencies. Bypassing the REF pin to a quiet ground plane filters the V^+ pin or GND pin noise that is sensed by the REF pin voltage divider and applied to the noninverting input of output amplifier A_O. Any common I•R drops generated by pulsating ground currents in common with the REF pin filter capacitor can compromise the filtering performance and should be avoided.

If the $\overline{SHDN}$ pin is not driven and is left floating, routing a PCB trace connecting Pins 1 and 8 under the part will act as a shield, and will help limit edge coupling from the inputs (Pins 2 and 3) to the $\overline{SHDN}$ pin. Periodic pulses on the inputs with fast edges may glitch the high impedance $\overline{SHDN}$ pin, periodically putting the part into low power shutdown. Additional precaution against this may be taken by adding an optional small (~10pF) capacitor may be tied between V^+ (Pin 1) and Pin 8.

Finally, when connecting the LT1999 inputs to the sense resistor, it is important to use good Kelvin sensing practices (sensing the resistor in a way that excludes PCB trace I•R voltage drops). For sense resistors less than 1Ω, one might consider using a 4-wire sense resistor to sense the resistive element accurately.

Selection of the Current Sense Resistor

The external sense resistor selection presents a delicate trade-off between power dissipation in the resistor and current measurement accuracy.

In high current applications, the user may want to minimize the power dissipated in the sense resistor. The sense resistor current will create heat and voltage loss, degrading efficiency. As a result, the sense resistor should be as small as possible while still providing adequate dynamic range required by the measurement. The dynamic range is the ratio between the maximum accurately produced signal generated by the voltage across the sense resistor, and the minimum accurately reproduced signal. The minimum accurately reproduced signal is primarily dictated by the voltage offset of the LT1999. The maximum accurately reproduced signal is dictated by the output swing of the LT1999.

Thus the dynamic range for the LT1999 can be thought of the maximum sense voltage divided by the input referred voltage offset or:

$$\text{Dynamic Range} = \frac{\Delta V_{OUT(MAX)}}{GAIN \bullet V_{OSI}}$$

The above equation tells us that the dynamic range is inversely proportional to the gain of the LT1999. Thus, if accuracy is of greater importance than efficiency or power loss, the LT1999-10 used with the highest valued sense resistor possible is recommended. If efficiency, heat generated, and power loss in the resistive shunt is the primary concern, the LT1999-50 and the lowest value sense resistor possible is recommended. The LT1999-20 is available for applications somewhere in between these two extremes.

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APPLICATIONS INFORMATION

Pinout Option Engineered for FMEA (Failure Mode and Effects Analysis)

The LT1999 family of ICs is available with an 8-lead MSOP pinout option engineered for FMEA (Failure Mode and Effects Analysis): (LT1999-10F, LT1999-20F and the LT1999-50F). See Figure 5 below.

The LT1999-XXF is designed to meet the most stringent automotive requirements and to satisfactorily survive single faults due to the most common PCB defects: 1) open pins due to cold solder joints and 2) adjacent pin short circuits due to adjacent pin solder bridging. The No-Connect Pin (Pin 3) has been inserted between the input pin (–IN) and the V^+ supply pin to isolate the input voltages which may range from –5V to 80V from solder bridging to the V^+ supply (typically 5V). Pin 3 is not connected internally to the die and should be left unconnected.

The purpose of the FMEA is to emulate single faults and determine whether or not they are destructive and/or lead to conditions which could damage surrounding components. The LT1999-XXF is configured as shown in Figure 2, with an input common mode of either 12V or 0V. Each pin is systematically shorted to its adjacent pin (emulating solder bridging) and the resulting effects recorded. Each pin is then opened (emulating a cold solder joint) with the resulting effects recorded.

In all instances, the LT1999-XXF recovers when these fault conditions are removed. Furthermore, the output pin (OUT) has been verified to never exceed the pin's nominal output range of 0V to 5V during fault testing.

Table 1 lists the behavior which results from shorting adjacent pins and Table 2 details the behavior from opening any pin.

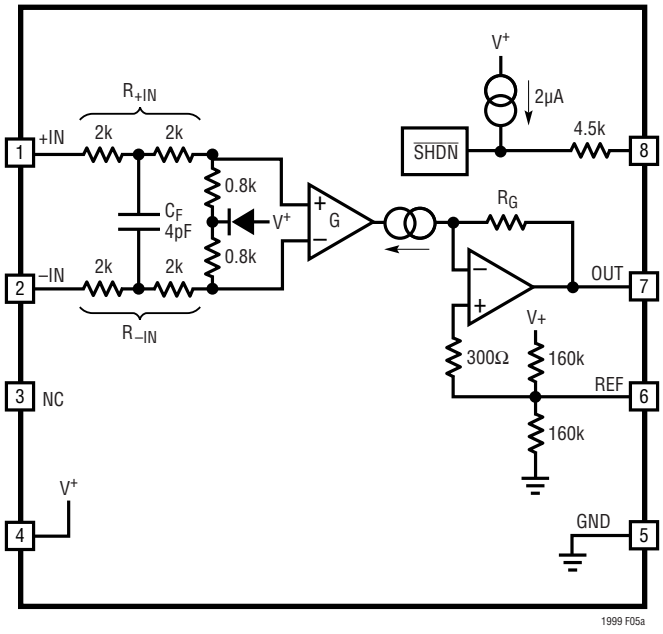

Figure 5. Simplified Block Diagram of the LT1999-XXF

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APPLICATIONS INFORMATION

Table 1. Behavior due to Adjacent Pin-to-Pin Shorts for the LT1999-10F, LT1999-20F, or the LT1999-50F

Adjacent Pin Short Test: (V^+ = 5V, Tested at V_{CM} = 0V, V_{CM} = 12V, V_{CM} = 80V)			
PIN #	**Adjacent Pins Shorted**	**Recovery when Fault is removed**	**BEHAVIOR**
1 – 2	+IN – –IN	YES	V_{OUT} approaches the voltage on pin V_{REF}.
2 – 3	–IN – NC	YES	The circuit behaves normally.
3 – 4	NC – V+	YES	The circuit behaves normally.
5 – 6	GND – REF	YES	V_{OUT} follows the voltage on Pin 6 or 0V.
6 – 7	REF – OUT	YES	V_{OUT} approaches 5.0V
7 – 8	OUT – $\overline{SHDN}$	YES	Supply Current drops by 5%.

Table 2. Behavior due to open pins for the LT1999-10F, LT1999-20F, or the LT1999-50F

Open Pin Test (V^+ = 5V, Tested at V_{CM} = 0V, V_{CM} = 12V, V_{CM} = 80V)			
PIN #	**Pin Opened**	**Recovery when Fault is removed**	**BEHAVIOR**
1	+IN	YES	V_{OUT} may go to either V^+ or GND, depending on the voltage applied to –IN. Generally, for –5V< –IN< 4V, OUT will be near 5V. For –IN > 5V, OUT will be near 0V. In the range of 4V < –IN < 5V, OUT may go to either V^+ or GND, depending on the voltage applied to –IN. The open input (+IN) is biased internal to the IC to one diode below V^+.
2	–IN	YES	V_{OUT} may go to either V^+ or GND, depending on the voltage applied to +IN. Generally, for –5V < +IN < 4V, OUT will be near 0V. For +IN > 5V, OUT will be at 5V. In the range of 4V < –IN < 5V, OUT may go to either V+ or GND, depending on the voltage applied to +IN. The open input (–IN) is biased internal to the IC to one diode below V^+.
3	NC	YES	The circuit behaves normally.
4	V^+	YES	The circuit will behave as if powered off.
5	GND	YES	OUT, REF will float up towards 3.9V.
6	REF	YES	The circuit behaves normally with more broadband noise on OUT.
7	OUT	YES	No V_{OUT} signal.
8	$\overline{SHDN}$	YES	The low power shutdown feature will not function, otherwise the circuit behaves normally in the active state.

FMEA information in this document (not limited to, but including the description of behavior under specific pin-connection conditions) is provided for convenience only. Ultimately, the end-user is responsible for verifying proper and reliable operation in each actual application. Linear Technology assumes no liability whatsoever with providing this information.

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APPLICATIONS INFORMATION

Fuse Monitor

The inputs can be overdriven without fear of damaging the LT1999. This makes the LT1999 ideal for monitoring fuses if either +IN or –IN are shorted to ground while the other is at the full common mode supply voltage (see Figure 6). If the fuse in Figure 6 opens with the +IN tied to the positive supply, the load will pull –IN to GND. The output will be forced to the positive V^+ supply rail. If it is desired that the output be near ground if the fuse opens, it is a simple matter of swapping the inputs. Precautions should be followed: First, when the inputs are stressed differentially due to the fuse blowing open, a large voltage drop will be placed across the +IN to –IN pins, dissipating power in the precision on-chip input resistors. Precaution should be taken to prevent junction temperatures from exceeding the Absolute Maximum ratings (see Note 3 in the Electrical Characteristics section). Secondly, if the load is inductive, and the fuse blows open without a clamp diode, energy stored in the inductive load will be dissipated in the LT1999, which could cause damage. A simple steering diode as shown in Figure 6 will prevent this from happening, and will protect the LT1999 from damage.

Finally, the user should be aware that in fuse monitoring applications with the sense voltage ($V_{SENSE} = V_{+IN} – V_{–IN}$) being driven in excess of –25V, the output of the LT1999 will undergo phase reversal (seeFigure 7).

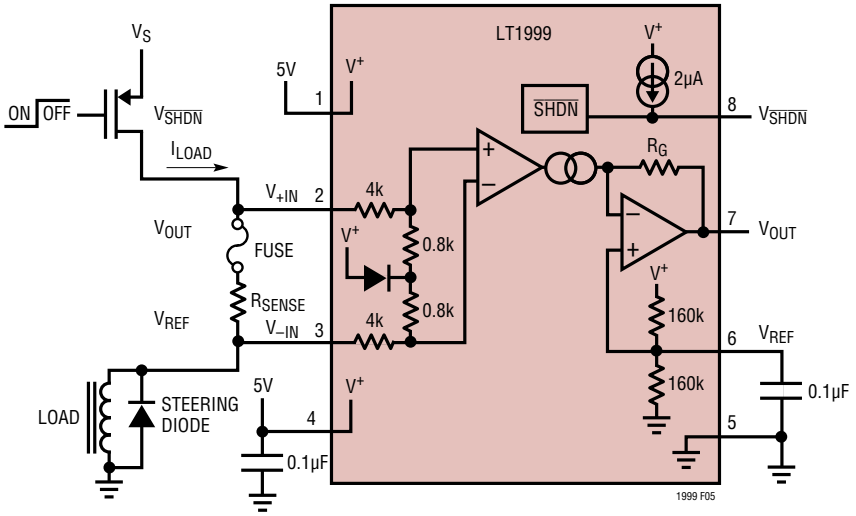

Figure 6. Using the LT1999 to Monitor a Fuse

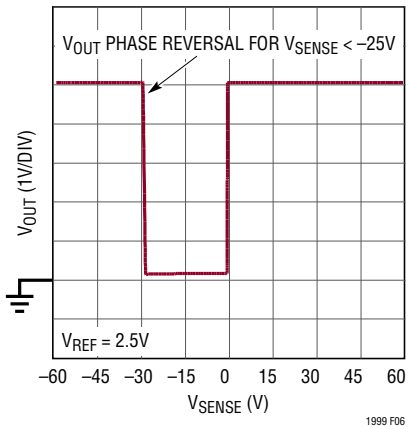

Figure 7. A Plot of the LT1999's Output Voltage vs V_{SENSE} ($V_{SENSE} = V_{+IN} – V_{–IN}$). In Applications Where the Sense Voltage Is Driven in Excess of –25V, the Output of the LT1999 Will Undergo Phase Reversal

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TYPICAL APPLICATIONS

Solenoid Current Monitor

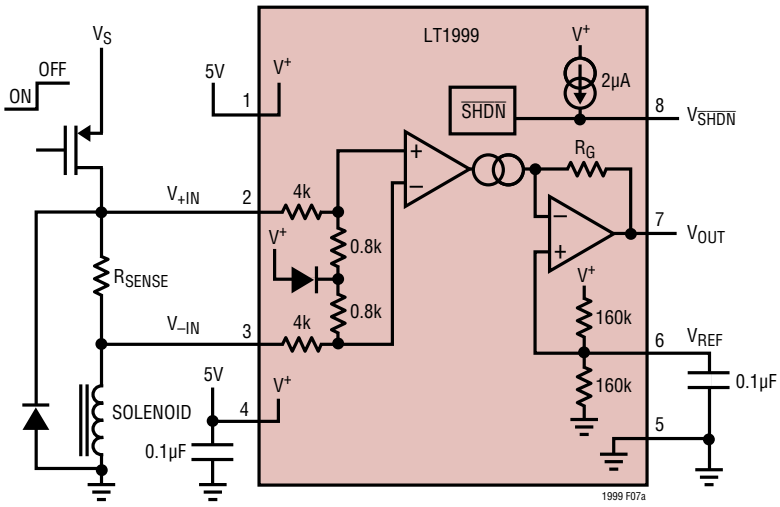
The solenoid of Figure 8 consists of a coil of wire in an iron case with permeable plunger that acts as a movable element. When the MOSFET turns on, the diode is reversed biased off, and current flows through R_{SENSE} to actuate the solenoid. If the MOSFET is turned off, the current in the MOSFET is interrupted, but the energy stored in the solenoid causes the diode to turn on and current to freewheel in the loop consisting of the diode, R_{SENSE} and the solenoid.

Figure 8 shows the LT1999 monitoring currents in a ground referenced solenoid used when the coil is hard tied to the case, and is tied to ground. Figure 9 shows a supply referenced solenoid whose coil is insulated from the case. The LT1999 will interface equally well to either of these two configurations.

Bidirectional PWM Motor Monitor

Pulse width modulation is commonly used to efficiently vary the average voltage applied across a DC motor. The H-bridge topology of Figure 10 allows full 4-quadrant control: clockwise control, counter-clockwise control, clockwise regeneration, and counter-clockwise regeneration. The LT1999 in conjunction with a non-inductive current shunt is used to monitor currents in the rotor. The LT1999 can be used to detect stuck rotors, provide detection of overcurrent conditions in general, or provide current mode feedback control.

Figure 11 shows a plot of the output voltage of the LT1999.



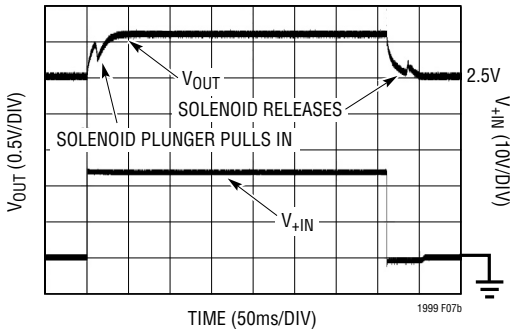


Figure 8. Solenoid Current Monitor for Ground Tied Solenoid. The Common Mode Inputs to the LT1999 Switch Between V_S and One Diode Drop Below Ground

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TYPICAL APPLICATIONS

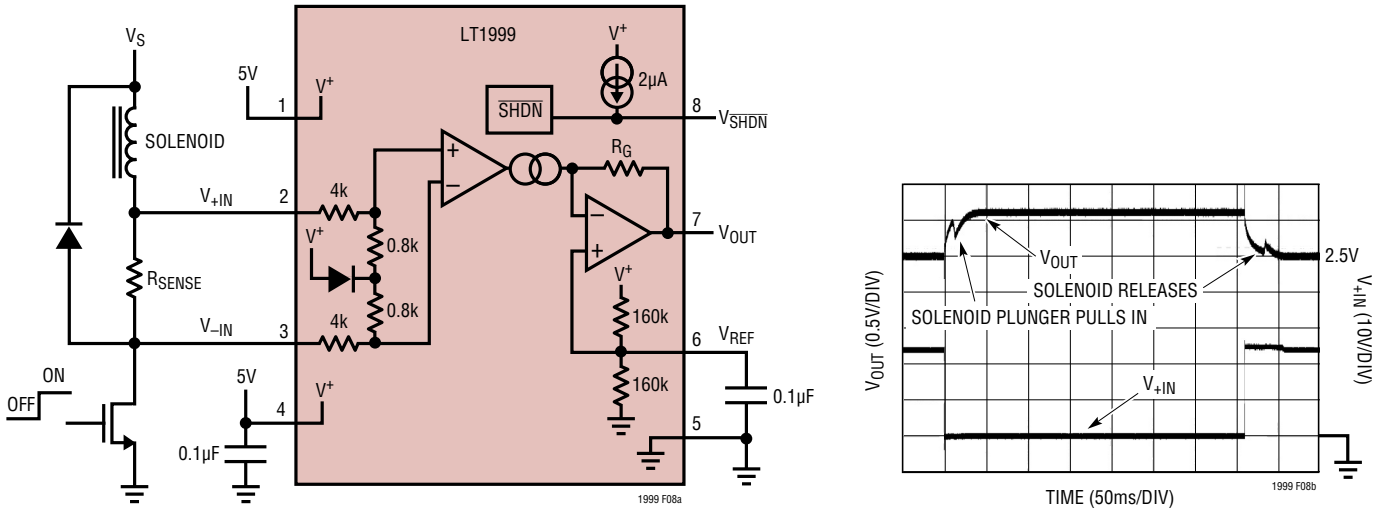

Figure 9. Solenoid Current Monitor for Non-Grounded Solenoids. This Circuit Performs the Same Function as Figure 7 Except One End of the Solenoid Is Tied to V_S. The Common Mode Voltage of Inputs of the LT1999 Switch Between Ground and One Diode Drop Above V_S

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TYPICAL APPLICATIONS

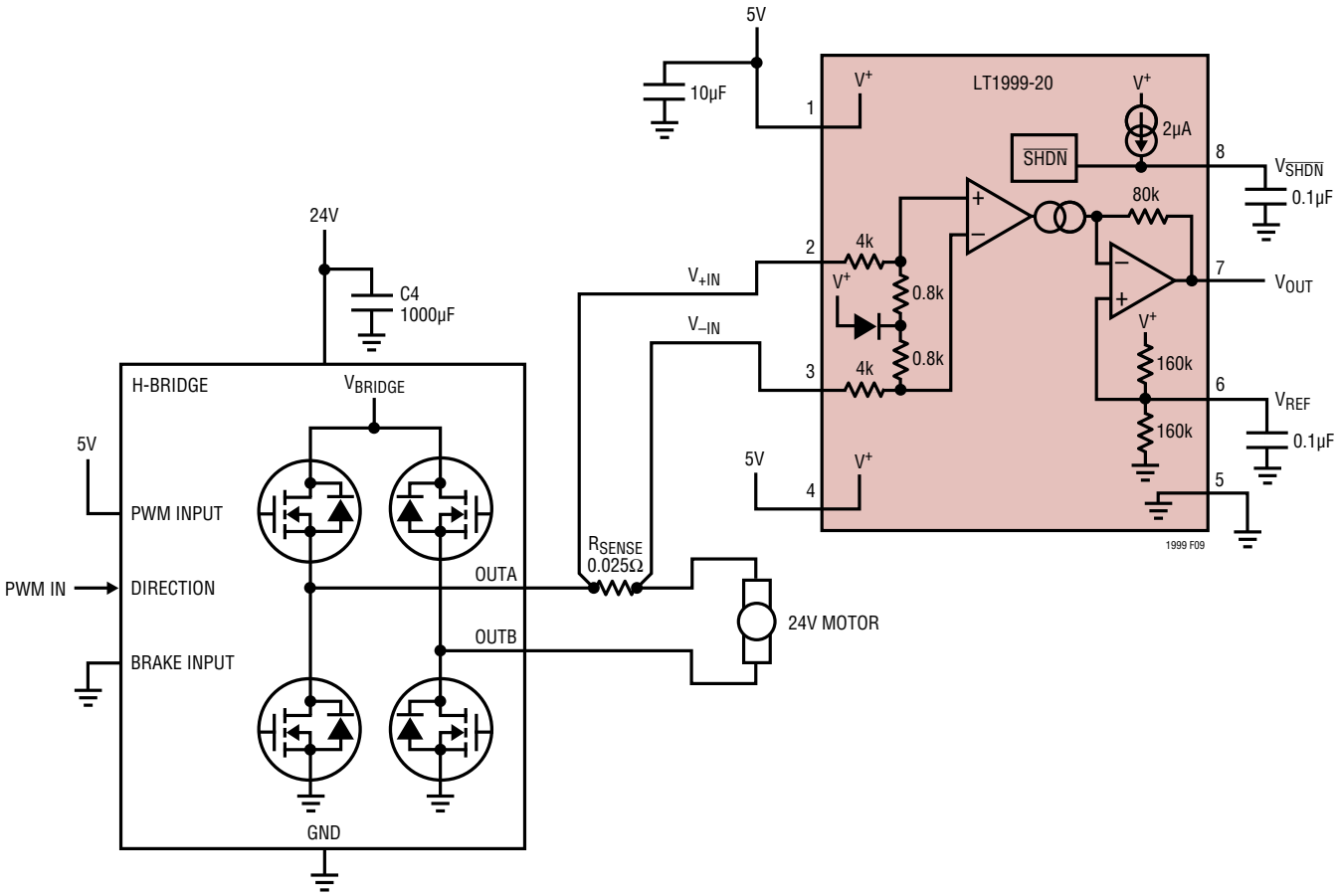

Figure 10. Armature Current Monitor for DC Motor Applications

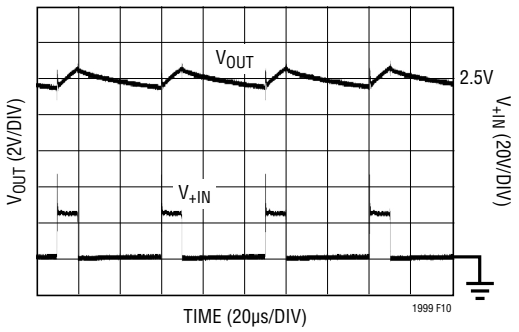

Figure 11. LT1999 Output Waveforms for the Circuit of Figure 10

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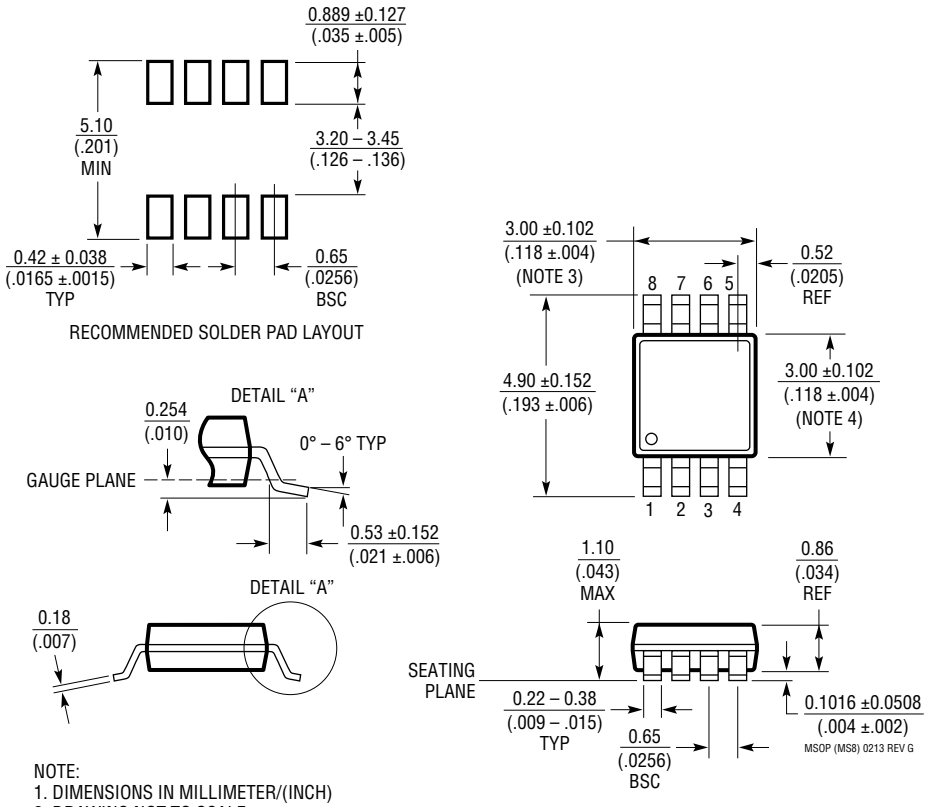
PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

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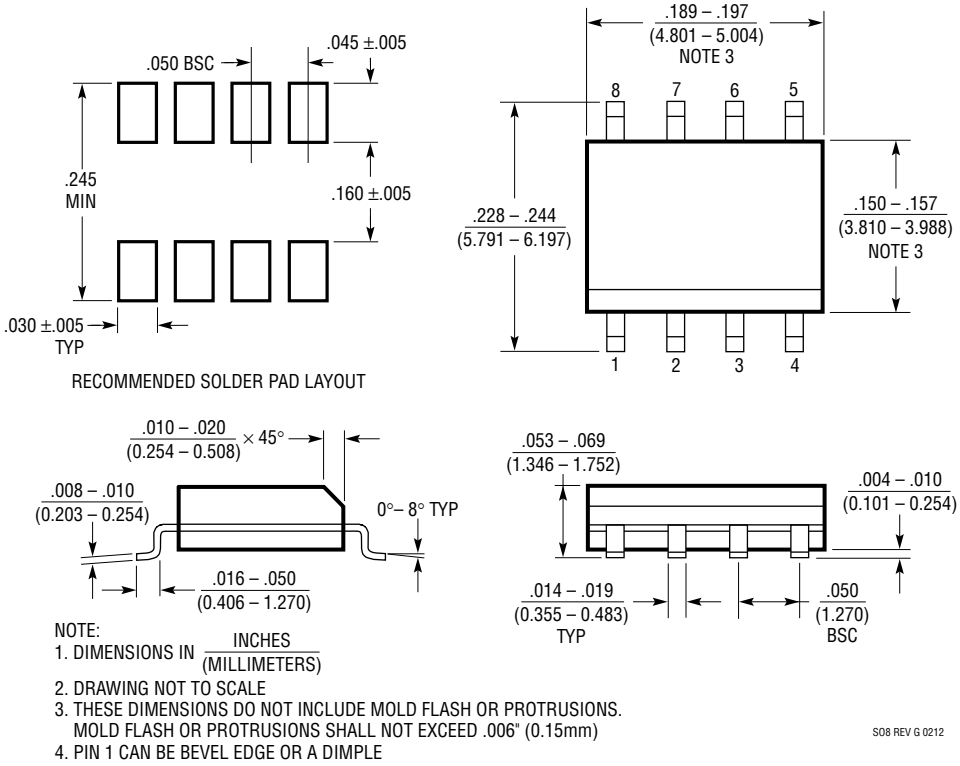
PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

S08 REV G 0212

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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	5/11	Revised +IN and –IN pin descriptions in Pin Functions section	12
B	3/12	Revised Voltage Output Swing Low specification (V_{OUT}) under a loaded condition of 1kΩ to mid-supply.	4, 6
		Updated Figure 4 to multicolor.	16
C	2/15	Addition of MSOP Pinout Option Engineered for FMEA	All
		Correction to AV Specification for LT1999-50 from 48.75 to 49.75	5
		Update to Pin Functions to include Pinout Option Engineered for FMEA	12
		Addition of New Application Information "Pinout Option Engineered for FMEA"	18, 19
		Addition of Figure 5 and Renumbering of Figures 6 to 11	18 to 23
		Addition of Table 1 and Table 2	19
D	6/15	LT1999F added to Figure 1 (Simplified Block Diagram)	13
		LT1999F added to Figure 2 (Test Circuit)	14
		Additional test condition (V_{CM} = 80) added to table 1 and table 2	19
		Note added regarding the use of FMEA information	19
E	9/19	Added Automotive Grade products, updated data sheet format	All

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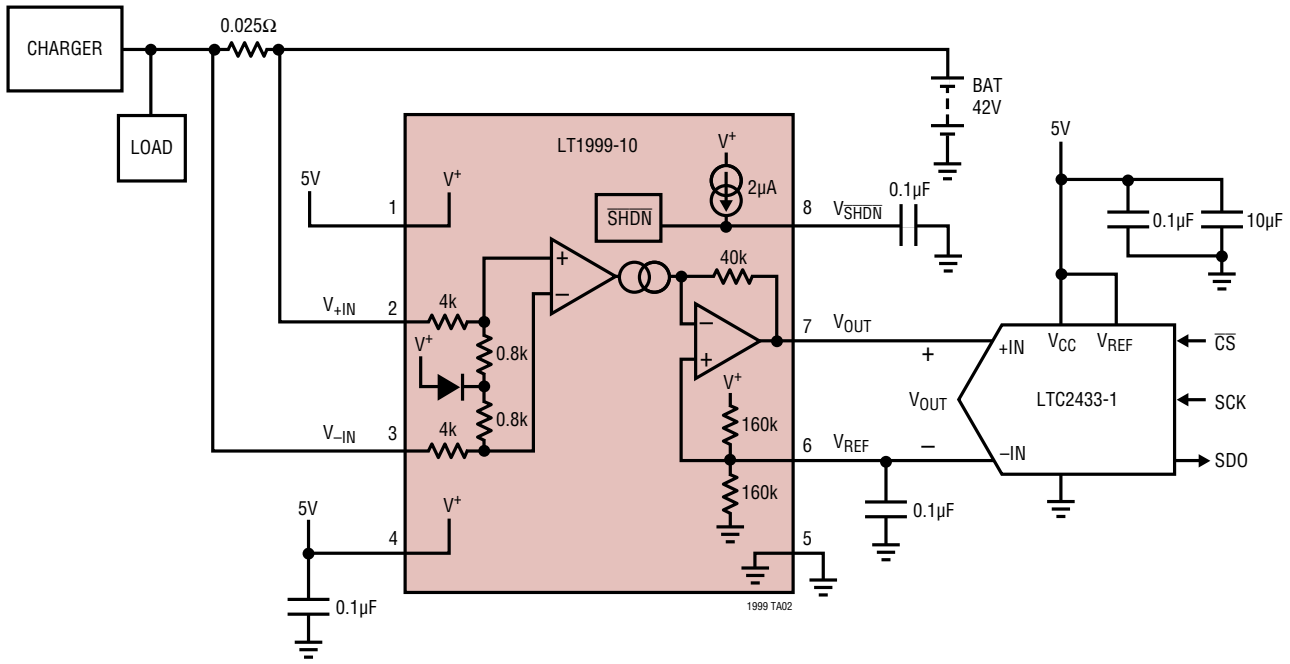
TYPICAL APPLICATION

Battery Charge Current and Load Current Monitor
V_{OUT} = 0.25V/A, Maximum Measured Current ±9.5A



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1787/ LT1787HV	Precision, Bidirectional High Side Current Sense Amplifier	2.7V to 60V Operation, 75μV Offset, 60μA Current Draw
LT6100	Gain-Selectable High Side Current Sense Amplifier	4.1V to 48V Operation, Pin-Selectable Gain: 10V/V, 12.5V/V, 20V/V, 25V/V, 40V/V, 50V/V
LTC6101/ LTC6101HV	High Voltage High Side Current Sense Amplifier	4V to 60V/5V to 100V Operation, External Resistor Set Gain, SOT23
LTC6102/ LTC6102HV	Zero Drift High Side Current Sense Amplifier	4V to 60V/5V to 100V Operation, ±10μV Offset, 1μs Step Response, MSOP8/DFN Packages
LTC6103	Dual High Side Precision Current Sense Amplifier	4V to 60V, Gain Configurable, 8-Pin MSOP Package
LTC6104	Bidirectional, High Side Current Sense	4V to 60V, Gain Configurable, 8-Pin MSOP Package
LT6106	Low Cost, High Side Precision Current Sense Amplifier	2.7V to 36V, Gain Configurable, SOT23 Package
LT6105	Precision, Extended Input Range Current Sense Amplifier	–0.3 to 44V, Gain Configurable, 8-Pin MSOP Package
LTC4150	Coulomb Counter/Battery Gas Gauge	Indicates Charge Quantity and Polarity
LT1990	Precision, 100μA Gain Selectable Amplifier	2.7V to 36V Operation, CMRR > 70dB, Input Voltage = ±250V
LT1991	±250V Input Range Difference Amplifier	2.7V to 36V Operation, 50μV Offset, CMRR > 75B, Input Voltage = ±60V
LT1637/LT1638	1.1/1.2MHz, 0.4V/μs Over-The-Top, Rail-to-Rail Input and Output Amplifier	0.4V/μs Slew Rate, 230μA per Amplifier

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