

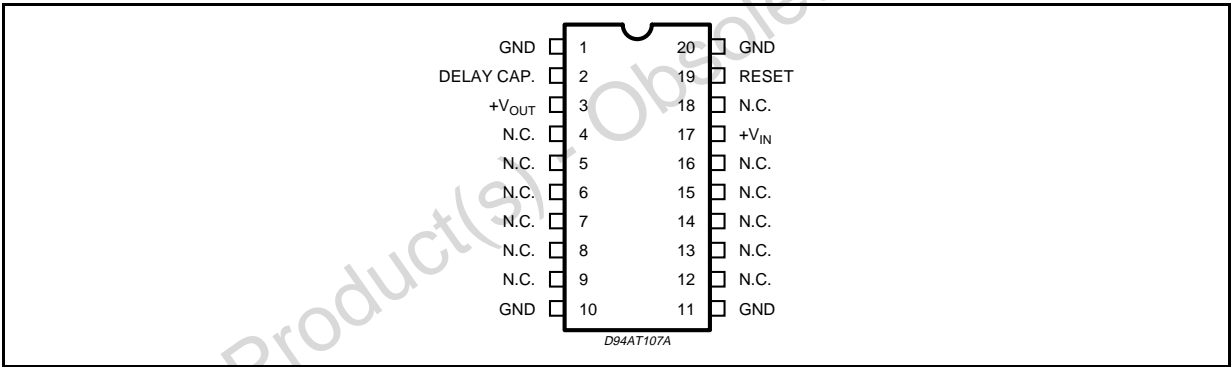
L4947PD

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	35	V
	DC Reverse Input Voltage	- 18	V
	Transient Input Overvoltages : Load Dump :	80	V
	$5\text{ms} \leq t_{\text{rise}} \leq 10\text{ms}$ τ_f Fall Time Constant = 100ms $R_{\text{SOURCE}} \geq 0.5\Omega$	- 80	V
	Field Decay : $5\text{ms} \leq t_{\text{fall}} \leq 10\text{ms}$, $R_{\text{SOURCE}} \geq 10\Omega$ τ_r Rise Time Constant = 33ms	± 100	V
	Low Energy Spike : $t_{\text{rise}} = 1\mu\text{s}$, $t_{\text{fall}} = 500\mu\text{s}$, $R_{\text{SOURCE}} \geq 10\Omega$ f_r Repetition Frequency = 5Hz		
V_R	Reset Output Voltage	35	V
T_J , T_{stg}	Junction and Storage Temperature Range	- 55 to 150	°C

Note: The circuit is ESD protected according to MIL-STD-883C.

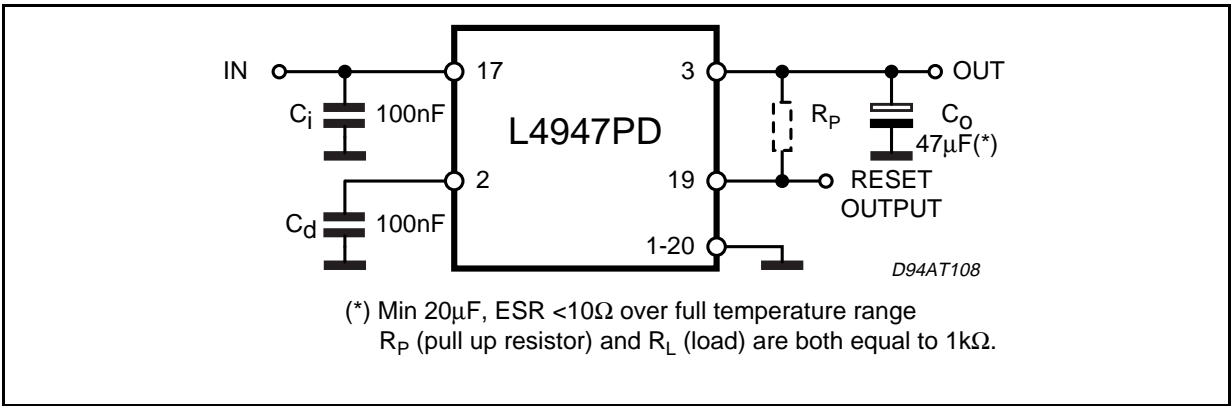
PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{\text{th j-case}}$	Thermal Resistance Junction-case	Max 3	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (refer to the test circuit, $V_i = 14.4\text{V}$, $C_o = 47\mu\text{F}$, $\text{ESR} < 10\Omega$, $R_p = 1\text{K}\Omega$, $R_L = 1\text{K}\Omega$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	$I_o = 0\text{mA}$ to 500mA Over Full T Range $T_J = 25^\circ\text{C}$	4.80 4.90	5.00 5.00	5.20 5.10	V V
V_i	Operating Input Voltage	$I_o = 0\text{mA}$ to (*) 500mA	6		26	V
ΔV_o	Line Regulation	$V_i = 6\text{V}$ to 26V ; $I_o = 5\text{mA}$		5	50	mV
ΔV_o	Load Regulation	$I_o = 5\text{mA}$ to 500mA		15	60	mV
$V_i - V_o$	Dropout Voltage	$I_o = 500\text{mA}$, $T_J = 25^\circ\text{C}$ Over Full T Range		0.40	0.55 0.75	V V
I_q	Quiescent Current	$I_o = 0\text{mA}$, $T_J = 25^\circ\text{C}$ $I_o = 0\text{mA}$ Over Full T $I_o = 500\text{mA}$ Over Full T		5 6.5 110	10 13 180	mA mA mA
$\frac{\Delta V_o}{T}$	Temperature Output Voltage Drift			-0.5		mV/ $^\circ\text{C}$
SVR	Supply Volt. Rej.	$I_o = 350\text{mA}$; $f = 120\text{Hz}$ $C_o = 100\mu\text{F}$; $V_i = 12\text{V} \pm 5V_{pp}$	50	60		dB
I_{sc}	Output Short Circuit Current		0.50	0.80	1.50	A
V_R	Reset Output Saturation Voltage	$1.5\text{V} < V_o < V_{RT(\text{off})}$, $I_R = 1.6\text{mA}$ $3.0\text{V} < V_o < V_{RT(\text{off})}$, $I_R = 8\text{mA}$			0.40 0.40	V V
I_R	Reset Output Leakage Current	V_o in Regulation, $V_R = 5\text{V}$			50	μA
$V_{RT \text{ peak}}$	Power On-Off Reset out Peak Voltage	$1\text{K}\Omega$ Reset Pull-up to V_o		0.65	1.0	V
$V_{RT(\text{off})}$	Power OFF V_o Threshold	V_o @ Reset Out H to L Transition	4.75	$V_o - 0.15$		V
$V_{RT(\text{on})}$	Power ON V_o Threshold	V_o @ Reset Out L to H Transition		$V_{RT(\text{off})} + 0.05$	$V_o - 0.04$	V
V_{Hyst}	Power ON-Off Hysteresis	$V_{RT(\text{on})} - V_{RT(\text{off})}$		0.05		V
V_d	Delay Comparator Threshold	V_d @ Reset Out L to H Transition	3.65	4.00	4.35	V
		V_d @ Reset Out H to L Transition	3.20	3.55	3.90	V
V_{dH}	Delay Comparator Hysteresis			0.45		V
I_d	Delay Capacitor Charging Current	$V_d = 3\text{V}$, $T_J = 25^\circ\text{C}$		20		μA
V_{disch}	Delay Capacitor Discharge Voltage	$V_o < V_{RT(\text{off})}$		0.55	1.20	V
T_d	Power on Reset Delay Time	$C_d = 100\text{nF}$, $T_J = 25^\circ\text{C}$	10	20	30	ms

(*) For a DC voltage $26 < V_i < 37\text{V}$ the device is not operating

FUNCTIONAL DESCRIPTION

The L4947PD is a very low drop 5V/0.5A voltage regulator provided with a reset function and therefore particularly suited to meet the requirements of supplying the microprocessor systems used in automotive and industrial applications.

The block diagram shows the basic structure of the device : the reference, the error amplifier, the driver, the power PNP, the protection and reset

functions.

The power stage is a Lateral PNP transistor which allows a very low dropout voltage (typ. 400mV at $T_J = 25^\circ\text{C}$, max. 750mV over the full temperature range @ $I_o = 500\text{mA}$). The typical curve of the dropout voltage as a function of the junction temperature is shown in Fig. 1 : that is the worst case, where $I_o = 500\text{mA}$.

The current consumption of the device (quiescent

current) is maximum 13mA - over full T - when no load current is required.

The internal antisaturation circuit allows a drastic reduction in the current peak which takes place during the start up.

The reset function supervises the regulator output voltage inhibiting the microprocessor when the device is out of regulation and resetting it at the power-on after a settable delay. The reset is LOW when the output voltage value is lower than the reset threshold voltage. At the power-on phase the output voltage increases (see Fig. 2) and - when it reaches the power-on V_O threshold V_{RT} (On) - the reset output becomes HIGH after a delay time set by the external capacitor C_d . At the power-off the output voltage decreases : at the $V_{RT(Off)}$ threshold value ($V_O - 0.15V$ typ. value) the reset output instantaneously goes down (LOW status) inhibiting the microprocessor. The typical

Figure 1: Typical Dropout Voltage vs. T_j
($I_o = 500mA$).

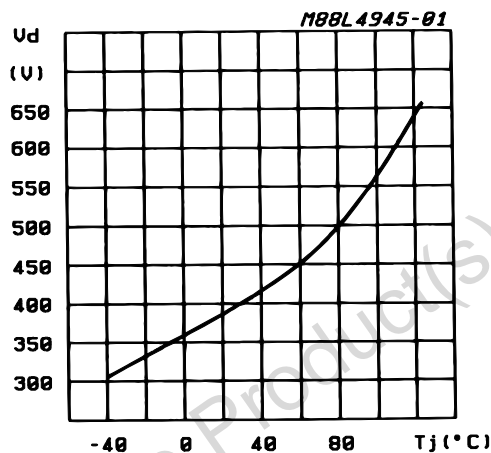
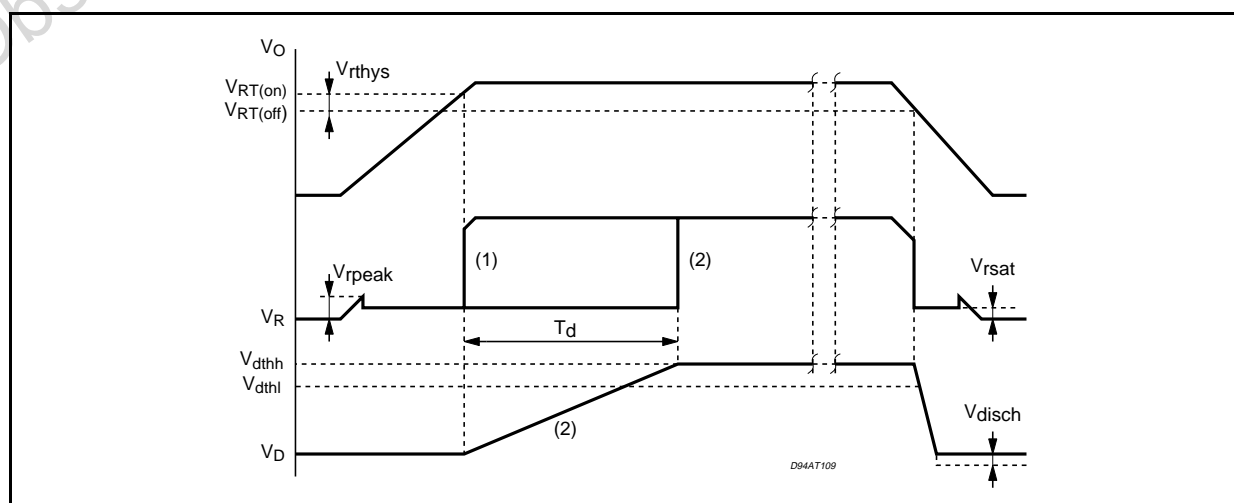


Figure 2: Reset Waveforms:

- (1) Without External Capacitor C_d .
- (2) With External Capacitor C_d .



power on-off hysteresis is 50mV.

The three gain stages (operational amplifier, driver and power PNP) require the external capacitor ($C_{omin} = 20\mu F$) to guarantee the global stability of the system.

Load dump and field decay protections ($\pm 80V$), reverse voltage ($-18V$) and short circuit protection, thermal shutdown are the main features that make the L4947PD specially suitable for applications in the automotive environment.

EXTERNAL COMPENSATION

Since the purpose of a voltage regulator is to supply and load variations, the open loop gain of the regulator must be very high at low frequencies. This may cause instability as a result of the various poles present in the loop. To avoid this instability dominant pole compensation is used to reduce phase shift due to other poles at the unity gain frequency. The lower the frequency of these other poles at the unity gain frequency. The lower the frequency of these other poles, the greater must be capacitor used to create the dominant pole for the same DC gain.

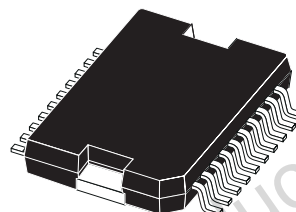
Where the output transistor is a lateral PNP type there is a pole in the regulation loop at a frequency too low to be compensated by a capacitor which can be integrated. An external compensation is therefore necessary so a very high value capacitor must be connected from the output to ground.

The parasitic equivalent series resistance of the capacitor used adds a zero to the regulation loop. This zero may compromise the stability of the system since its effect tends to cancel the effect of the pole added. In regulators this ESR must be less than 3Ω and the minimum capacitor value is $47\mu F$.

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	10° (max.)					
S	8° (max.)					
T		10			0.394	

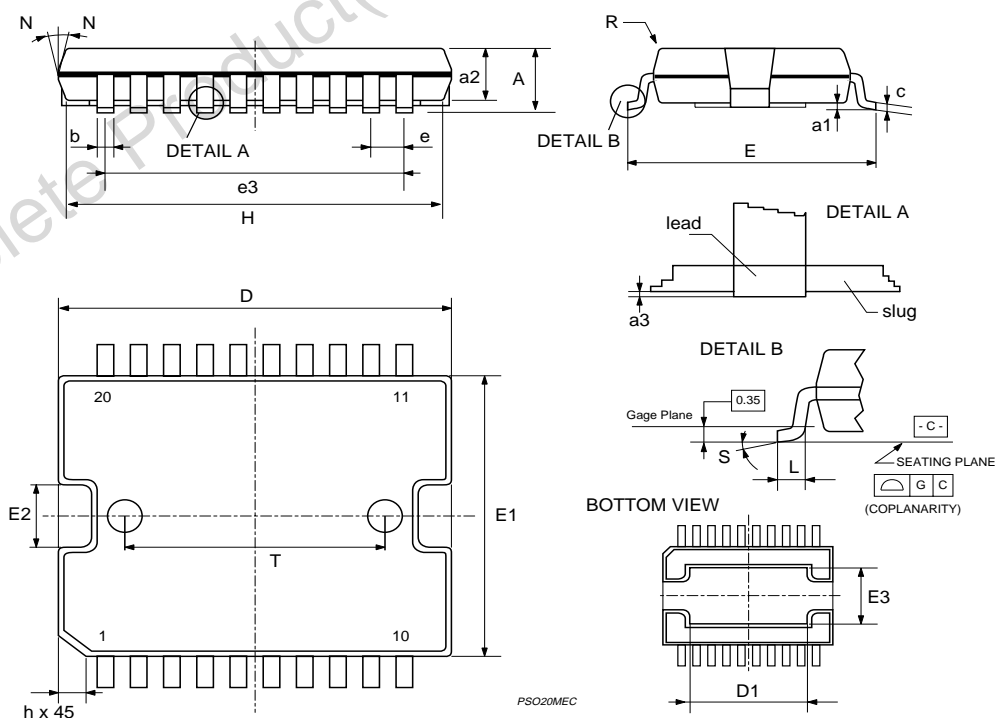
(1) "D and F" do not include mold flash or protrusions.
- Mold flash or protrusions shall not exceed 0.15 mm (0.006").
- Critical dimensions: "E", "G" and "a3"

OUTLINE AND MECHANICAL DATA



JEDEC MO-166

PowerSO20



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