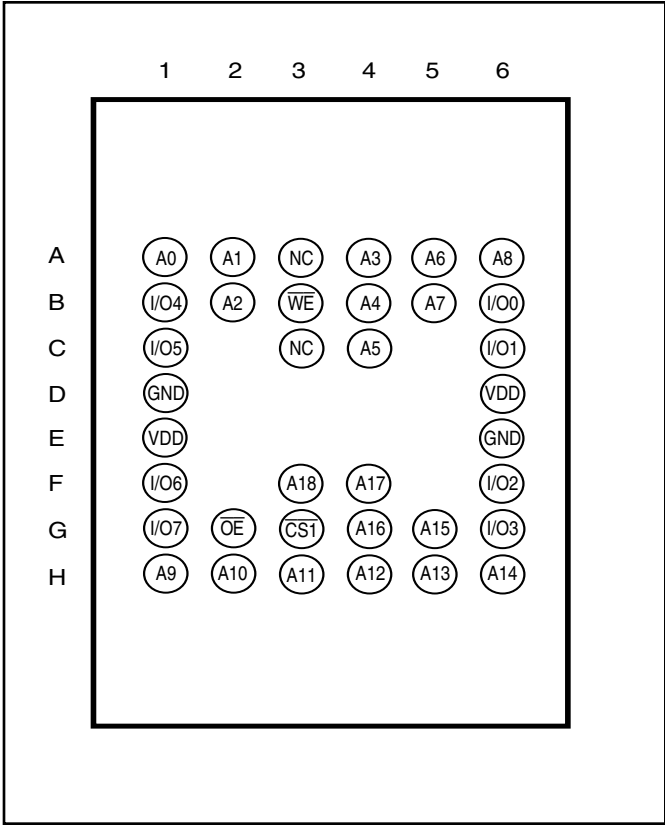


IS62WV5128ALL, IS62WV5128BLL

PIN DESCRIPTIONS

|                 |                     |
|-----------------|---------------------|
| A0-A18          | Address Inputs      |
| CS1             | Chip Enable 1 Input |
| OE              | Output Enable Input |
| WE              | Write Enable Input  |
| I/O0-I/O7       | Input/Output        |
| NC              | No Connection       |
| V <sub>DD</sub> | Power               |
| GND             | Ground              |

36-pin mini BGA (B) (6mm x 8mm)  
(Package Code B)

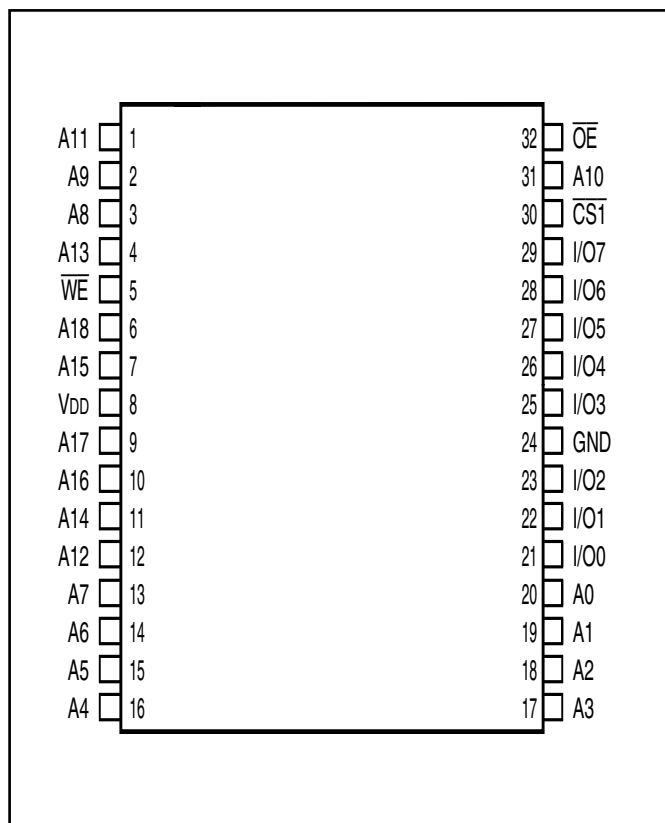


**PIN DESCRIPTIONS**

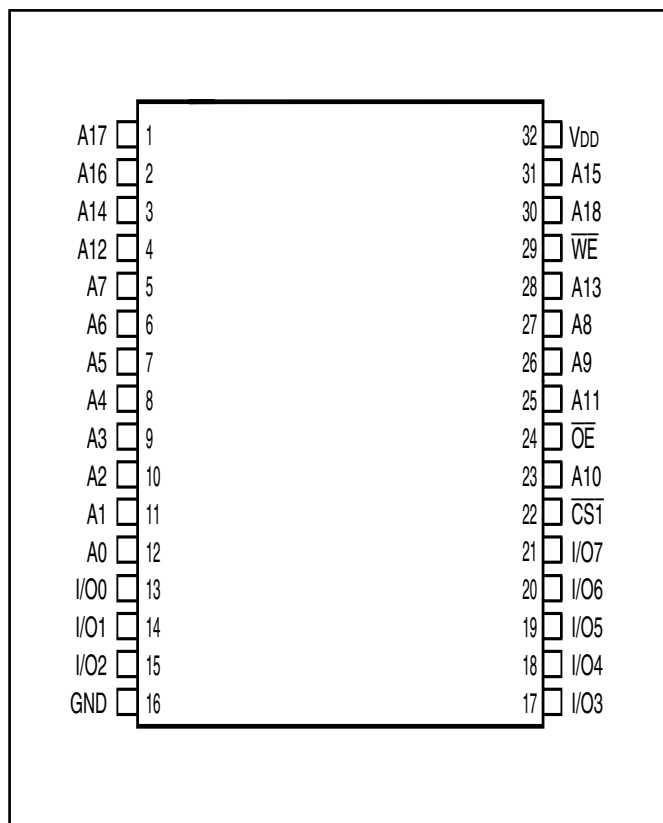
|                 |                     |
|-----------------|---------------------|
| A0-A18          | Address Inputs      |
| CS1             | Chip Enable 1 Input |
| OE              | Output Enable Input |
| WE              | Write Enable Input  |
| I/O0-I/O7       | Input/Output        |
| V <sub>DD</sub> | Power               |
| GND             | Ground              |

**PIN CONFIGURATION**

32-pin TSOP (TYPE I), (Package Code T)  
32-pin sTSOP (TYPE I) (Package Code H)



32-pin SOP (Package Code Q)  
32-pin TSOP (TYPE II) (Package Code T2)





## IS62WV5128ALL, IS62WV5128BLL

### OPERATING RANGE ( $V_{DD}$ )

| Range      | Ambient Temperature | IS62WV5128ALL | IS62WV5128BLL |
|------------|---------------------|---------------|---------------|
| Commercial | 0°C to +70°C        | 1.65V - 2.2V  | 2.5V - 3.6V   |
| Industrial | -40°C to +85°C      | 1.65V - 2.2V  | 2.5V - 3.6V   |

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol     | Parameter                            | Value                | Unit |
|------------|--------------------------------------|----------------------|------|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | -0.2 to $V_{DD}+0.3$ | V    |
| $V_{DD}$   | $V_{DD}$ Related to GND              | -0.2 to $V_{DD}+0.3$ | V    |
| $T_{STG}$  | Storage Temperature                  | -65 to +150          | °C   |
| $P_T$      | Power Dissipation                    | 1.0                  | W    |

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol         | Parameter           | Test Conditions                                   | $V_{DD}$  | Min. | Max.           | Unit          |
|----------------|---------------------|---------------------------------------------------|-----------|------|----------------|---------------|
| $V_{OH}$       | Output HIGH Voltage | $I_{OH} = -0.1 \text{ mA}$                        | 1.65-2.2V | 1.4  | —              | V             |
|                |                     | $I_{OH} = -1 \text{ mA}$                          | 2.5-3.6V  | 2.2  | —              | V             |
| $V_{OL}$       | Output LOW Voltage  | $I_{OL} = 0.1 \text{ mA}$                         | 1.65-2.2V | —    | 0.2            | V             |
|                |                     | $I_{OL} = 2.1 \text{ mA}$                         | 2.5-3.6V  | —    | 0.4            | V             |
| $V_{IH}$       | Input HIGH Voltage  |                                                   | 1.65-2.2V | 1.4  | $V_{DD} + 0.2$ | V             |
|                |                     |                                                   | 2.5-3.6V  | 2.2  | $V_{DD} + 0.3$ | V             |
| $V_{IL}^{(1)}$ | Input LOW Voltage   |                                                   | 1.65-2.2V | -0.2 | 0.4            | V             |
|                |                     |                                                   | 2.5-3.6V  | -0.2 | 0.6            | V             |
| $I_{LI}$       | Input Leakage       | $GND \leq V_{IN} \leq V_{DD}$                     |           | -1   | 1              | $\mu\text{A}$ |
| $I_{LO}$       | Output Leakage      | $GND \leq V_{OUT} \leq V_{DD}$ , Outputs Disabled |           | -1   | 1              | $\mu\text{A}$ |

Notes:

1.  $V_{IL}$  (min.) = -1.0V for pulse width less than 10 ns.

CAPACITANCE<sup>(1)</sup>

| Symbol           | Parameter                | Conditions            | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance        | V <sub>IN</sub> = 0V  | 8    | pF   |
| C <sub>OUT</sub> | Input/Output Capacitance | V <sub>OUT</sub> = 0V | 10   | pF   |

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

| Parameter                                      | IS62WV5128ALL<br>(Unit)       | IS62WV5128BLL<br>(Unit)       |
|------------------------------------------------|-------------------------------|-------------------------------|
| Input Pulse Level                              | 0.4V to V <sub>DD</sub> -0.2V | 0.4V to V <sub>DD</sub> -0.3V |
| Input Rise and Fall Times                      | 5 ns                          | 5ns                           |
| Input and Output Timing<br>and Reference Level | V <sub>REF</sub>              | V <sub>REF</sub>              |
| Output Load                                    | See Figures 1 and 2           | See Figures 1 and 2           |

|                  | IS62WV5128ALL<br>1.65 - 2.2V | IS62WV5128BLL<br>2.5V - 3.6V |
|------------------|------------------------------|------------------------------|
| R1(Ω)            | 3070                         | 3070                         |
| R2(Ω)            | 3150                         | 3150                         |
| V <sub>REF</sub> | 0.9V                         | 1.5V                         |
| V <sub>TM</sub>  | 1.8V                         | 2.8V                         |

AC TEST LOADS

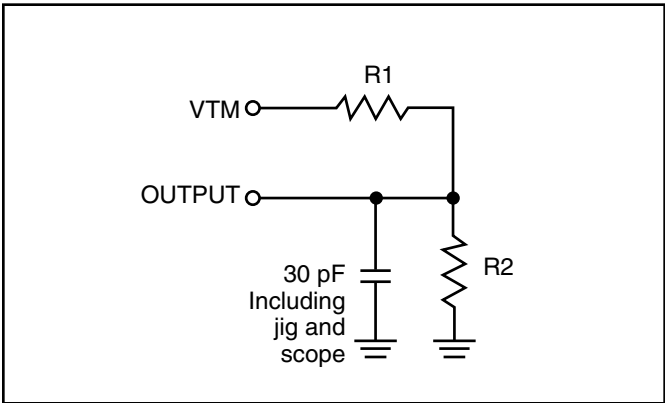


Figure 1

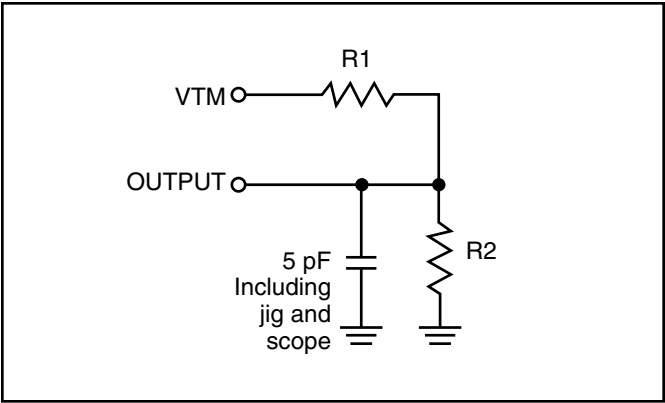


Figure 2



## IS62WV5128ALL, IS62WV5128BLL

### POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

#### 62WV5128ALL (1.65V - 2.2V)

| Symbol           | Parameter                                        | Test Conditions                                                                                                                           | Max.<br>70 ns                | Unit |
|------------------|--------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|------|
| I <sub>CC</sub>  | V <sub>DD</sub> Dynamic Operating Supply Current | V <sub>DD</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>                                                                  | Com.<br>Ind.<br>25<br>30     | mA   |
| I <sub>CC1</sub> | Operating Supply Current                         | V <sub>DD</sub> = Max., CS1 = 0.2V<br>WE = V <sub>DD</sub> -0.2V<br>f=1MHz                                                                | Com.<br>Ind.<br>10<br>10     | mA   |
| I <sub>SB1</sub> | TTL Standby Current (TTL Inputs)                 | V <sub>DD</sub> = Max.,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>CS1 = V <sub>IH</sub> ,<br>f = 1 MHz                   | Com.<br>Ind.<br>0.35<br>0.35 | mA   |
| I <sub>SB2</sub> | CMOS Standby Current (CMOS Inputs)               | V <sub>DD</sub> = Max.,<br>CS1 ≥ V <sub>DD</sub> - 0.2V,<br>V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or<br>V <sub>IN</sub> ≤ 0.2V, f = 0 | Com.<br>Ind.<br>15<br>15     | μA   |

Note:

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

### POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

#### 62WV5128BLL (2.5V - 3.6V)

| Symbol           | Parameter                                        | Test Conditions                                                                                                                           | Max.<br>55 ns                | Unit |
|------------------|--------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|------|
| I <sub>CC</sub>  | V <sub>DD</sub> Dynamic Operating Supply Current | V <sub>DD</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>                                                                  | Com.<br>Ind.<br>40<br>45     | mA   |
| I <sub>CC1</sub> | Operating Supply Current                         | V <sub>DD</sub> = Max., CS1 = 0.2V<br>WE = V <sub>DD</sub> -0.2V<br>f=1MHz                                                                | Com.<br>Ind.<br>15<br>15     | mA   |
| I <sub>SB1</sub> | TTL Standby Current (TTL Inputs)                 | V <sub>DD</sub> = Max.,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>CS1 = V <sub>IH</sub> ,<br>f = 1 MHz                   | Com.<br>Ind.<br>0.35<br>0.35 | mA   |
| I <sub>SB2</sub> | CMOS Standby Current (CMOS Inputs)               | V <sub>DD</sub> = Max.,<br>CS1 ≥ V <sub>DD</sub> - 0.2V,<br>V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or<br>V <sub>IN</sub> ≤ 0.2V, f = 0 | Com.<br>Ind.<br>15<br>15     | μA   |

Note:

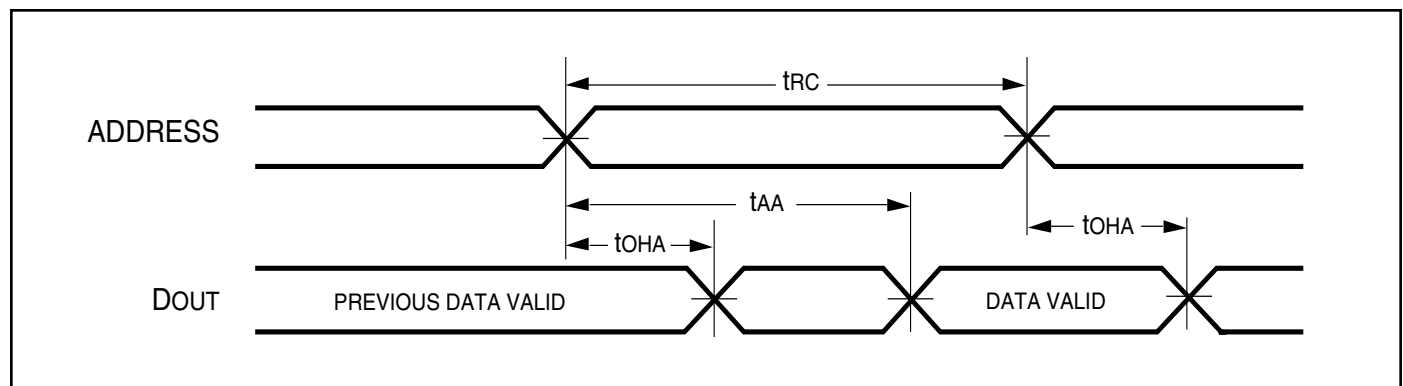
- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)**

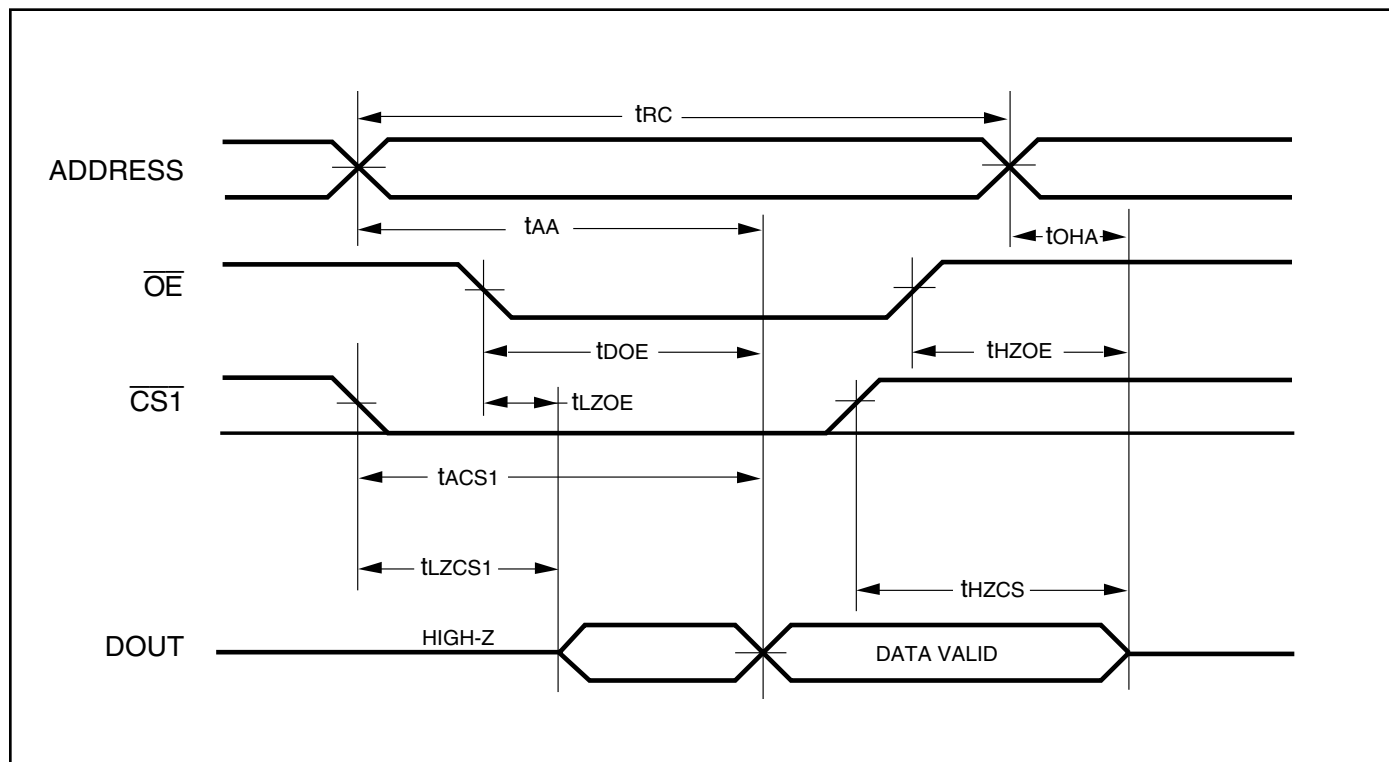
| Symbol           | Parameter            | 55 ns |      | 70 ns |      | Unit |
|------------------|----------------------|-------|------|-------|------|------|
|                  |                      | Min.  | Max. | Min.  | Max. |      |
| $t_{RC}$         | Read Cycle Time      | 55    | —    | 70    | —    | ns   |
| $t_{AA}$         | Address Access Time  | —     | 55   | —     | 70   | ns   |
| $t_{OHA}$        | Output Hold Time     | 10    | —    | 10    | —    | ns   |
| $t_{ACS1}$       | CS1 Access Time      | —     | 55   | —     | 70   | ns   |
| $t_{DOE}$        | OE Access Time       | —     | 25   | —     | 35   | ns   |
| $t_{HZOE}^{(2)}$ | OE to High-Z Output  | —     | 20   | —     | 25   | ns   |
| $t_{LZOE}^{(2)}$ | OE to Low-Z Output   | 5     | —    | 5     | —    | ns   |
| $t_{HZCS1}$      | CS1 to High-Z Output | 0     | 20   | 0     | 25   | ns   |
| $t_{LZCS1}$      | CS1 to Low-Z Output  | 10    | —    | 10    | —    | ns   |

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to  $V_{DD}-0.2V/V_{DD}-0.3V$  and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

**AC WAVEFORMS****READ CYCLE NO. 1<sup>(1,2)</sup> (Address Controlled) (CS1 = OE =  $V_{IL}$ , WE =  $V_{IH}$ )**

## AC WAVEFORMS

READ CYCLE NO. 2<sup>(1,3)</sup> (CS1, OE Controlled)

## Notes:

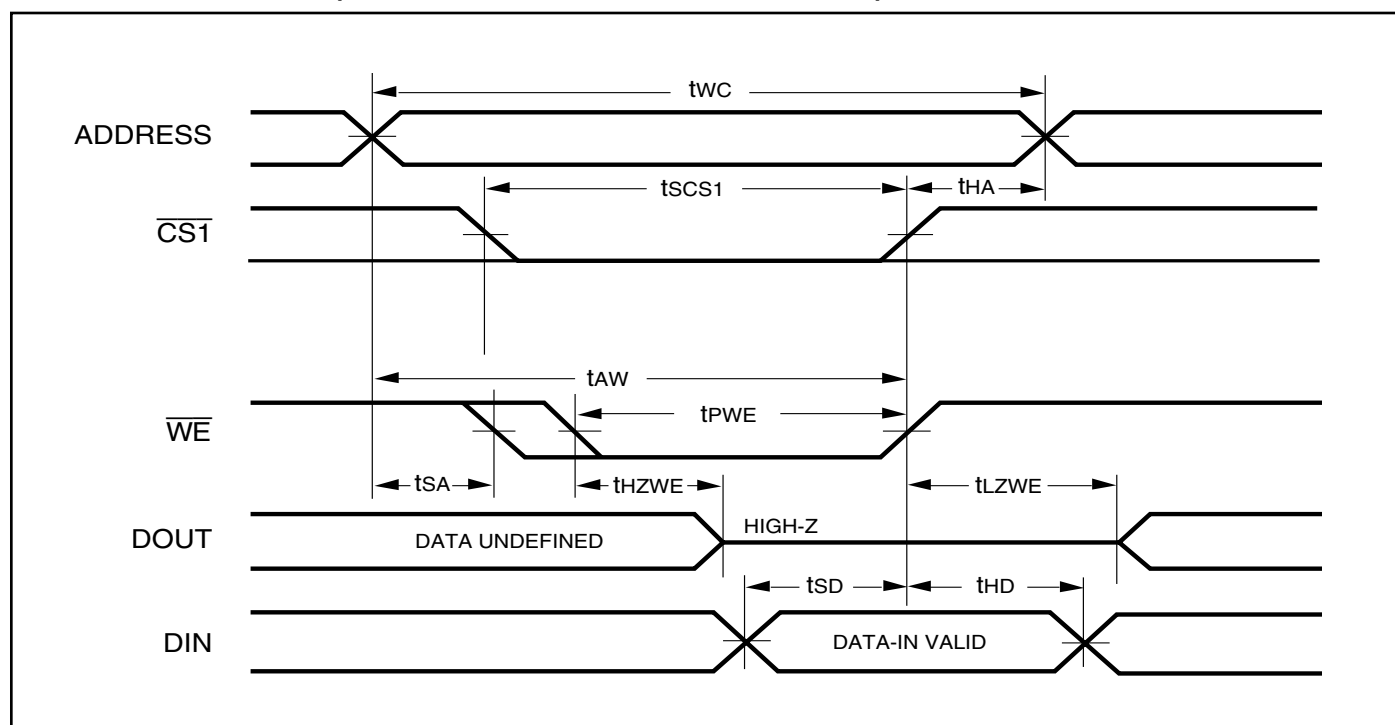
1. WE is HIGH for a Read Cycle.
2. The device is continuously selected. OE, CS1 =  $V_{IL}$ . WE =  $V_{IH}$ .
3. Address is valid prior to or coincident with CS1 LOW transition.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup> (Over Operating Range)**

| Symbol                           | Parameter                       | 55 ns |      | 70 ns |      | Unit |
|----------------------------------|---------------------------------|-------|------|-------|------|------|
|                                  |                                 | Min.  | Max. | Min.  | Max. |      |
| t <sub>WC</sub>                  | Write Cycle Time                | 55    | —    | 70    | —    | ns   |
| t <sub>SCS1</sub>                | CS1 to Write End                | 45    | —    | 60    | —    | ns   |
| t <sub>AW</sub>                  | Address Setup Time to Write End | 45    | —    | 60    | —    | ns   |
| t <sub>HA</sub>                  | Address Hold from Write End     | 0     | —    | 0     | —    | ns   |
| t <sub>SA</sub>                  | Address Setup Time              | 0     | —    | 0     | —    | ns   |
| t <sub>PWE</sub>                 | WE Pulse Width                  | 40    | —    | 50    | —    | ns   |
| t <sub>SD</sub>                  | Data Setup to Write End         | 25    | —    | 30    | —    | ns   |
| t <sub>HD</sub>                  | Data Hold from Write End        | 0     | —    | 0     | —    | ns   |
| t <sub>HZWE</sub> <sup>(3)</sup> | WE LOW to High-Z Output         | —     | 20   | —     | 20   | ns   |
| t <sub>LZWE</sub> <sup>(3)</sup> | WE HIGH to Low-Z Output         | 5     | —    | 5     | —    | ns   |

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4V to V<sub>DD</sub>-0.2V/V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of CS1 LOW and WE LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

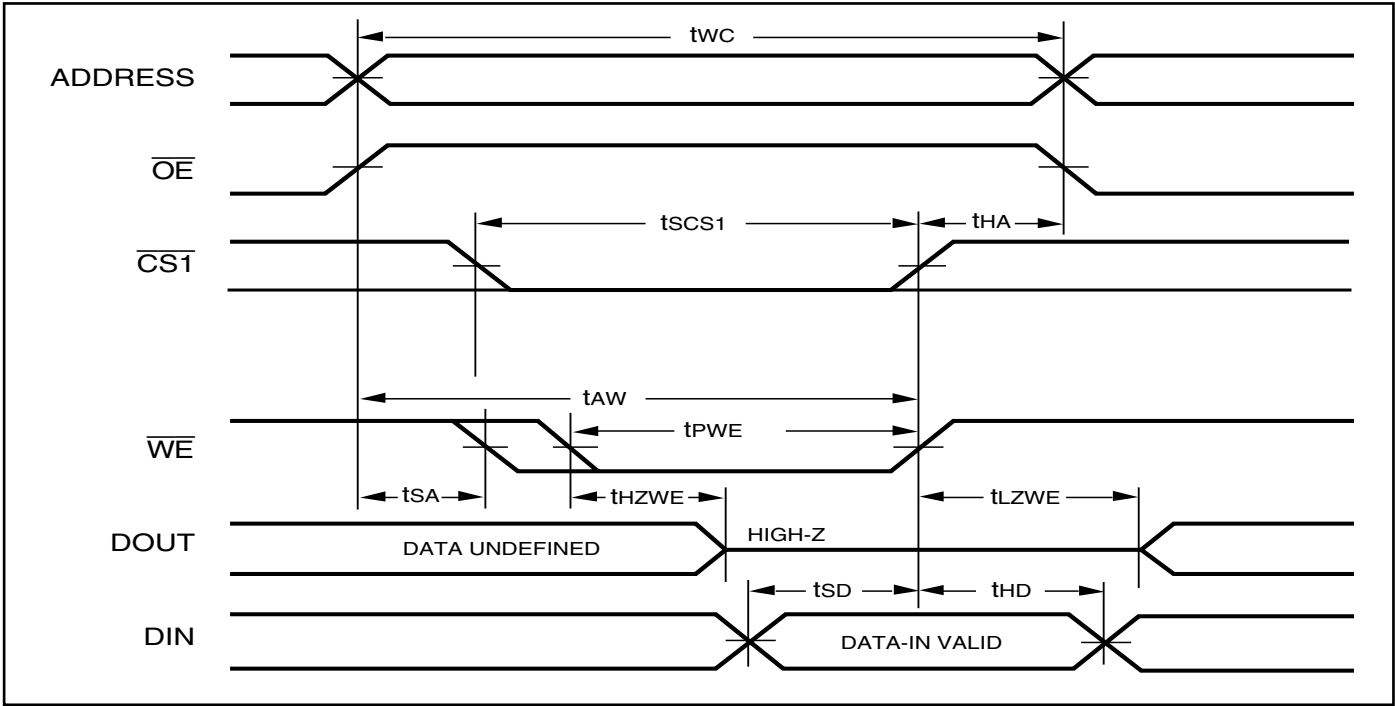
**AC WAVEFORMS****WRITE CYCLE NO. 1 (CS1 Controlled, OE = HIGH or LOW)**



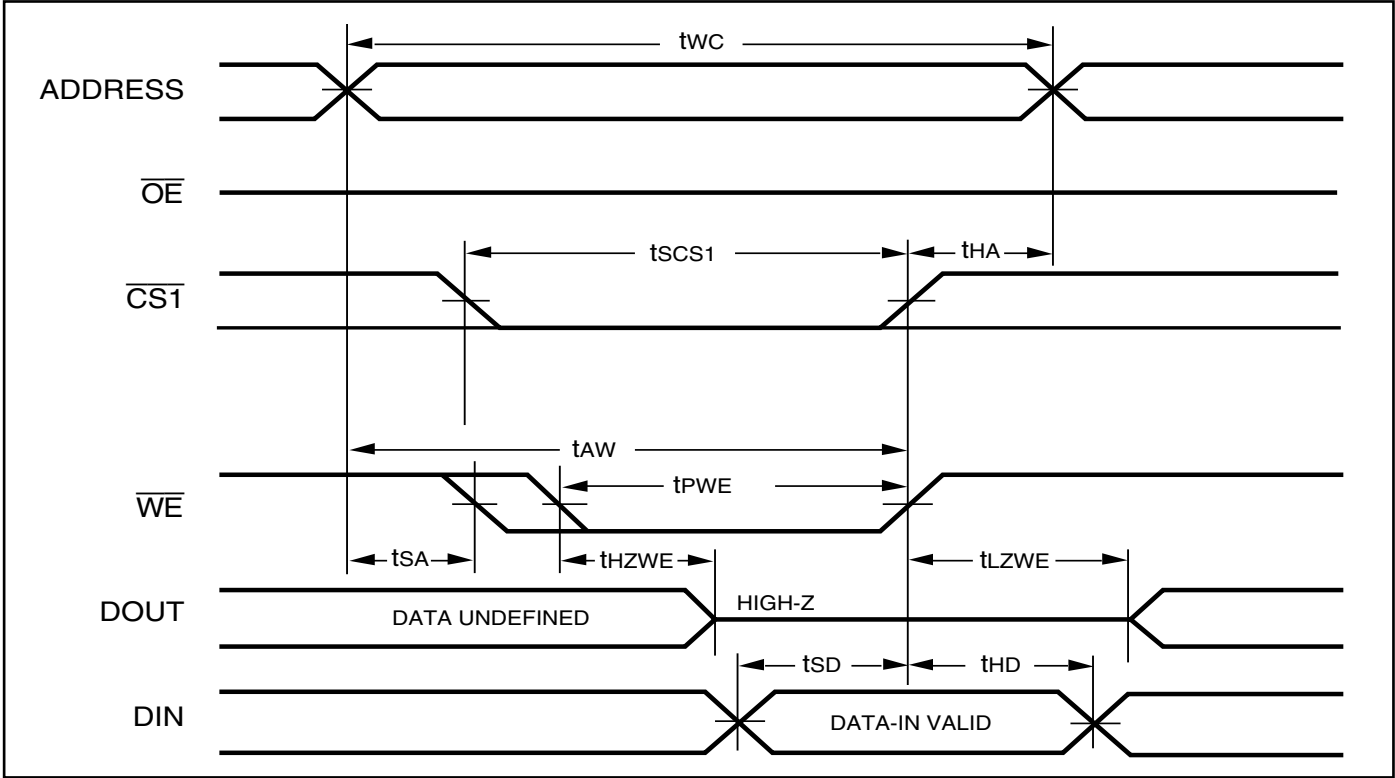


IS62WV5128ALL, IS62WV5128BLL

WRITE CYCLE NO. 2 (WE Controlled: OE is HIGH During Write Cycle)

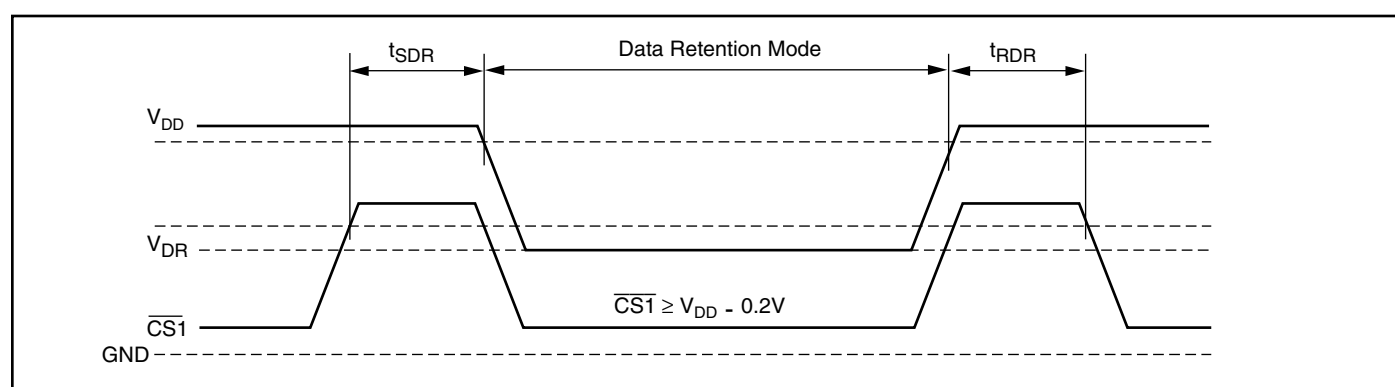


WRITE CYCLE NO. 3 (WE Controlled: OE is LOW During Write Cycle)



**DATA RETENTION SWITCHING CHARACTERISTICS**

| Symbol           | Parameter                          | Test Condition                                       | Min.            | Max. | Unit |
|------------------|------------------------------------|------------------------------------------------------|-----------------|------|------|
| V <sub>DR</sub>  | V <sub>DD</sub> for Data Retention | See Data Retention Waveform                          | 1.2             | 3.6  | V    |
| I <sub>DR</sub>  | Data Retention Current             | V <sub>DD</sub> = 1.2V, CS1 ≥ V <sub>DD</sub> - 0.2V | —               | 15   | μA   |
| t <sub>SDR</sub> | Data Retention Setup Time          | See Data Retention Waveform                          | 0               | —    | ns   |
| t <sub>RDR</sub> | Recovery Time                      | See Data Retention Waveform                          | t <sub>RC</sub> | —    | ns   |

**DATA RETENTION WAVEFORM (CS1 Controlled)**



## IS62WV5128ALL, IS62WV5128BLL

### ORDERING INFORMATION

IS62WV5128ALL (1.65V-2.2V)

Industrial Range: -40°C to +85°C

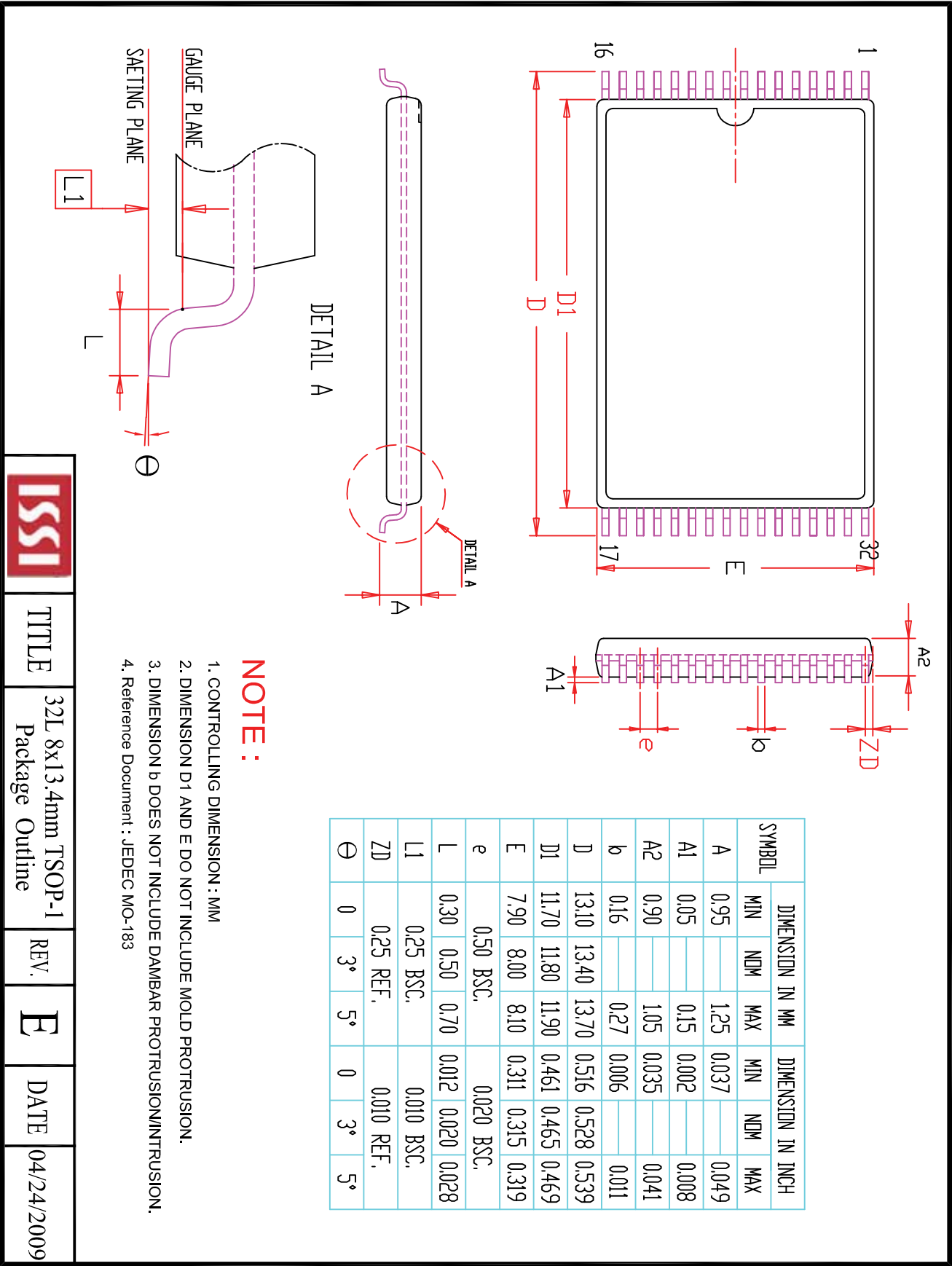
| Speed (ns) | Order Part No.     | Package            |
|------------|--------------------|--------------------|
| 70         | IS62WV5128ALL-70BI | mini BGA (6mmx8mm) |

### ORDERING INFORMATION

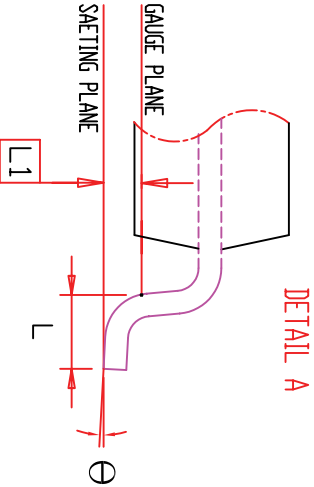
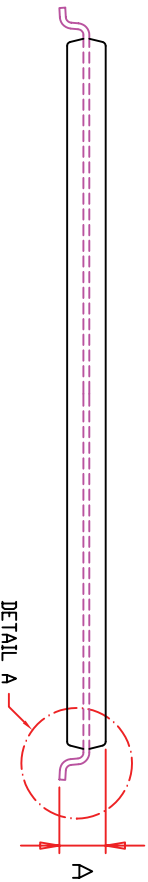
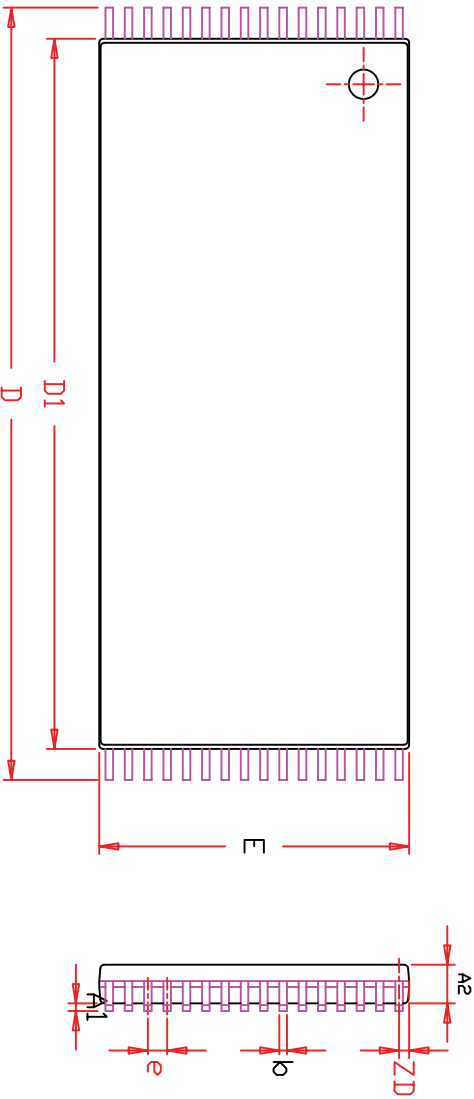
IS62WV5128BLL (2.5V - 3.6V)

Industrial Range: -40°C to +85°C

| Speed (ns) | Order Part No.       | Package                       |
|------------|----------------------|-------------------------------|
| 55         | IS62WV5128BLL-55TLI  | TSOP, TYPE I, Lead-free       |
| 55         | IS62WV5128BLL-55QLI  | SOP, Lead-free                |
| 55         | IS62WV5128BLL-55T2LI | TSOP, TYPE II, Lead-free      |
| 55         | IS62WV5128BLL-55HLI  | sTSOP, TYPE I, Lead-free      |
| 55         | IS62WV5128BLL-55BI   | mini BGA (6mmx8mm)            |
| 55         | IS62WV5128BLL-55BLI  | mini BGA (6mmx8mm), Lead-free |



**IS62WV5128ALL, IS62WV5128BLL**

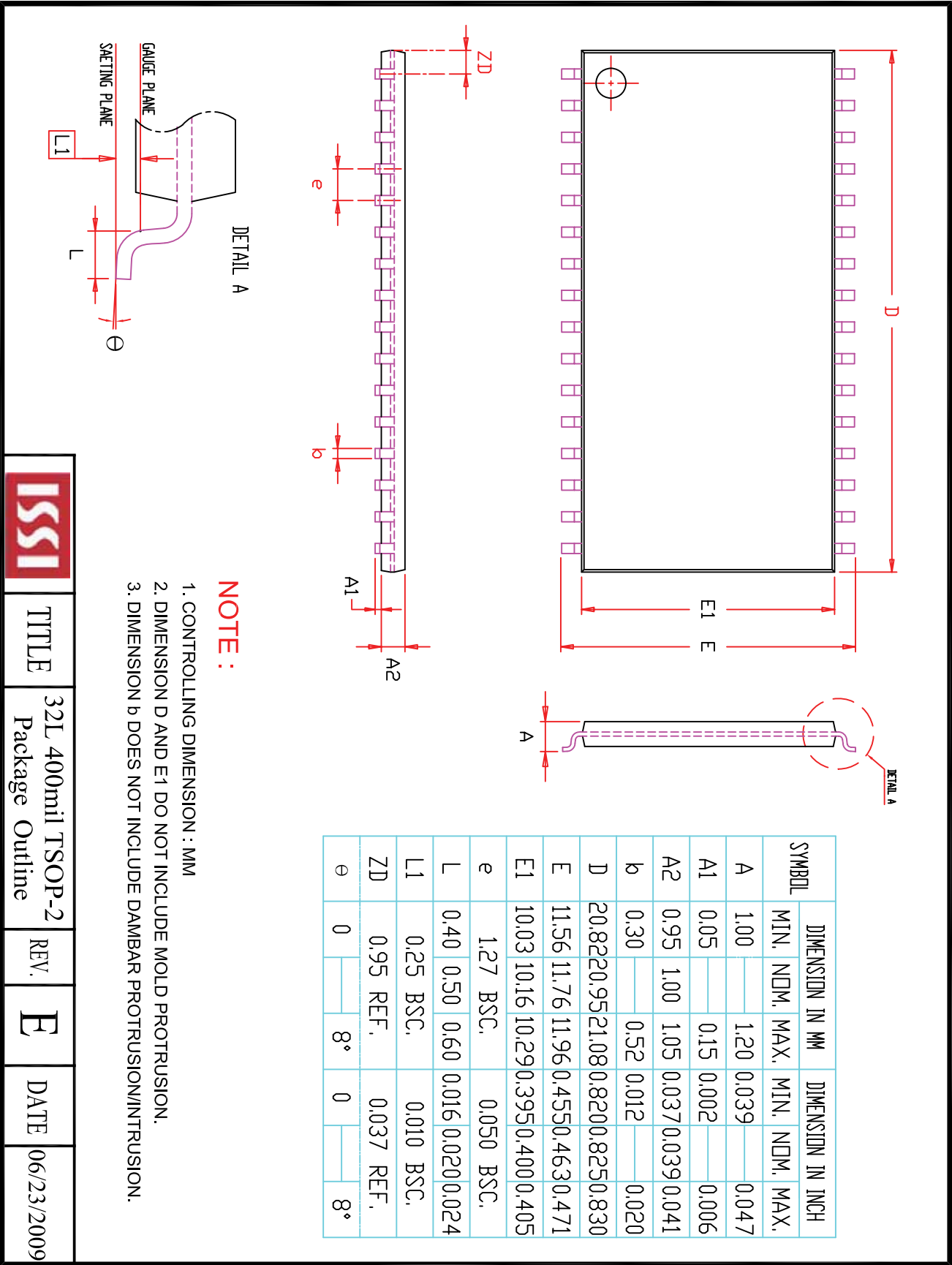


| SYMBOL | DIMENSION IN MM |           |       |
|--------|-----------------|-----------|-------|
|        | MIN             | NOM       | MAX   |
| A      | 1.00            |           | 1.20  |
| A1     | 0.05            |           | 0.20  |
| A2     | 0.95            | 1.00      | 1.05  |
| b      | 0.17            |           | 0.27  |
| D      | 19.80           | 20.00     | 20.20 |
| D1     | 18.30           | 18.40     | 18.50 |
| E      | 7.80            | 8.00      | 8.20  |
| e      |                 | 0.50 BSC. |       |
| L      | 0.40            |           | 0.70  |
| L1     |                 | 0.25 BSC. |       |
| Θ      | 0               | 5°        | 8°    |

**NOTE :**

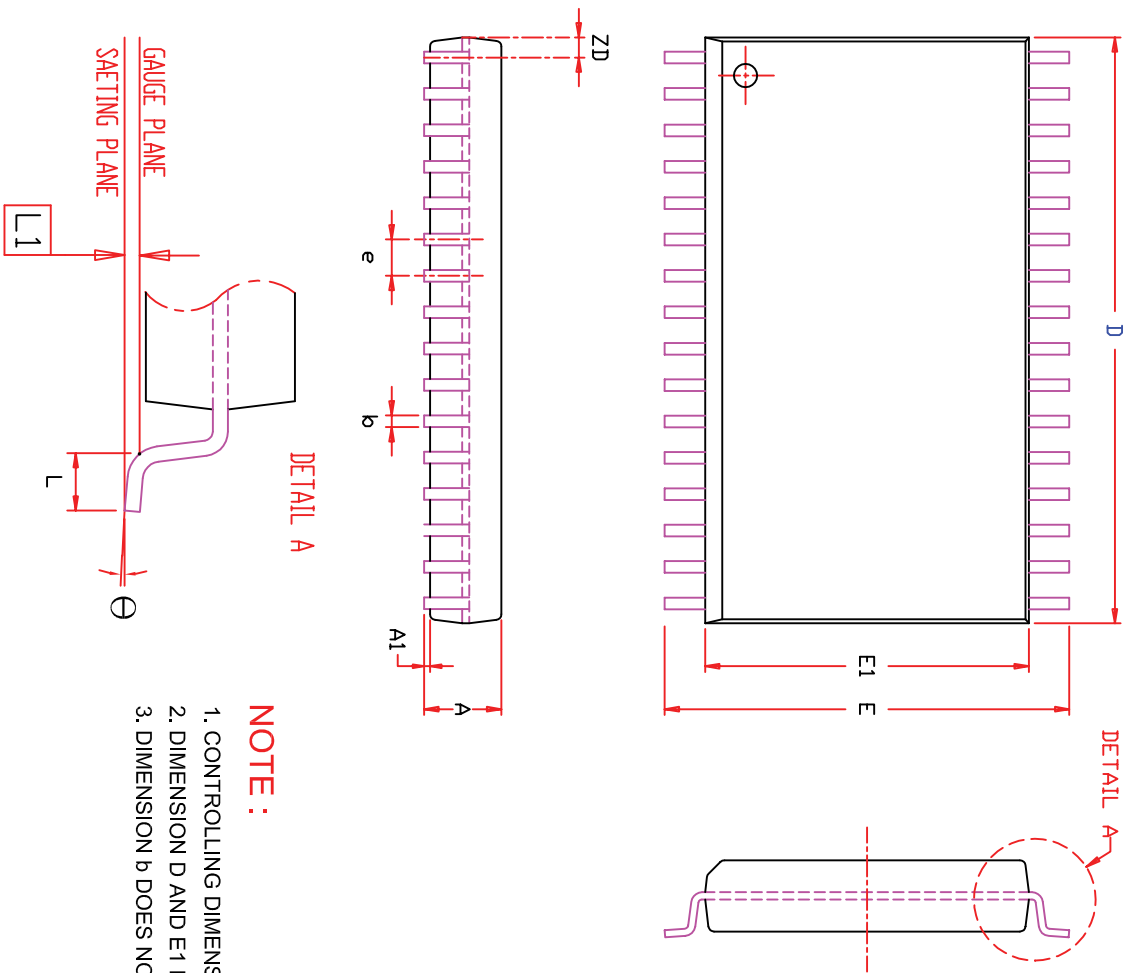
1. Controlling dimension : mm
2. Dimension D1 adn E do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

|       |                                      |      |   |            |
|-------|--------------------------------------|------|---|------------|
| ISSI® | TITLE                                | REV. | E | DATE       |
|       | 32L 8x20mm TSOP-1<br>Package Outline |      |   | 06/08/2006 |





IS62WV5128ALL, IS62WV5128BLL



| SYMBOL | DIMENSION IN MM |      |             | DIMENSION IN INCH |      |       |
|--------|-----------------|------|-------------|-------------------|------|-------|
|        | MIN.            | NOM. | MAX.        | MIN.              | NOM. | MAX.  |
| A      | 2.62            |      | 3.05        | 0.103             |      | 0.120 |
| A1     | 0.05            |      | 0.30        | 0.002             |      | 0.012 |
| b      | 0.33            |      | 0.51        | 0.013             |      | 0.020 |
| D      | 20.24           |      | 20.750.797  |                   |      | 0.817 |
| E      | 13.79           |      | 14.450.543  |                   |      | 0.569 |
| E1     | 11.18           |      | 11.43 0.440 |                   |      | 0.450 |
| e      | 1.27            | BSC. |             | 0.050             | BSC. |       |
| L      | 0.38            |      | 1.27        | 0.015             |      | 0.050 |
| L1     | 0.25            | BSC. |             | 0.010             | BSC. |       |
| ZD     | 0.725           | REF. |             | 0.029             | REF. |       |
| theta  | 0               |      | 8°          | 0                 |      | 8°    |

NOTE:

- 1. CONTROLLING DIMENSION : MM
- 2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
- 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

|      |       |                                   |      |   |      |            |
|------|-------|-----------------------------------|------|---|------|------------|
| ISSI | TITLE | 32L 450mil SOP<br>Package Outline | REV. | F | DATE | 09/23/2013 |
|------|-------|-----------------------------------|------|---|------|------------|

