12 Bit A/D Converter With 3-State Binary Outputs

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (GND to V^+) ..... +6.2V
Negative Supply Voltage (GND to V^-) ..... -9V
Analog Input Voltage (Lo or Hi) (Note 1) ..... V^+ to V^-
Reference Input Voltage (Lo or Hi) (Note 1) .. V^+ to V^-
Digital Input Voltage
(Pins 2-27) (Note 2) .... GND - 0.3V ≤ V_{IN} ≤ V^+ + 0.3V
Power Dissipation (Note 3)
Cerdip Package ..... 1W @ +85°C
Plastic Package ..... 500mW @ +70°C
Plastic Chip Carrier (Quad) ..... 400mW @ +70°C

Operating Temperature
Cerdip Package (MJL) ..... -55°C ≤ T_A ≤ +125°C
Cerdip Package (CJL) ..... -20°C ≤ T_A ≤ +85°C
Plastic Package (CPL) ..... 0°C ≤ T_A ≤ +70°C
Plastic Chip Carrier
(Quad) Package (Q) ..... 0°C ≤ T_A ≤ 70°C
Storage Temperature ..... -65°C ≤ T_A ≤ +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(All parameters with V^+ = +5V, V^- = -5V, GND = 0V, T_A = 25°C, unless noted.)

ANALOG SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading		V_{IN} = 0.0V Full Scale = 409.6mV	-0000_8	$\pm0000_8$	$+0000_8$	Octal Reading
Ratiometric Reading		V_{IN} = V_{REF} V_{REF} = 204.8mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
Non-Linearity (Max deviation from best straight line fit)		Full Scale = 409.6mV to 4.096V Over full operating temperature range.	1	±.2	+1	Counts
Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale)		Full Scale = 409.6mV to 4.096V Over full operating temperature range.	-1	±.2	+1	Counts
Common Mode Rejection Ratio	CMRR	V_{CM} ±1V, V_{IN} = 0V Full Scale = 409.6mV		50		μV/V
Input Common Mode Range	VCMR	Input Hi, Input Low, Common	V^- +1.5		V^+ -1.5	V
Noise (p-p value not exceeded 95% of time)	e_n	V_{IN} = 0V Full Scale = 409.6mV		15		μV
Leakage current at Input	I_{ILK}	V_{IN} = 0 All devices 25°C ICL7109CPL 0°C ≤ T_A ≤ +70°C ICL7109IDC -25°C ≤ T_A ≤ +85°C ICL7109MDL -55°C ≤ T_A ≤ +125°C		1 20 100 2	10 100 250 5	pA pA pA nA
Zero Reading Drift		V_{IN} = 0V		0.2	1	μV/°C
Scale Factor Temperature Coefficient		V_{IN} = 408.9mV = > 7770_8 reading Ext. Ref. 0 ppm/°C		1	5	ppm/°C
Supply Current V^+ to GND	I^+	V_{IN} = 0, Crystal Osc. 3.58MHz test circuit Pins 2-21, 25, 26, 27, 29, open		700	1500	μA
Supply Current V^+ to V^-	I_{SUPP}			700	1500	μA
Ref Out Voltage	V_{REF}	Referred to V^+, 25kΩ between V^+ and REF OUT	-2.4	-2.8	-3.2	V
Ref Out Temp. Coefficient		25kΩ between V^+ and REF OUT		80		ppm/°C
Input Common Mode Range	V_{CM}	IN HI, IN LO, COMMON	V^- +1.5	V^+ -0.5 to V^- +1.0	V^+ -1.0	V

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100 μA.

Note 2: Due to the SCR structure inherent in the process used to fabricate these devices, connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources other than the same power supply be applied to the ICL7109 before its power supply is established, and that in multiple supply systems the supply to the ICL7109 be activated first.

Note 3: This limit refers to that of the package and will not be obtained during normal operation.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

12 Bit A/D Converter With 3-State Binary Outputs

- **Zero Integrator Phase ensures fast overload recovery**
- **"Crosstalk" and Hysteresis Eliminated**
- **Bus Driving Capability Enhanced**
- **Maxim Quality and Reliability**
- **Significantly Improved ESD Protection (Note 4)**

ABSOLUTE MAXIMUM RATINGS

This device conforms to the Absolute Maximum Ratings on the adjacent page.

ELECTRICAL CHARACTERISTICS

(V^+ = +5V, V^- = -5V, GND = 0V, T_A = 25°C; Test Circuit Figure 1; unless noted.)

ANALOG SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Overload Recovery Time				**0**	**1**	**Measurement Cycles**
Zero Input Reading		V_{IN} = 0.0V Full Scale = 409.6mV	-0000_8	$\pm 0000_8$	$+0000_8$	Octal Reading
Ratiometric Reading		$V_{IN} = V_{REF}$ V_{REF} = 204.8mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
Non-Linearity (Max deviation from best straight line fit)		Full Scale = 409.6mV to 2.048V Over full operating temperature range. (Note 5)	-1	±.2	+1	Counts
Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale)		Full Scale = 409.6mV to 2.048V Over full operating temperature range (Note 5)	-1	±.2	+1	Counts
Common Mode Rejection Ratio	CMRR	V_{CM} ±1V, V_{IN} = 0V Full Scale = 409.6mV		50		µV/V
Input Common Mode Range	V_{CMR}	Input Hi, Input Low, Common	V^- +1.5		V^+-1.5	V
Noise (p-p value not exceeded 95% of time)	e_n	V_{IN} = 0V Full Scale = 409.6mV		15		µV
Leakage Current at Input	I_{ILK}	V_{IN} = 0V All devices, T_A = 25°C ICL7109CPL CQ 0°C ≤ T_A ≤ +70°C ICL7109IJL -20°C ≤ T_A ≤ +85°C ICL7109MJL -55°C ≤ T_A ≤ +125°C		1 20 100 2	10 100 250 5	pA pA pA nA
Zero Reading Drift		V_{IN} = 0V		0.2	1	µV/°C
Scale Factor Temperature Coefficient		V_{IN} = 408.9mV = 7770_8 reading Ext. Ref. 0 ppm/°C		1	5	ppm/°C
Supply Current V^+ to GND	I^+	V_{IN} = 0, Crystal Osc. 3.58MHz test circuit Pins 2-21, 25, 26, 27, 29 open		700	1500	µA
Supply Current V^+ to V^-	I_{SUPP}			700	1500	µA
Ref Out Voltage	V_{REF}	Referred to V^+, 25kΩ between V^+ and REF OUT	-2.4	-2.8	-3.2	V
Ref Out Temp. Coefficient		25kΩ between V^+ and REF OUT		80		ppm/°C

Note 4: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (test circuit per Mil Std 883, Method 3015.1).

Note 5: A 4.096V full scale voltage exceeds the Common Mode Voltage Range of the device. The full scale voltage has therefore been changed to 2.048V.

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ELECTRICAL CHARACTERISTICS

(All parameters with V^+ = +5V, V^- = -5V, GND = 0V, T_A = 25°C, unless noted.)

DIGITAL SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}	I_{OUT} = 100μA Pins 2-16, 18, 19, 20	3.5	4.3		V
Output Low Voltage	V_{OL}	I_{OUT} = 1.6mA		0.2	0.4	V
Output Leakage Current		Pins 3-16 high impedance		±.01	±1	μA
Control I/O Pullup Current		Pins 18, 19, 20 V_{OUT} = V^+ -3V MODE input at GND		5		μA
Control I/O Loading		HBEN Pin 19 LBEN Pin 18			50	pF
Input High Voltage	V_{IH}	Pins 18-21, 26, 27 referred to GND	2.5			V
Input Low Voltage	V_{IL}	Pins 18-21, 26, 27 referred to GND			1	V
Input Pull-up Current		Pins 26, 27 V_{OUT} = V^+ -3V		5		μV
Input Pull-up Current		Pins 17, 24 V_{OUT} = V^+ -3V		25		μA
Input Pull-down Current		Pin 21 V_{OUT} = GND +3V		5		μA
Oscillator Output Current	High O_{OH}	V_{OUT} = 2.5V		1		mA
	Low O_{OL}	V_{OUT} = 2.5V		1.5		mA
Buffered Oscillator Output Current	High BO_{OH}	V_{OUT} = 2.5V		2		mA
	Low BO_{OL}	V_{OUT} = 2.5V		5		mA
MODE Input Pulse Width	t_W		50			ns

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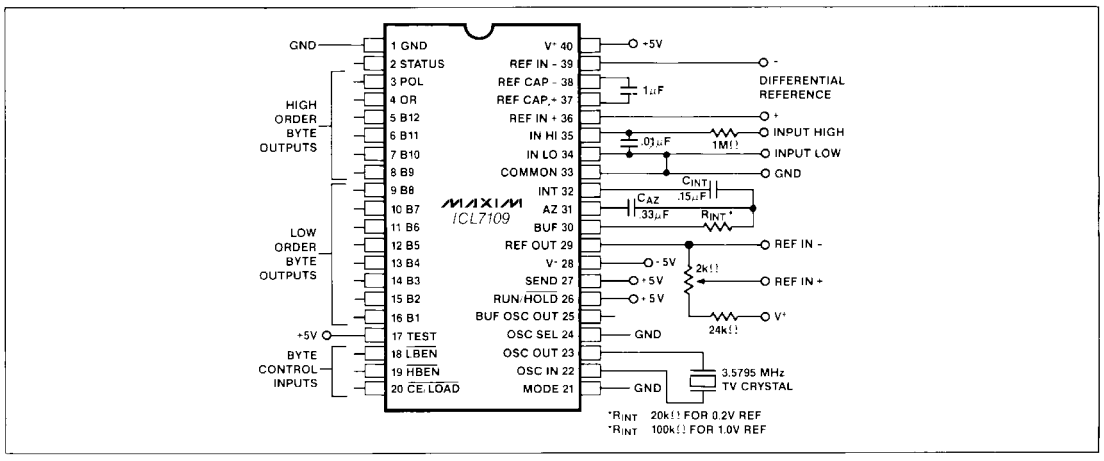

Figure 1. ICL7109 Test Circuit

ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page. (V^+ = +5V, V^- = -5V, GND = 0V, T_A = 25°C, unless noted.)

DIGITAL SECTION

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage		**V_{OH}**	**Pins 2-16, 18-20. I_{OUT} = 1mA** **I_{OUT} = 100µA**	**3.5** **4.0**	**4.3** **4.5**		**V** **V**
Output Low Voltage		V_{OL}	I_{OUT} = -1.6mA		0.2	0.4	V
Output Leakage Current			Pins 3-16 high impedance		±.01	±1	µA
Control I/O Pullup Current			**Pins 18, 19, 20 V_{OUT} = V^- -3V** **MODE input at GND**	**2**	**5**	**20**	**µA**
Control I/O Loading			HBEN Pin 19, LBEN Pin 18			50	pF
Input High Voltage		V_{IH}	Pins18-21, 26, 27 referred to GND	2.5			V
Input Low Voltage		V_{IL}	Pins 18-21, 26, 27 referred to GND			1	V
Input Pull-up Current			**Pins 26, 27 V_{OUT} = V^+ -3V**	**2**	**5**	**20**	**µA**
Input Pull-up Current			**Pins 17, 24 V_{OUT} = V^+ -3V**	**5**	**100**	**300**	**µA**
Input Pull-down Current			**Pin 21 V_{OUT} = GND +3V**	**2**	**5**	**20**	**µA**
Oscillator Output Current	**High**	**O_{OH}**	**V_{OUT} = 2.5V**	**1**	**2**		**mA**
	Low	**O_{OL}**	**V_{OUT} = 2.5V**	**1.5**	**3**		**mA**
Buffered Oscillator Output Current	**High**	**BO_{OH}**	**V_{OUT} = 2.5V**	**2**	**4**		**mA**
	Low	**BO_{OL}**	**V_{OUT} = 2.5V**	**5**	**10**		**mA**
MODE Input Pulse Width		t_W	(Note 6)	50			ns
Byte Enable Width		t_{BEA}	(Note 6)	350	100		ns
Data Access Time from Byte Enable		t_{DAB}	(Note 6)		150	350	ns
Data Hold Time from Byte Enable		t_{DHB}	(Note 6)		100	300	ns
Chip Enable Width		t_{CEA}	(Note 6)	400	120		ns
Data Access Time from Chip Enable		t_{DAC}	(Note 6)		175	400	ns
Data Hold Time from Chip Enable		t_{DHC}	(Note 6)		150	400	ns

Note 6: Guaranteed by design; sample tested only.

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Table 1. PIN FUNCTIONS

PIN	FUNCTION	TYPE	DESCRIPTION
1	GND		Ground return for digital logic, 0V
2	STATUS	Output	HI = Converter in integrate phase, or deintegrate phase until data is latched LO = Converter in zero-integrator phase, auto-zero phase, or deintegrate phase after data is latched.
3	POL	Three state data output bits	Polarity — HI = Positive input.
4	OR		Overrange — HI = Overranged
5	B12		Bit 12 = Most significant bit
6	B11		Bit 11
7	B10		Bit 10
8	B9		Bit 9
9	B8		Bit 8
10	B7		Bit 7
11	B6		Bit 6
12	B5		Bit 5
13	B4		Bit 4
14	B3		Bit 3
15	B2		Bit 2
16	B1		Bit 1 = Least significant bit.
17	TEST	Input	HI = Normal operation LO = All output bits high. MID = Counter output latches enabled. Connect to +5V if not used.
18	$\overline{LBEN}$	Input Output	Low Byte Enable. When MODE is low and $\overline{CE/LOAD}$ is low, taking Low Byte Enable low activates low order byte outputs B1-B8. In handshake mode (when MODE is HI) this pin becomes a low byte flag output.
19	$\overline{HBEN}$	Input Output	High Byte Enable. When MODE is low and $\overline{CE/LOAD}$ is low, taking High Byte Enable low activates high order byte outputs B9-B12, POL & OR. In handshake mode (when MODE is HI) this pin becomes a high byte flag output.
20	$\overline{CE/LOAD}$	Input Output	When MODE is low, taking Chip Enable/Load high disables B1-B12, POL & OR. Taking it low enables B1-B12, POL & OR if $\overline{HBEN}$ and $\overline{LBEN}$ are low. In handshake mode (when MODE is HI) this pin becomes a load strobe output.
21	MODE	Input	LO = Converter in direct output mode. Makes $\overline{LBEN}$, $\overline{HBEN}$ & $\overline{CE/LOAD}$ act as inputs controlling byte outputs directly. HI = Converter in handshake mode. Makes $\overline{LBEN}$, $\overline{HBEN}$ & $\overline{CE/LOAD}$ act as outputs.
22	OSC IN	Input	Oscillator input.
23	OSC OUT	Output	Oscillator output.
24	OSC SEL	Input	Taking Oscillator Select high or leaving it open configures OSC IN, OSC OUT & BUF OSC OUT as an RC oscillator. Clock frequency = BUF OSC OUT frequency. Taking it low configures OSC IN & OSC OUT for crystal oscillators. Clock frequency = BUF OSC OUT frequency ÷ 58.
25	BUF OSC OUT	Output	Buffered Oscillator Output
26	RUN/$\overline{HOLD}$	Input	HI = Continuous conversions every 8192 clock pulses. LO = Converter stops in auto-zero after completing the conversion in progress.
27	SEND	Input	Indicates ability of external device to accept data when converter is in handshake mode. Connect to +5V if not used.
28	V^-		Negative supply. Nominally -5V from GND.
29	REF OUT	Output	Reference voltage output. Nominally 2.8V below V^+.
30	BUFFER	Output	Buffer Amplifier Output.
31	AUTO-ZERO		Inside foil of C_{AZ} connects here.
32	INTEGRATOR	Output	Outside foil of C_{INT} connects here.
33	COMMON		Analog Common.
34	INPUT LO		Low side of differential input.
35	INPUT HI		High side of differential input.
36	REF IN$^-$		Positive input of differential reference.
37	REF CAP$^-$		Positive side of reference capacitor.
38	REF CAP$^-$		Negative side of reference capacitor.
39	REF IN$^-$		Negative input of differential reference.
40	V^+	Input	Positive supply. Nominally +5V from GND.

Note: All digital levels are positive true.

12 Bit A/D Converter With 3-State Binary Outputs

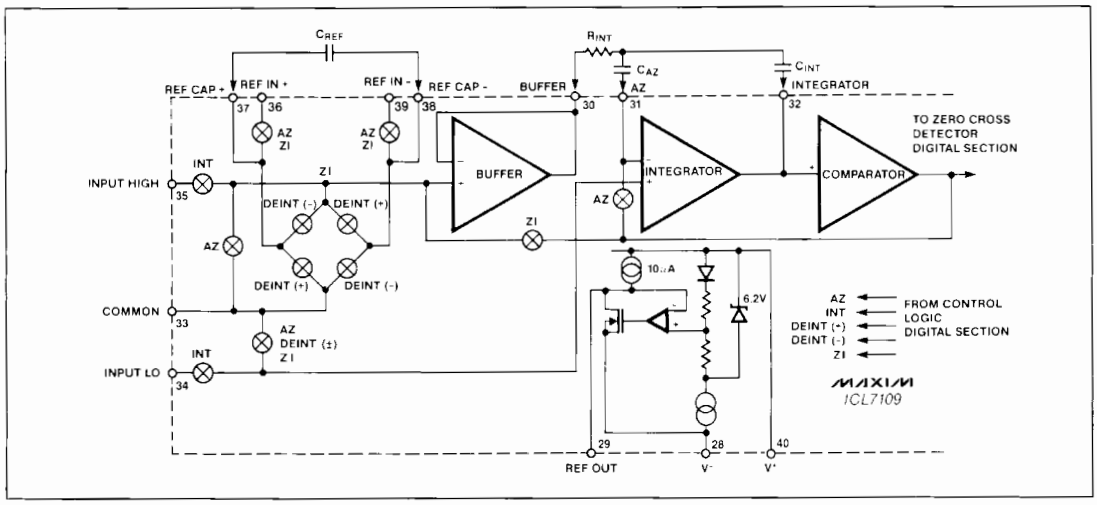

Figure 2. Analog Section

Detailed Description

Analog Section

The equivalent circuit of the Analog Section of the ICL7109 is shown in Figure 2. The circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle) when the RUN/$\overline{\text{HOLD}}$ input is left open or connected to V^+. Each measurement cycle is divided into four phases as shown in Figure 3. They are:

1. Auto-Zero (AZ)
2. Signal Integrate (INT)
3. De-integrate (DE)
4. Zero Integrator (ZI)

Auto-Zero Phase

Three events occur during Auto-zero. The inputs, In-Hi and In-Lo, are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. Lastly, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the comparator, buffer amplifier and integrator. The inherent noise of the system determines the A-Z accuracy. In any event, the offset referred to the input is less than 10 μV.

Signal Integrate Phase

The internal input high (In-Hi) and input low (In-Lo) are connected to the external pins, the internal short is removed and the auto-zero loop is opened. The converter then integrates the differential voltage between In-Hi and In-Lo for a fixed time of 2048 clock periods. Note that this differential voltage must be within the common mode range of the inputs. The polarity of the integrated signal is determined at the end of this phase.

De-integrate Phase

The third phase is De-integrate, also known as reference integrate. Input high is internally connected across the previously charged reference capacitor and input low is internally connected to analog Common. The polarity detection circuit connects the reference capacitor with the polarity such that the integrator output returns with a fixed slope to the zero level established in the Auto-Zero phase. The time required for the output to return to zero (represented by the number of clock periods counted) is proportional to the input signal.

Zero Integrator Phase

Input low is shorted to analog Common and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return rapidly to zero (See Figure 3). This phase normally lasts between 16 and 32 clock pulses but is extended to 1552 clock pulses after an overrange conversion.

This phase will remove any residual charge left on the integrator capacitor after an overload reading. This Zero Integrator phase virtually eliminates the problem of interaction or "crosstalk" between the various channels of a Maxim ICL7109 based multiple channel data acquisition system. Without the zero integrator phase, an overload on one channel would leave charge on the integrator capacitor, which would then be transferred to the autozero capacitor during the autozero cycle, resulting in an erroneous reading for the next channel that is measured after the channel with the overload.

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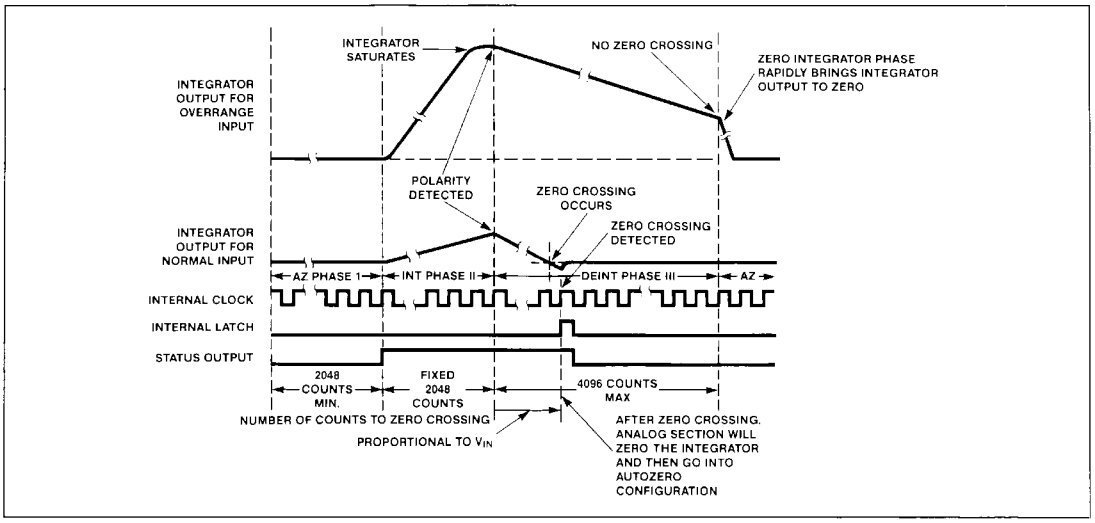

Figure 3. Conversion Timing (RUN/$\overline{HOLD}$ Pin High)

Differential Input

Differential input voltages anywhere within the common-mode range of the input amplifier can be accepted (specifically from 1.5V below the positive supply to 1.5V above the negative supply). The system has a CMRR of 86dB typical in this range. For optimum performance the input voltage at In-Lo and In-Hi should not come within 2 volts of either the positive or negative supply. Care must be exercised to ensure that the integrator output does not saturate, since the integrator also swings with the common-mode voltage. A large positive common-mode voltage with a near full-scale negative differential input voltage is a worst-case condition. When most of the swing has been used up by the positive common-mode voltage, the negative input signal drives the integrator positive. The integrator output swing can be reduced to less than the recommended 4V full-scale swing with little loss of accuracy in these critical applications. The integrator output can swing within 0.3V of either supply without loss of linearity.

The ICL7109 has been optimized for operation with analog common near digital ground. This allows for a 4V full scale integrator swing positive or negative which maximizes performance of the analog section with ±5V power supplies.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll over voltage. This is caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. The reference capacitor can gain charge (increase voltage) if there is a large common-mode voltage. This is the result of a positive signal de-integration. In contrast, the reference capacitor will lose charge (decrease voltage) when de-integrating a negative input signal. Roll over error defines this difference in reference for positive or negative input voltages. This error can be held to less than one half count for worst-case condition by using an optimum reference capacitor. (See component value selection.)

By having the reference common mode voltage near or at analog COMMON, the roll-over error from these sources is minimized.

Component Value Selection

Care must be exercised in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate for optimum performance of the analog section. The optimum values must be selected for each application.

Integrating Resistor

Both the integrator and buffer amplifier have a class A output stage with a quiescent current of 100 μA, which can supply 20 μA with negligible non-linearity. The integrating resistor should be small enough that undue leakage requirements are not placed on the PC board, but large enough to keep the output current less than 40 μA. For 2.048 volt full scale, 100kΩ is optimum and similarly a 20kΩ is optimum for a 409.6mV scale. For other full scale voltages, R_{INT} should be selected by the relation

$$R_{INT} = \frac{\text{full scale voltage (mV)}}{20\ \mu A}\ k\Omega$$

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Integrating Capacitor

C_{INT} (the integrating capacitor) should be selected for maximum integrator output voltage swing without saturation of the integrator (at 0.3 volt from either supply). A ±3.5 to ±4 volt integrator output swing is ideal for the ICL7109 with a ±5 volt supplies and analog common connected to GND. Nominal values for C_{INT} and C_{AZ} are 0.15 μF and 0.33 μF, respectively, for 7½ conversions per second (61.44kHz clock frequency). These values should be changed to maintain the integrator output voltage swing, if different clock frequencies are used. The value of C_{INT} is generally given by

$$C_{INT} = \frac{(2048 \times \text{clock period})\ (20\ \mu A)}{\text{Integrator output voltage swing (V)}}\ \mu F$$

To prevent roll-over and linearity errors a low dielectric absorption capacitor is required. Polypropylene capacitors give undetectable errors at reasonable cost up to 85°C. Teflon™ capacitors are recommended for the military temperature range. Polypropylene and Teflon™ capacitors should give less than 0.5 count of error due to dielectric absorption even though their absorption characteristics vary somewhat from unit to unit.

Auto-Zero Capacitor

The Maxim ICL7109 has a zero integrator phase which ensures that any charge left on the integrator after an overrange reading is removed before the autozero phase is started. This zero integrator phase allows the use of larger values of autozero capacitors than allowed with other manufacturer's ICL7109s. Normally, the optimum value of the autozero capacitor is between 2 and 4 times the value of the integrator capacitor. The typical value of the autozero capacitor is 0.33 μF. Lower values of C_{AZ} increase the noise in the autozero loop; very large values will take a longer time to charge to the proper value after power-up.

The outer foil of C_{AZ} should be connected to the R_{INT}, C_{INT} summing junction and the inner foil to pin 31 for optimal rejection of stray pickup. Similarly, the inner foil of C_{INT} should be connected to the RC summing junction, and the outer foil of C_{INT} should be connected to pin 32. Above 85°C, Teflon™, or equivalent capacitors are recommended for their low leakage characteristics.

Reference Capacitor

Good results can be achieved in most applications with a 1 μF capacitor. A larger value is required to prevent roll-over error where a 409.6mV scale is used and a large common mode voltage exists (i.e., the reference low is not at analog common). The roll-over error can generally be held to one half count by 10 μF in this case. Above 85°C, Teflon™, or equivalent capacitors are again recommended for their low leakage characteristics.

Reference Voltage

An analog input of $V_{IN} = 2 \times V_{REF}$ generates a full scale output of 4096 counts. For a normalized scale, a reference of 204.8mV should be used for a 409.6mV full scale (100 μV per LSB), and 1.024V reference should be used for a 2.048V full scale (500 μV per LSB). There will exist a scale factor other than unity between the absolute output voltage to be measured and a desired digital output in many applications where the A/D is sensing the output of a transducer. In a weighing system, for example, the designer could possibly want a full scale reading when the voltage from the transducer is 0.682V. The input voltage should be measured directly and a reference voltage of 0.341V should be used instead of dividing the input down to 409.6mV. 34kΩ and 0.15 μF are suitable values for the integrating resistor and capacitor. A divider on the input is thus avoided. When a zero reading is desired for non-zero input, another advantage of this system is realized. Examples might include temperature and weight measurements with an offset or tare. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. It may be more efficient, however, to perform this type of scaling or tare subtraction digitally using software in processor-based systems using the ICL7109.

Reference Sources

A major factor in the overall absolute accuracy of the converter is the stability of the reference voltage. The resolution of the ICL7109 at 12 bits is 244 ppm or one part in 4096. Therefore, a temperature difference of 3°C will introduce a one-bit error if the reference has a temperature coefficient of 80 ppm/°C (like the onboard reference). Where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made, an external high quality reference should be used.

To generate a suitable reference voltage, the ICL7109 provides a REFerence OUTput (pin 29) which may be used with a resistive divider. This output will sink up to about 20mA without a significant output variation. A pullup bias device which sources about 10 μA is also provided. The output voltage is nominally 2.8V below V^+, and has a temperature coefficient of ±80 ppm/°C typical. REF^+ should be connected to the wiper of a precision potentiometer between REF OUT and V^+, and REF OUT (Pin 29) should be connected to REF^- (pin 39) when using the onboard reference. Shown in the test circuit is the circuit for a 204.8mV reference. The fixed resistor should be removed for a 1V reference, and a 25kΩ precision

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potentiometer between REF OUT and V+ should be used.

Note that if pins 29 and 39 are tied together and pins 39 and 40 accidentally shorted (e.g., during testing), the reference supply will sink sufficient current to destroy the device. By placing a 1kΩ resistor in series with pin 39, this can be avoided.

Detailed Description

Digital Section

The digital section (Figure 4) includes: 1) the clock oscillator and divider circuit; 2) a 12-bit binary counter with output latches and TTL-compatible three-state output drivers; 3) control logic; and 4) UART handshake logic.

Note: The term "clock cycles" as used in the following discussion relates to the internal clock, which is the oscillator output ÷ 58 when OSC SEL is low.

Three-State Outputs

The ICL7109 has 14 three-state outputs: 12 data bits, 1 polarity bit, and 1 overrange bit. These bits are enabled either by the $\overline{CE}$/LOAD, $\overline{LBEN}$ and $\overline{HBEN}$ control signals (see Table 2), or by entering the Handshake mode.

$\overline{CE}$/LOAD, $\overline{LBEN}$, and $\overline{HBEN}$

These three control pins can function as either inputs or outputs. In the Direct interface mode (see "Interfacing" below), these three pins are Chip Enable and Byte Enable inputs. In the Handshake mode these three pins become outputs that load data into the UART. These pins will be outputs while a handshake transfer is in progress or at any time that the Mode input is high.

Run/$\overline{Hold}$ Input

When the Run/$\overline{Hold}$ input is tied high, the ICL7109 continuously performs A/D conversions with a fixed length of 8192 clock cycles per conversion. When Run/$\overline{Hold}$ is taken low, the ICL7109 will complete the conversion in progress, then wait in the autozero phase. After the minimum autozero time has been completed, a high-going pulse on Run/$\overline{Hold}$ of at least 200 nanoseconds is required to start a new conversion; but any pulses during a conversion or up to 2048 clock cycles after Status goes low will be ignored. If the ICL7109 is holding at the end of the autozero phase, a new conversion will start and Status will go high within 7 clock cycles after Run/$\overline{Hold}$ goes high.

In addition to starting and stopping conversions, the Run/$\overline{Hold}$ pin can also be used to minimize conversion time. If Run/Hold is high, each conversion takes a full 8192 clock cycles, with the De-integrate phase taking 4096 clock cycles independent of input voltage. On the other hand, if Run/$\overline{Hold}$ is low at any time after Status goes low, the ICL7109 immediately jumps to the Auto-Zero phase rather than taking a full 4096 clock cycles for De-integrate. A simple way to ensure minimum conversion time is to drive the Run/$\overline{Hold}$ input with the Buffered Oscillator Output. When this is done, the conversion time is dependent on the input voltage: 4096 clock cycles for a zero voltage input, rising to 8192 clock cycles for full scale or overrange inputs.

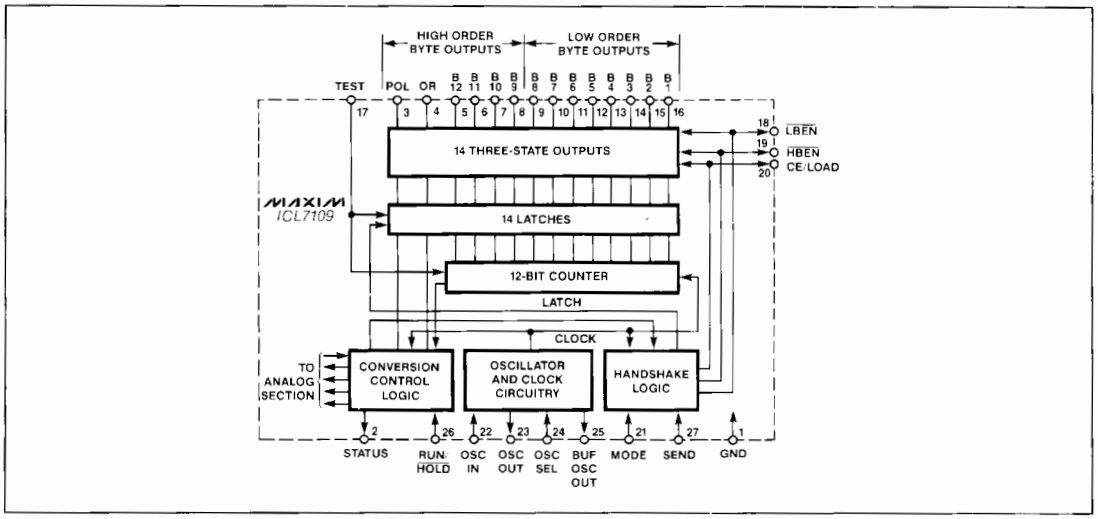


Figure 4. Digital Section

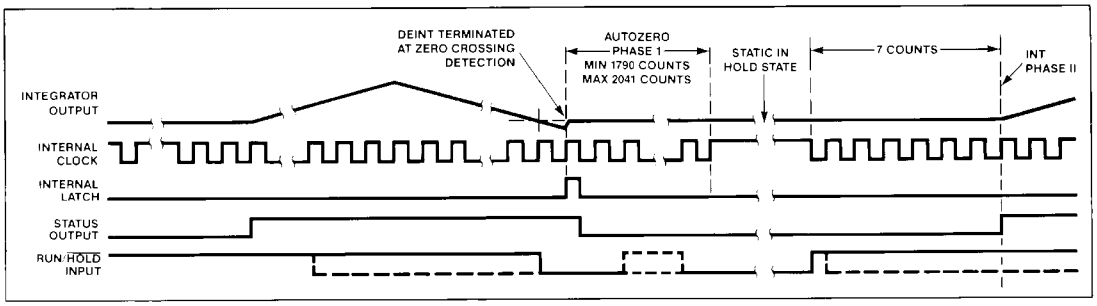


Figure 5. RUN/HOLD Operation

Mode Input

The Mode input is used to control the converter output mode. The converter is in its Direct output mode, where the output data is directly accessible under the control of the chip and byte enable inputs when the Mode pin is low or left open. (To ensure a low level when the pin is left open, this input is provided with an internal pulldown resistor.) When the Mode input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "Direct" mode. The converter will output data in the handshake mode at the end of every conversion cycle when the Mode input remains high. (See "Handshake Mode" section for more details.)

Send Input

The Send Input is a handshake control input used during handshake transfers. The use of Send to control a handshake interface is discussed in the "Interfacing" section, below.

The Maxim ICL7109 contains an improved power-up reset circuit that ensures that the ICL7109 powers up in the Direct mode if the Mode input is low, but other manufacturer's ICL7109s may power up in the Handshake mode even if the Mode input is held low. Although the Send input on the Maxim ICL7109 can be tied either high or low if only the Direct mode is used, other manufacturer's ICL7109s require that the Send input be tied high so that the ICL7109 will return to the Direct mode in 7 clock cycles if the Handshake mode is inadvertently entered on power-up.

Oscillator

The ICL7109 has a versatile three terminal oscillator that may be operated as a crystal or RC oscillator. It also may be overdriven by an external clock source. To optimize it for crystal or RC operation, the Oscillator Select input changes the internal configuration of the oscillator. The oscillator is configured for RC operation when the Oscillator Select input is high or left open (the input is provided with an internal pullup resistor), and the internal clock will be of the same phase and frequency as the signal at the Buffered Oscillator Output. (See Figure 6 for the resistor and capacitor connections.) Oscillation will occur in the circuit at a frequency given by f = 0.45/RC. The oscillator resistor should be 100kΩ. The capacitor value should be chosen such that 2048 clock periods are close to an integral multiple of the 60Hz period for optimum 60Hz line rejection, but the capacitor value should not be less than 50pF.

A feedback device and input and output capacitors are added to the oscillator when the Oscillator Select input is low. With no external components, the oscillator will function with most crystals in the 1 to 5MHz range. (See Figure 7.) A fixed ÷ 58 circuit is inserted between the Buffered Oscillator Output and the internal clock by taking the Oscillator Select input low. This division ratio provides 33.18ms integration time, by using a 3.58MHz TV crystal.

$$T = (2048 \text{ clock periods}) \times \frac{58}{3.58\text{MHz}} = 33.18\text{ms}$$

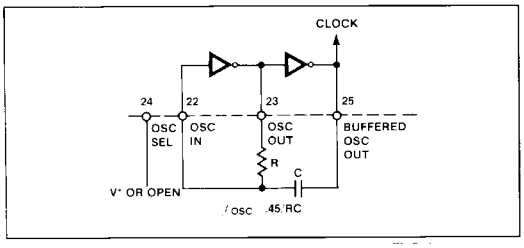


Figure 6. RC Oscillator

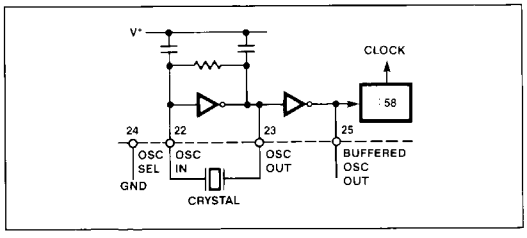


Figure 7. Crystal Oscillator

12 Bit A/D Converter With 3-State Binary Outputs

This time is quite close to 33.33ms or two 60Hz periods. The error is lower than one percent, which will yield better than 40dB of 60Hz rejection. If at any time the oscillator is to be overdriven, the overdriving signal should be applied at the Oscillator Input, and the Oscillator Output should be left open. When Oscillator Select is left open, the internal clock will be of the same duty cycle, frequency and phase as the input signal. The clock will be the input frequency divided by 58 when Oscillator Select is at Ground. The divide by 58 circuit will operate reliably up to about 5MHz (Oscillator Select low), while the converter itself will operate at clock rates up to 2 MHz (Oscillator Select high). This implies a conversion rate of 244 conversions/sec. To operate the converter at these rates the auto-zero and integrating capacitors must be scaled using the guidelines in the Component Selection section. As the conversion rate increases, the accuracy of the converter is compromised, primarily due to noise and the delay of the comparator. If the clock period is less than the comparator delay (typically 1-3 μsec.), the low order bits become meaningless. At 2 MHz, typical readings with the inputs shorted may be 4-10 counts, rendering the 4 LSBs meaningless.

Note: At 15 conversions per second, the integration time of 2048 clock pulses equals one complete period of 60 Hz. This is therefore the maximum conversion rate that will provide 60 Hz noise rejection.

Status Output

At the end of a conversion cycle the Status output goes low, one-half clock period after new data from the conversion has been stored in the output latches. Status goes high at the beginning of Signal Integrate (Phase II). Figure 3 shows the timing details. This signal may be utilized as a flag indicating "data valid" for monitoring the status of the converter or to drive interrupts since data never changes while Status is low.

Test Input

The counter output latches are enabled when the Test input is taken to a level halfway between V^+ and Ground, allowing the counter contents to be examined. When the Test input is grounded, the internal clock is disabled and the counter outputs are all forced into the high state. The counter outputs will be clocked to the low state when the input returns to the 1/2 (V^+ -Ground) voltage (or to V^+) and one clock is applied. This facilitates testing of the counter and the output drivers.

Although the Test pin has an internal pullup, it should be tied high if not used. This ensures that high speed transitions on adjacent pins (particularly LBEN) do not inadvertently activate the test mode.

Table 2. DIRECT MODE TRUTH TABLE

$\overline{CE}$/LOAD	$\overline{LBEN}$	$\overline{HBEN}$	B1-B8	B9-B12, POL,OR
1	X	X	Hi-Z	Hi-Z
0	1	1	Hi-Z	Hi-Z
0	0	1	Data Out	Hi-Z
0	1	0	Hi-Z	Data Out
0	0	0	Data Out	Data Out

Interfacing

Direct Mode

The ICL7109 is in the Direct mode when the Mode pin is low. In this mode the output interface is a simple parallel interface with a Chip Enable ($\overline{CE}$/Load) and two byte enables ($\overline{HBEN}$ and $\overline{LBEN}$). As shown in the truth table of Table 2, the least significant 8 bits of data are enabled when both $\overline{CE}$/Load and $\overline{LBEN}$ are low. The upper 4 bits of data, polarity, and overrange are enabled whenever $\overline{CE}$/Load and $\overline{HBEN}$ are low. The Maxim version of the ICL7109 has significantly enhanced current sourcing capability, which enables it to rapidly drive the large capacitances often found on microcomputer busses.

In Figure 12, an approach to interfacing several ICL7109s to a bus is shown. This is achieved by using the $\overline{CE}$/Load inputs (decoded from an address possibly) to select the desired converter, and tying the $\overline{HBEN}$ and $\overline{LBEN}$ signals to several converters together.

The ICL7109 can also be controlled through I/O peripheral ports, as shown in Figures 14, 15 and 16. Figures 13 through 16 are some practical circuits utilizing the parallel three-state output capabilities of the ICL7109. Shown in Figure 16 is a straightforward interface to the Intel MCS-48, -80 and -85 systems via an 8255 PPI, where the ICL7109 data outputs are active at all times. The 8155 I/O ports may be utilized in the same way. Although a read performed while the data latches are undergoing updates will lead to scrambled data, this interface can be used in a read-

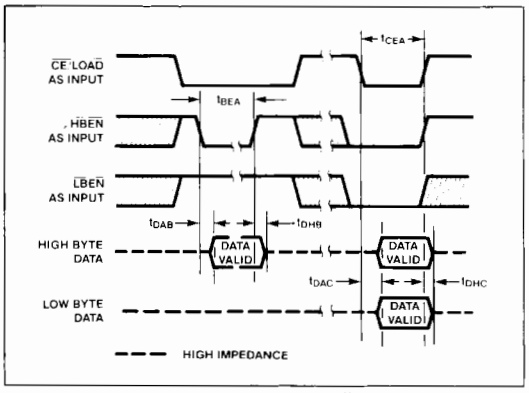


Figure 8. Direct Mode Output Timing

anytime mode. One way of solving this problem is to read the Status output as well. If it is high, read the data a second time after a delay of more than 1/2 converter clock period. If Status is still high, the first reading is correct. If Status is now low, the second reading is correct. On the other hand, the problem of timing is completely avoided by using a read-after-update sequence. (See Figure 14.) Data can be accessed by the high to low transition of the Status output driving an interrupt to the microprocessor. Figure 14 also demonstrates the Run/Hold input being used to initiate conversions under software control.

Figure 15 shows a similar interface to 650X or 680X systems. The transition of the Status output from high to low generates an interrupt via the Control Register B CB1 line. Note that CB2 controls the Run/Hold pin through Control Register B. This application permits software-controlled initiation of conversions.

Direct interfacing to most microprocessor busses is allowed by the three-state output capability of the ICL7109. (See Figure 13 and the typical operating circuit on the first page.) It is important that the requirements for setup and hold times, and minimum pulse widths are met. There are also drive limitations on long busses that should be noted. In general, this type of interface is favored only if the memory peripheral address density is low so that simple address decoding can be used. Interrupt handling can mandate several extra components. The use of interfacing devices will simplify the system in many cases.

Handshake Mode

Handshake Mode permits the interface with a number of external devices. For example, byte enables may be used as load enables or as byte identification flags, and external latches may be clocked by the rising edge of $\overline{CE}$/Load.

The handshake mode is specifically designed to directly interface the ICL7109 to industry standard UARTs, with no external logic required. The ICL7109 is in the handshake mode whenever the Mode input is high. In the handshake mode the $\overline{CE}$/Load, $\overline{LBEN}$ and $\overline{HBEN}$ pins are outputs and Send is an input. A typical UART to ICL7109 interface is shown in Figure 18, with the interface timing shown in Figures 9 through 11.

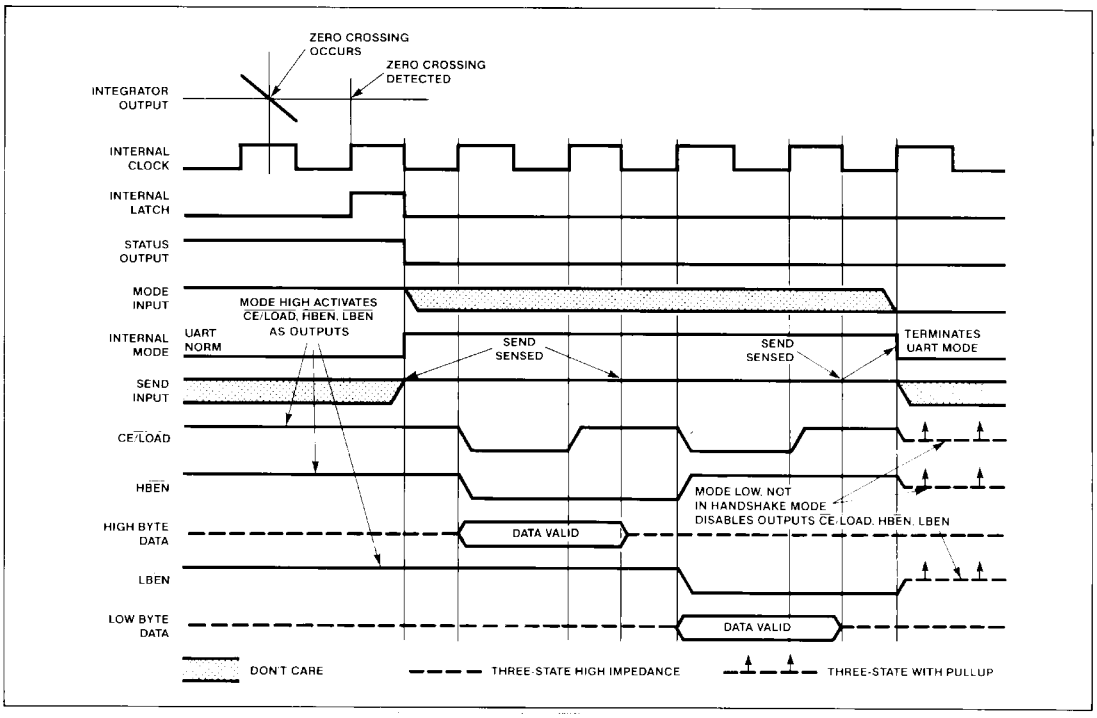


Figure 9. Handshake With Send Held Positive

12 Bit A/D Converter With 3-State Binary Outputs

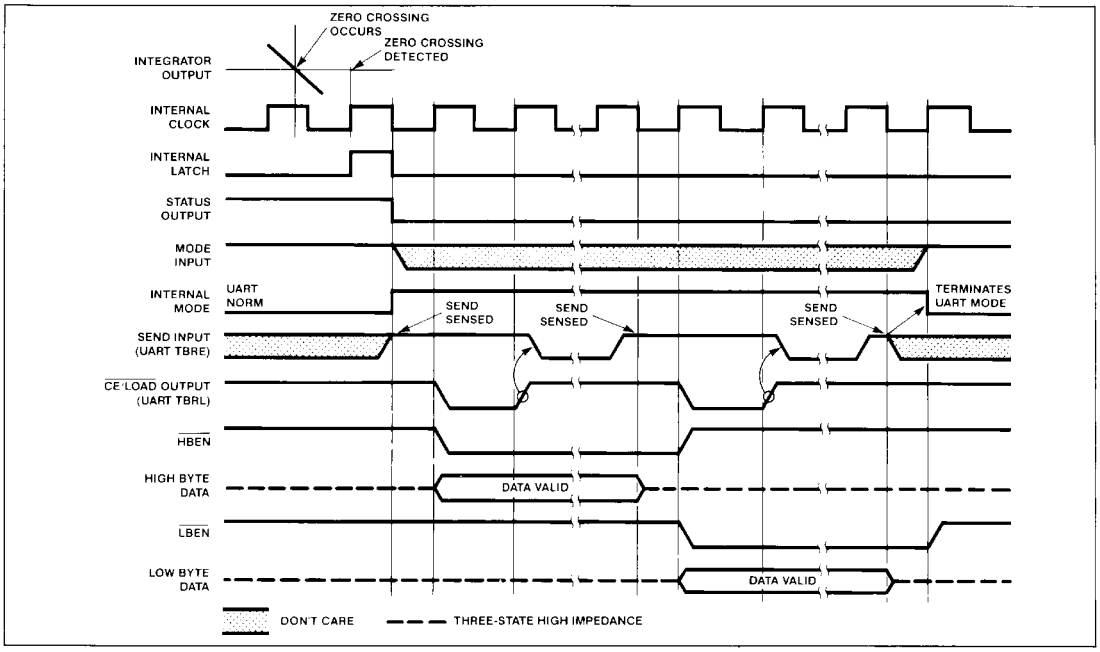


Figure 10. Handshake - Typical UART Interface Timing

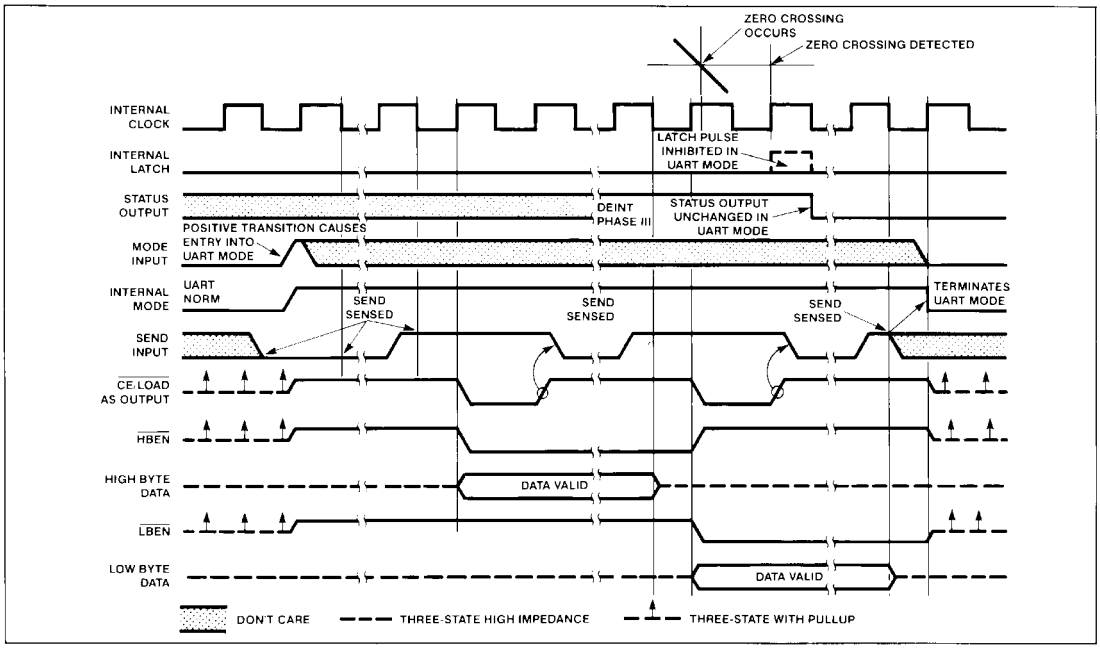


Figure 11. Handshake Triggered By Mode

When Mode is continuously held high, a new UART transmission will be started when Status goes low, provided Send is high at that time. As shown in Figure 10 the high byte of data will be written into the UART by the first pulse of $\overline{CE}$/Load. The $\overline{TBRE}$ signal of the UART will momentarily go low upon receiving the data. After the UART transfers the data to the transmitter register, the UART's $\overline{TBRE}$ output drives the ICL7109's Send input high. The ICL7109 senses the high level on the Send input and loads the low byte of data into the UART with a second pulse of $\overline{CE}$/Load. The ICL7109 continues its conversion cycles while this handshake takes place, and if the UART's $\overline{TBRE}$ has driven the ICL7109 Send input high by the end of the next conversion, the data transfer sequence will repeat. If the UARTs $\overline{TBRE}$ (and therefore the ICL7109's Send input) is low when the ICL7109 completes the next conversion, the internal latch pulse is inhibited and the data from that conversion is lost.

A handshake transfer can be initiated by a high-going pulse on the Mode pin. Upon receiving a high going pulse, the ICL7109 sets an internal Mode latch and will start a handshake transmission when Status goes low at the end of the next conversion. An alternate method of controlling the ICL7109 is to leave Mode high and initiate conversions via the Run/$\overline{Hold}$ input. With this method the ICL7109 will first make a conversion then transmit the data. Another method of initiating a transmission is shown in Figure 11. Here Mode is pulsed high while Send is low. A UART transmission is started when Send is taken high (at least 2 negative clock edges later).

The UART mode is also useful in interfacing the ICL7109 to I/O ports such as the 8255 and 6520. Figure 17 is an example of such an interface. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the Send input to the ICL7109, and using the $\overline{CE}$/Load to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1. The next conversion's result will be strobed into the port if the 8255 IBF flag is low and the ICL7109 is in handshake mode. The strobe will cause IBF to go high (Send goes low) which will prevent the ICL7109 from loading the second byte of data. The PPI will generate an interrupt. When executed, the result is that the data is read. The IBF will be reset low when the byte is read which causes the ICL7109 to sequence into the next byte. Figure 17 shows the PC7 line of the PPI connected to the Mode input of the ICL7109. If this input is tied high or left high, the data from every conversion will be sequenced into the system (provided the data access takes less time than a conversion). The output sequence can be obtained on demand by using the PC7 output to drive the Mode input. Note that the 8255 can service another peripheral device since only one port is used. The 8155 can utilize the same arrangement.

The ICL7109 is not limited to the applications described here. These examples show some of the many interfaces and uses of the ICL7109 and merely provide a point of departure for users to develop appropriate systems. Many of the suggestions made here may be combined. More specifically, the uses of the Mode, Status, and Run/$\overline{Hold}$ signals may be mixed.

Typical Applications

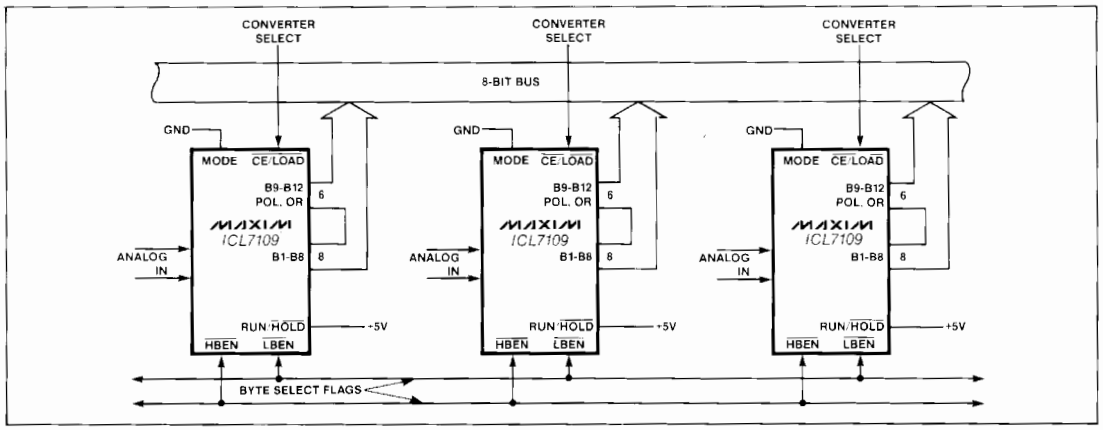


Figure 12. Three-stating several 7109s to a Bus

12 Bit A/D Converter With 3-State Binary Outputs

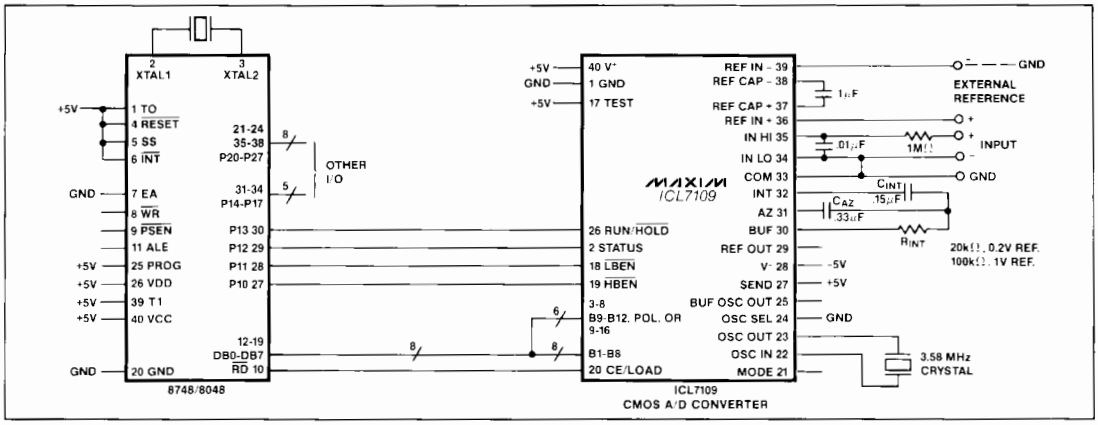


Figure 13. Typical Connection Diagram Parallel Interface with MCS-48 Microcomputer

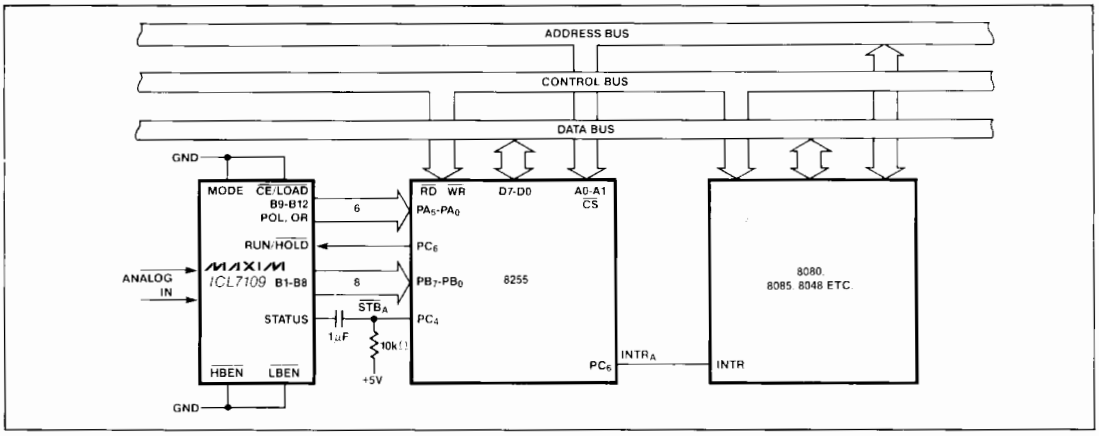


Figure 14. Full-time Parallel Interface to MCS-48, -80, -85 Microcomputers with Interrupt

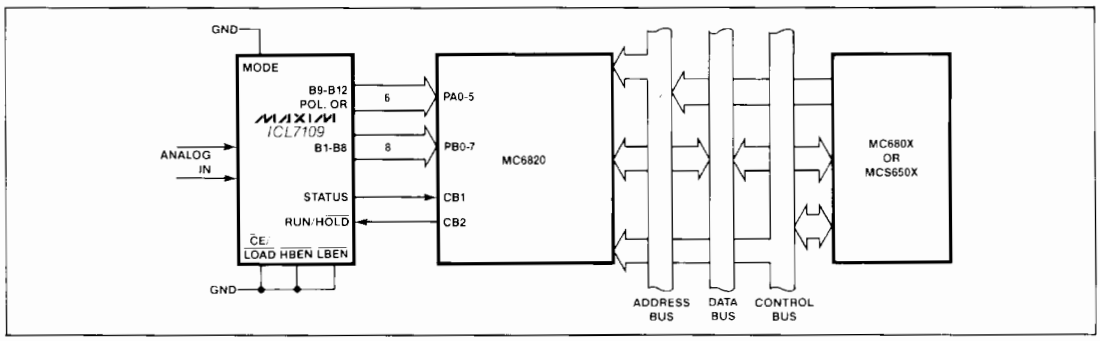


Figure 15. Full-time Parallel Interface to MS680X or MCS650X Microprocessors

12 Bit A/D Converter With 3-State Binary Outputs

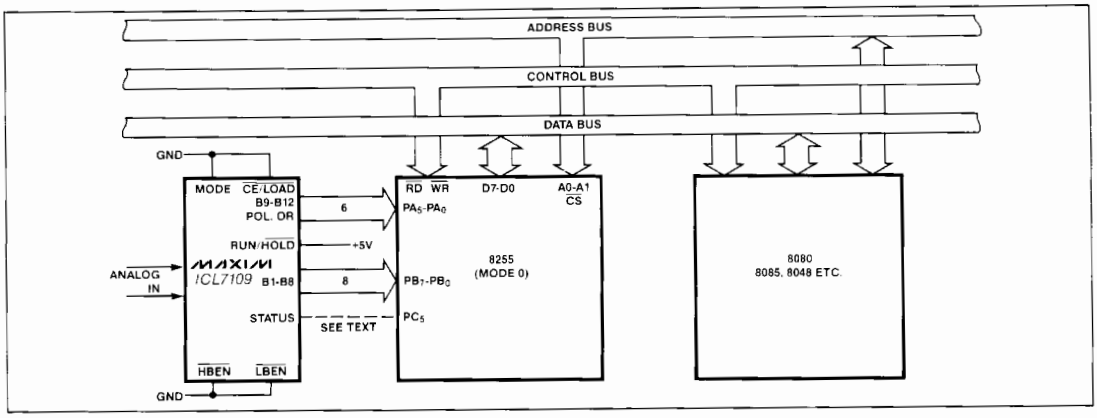


Figure 16. Full-time Parallel Interface to MCS-48, -80, -85 Microcomputer Systems

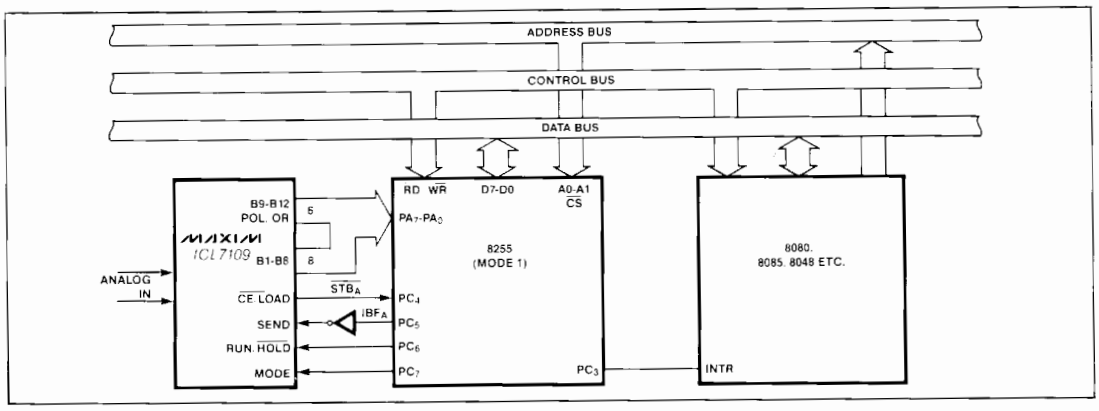


Figure 17. Handshake Interface - ICL7109 to MCS-48, -80, -85

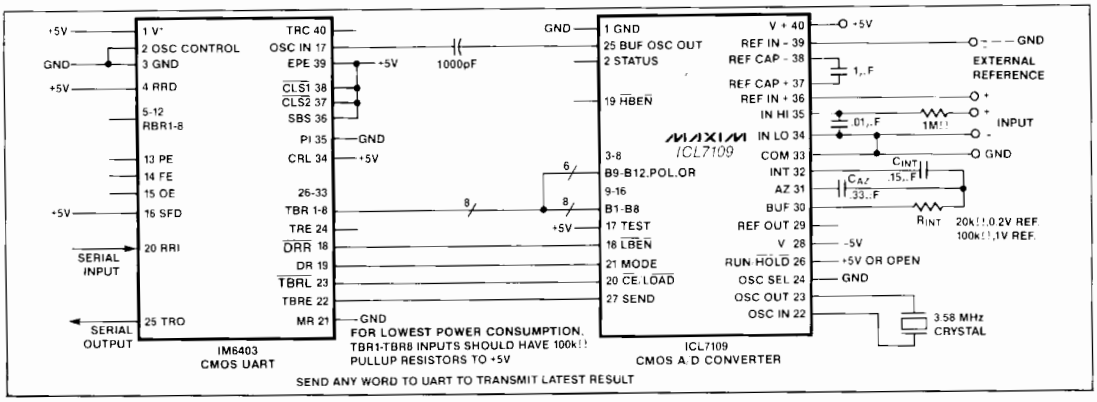
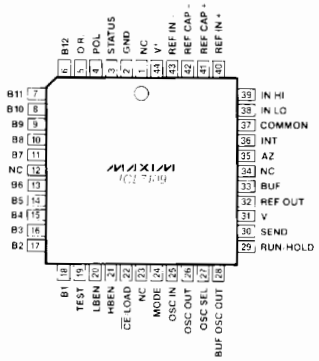


Figure 18. Typical Connection Diagram UART Interface

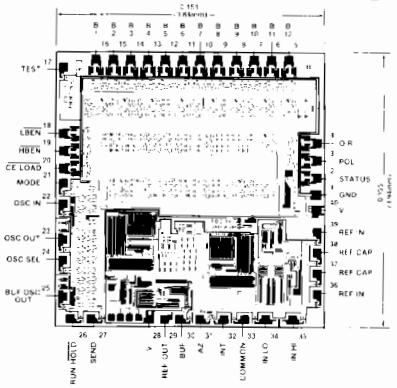
12 Bit A/D Converter With 3-State Binary Outputs

Pin Configuration

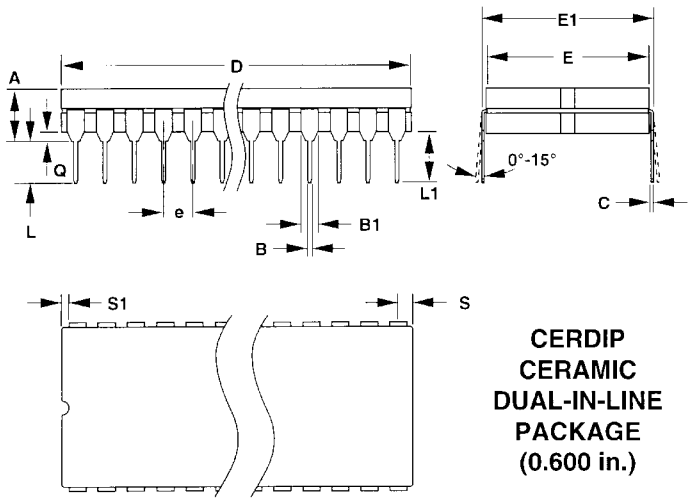


44 Lead Plastic Chip Carrier (Quad Pak)

Chip Topography



Package Information

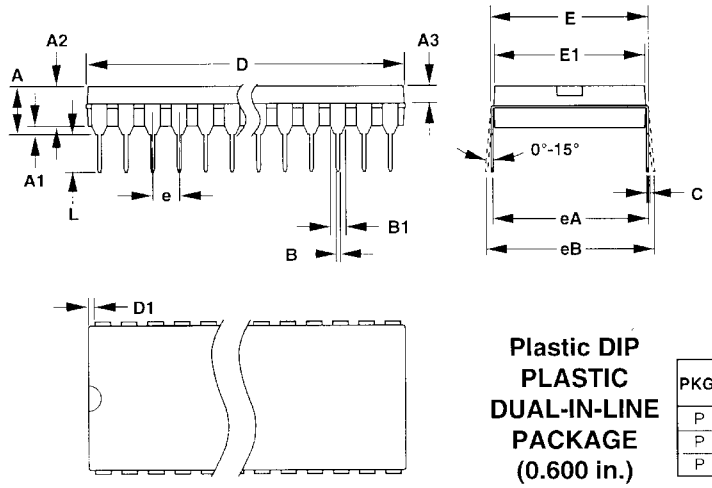


**CERDIP
CERAMIC
DUAL-IN-LINE
PACKAGE
(0.600 in.)**

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.232	–	5.89
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.500	0.620	12.70	15.75
E1	0.590	0.630	14.99	16.00
e	0.100		2.54	
L	0.120	0.200	3.05	5.08
L1	0.150	–	3.81	–
Q	0.015	0.075	0.38	1.91
S	–	0.100	–	2.54
S1	0.005	–	0.13	–

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	24	–	1.290	–	32.77
D	28	–	1.490	–	37.85
D	40	–	2.096	–	53.24

21-0046A



**Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.600 in.)**

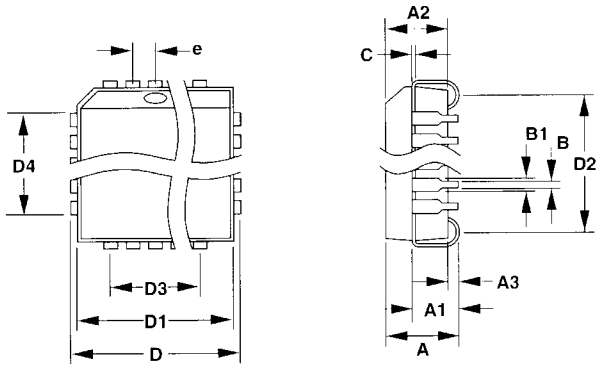
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.050	0.090	1.27	2.29
E	0.600	0.625	15.24	15.88
E1	0.525	0.575	13.34	14.61
e	0.100	–	2.54	–
eA	0.600	–	15.24	–
eB	–	0.700	–	17.78
L	0.120	0.150	3.05	3.81

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	24	1.230	1.270	31.24	32.26
P	D	28	1.430	1.470	36.32	37.34
P	D	40	2.025	2.075	51.44	52.71

21-0044A

12 Bit A/D Converter With 3-State Binary Outputs

Package Information (continued)



PLCC
PLASTIC
LEADED CHIP CARRIER

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.145	0.156	3.68	3.96
A3	0.020	–	0.51	–
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
e	0.050		1.27	

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	20	0.385	0.395	9.78	10.03
D1		0.350	0.356	8.89	9.04
D2		0.290	0.330	7.37	8.38
D3		0.200 REF		5.08 REF	
D	28	0.485	0.495	12.32	12.57
D1		0.450	0.456	11.43	11.58
D2		0.390	0.430	9.91	10.92
D3		0.300 REF		7.62 REF	
D4		0.300	–	7.62	–
D	44	0.685	0.695	17.40	17.65
D1		0.650	0.656	16.51	16.66
D2		0.590	0.630	14.99	16.00
D3		0.500 REF		12.70 REF	
D4		0.470	–	11.94	–
D	68	0.985	0.995	25.02	25.27
D1		0.950	0.958	24.13	24.33
D2		0.890	0.930	22.61	23.62
D3		0.800 REF		20.32 REF	
D4		0.625	–	15.87	–

21-0049B