HMC720* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMC720LP3E Evaluation Board

DOCUMENTATION

Data Sheet

- HMC720 Data Sheet

TOOLS AND SIMULATIONS

- HMC720 IBIS Model

REFERENCE MATERIALS

Quality Documentation

- HMC Legacy PDN: PCN120009
- Package/Assembly Qualification Test Report: 16L 3x3mm QFN Package (QTR: 11003 REV: 02)
- Package/Assembly Qualification Test Report: LC3, LC3B, LC3C (QTR: 2014-00376 REV: 01)
- Package/Assembly Qualification Test Report: LP2, LP2C, LP3, LP3B, LP3C, LP3D, LP3F, LP3G (QTR: 2014-0364)
- Semiconductor Qualification Test Report: BiCMOS-C (QTR: 2013-00241)

DESIGN RESOURCES

- HMC720 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMC720 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

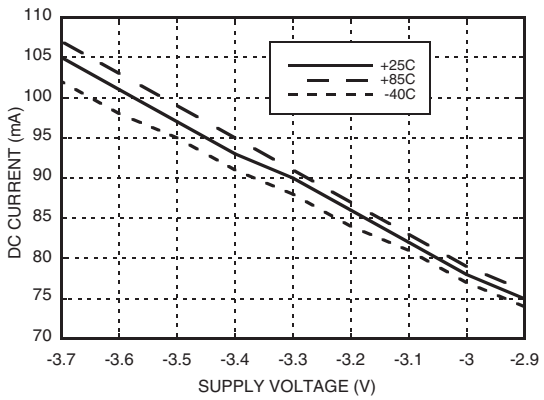
14 Gbps, FAST RISE TIME 1:2 FANOUT BUFFER w/ PROGRAMMABLE OUTPUT VOLTAGE

Electrical Specifications (continued)

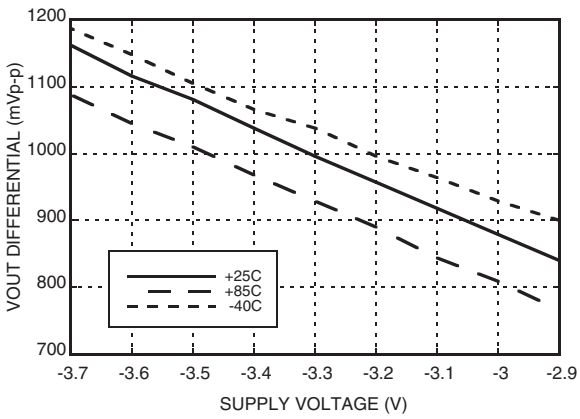
Parameter	Conditions	Min.	Typ.	Max	Units
Output Return Loss	Frequency <13 GHz		10		dB
Small Signal Gain			27		dB
Random Jitter J_R	rms			0.2	ps rms
Deterministic Jitter, J_D	δ - δ, 2^{15}-1 PRBS input [1]		2	6	ps
Propagation Delay, td			120		ps
D1 to D2 Data Skew, t_{SKEW}			0		ps
VR Pin Current	VR = 0.0 V		2		mA
VR Pin Current	VR = +0.4 V			3.5	mA

[1] Deterministic jitter measured at 13 GHz with a 300 mVp-p, 2^{15}-1 PRBS input sequence.

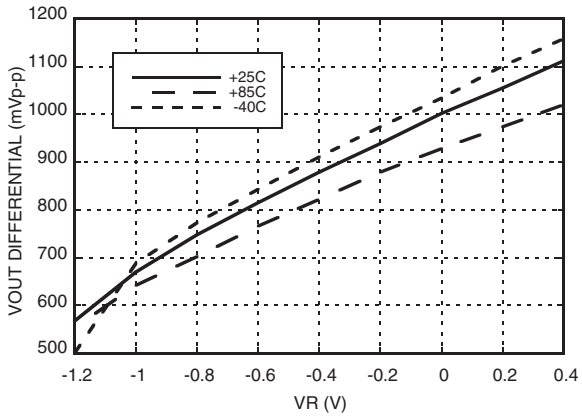
DC Current vs. Supply Voltage [1][2]



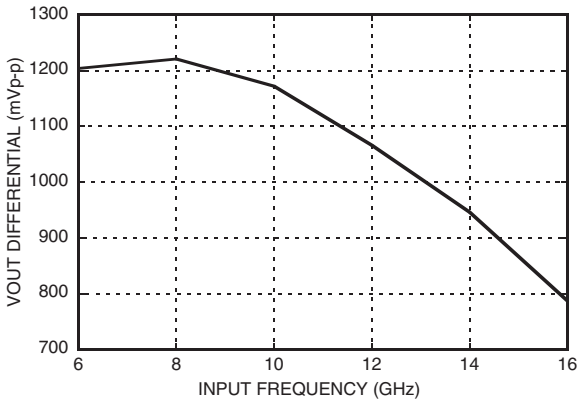
Output Differential Voltage vs. Supply Voltage [1][3]



Output Differential Voltage vs. VR [3][4]



Output Differential Voltage vs. Frequency [1][4]



[1] VR = 0.0 V [2] Frequency = 13 GHz [3] Frequency = 10 GHz [4] Vee = -3.3 V

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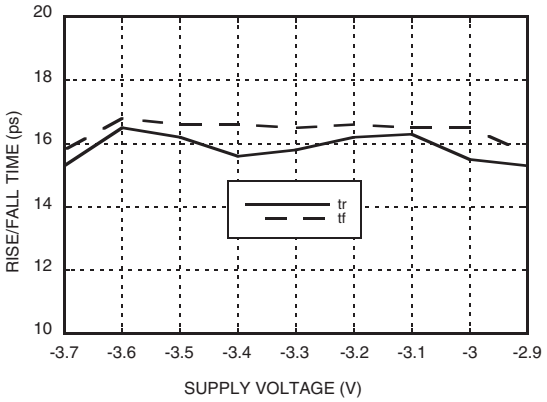
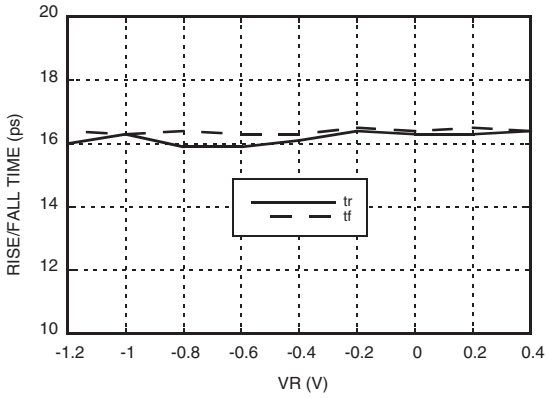
14 Gbps, FAST RISE TIME 1:2 FANOUT BUFFER w/ PROGRAMMABLE OUTPUT VOLTAGE

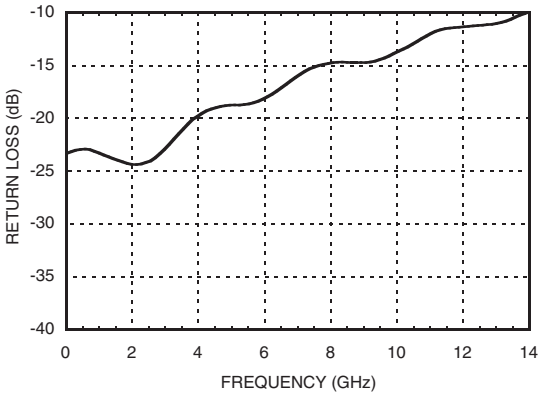
Rise / Fall Time vs. Supply Voltage [1][2]



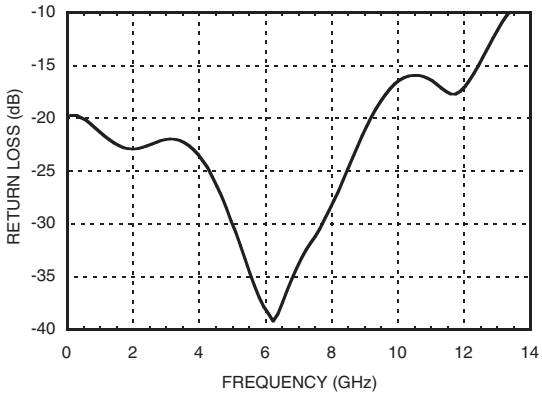
Rise / Fall Time vs. VR [2][3]



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



[1] VR = 0.0 V [2] Frequency = 13 GHz [3] Vee = -3.3 V

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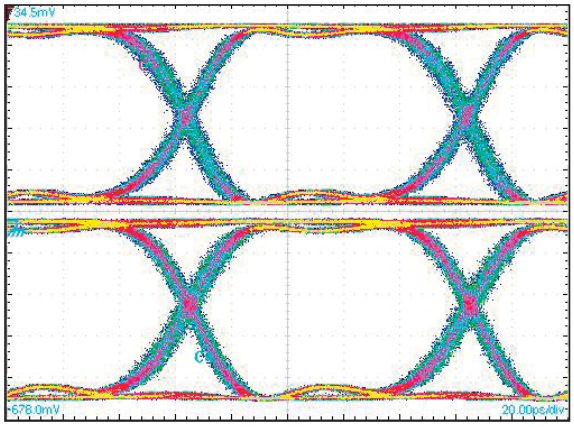
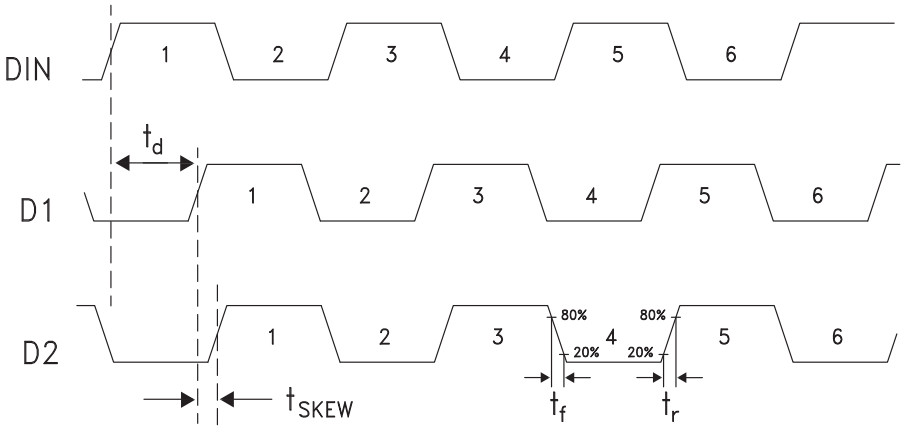
Eye Diagram



[1] Test Conditions:
Pattern generated with an Agilent N4903A Serial BERT.
Eye Diagram presented on a Tektronix CSA 8000.
Device input = 10 Gbps PN code, Vin = 300 mVp-p differential.
Both output channels shown.

Timing Diagram



Truth Table

Input	Outputs	
DIN	D1	D2
L	L	L
H	H	H
Notes: DIN = DINP - DINN D1 = D1P - D1N D2 = D2P - D2N	H - Positive differential voltage L - Negative differential voltage	

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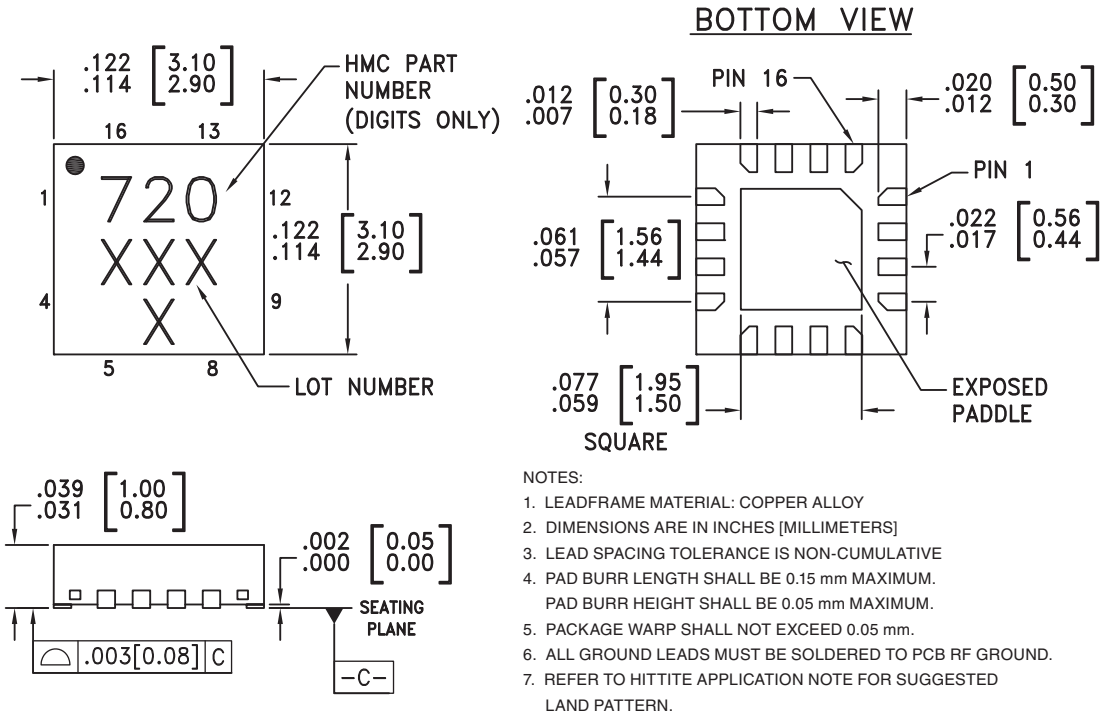
Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.75 V to +0.5 V
Input Signals	-2 V to +0.5 V
Output Signals	-1.5 V to +1 V
Junction Temperature	125 °C
Continuous Pdiss (T = 85 °C) (derate 20.4 mW/°C above 85 °C)	0.816 W
Thermal Resistance (Rth_{j-p}) Worst case junction to package paddle	49 °C/W
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C
ESD Sensitivity (HBM)	Class 1C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15 mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05 mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm.
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.
8. PADDLE MUST BE SOLDERED TO Vee.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC720LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	720 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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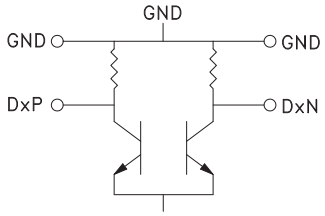
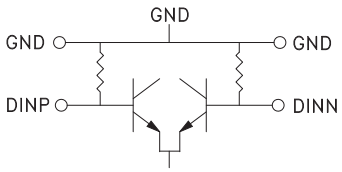
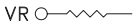
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 12	GND	Signal Grounds	
2, 3 10, 11	D1P, D1N D2N, D2P	Differential Clock / Data Outputs: Current Mode Logic (CML) referenced to positive supply.	
6, 7	DINP, DINN	Differential Clock / Data Inputs: Current Mode Logic (CML) referenced to positive supply	
13, 16	GND	Supply Ground	
14	VR	Output level control. Output level may be adjusted by either applying a voltage to VR per “Output Differential vs. VR” plot.	
15, Package Base	Vee	Negative Supply	

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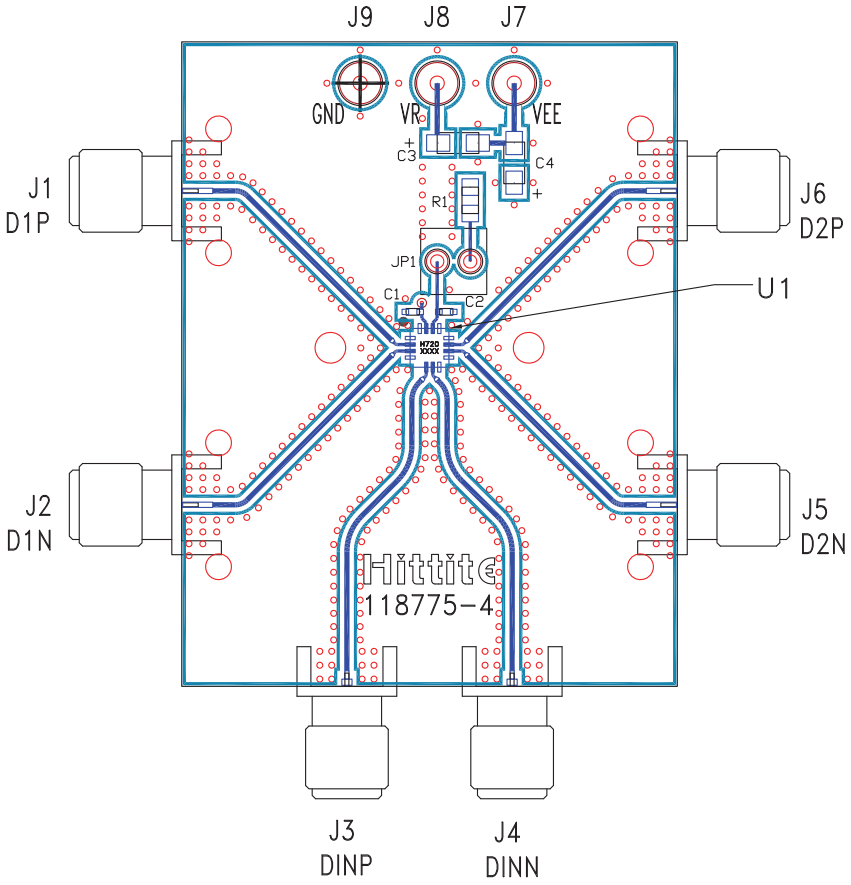
Evaluation PCB



List of Materials for Evaluation PCB 118777 [1]

Item	Description
J1 - J6	PCB Mount SMA RF Connectors
J7 - J9	DC Pin
JP1	0.1" Header with Shorting Jumper
C1, C2	100 pF, Capacitor, 0402 Pkg
C3, C4	4.7 µF Capacitor, Tantalum
R1	10 Ohm Resistor, 0603 Pkg.
U1	HMC720LP3E High Speed Logic, Fanout Buffer
PCB [2]	118775 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed packaged base should be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to GND for normal operation.

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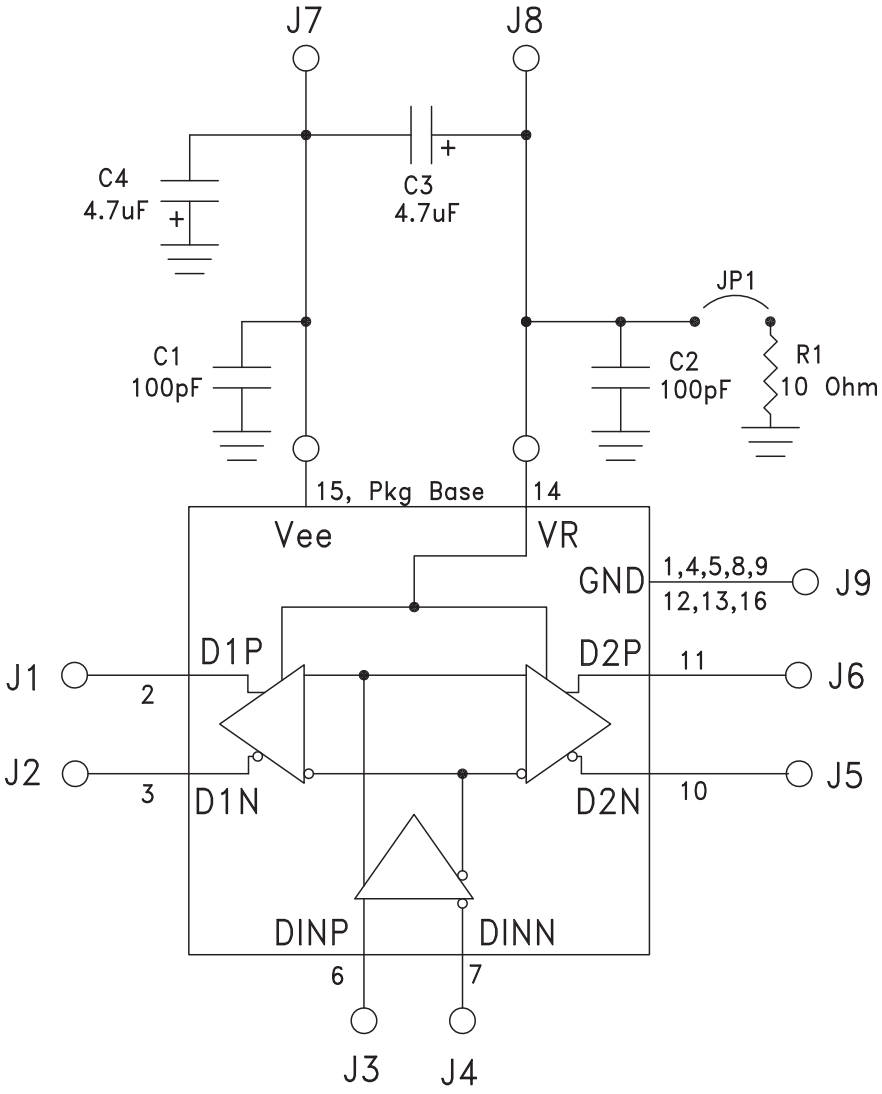
Application Circuit



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