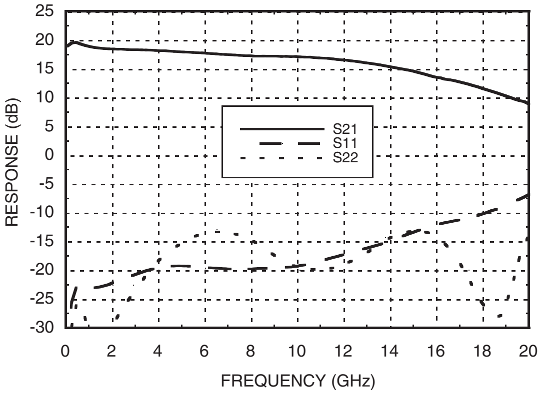
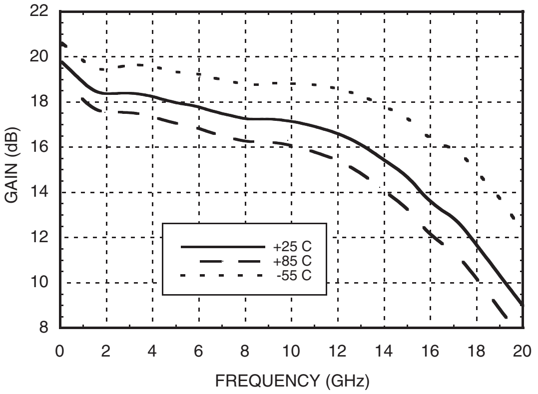
GaAs PHEMT MMIC POWER AMPLIFIER, DC - 18 GHz

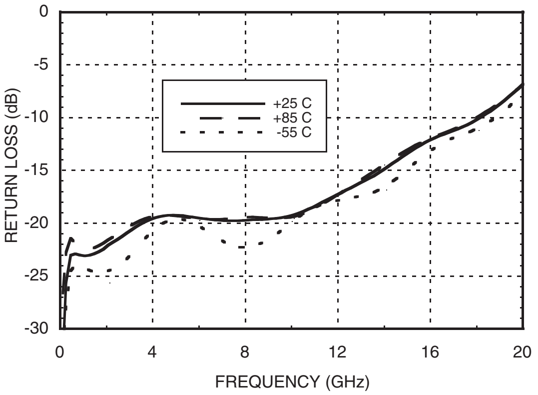
Gain & Return Loss



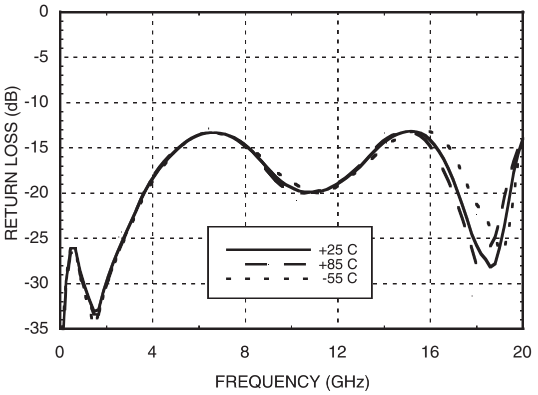
Gain vs. Temperature



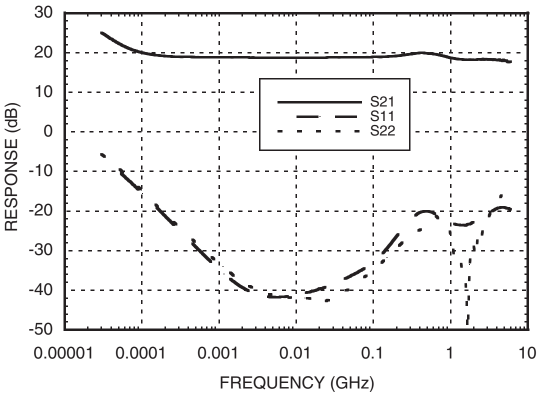
Input Return Loss vs. Temperature



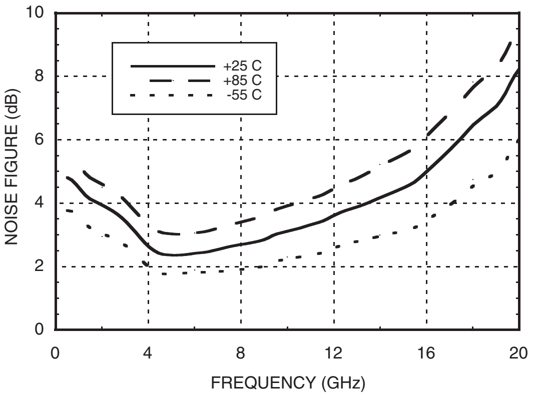
Output Return Loss vs. Temperature



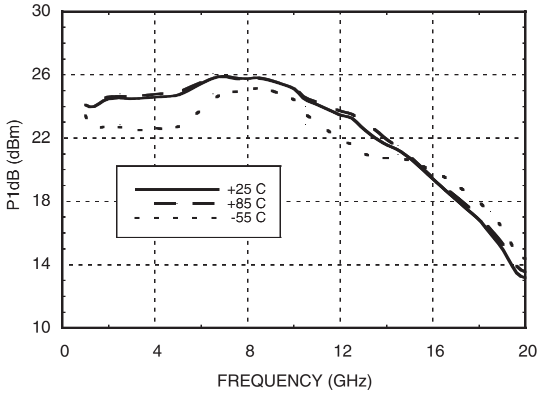
Low Frequency Gain & Return Loss



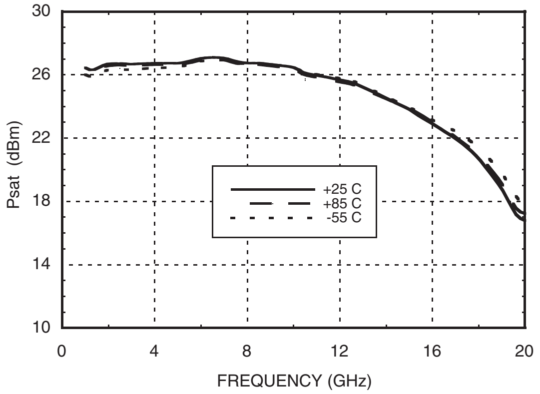
Noise Figure vs. Temperature



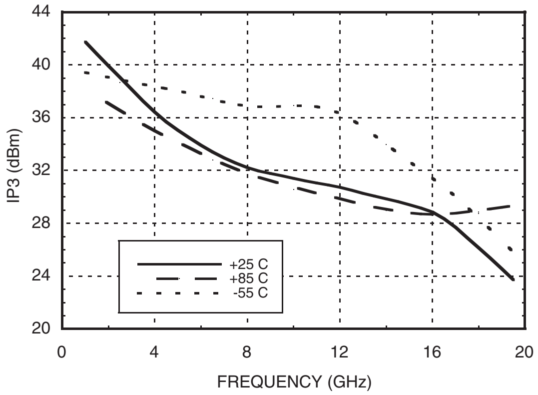
Output P1dB vs. Temperature



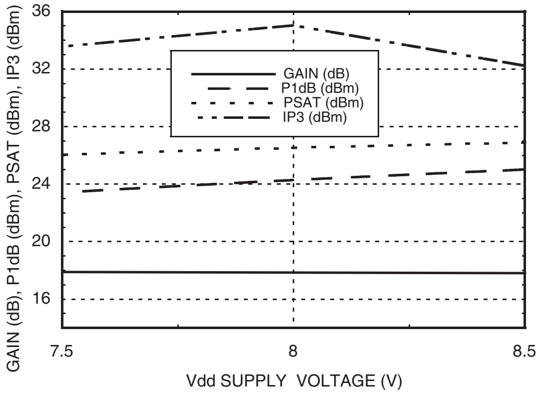
Output Psat vs. Temperature



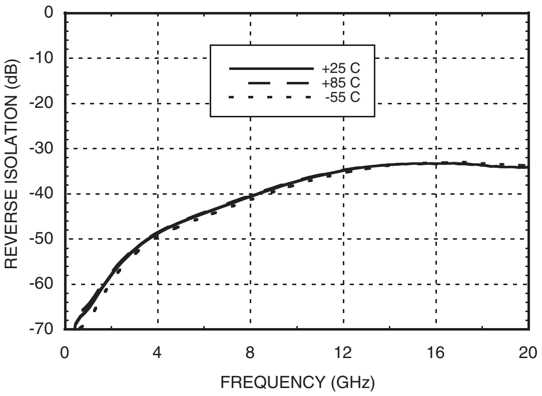
Output IP3 vs. Temperature



Gain, Power & Output IP3 vs. Supply Voltage @ 5 GHz, Fixed Vgg



Reverse Isolation vs. Temperature



GaAs PHEMT MMIC POWER AMPLIFIER, DC - 18 GHz

Absolute Maximum Ratings

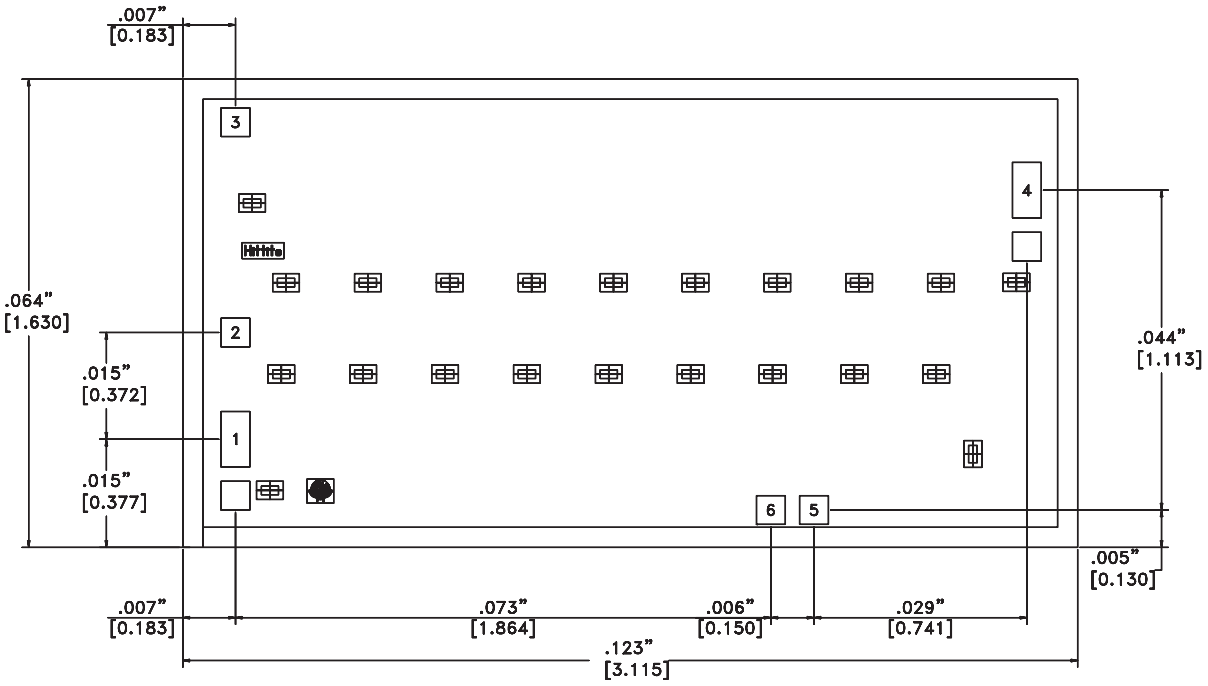
Drain Bias Voltage (Vdd)	+9 Vdc
Gate Bias Voltage (Vgg1)	-2 to 0 Vdc
Gate Bias Voltage (Vgg2)	(Vdd -8) Vdc to Vdd
RF Input Power (RFIN)(Vdd = +8 Vdc)	+16 dBm
Channel Temperature	175 °C
Continuous Pdiss (T= 85 °C) (derate 51.5 mW/°C above 85 °C)	4.64 W
Thermal Resistance (channel to die bottom)	19.4 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-55 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Typical Supply Current vs. Vdd

Vdd (V)	Idd (mA)
+7.5	292
+8.0	290
+8.5	288

Outline Drawing



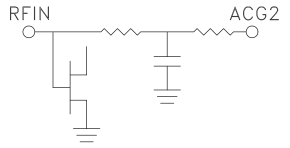
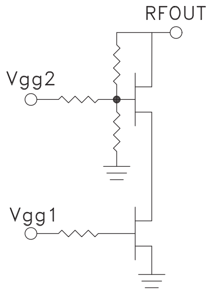
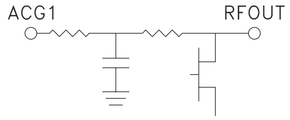
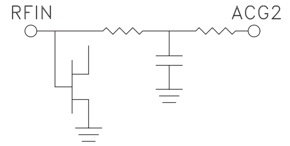
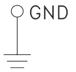
Die Packaging Information [1]

Standard	Alternate
GP-1 (Gel Pack)	[2]

[1] Refer to the "Packaging Information" section for die packaging dimensions.
[2] For alternate packaging information contact Hittite Microwave Corporation.

NOTES:
1. ALL DIMENSIONS IN INCHES [MILLIMETERS]
2. NO CONNECTION REQUIRED FOR UNLABELED BOND PADS
3. DIE THICKNESS IS 0.004 (0.100)
4. TYPICAL BOND PAD IS 0.004 (0.100) SQUARE
5. BACKSIDE METALLIZATION: GOLD
6. BACKSIDE METAL IS GROUND
7. BOND PAD METALIZATION: GOLD

Pad Descriptions

Pad Number	Function	Description	Interface Schematic
1	RFIN	This pad is DC coupled and matched to 50 Ohms.	
2	Vgg2	Gate Control 2 for amplifier. +3V should be applied to Vgg2 for nominal operation. Vgg2 may be adjusted between 0 to +5V to temperature compensate gain.	
4	RFOUT & Vdd	RF output for amplifier. Connect the DC bias (Vdd) network to provide drain current (Idd). See application circuit herein.	
5	Vgg1	Gate Control 1 for amplifier. Adjust between -2 to 0V to achieve Idd= 290 mA.	
3	ACG1	Low frequency termination. Attach bypass capacitor per application circuit here in.	
6	ACG2	Low frequency termination. Attach bypass capacitor per application circuit here in.	
Die Bottom	GND	Die bottom must be connected to RF/DC ground.	

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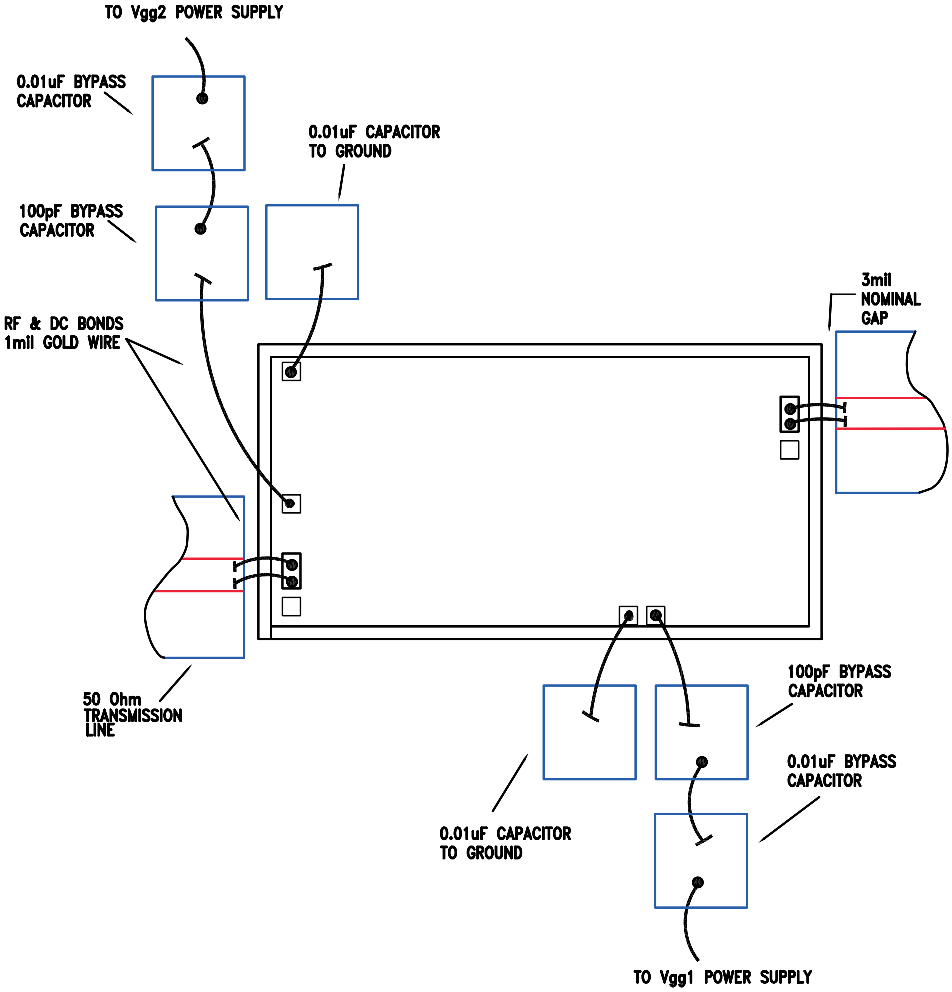
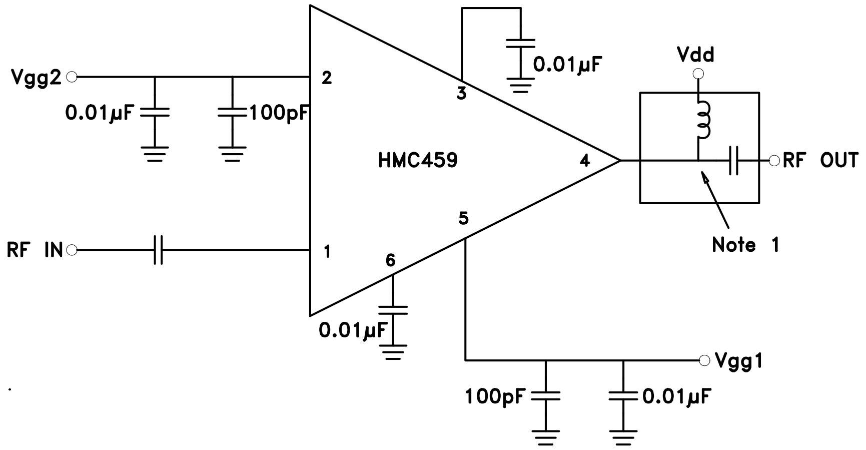
Assembly Diagram



Application Circuit



NOTE 1: Drain Bias (Vdd) must be applied through a broadband bias tee or external bias network.

Mounting & Bonding Techniques for Millimeterwave GaAs MMICs

The die should be attached directly to the ground plane eutectically or with conductive epoxy (see HMC general Handling, Mounting, Bonding Note).

50 Ohm Microstrip transmission lines on 0.127mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). If 0.254mm (10 mil) thick alumina thin film substrates must be used, the die should be raised 0.150mm (6 mils) so that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102mm (4 mil) thick die to a 0.150mm (6 mil) thick molybdenum heat spreader (moly-tab) which is then attached to the ground plane (Figure 2).

Microstrip substrates should brought as close to the die as possible in order to minimize bond wire length. Typical die-to-substrate spacing is 0.076mm to 0.152 mm (3 to 6 mils).

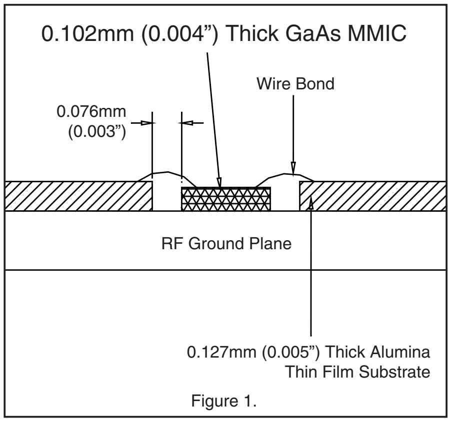


Figure 1.

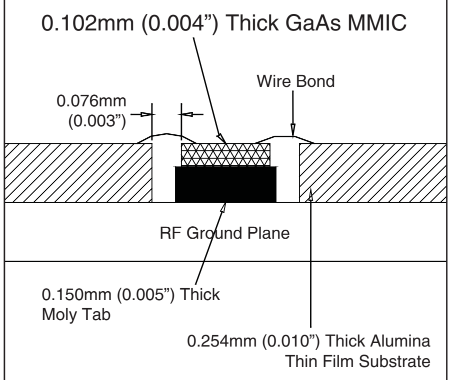


Figure 2.

Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity: Follow ESD precautions to protect against ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip may have fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat.

Eutectic Die Attach: A 80/20 gold tin preform is recommended with a work surface temperature of 255 °C and a tool temperature of 265 °C. When hot 90/10 nitrogen/hydrogen gas is applied, tool tip temperature should be 290 °C. DO NOT expose the chip to a temperature greater than 320 °C for more than 20 seconds. No more than 3 seconds of scrubbing should be required for attachment.

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer’s schedule.

Wire Bonding

Ball or wedge bond with 0.025mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31mm (12 mils).

Notes: