FAIRCHILD SEMICONDUCTOR®

February 2010

FDP2710_F085

N-Channel PowerTrench® MOSFET

250V, 50A, 47mΩ

Features

- Typ $r_{DS(on)}$ = 38mΩ at V_{GS} = 10V, I_D = 50A
- Typ $Q_{g(TOT)}$ = 78nC at V_{GS} = 10V
- Fast switching speed
- Low gate charge
- High performance trench technology for extremely low RDS(on)
- High power and current handling capability
- Qualified to AEC Q101
- RoHS Compliant

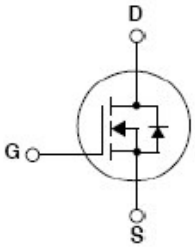
General Description

This N-Channel MOSFET is produced using Fairchil Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Applications

- PDP application
- Hybrid Electric Vehicle DC/DC converters

TO-220AB
FDP SERIES



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	250	V
V_{GS}	Gate to Source Voltage	±30	V
I_D	Drain Current Continuous (T_C < 50°C, V_{GS} = 10V)	50	A
	Continuous (T_{amb} = 25°C, V_{GS} = 10V, with $R_{\theta JA}$ = 62°C/W)	4	
	Pulsed	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 1)	483	mJ
P_D	Power Dissipation	403	W
	Derate above 25°C	3.2	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Maximum Thermal Resistance Junction to Case	0.31	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient (Note 2)	62	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP2710	FDP2710_F085	TO220	Tube	NA	50 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	250	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	-	0.25	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 250V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 250V, V_{GS} = 0V, T_C = 125°C	-	-	500	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±30V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	3	3.9	5	V
$r_{DS(on)}$	Drain to Source On Resistance	I_D = 50A, V_{GS}= 10V,	-	38	47	mΩ
		I_D = 50A, V_{GS}= 10V, T_J = 150°C	-	104	129	
g_{FS}	Forward Transconductance	I_D = 25A, V_{DS}= 10V	-	63	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	5690	-	pF
C_{oss}	Output Capacitance		-	425	-	pF
C_{rss}	Reverse Transfer Capacitance		-	115	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 20V	V_{GS} = 0 to 10V, V_{DD} = 125V, I_D = 50A	-	78	101	nC
Q_{gs}	Gate to Source Gate Charge		-	31	-	nC
Q_{gd}	Gate to Drain “Miller“ Charge		-	20	-	nC

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 125V, I_D = 50A V_{GS} = 10V, R_{GEN} = 25Ω	-	85	-	ns
t_r	Rise Time		-	183	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	140	-	ns
t_f	Fall Time		-	121	-	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain-Source Diode Forward Current		-	-	50	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		-	-	150	A
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 50A	-	0.9	1.2	V
t_{rr}	Reverse Recovery Time	I_{SD} = 50A, dI_{SD}/dt = 100A/μs	-	166	216	ns
Q_{rr}	Reverse Recovery Charge		-	1	1.3	uC

Notes:

1: Starting T_J = 25°C, L = 1.68mH, I_{AS} = 24A.

2: Pulse width 100s

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/
All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Typical Characteristics

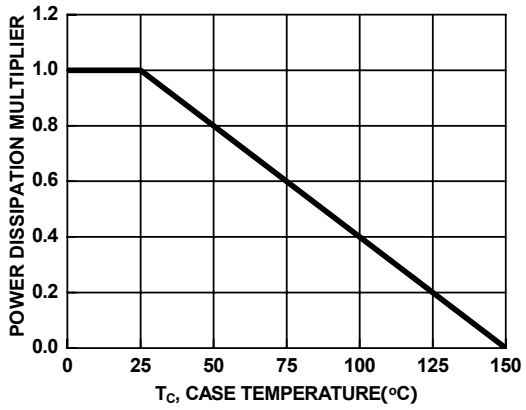


Figure 1. Normalized Power Dissipation vs Case Temperature

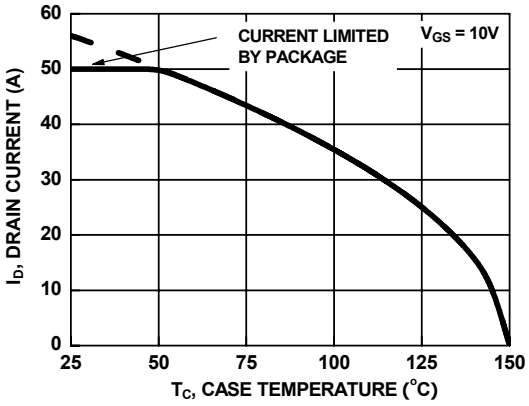


Figure 2. Maximum Continuous Drain Current vs Case Temperature

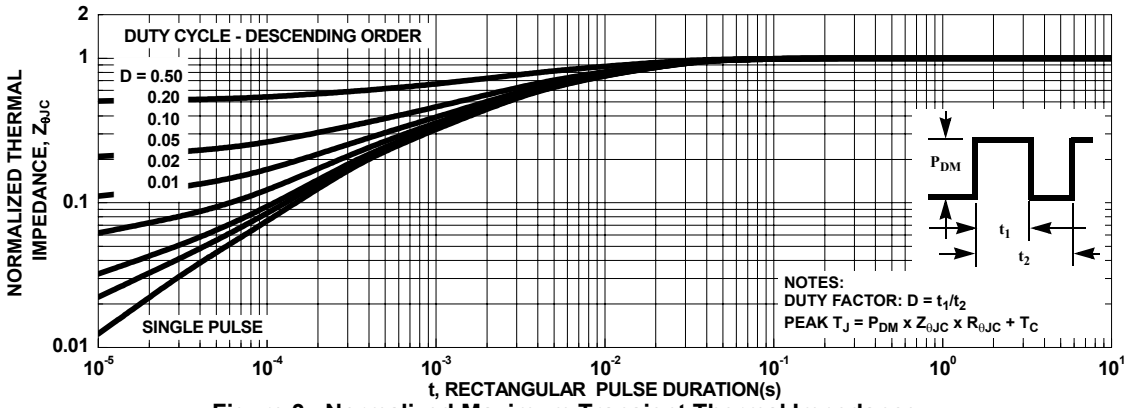


Figure 3. Normalized Maximum Transient Thermal Impedance

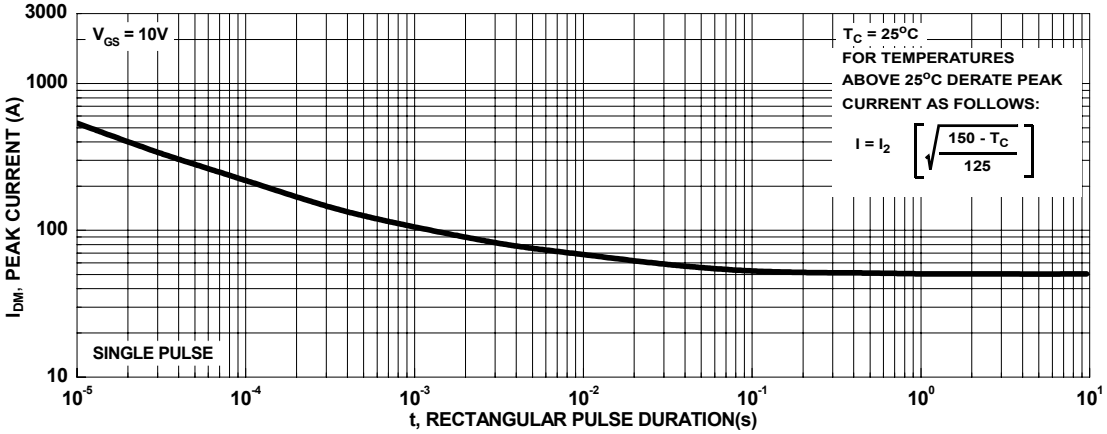


Figure 4. Peak Current Capability

Typical Characteristics

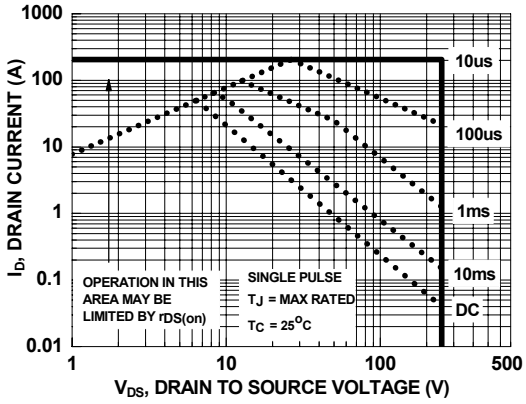
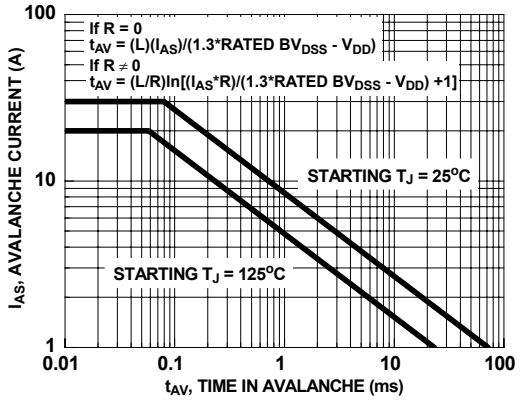


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

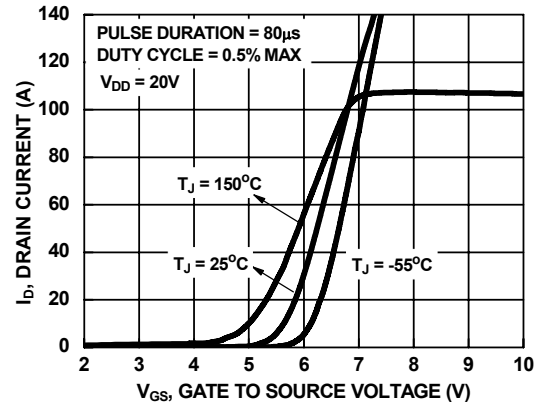


Figure 7. Transfer Characteristics

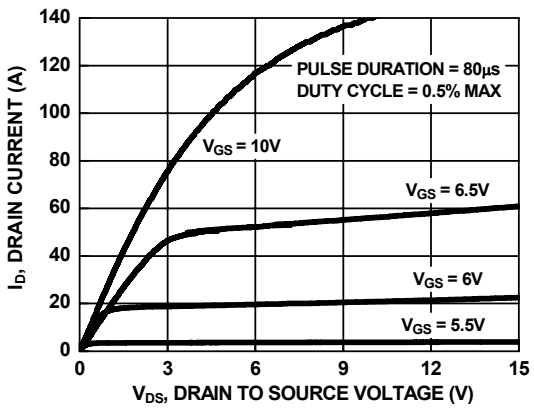


Figure 8. Saturation Characteristics

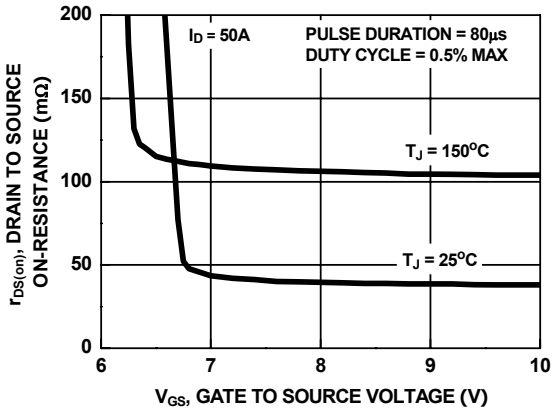


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

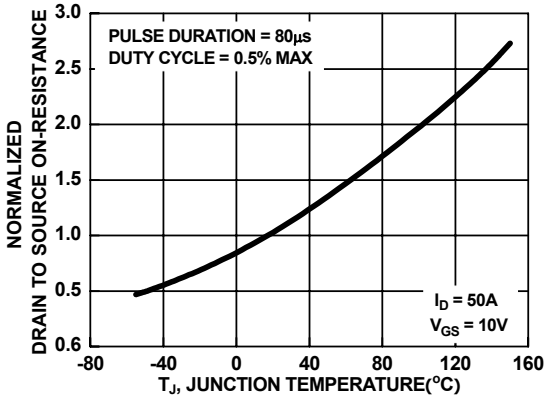


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics

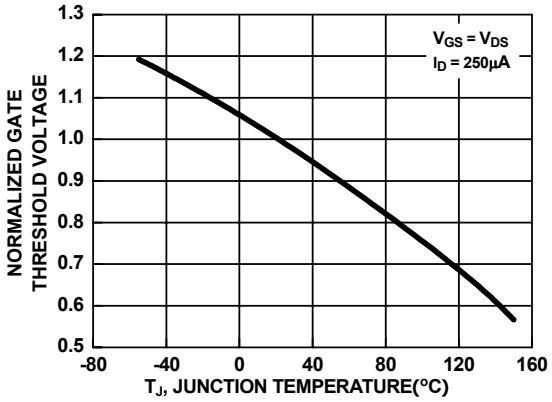


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

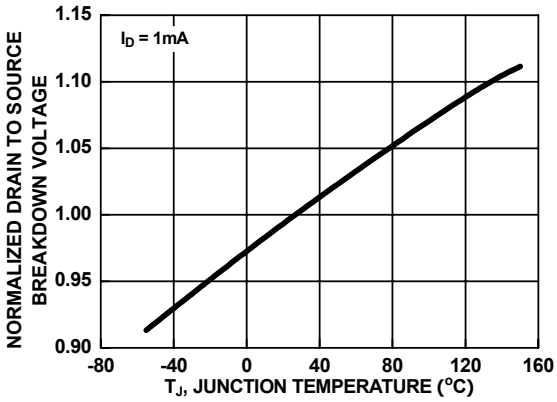


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

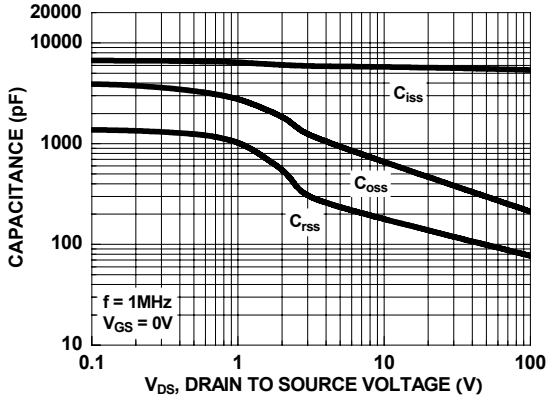


Figure 13. Capacitance vs Drain to Source Voltage

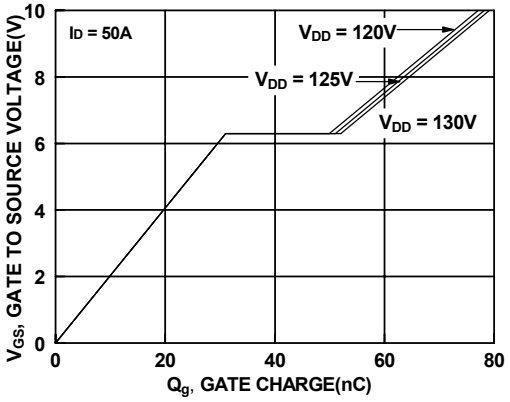


Figure 14. Gate Charge vs Gate to Source Voltage

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Rev. I47

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