

EQCO850SC.3-HS/EQCO875SC.3-HS

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EQCO850SC.3-HS/EQCO875SC.3-HS

1.0 DEVICE OVERVIEW

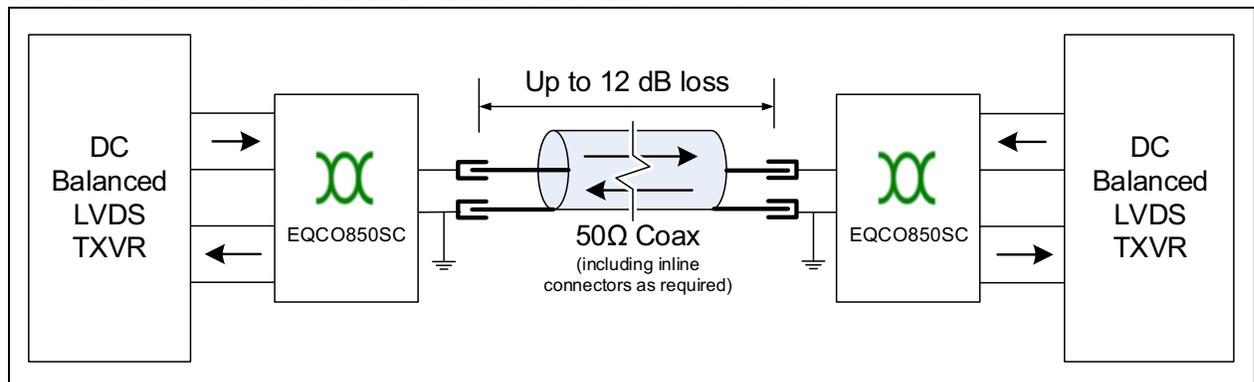
The EQCO850SC-HS (EQCO875SC-HS) is ideally suited for simplex and duplex LVDS connections over 50Ω (75Ω) coax cables between 500 Mbps and 1.25 Gbps. For correct operation, the signals must be NRZ (Non-Return-to-Zero) encoded and DC balanced with a maximum run length of ten bits. Excellent EMI/RFI coax cable shielding allows for good EMI properties.

The EQCO850SC-HS operates with a variety of 50Ω coax cables, including the cost-effective 2.8 mm diameter RTK cable (e.g., Leoni Dakar 302) commonly used for radio and navigation antennas in automotive applications. This cable fits well with the standardized (DIN and USCAR), high-performance, cost-effective RF connectors: SAE/USCAR-18 "FAKRA/SMB RF Connector".

The EQCO875SC-HS is typically useful in situations where legacy 75Ω cables are present.

Figure 1-1 illustrates a typical LVDS coaxial connection. It can be used for Gigabit Ethernet connections over a single coax cable.

FIGURE 1-1: TYPICAL LVDS LINK USING EQCO850SC-HS



EQCO850SC.3-HS/EQCO875SC.3-HS

FIGURE 1-2: EQCO850SC.3-HS PIN DIAGRAM (VIEWED FROM TOP)

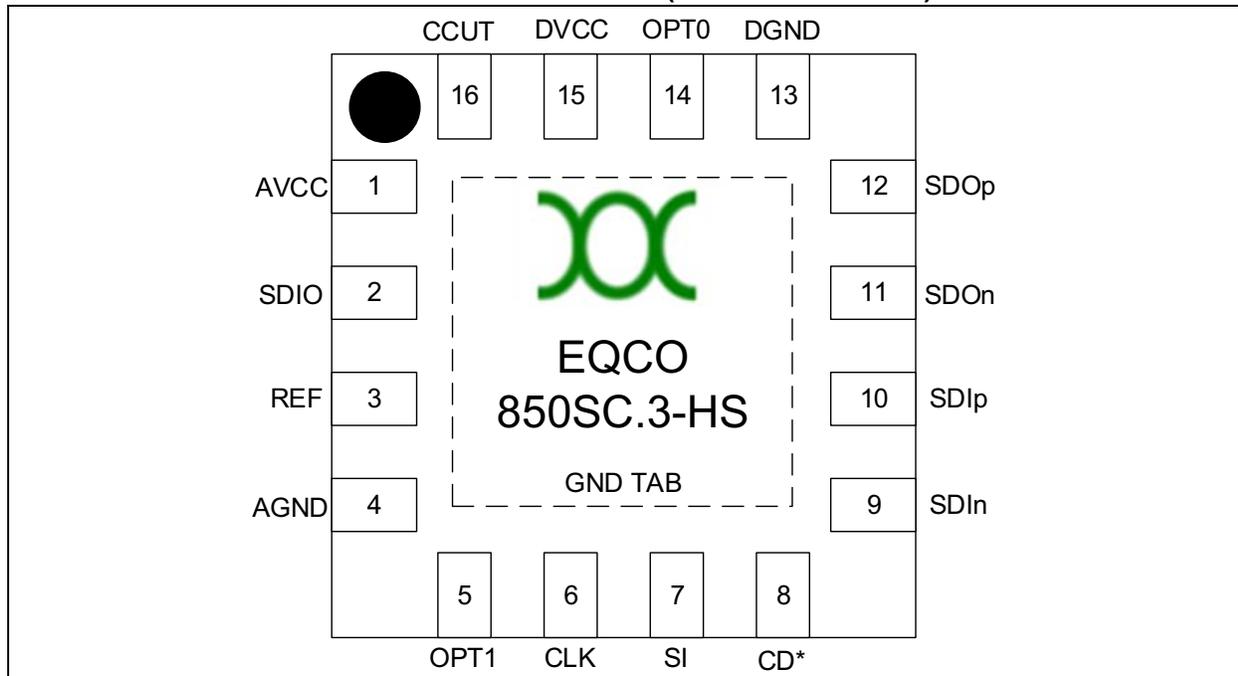
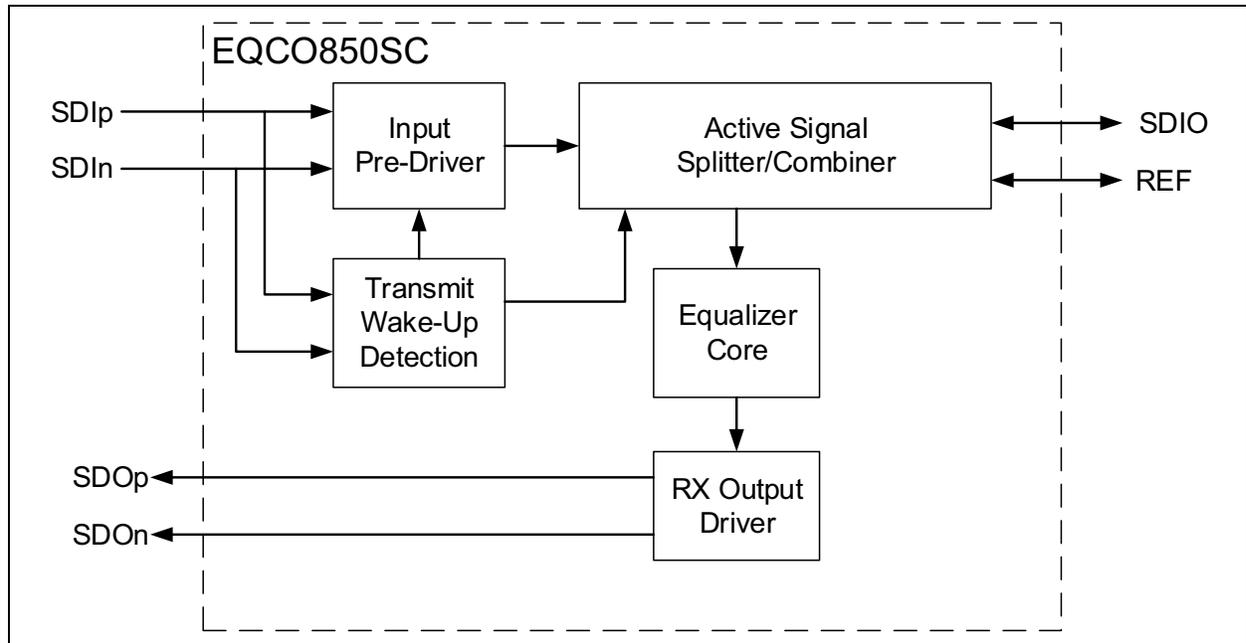


TABLE 1-1: EQCO850SC.3-HS PIN DESCRIPTIONS

Pin Number	Pin Name	Signal Type	Description
(TAB)	GND	Power	Connect to ground of power supply.
15	DVCC	Power	Connect to +3.3V of power supply.
13	DGND	Power	Connect to ground of power supply.
1	AVCC	Power	Analog VCC. Connect to +3.3V of power supply via RF choke and capacitor to cable outer screen.
4	AGND	Power	Analog GND. Connect to cable outer screen.
2	SDIO	Bidirectional	Serial Input/Output. Connect to center conductor of 50Ω coax cable.
3	REF	Bidirectional	Reference. Connect through 50Ω resistor (or impedance matched to cable) to cable outer screen.
8	CD	Output (open drain)	Leave unconnected. Use of this pin is not advised in practice.
10, 9	SDIp/SDIn	Input	Positive/negative differential serial input. Connect to the LVDS output.
12, 11	SDOp/SDOn	Output	Positive/negative differential serial input. Connect to the LVDS input.
14, 5	OPT0, OPT1	Input	Connect Opt0 and Opt1 both to DVCC (3.3V) for correct mode selection.
6, 7	CLK, SI	Input	Used for Production test. Connect to DGND.
16	CCUT	Analog	Not used in LVDS applications. Connect to Pin 15 DVCC.

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FIGURE 1-3: EQCO850SC-HS BLOCK DIAGRAM SHOWING ELECTRICAL CONNECTIONS



1.1 SDIp/SDIn

SDIp/SDIn together form a differential input pair. The serial data received on these pins will be transmitted on SDIO. The Input pre-driver automatically corrects for variations in signal levels and different edge slew rates at these inputs before they go into the Active Splitter/Combiner for transmission over the coax.

SDIp and SDIn inputs are differentially terminated by 100Ω on-chip. The center of the 100Ω is connected to DGND with a 10 kΩ resistor for DC biasing. The inputs also have protection diodes to ground for ESD purposes. Always AC-couple these inputs to the outputs of the LVDS driver.

A Transmit Wake-Up detection circuit puts both the Input pre-driver and the Active Signal Splitter/Combiner into a low-power mode when no signal is detected on the SDIp/SDIn signal pair.

1.2 SDIO/REF

The signal on the SDIO pin is the sum of the incoming signal (i.e. the signal transmitted by the EQCO850SC-HS on the far-end side of the coax) and the outgoing signal (i.e. the signal based on SDIp/SDIn). The far-end signal is extracted by subtraction of the near-end signal, and it is this voltage that the equalizer analyzes and adaptively equalizes for level and frequency response based on the knowledge that the originating signal is DC-balanced and run-length encoded before transmission.

The REF signal carries a precise anti-phase current to the transmit current on SDIO. REF must be connected directly to AGND at the connector (see [Figure 3-1](#)) via a resistor precisely matched to the impedance of the coaxial cable used.

1.3 SDOp/SDOn

SDOp/SDOn together form a differential pair outputting the reconstructed far-end transmit signal. The EQCO850SC-HS uses LVDS drivers with source matching for a 100Ω transmission line. This LVDS signal can normally be connected (subject to input common-mode requirements) directly to the RX signal pair of a standard LVDS receiver.

1.4 CLK, SI

These pins are used for production test and/or reserved for future options. For normal operation, connect them to DGND as indicated in [Table 1-1](#).

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2.0 CIRCUIT OPERATION

2.1 Pre-Driver

The pre-driver removes any dependency on the LVDS transmitter for the amplitude and rise time of the outgoing signal on SDIO.

2.2 Active Signal Splitter/Combiner

The active splitter/combiner controls the amplitude and rise time of the outgoing coax signal and transmits it via a precise 50Ω output termination resistor. The output resistor when balanced with the coax characteristic impedance also forms part of a hybrid splitter circuit which subtracts the TX output from the signal on the SDIO output to give yield the far end TX signal. The return loss of the coax termination is a key factor in the performance of the line hybrid.

2.3 Equalizer Core

The EQCO4850SC-HS has an embedded high-speed equalizer in the receive path with unique characteristics:

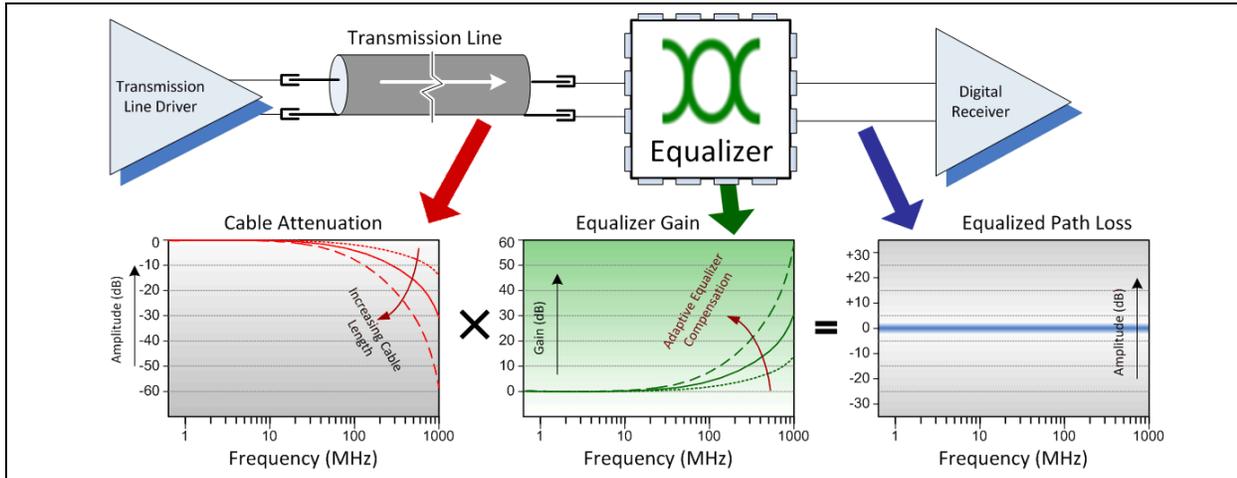
- Auto-adaptive

The equalizer controls a multiple-pole analog filter which compensates for attenuation of the cable, as illustrated in [Figure 2-1](#). The filter frequency response needed to restore the signal is automatically determined by the device using a time-continuous feedback loop that measures the frequency components in the signal. Upon the detection of a valid signal, the control loop converges within a few microseconds.

- Variable gain

EQCO850SC-HSs are used in pairs; one at each end of the coax. The EQCO850SC-HS can be used with any LVDS driver with a differential transmit amplitude in the range of 300 mV to 800 mV; the transmit amplitude on the coax is regulated by the input pre-driver. The receiver equalizer has variable gain to compensate for attenuation through the coax. Example equalizer performance measurements can be found in [Appendix B: Typical Operating Characteristics](#).

FIGURE 2-1: PRINCIPLE OF EQUALIZER OPERATION

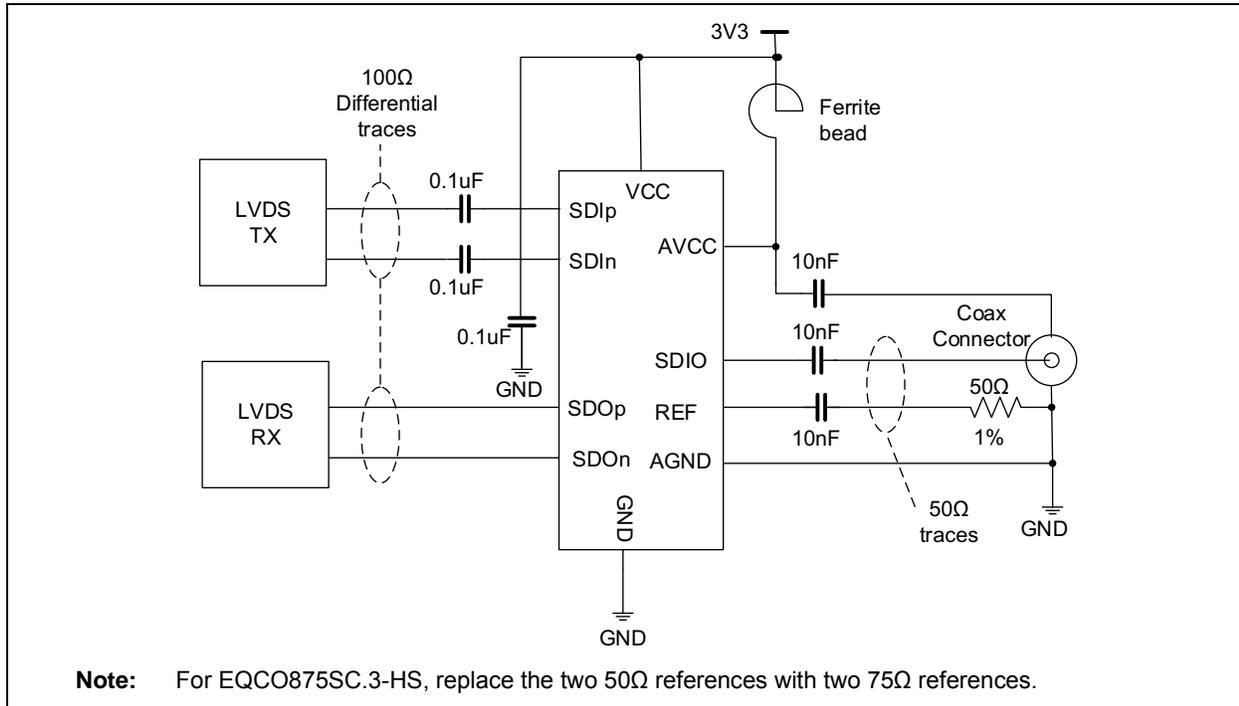


EQCO850SC.3-HS/EQCO875SC.3-HS

3.0 APPLICATION INFORMATION

Figure 3-1 illustrates a typical schematic implementation.

FIGURE 3-1: EQCO850SC.3-HS TYPICAL APPLICATION CIRCUIT



To improve isolation from noise on the board power plane and improve EMC immunity and emissions, it is recommended to power the transmit side of the equalizer (AVCC) through a ferrite bead. A 0.1 µF decoupling capacitor should be placed as close as possible to the chip between the VCC pin and the GND pin. Ground vias should be placed as close as possible to the device GND pins to minimize inductance.

In full duplex, the maximum-length performance depends on the level of near-end crosstalk and far-end return-loss. For full-duplex operation, position the chip close to the used connector.

All the elements need to have impedances according to the choice between a 50Ω system or a 75Ω system: the chips used on both sides, the impedances between the chip and the connector, the PCB connector itself, the connectors on the coax cable and the coax itself. If one impedance is wrong (e.g. a 75Ω BNC connector in a 50Ω system), this impedance discontinuity will cause a reflection, limiting the performance of the full-duplex maximum cable length.

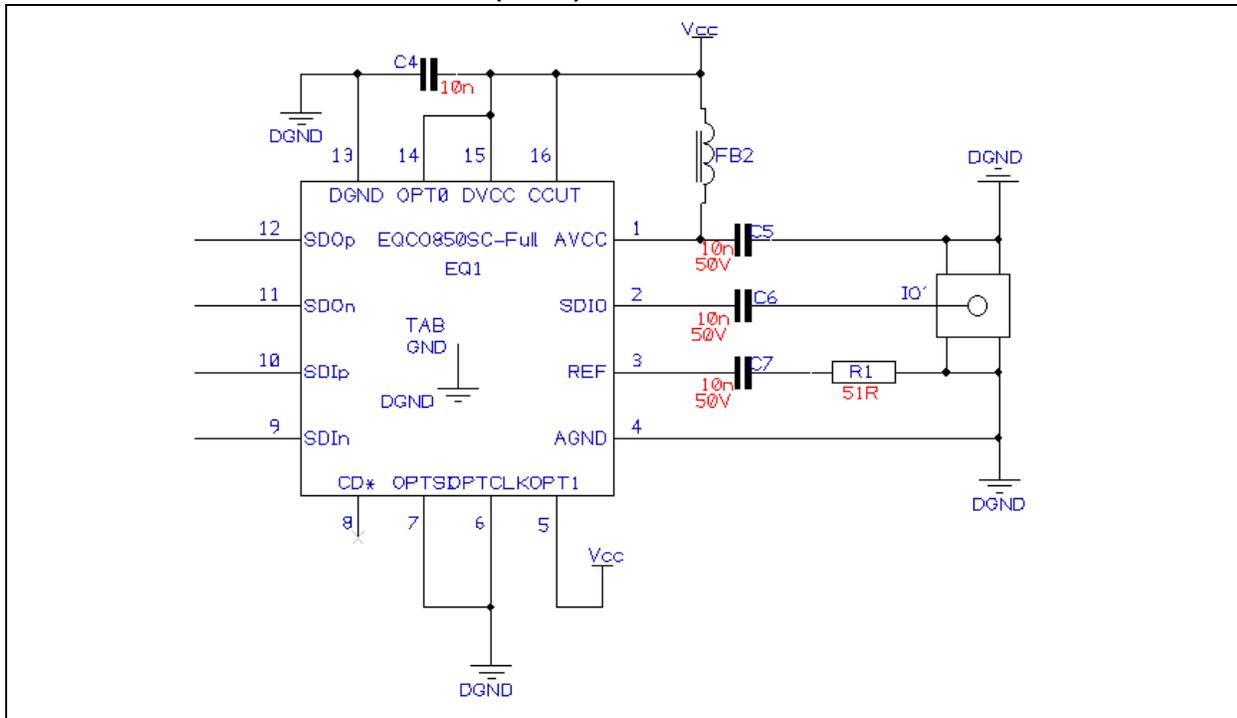
EQCO850SC.3-HS/EQCO875SC.3-HS

3.1 Guidelines for PCB Layout

Because signals are strongly attenuated by long cables, special attention should be paid to the PCB layout between the coaxial connector and the EQCO850SC-HS. The EQCO850SC-HS should be as close as is practical to the coaxial connector. The trace between the coaxial connector and the EQCO850SC-HS (EQCO875SC-HS) must be a 50Ω (75Ω) trace referenced to GND. To avoid noise pickup, other traces carrying digital signals or fast-switching signals should be placed as far away as possible from this trace.

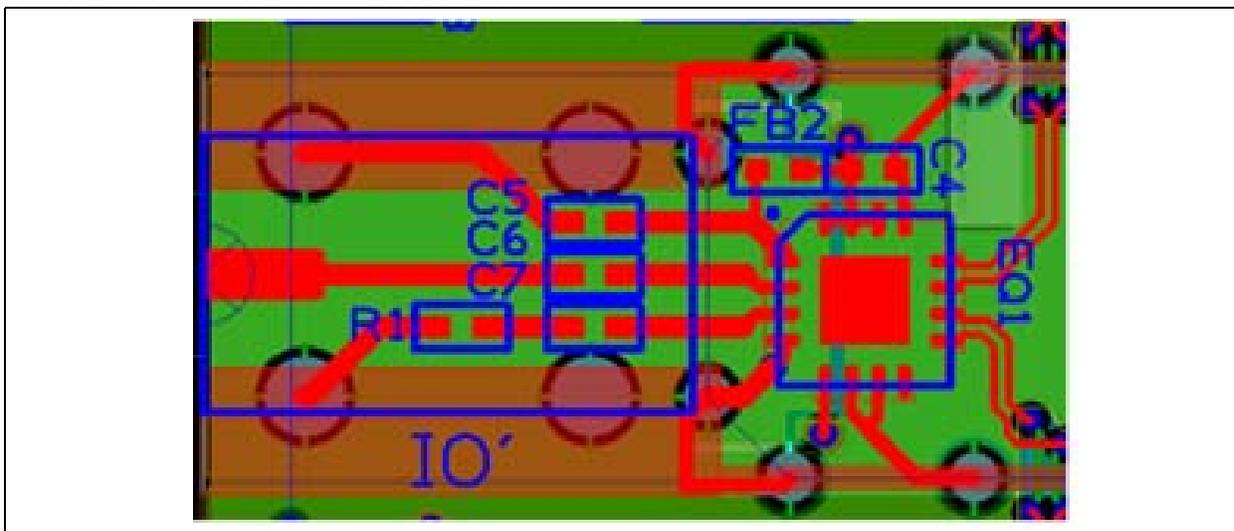
The following diagram shows the layout of the critical section of the PCB, from the coax connector to the twin differential input pairs:

FIGURE 3-2: CIRCUIT DIAGRAM (PART)



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FIGURE 3-3: RECOMMENDED LAYOUT



The ground layout of the EQCO850SC.3-HS is critical to the EMC and EMI performance of the circuit. The AGND connection should be made directly to the body of the connector as shown in [Figure 3-2](#). It should not be connected directly to the GND tab of the chip. Similarly, AVCC should be decoupled directly to the connector body (see position of C5). The termination resistor (R1 in [Figure 3-2](#) and [Figure 3-3](#)) must have its ground connection at the connector body and C7, and the connection between R1 and the connector must be kept as short as possible. The impedance of all the traces must be well-controlled, including on the connector itself.

The SDIp/SDIn and SDOp/SDOn differential traces should be matched in length to minimize time of arrival skew. For traces longer than a few millimeters, the impedance of the differential transmit and receive signals should be laid out as 100 Ω differential traces and the termination to the PHY should be placed close to the PHY, not to the EQCO850SC.3-HS.

[Figure 3-1](#) and [Figure 3-2](#) do not include power over coax, but when customers want to include power over coax, they should contact Microchip for recommended component selection. Component selection will depend on customer requirements.

Microchip can design a PCB layout capable of maximum cable length for any combination of impedance system (50 Ω or 75 Ω) and coax connector (SMA, BNC, DIN, SMB, etc.) on request.

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NOTES:

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4.0 ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

Stresses beyond those listed under this section may cause permanent damage to the device. These are stress ratings only and are not tested. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 4-1: ABSOLUTE MAXIMUM RATINGS

Parameter	Min.	Typ.	Max.	Units	Conditions
Storage Temperature	-65	—	+150	°C	
Ambient Temperature	-55	—	+125	°C	Power Applied
Operating Temperature	-40	—	+85	°C	Normal Operation (VCC = 3.3V ±5%)
Supply Voltage to Ground	-0.5	—	+4.0	V	
DC Input Voltage	-0.5	—	+4.0	V	
DC Voltage to Outputs	-0.5	—	+4.0	V	
Current into Outputs	—	—	90	mA	Outputs Low

TABLE 4-2: ELECTRICAL CHARACTERISTICS (OVER THE OPERATING VCC AND -40 TO +85°C RANGE)

Parameter	Min.	Typ.	Max.	Unit	Description
Power Supply					
V _{CC}	3.135	3.3	3.465	V	Supply voltage.
I _S	47.5	62.5	75.5	mA	Supply current, both transmitting and receiving.
I _{SR}	25	35	43	mA	Supply current when only receiving.
SDI_p/SDI_n Input (LVDS-like)					
ΔV _i	250	—	800	mV	Input amplitude V _{SDI_{p,n}} .
V _{turnon}	80	140	200	mV	Minimal ΔV _i to turn on transmit function.
V _{cmin}	Note 4	0	Note 4	V	Common-mode input voltage (terminated to DGND via 10 kΩ and with protection diodes).
R _{input}	93	104	117	Ω	Differential input termination.
SDIO Connection to Coax					
Z _{coax}	48 (72)	50 (75)	52 (78)	Ω	Coax cable characteristic impedance.
R _{SDIO}	46 (69)	51 (76)	55 (82)	Ω	Input impedance between SDIO and AGND.
R _{loss}	15	—	—	dB	Coax return-loss as seen on SDIO pin. Frequency range = 10 MHz-625 MHz.
ΔV _{TX}	270	325	380	mV	Transmit amplitude.
t _{rise_tx}	350	450	550	ps	Rise/fall time 20% to 80% of ΔV _{TX} .
Att _{max}	—	12	—	dB	Cable attenuation budget @ 625 MHz.
ΔV _{RXmin}	—	40	—	mV	Minimum input for fully reconstructed output.

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TABLE 4-2: ELECTRICAL CHARACTERISTICS (OVER THE OPERATING VCC AND -40 TO +85°C RANGE) (CONTINUED)

SDOp/SDOn Outputs (LVDS-compatible)					
ΔV_o	300	350	400	mV	Output amplitude $V_{SDOp,n}$.
V_{cmout}	1.1	1.2	1.3	V	Common-mode output voltage.
ΔV_{o_off}	-20	0	20	mV	Output amplitude $V_{SDOp,n}$ with equalizer off.
R_{output}	92	102	115	Ω	Differential termination between SDOp and SDOn.
t_{rise_o}	150	240	350	ps	Rise/fall time 20% to 80% of $V_{SDOp,n}$.

TABLE 4-3: JITTER PERFORMANCE

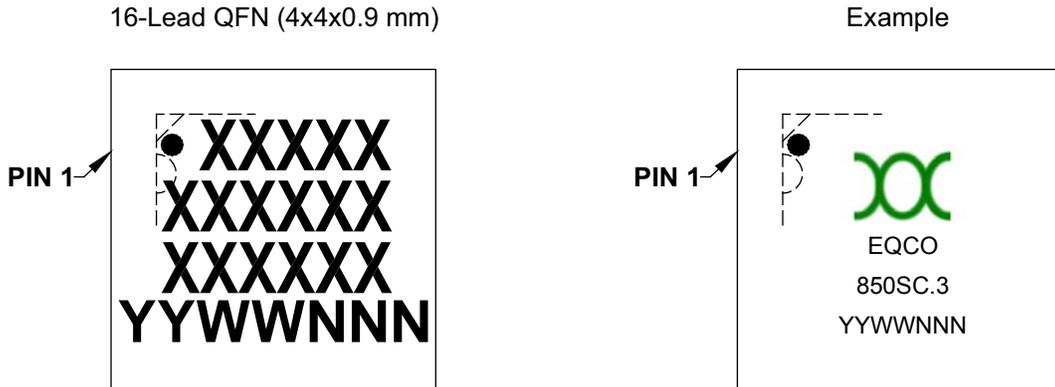
Parameter	Min.	Typ.	Max.	Units	Conditions
Jitter peak-to-peak on SDO	—	70	230	ps	1m RG174 coax; over full V_{CC} , ΔV_{TX} , and temp range; 125-1250 Mbps; pattern PRBS7
Jitter peak-to-peak on SDO	—	170	300	ps	16m RG174 coax; over full V_{CC} , ΔV_{TX} , and temp range; 125-1250 Mbps; pattern PRBS7

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5.0 PACKAGING INFORMATION

5.1 Package Marking Information

16-Lead Plastic Quad Flat, No Lead Package – 4x4x0.9 mm Body [QFN]



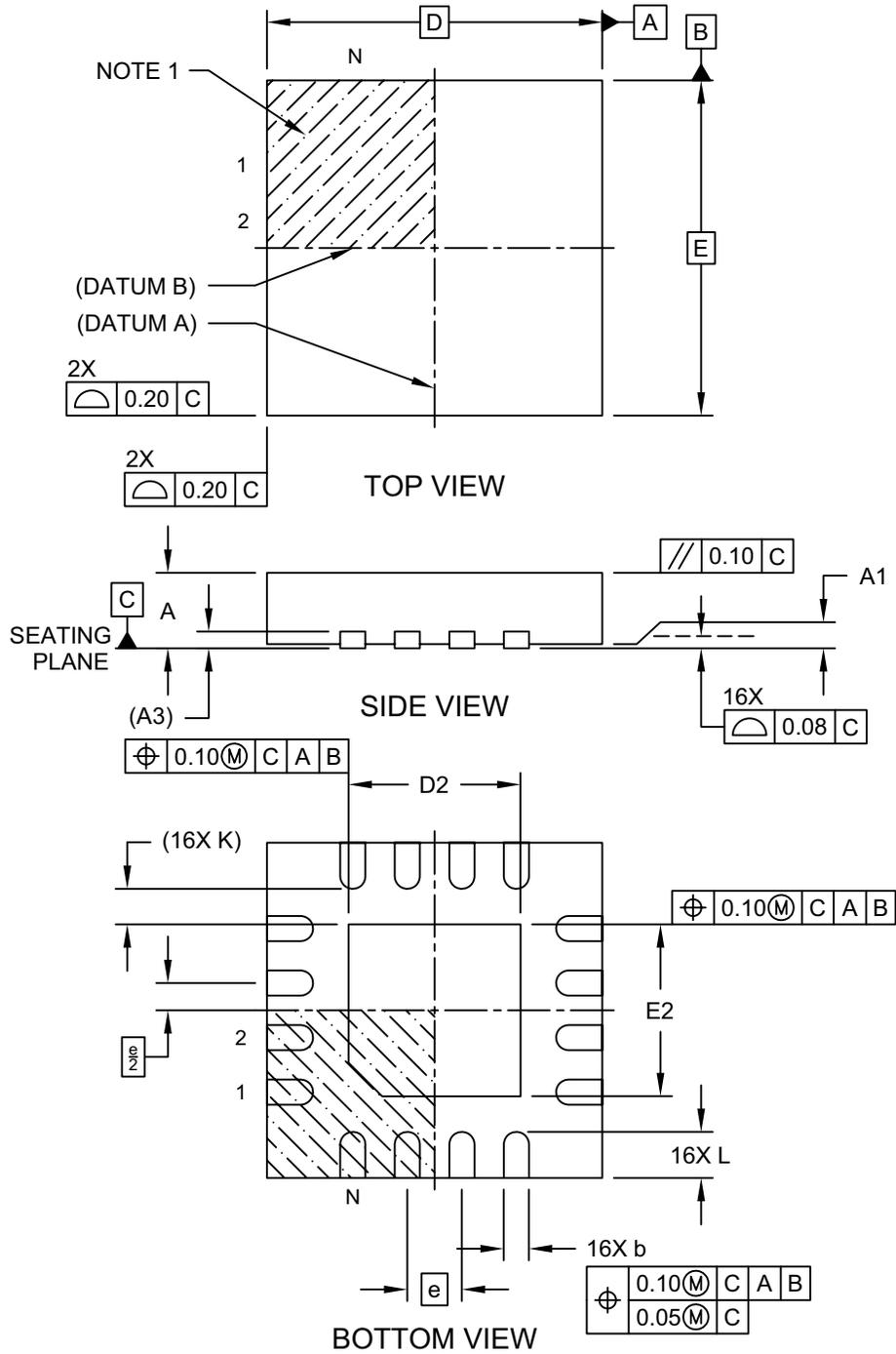
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC [®] designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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16-Lead Plastic Quad Flat, No Lead Package (8E) - 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

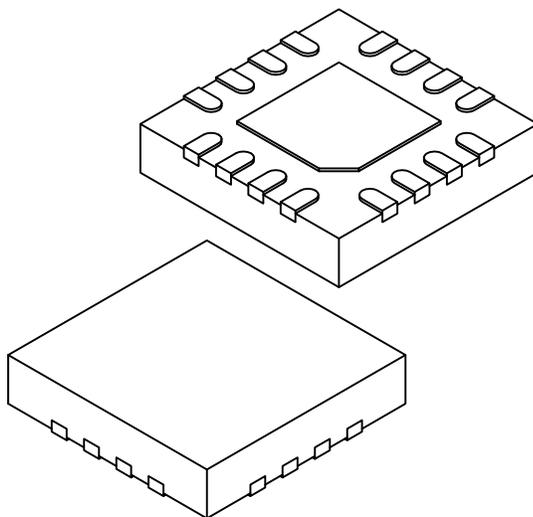


Microchip Technology Drawing C04-259B Sheet 1 of 2

EQCO850SC.3-HS/EQCO875SC.3-HS

16-Lead Plastic Quad Flat, No Lead Package (8E) - 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	16		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.87	0.95
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Width	E	4.00 BSC		
Exposed Pad Width	E2	1.95	2.05	2.15
Overall Length	D	4.00 BSC		
Exposed Pad Length	D2	1.95	2.05	2.15
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.45	0.55	0.65
Terminal-to-Exposed-Pad	K	0.425 REF		

Notes:

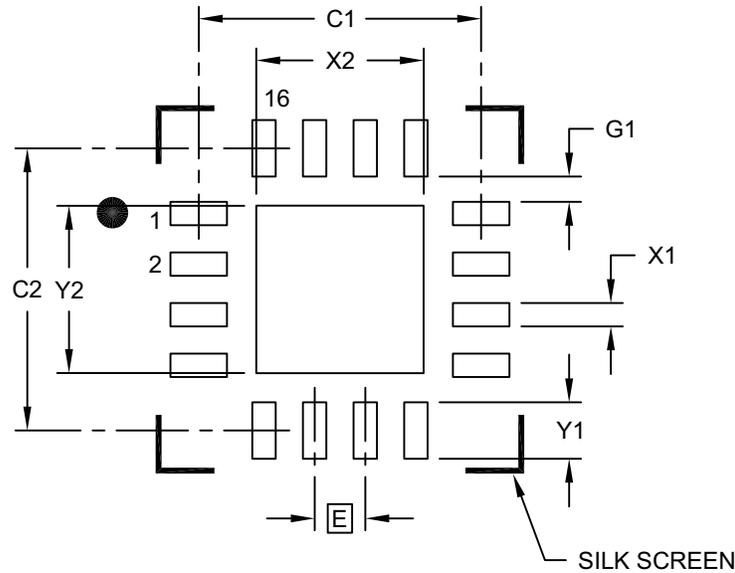
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-259B Sheet 2 of 2

EQCO850SC.3-HS/EQCO875SC.3-HS

16-Lead Plastic Quad Flat, No Lead Package (8E) - 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			2.15
Optional Center Pad Length	Y2			2.15
Contact Pad Spacing	C1		3.625	
Contact Pad Spacing	C2		3.625	
Contact Pad Width (X16)	X1			0.30
Contact Pad Length (X16)	Y1			0.725
Contact Pad to Center Pad (X16)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2259A

EQCO850SC.3-HS/EQCO875SC.3-HS

APPENDIX A: REVISION HISTORY

Revision C (April 2016)

- Revised Section 1.1 SDIp/SDIn

Revision B (April 2016)

- Updated [Section 5.0 “Packaging Information”](#).
- Removed electrostatic discharge ratings from [Table 4-1](#).
- Minor typographical changes.

Revision A (July 2015)

- This is the initial release of the document in the Microchip format. This replaces EqcoLogic document version 2.0.

TABLE A-1: REVISION HISTORY

Revision Level	Date	Correction
2v0	1/28/14	Targeting data sheet for LVDS and Gigabit Ethernet applications. Merging 50Ω and 75Ω systems into one data sheet. Temperature limits set to -45°C to +85°C.
1v0	4/30/10	Based on the EQCO800SC generic data sheet, adapted for LVDS

EQCO850SC.3-HS/EQCO875SC.3-HS

APPENDIX B: TYPICAL OPERATING CHARACTERISTICS

All measurements at $V_{CC} = 3.3V$, $temp = +25^{\circ}C$, data pattern = PRBS9, 630 mV PHY transmit amplitude.

FIGURE B-1: TYPICAL EYE AT SDO_p WITH A 1M COAX TYPE RG174

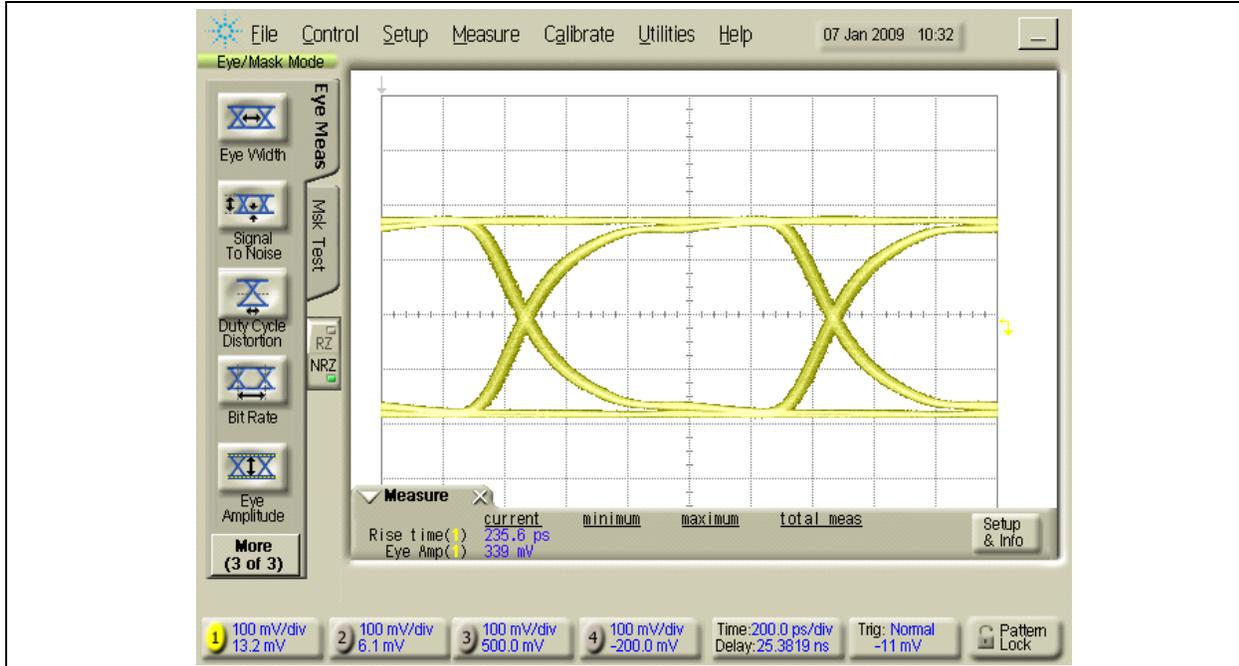
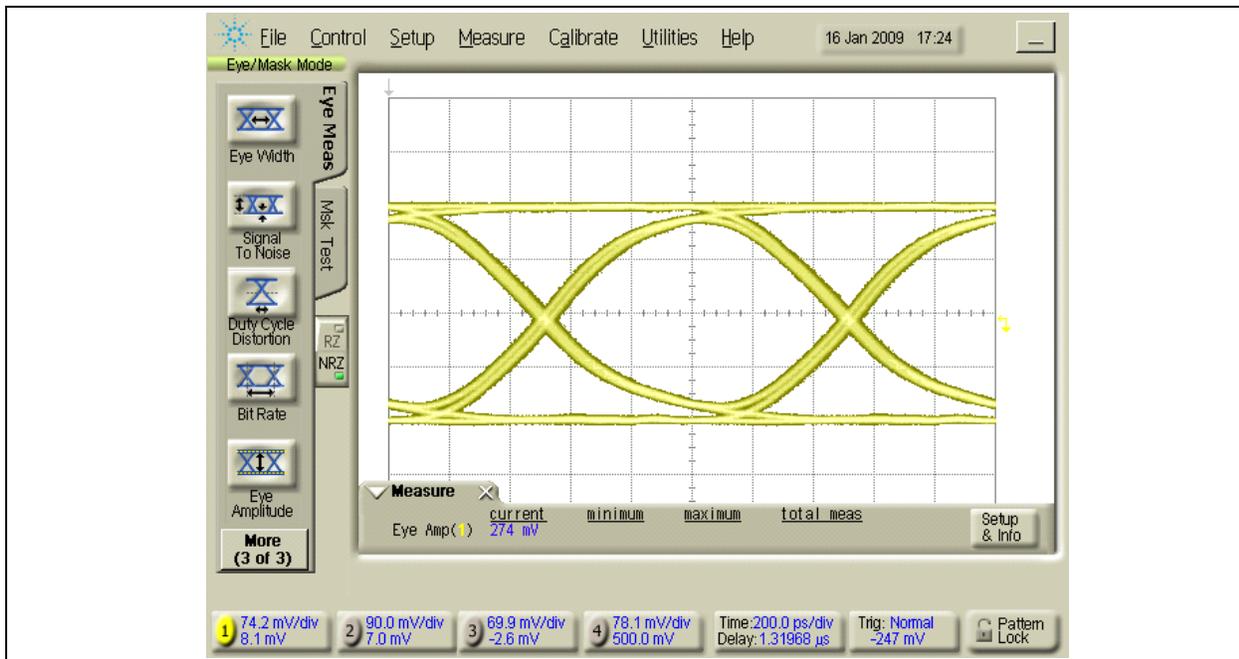


FIGURE B-2: TYPICAL EYE AT SDIO OUTPUT THROUGH 1M COAX CABLE



EQCO850SC.3-HS/EQCO875SC.3-HS

The following figures show a typical system link EYE-diagram at room temperature through a variable cable length full and half duplex. The differential output $V_{SD0p}-V_{SD0n}$ is shown. The duty cycle distortion is due to the use of a shielded twisted pair cable/connector. Duty cycle distortion is normally very small.

FIGURE B-3: 1M RG174, HALF-DUPLEX

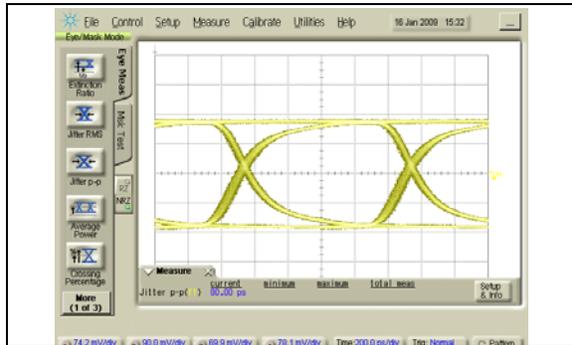


FIGURE B-7: 1M RG174, HALF-DUPLEX

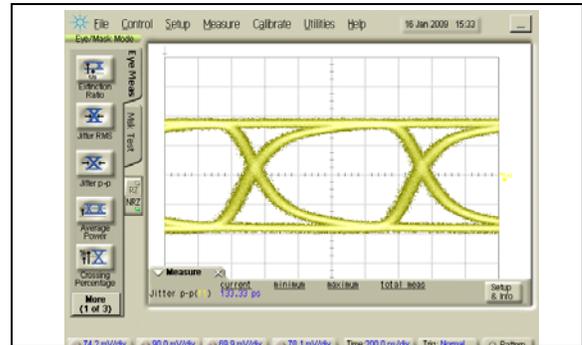


FIGURE B-4: 5M RG174, HALF-DUPLEX

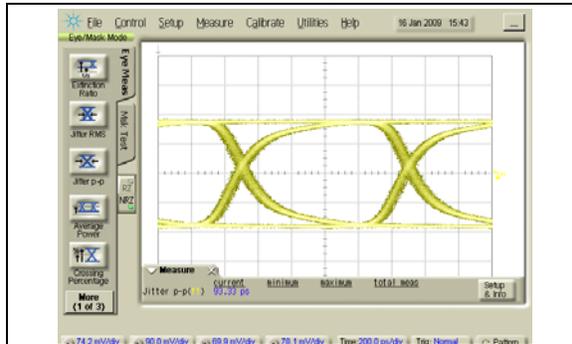


FIGURE B-8: 5M RG174, HALF-DUPLEX

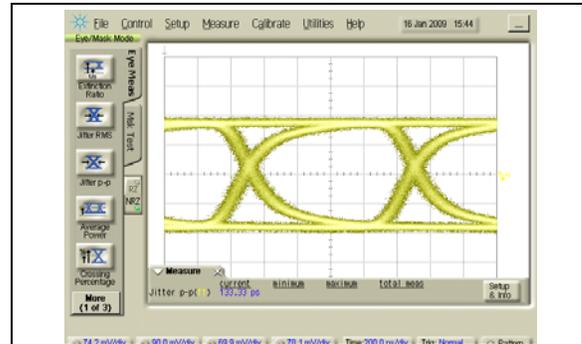


FIGURE B-5: 10M RG174, HALF-DUPLEX

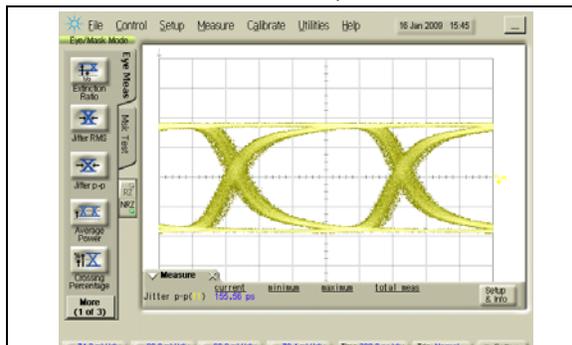


FIGURE B-9: 10M RG174, HALF-DUPLEX

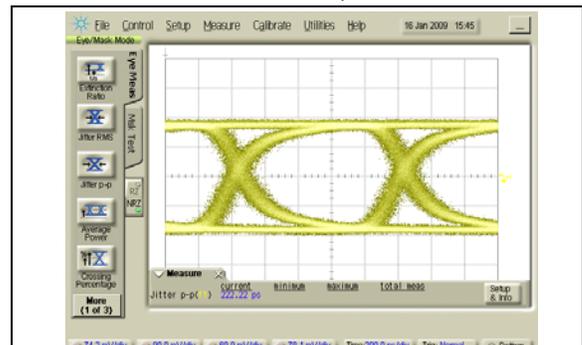


FIGURE B-6: 20M RG174, HALF-DUPLEX

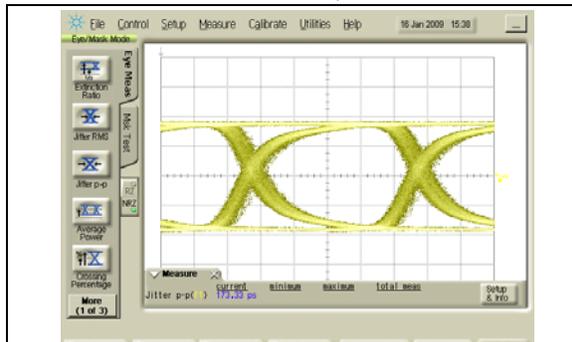
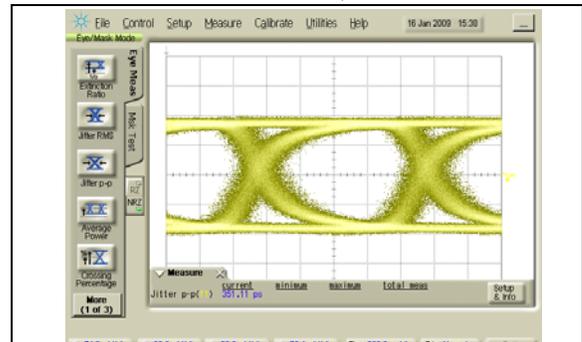


FIGURE B-10: 20M RG174, HALF-DUPLEX



EQCO850SC.3-HS/EQCO875SC.3-HS

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Technical support is available through the website at: <http://microchip.com/support>

EQCO850SC.3-HS/EQCO875SC.3-HS

PRODUCT IDENTIFICATION SYSTEM

To order parts, including industrial, or obtain information, for e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>XXXX</u>
Device	Package
Device: EQCO850SC.3-HS EQCO875SC.3-HS	
Package: TRAY = Tray "blank" = Tube	

Examples:

a) EQCO850SC.3-HS-TRAY = 50Ω Coax,
Industrial temperature,
16-Lead QFN package,
Tray packaging

b) EQCO875SC.3-HS = 75Ω Coax,
Industrial temperature,
16-Lead QFN package,
Tube packaging

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