

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit	
Drain-Source Voltage			VDSS	-40	V	
Gate-Source Voltage			Vgss	±20		
Continuous Drain Current	V _{GS} = -10V	(Notes 6 & 8)	al	-7.6	A	
		T _A = +70°C (Notes 6 & 8)		-6.1		
		(Notes 5 & 8)		-5.8		
		(Notes 5 & 9)		-6.9		
Pulsed Drain Current	Vgs = -10V	(Notes 7 & 8)	IDM	-28.0		
Continuous Source Current (Body Diode)		(Notes 6 & 8)	Is	-7.6]	
Pulsed Source Current (Body Diode)		(Notes 7 & 8)	I _{SM}	-28.0		
Avalanche Current (Note 8) L = 0.3mH		(Note 11)	las	-23	Α	
Avalanche Energy (Note 8) L = 0.3mH (Note		(Note 11)	Eas	79	mJ	

Thermal Characteristics (@TA = +25°C, unless otherwise specified.)

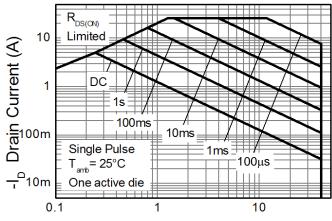
Characteristic	Symbol	Value	Unit	
D	(Notes 6 & 8)		2.14	
Power Dissipation Linear Derating Factor	(Notes 5 & 8)	PD	1.25	W
Linear Derating Factor	(Notes 5 & 9)		1.8	
	(Notes 6 & 8)		58	
Thermal Resistance, Junction to Ambient	(Notes 5 & 8)	R _{θJA}	100	900
	(Notes 5 & 9)		70	•C/W
hermal Resistance, Junction to Lead (Notes 8 & 10)		Rejl	51	
Operating and Storage Temperature Range	TJ, TSTG	-55 to +150	°C	

Notes:

- 5. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
- 6. Same as note (5), except the device is measured at $t \le 10$ sec.
- 7. Same as note (5), except the device is pulsed with D = 0.02 and pulse width $300 \mu s$.
- 8. For a dual device with one active die.
- 9. For a device with two active die running at equal power.
- 10. Thermal resistance from junction to solder-point (at the end of the drain lead).
- 11. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.



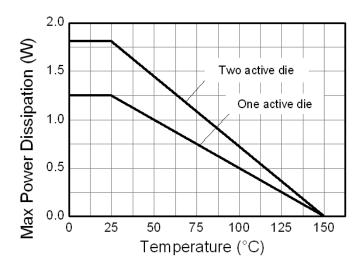
Thermal Characteristics



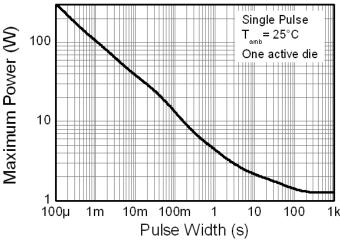
-V_{DS} Drain-Source Voltage (V)
P-channel Safe Operating Area

R(theta junction-to-ambient), R_{eJA} 100 Thermal Resistance (°C/W) One active die 80 60 D = 0.540 Single Pulse D = 0.2D=0.05 20 D = 0.110m 100m 10 100µ 1m 100 1k Pulse Width (s)

Transient Thermal Impedance



Derating Curve



Pulse Power Dissipation



Electrical Characteristics ($@T_A = +25$ °C, unless otherwise specified.)

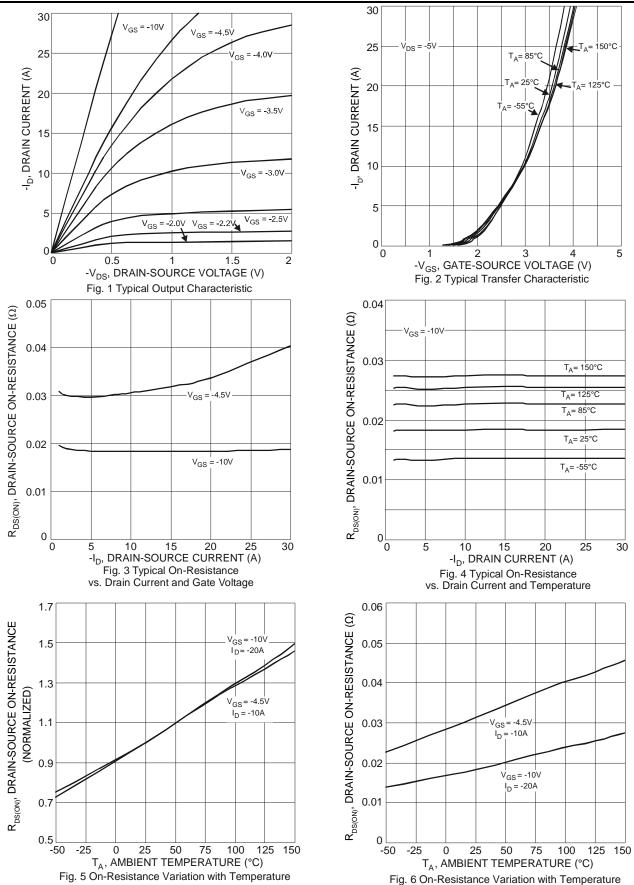
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage	BV _{DSS}	-40	_	_	V	I _D = -250µA, V _G S = 0V	
Zero Gate Voltage Drain Current	IDSS	_	_	-1.0	μΑ	V _{DS} = -40V, V _{GS} = 0V	
Gate-Source Leakage	Igss	_	_	±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$	
ON CHARACTERISTICS	ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	-0.8	-1.3	-1.8	V	I _D = -250μA, V _{DS} = V _{GS}	
Statia Drain Sauras On Basistanas (Nota 12)	_	_	18	25	mΩ	Vgs = -10V, ID = -3A	
Static Drain-Source On-Resistance (Note 12)	RDS(ON)		30	45		V _{GS} = -4.5V, I _D = -3A	
Forward Transconductance (Notes 12 & 13)	g FS	_	16.6	_	S	$V_{DS} = -5V, I_{D} = -3A$	
Diode Forward Voltage (Note 12)	V_{SD}	_	-0.7	-1.0	V	I _S = -1A, V _{GS} = 0V	
DYNAMIC CHARACTERISTICS (Note 13)						•	
Input Capacitance	Ciss	_	1640	_		V _{DS} = -20V, V _{GS} = 0V f = 1MHz	
Output Capacitance	Coss	_	179	_	pF		
Reverse Transfer Capacitance	Crss	_	128	_	I = IMHZ		
Gate Resistance	Rg	_	6.43	_	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$	
Total Gate Charge (Note 14)	Qg	_	14.0	_		Vgs = -4.5V	
Total Gate Charge (Note 14)	Qg	_	33.7	_	nC	V _{DS} = -20V	= -20V
Gate-Source Charge (Note 14)	Qgs	_	5.5	_	nC	V _G S = -10V	-3A
Gate-Drain Charge (Note 14)	Qgd	_	7.3	_			
Turn-On Delay Time (Note 14)	tD(ON)	_	6.9	_		V _{DD} = -20V, V _{GS} = -10V I _D = -3A	
Turn-On Rise Time (Note 14)	t _R		14.7	_			
Turn-Off Delay Time (Note 14)	t _{D(OFF)}	_	53.7	_	ns		
Turn-Off Fall Time (Note 14)	tF	_	30.9		1		

Notes:

^{12.} Measured under pulsed conditions. Pulse width ≤ 300µs; duty cycle ≤ 2%.
13. For design aid only, not subject to production testing.
14. Switching characteristics are independent of operating junction temperatures.



Typical Characteristics





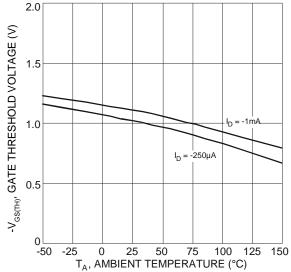
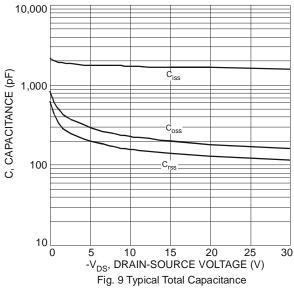
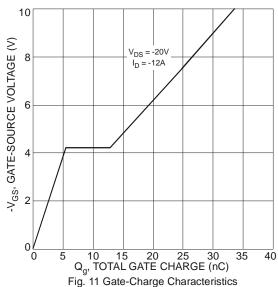
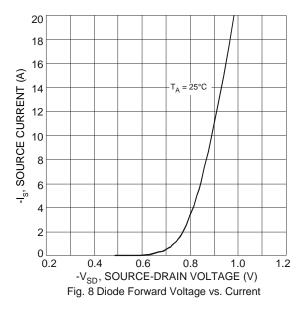
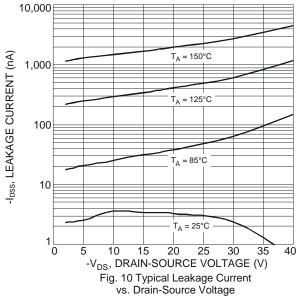


Fig. 7 Gate Threshold Variation vs. Ambient Temperature





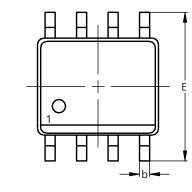


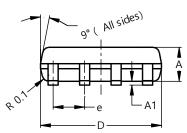


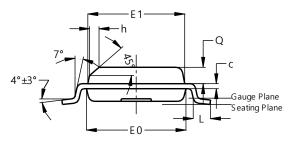


Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.







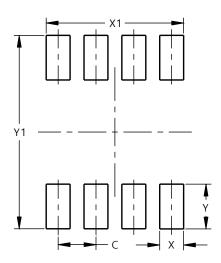
SO-8

SO-8					
Dim	Min	Max	Тур		
Α	1.40	1.50	1.45		
A1	0.10	0.20	0.15		
b	0.30	0.50	0.40		
С	0.15	0.25	0.20		
D	4.85	4.95	4.90		
Е	5.90	6.10	6.00		
E1	3.80	3.90	3.85		
E0	3.85	3.95	3.90		
е			1.27		
h			0.35		
L	0.62	0.82	0.72		
Ø	0.60	0.70	0.65		
All Dimensions in mm					

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.





Dimensions	Value (in mm)
С	1.27
X	0.802
X1	4.612
Υ	1.505
V1	6.50



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