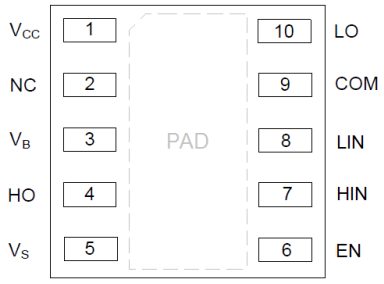
Pin Diagrams

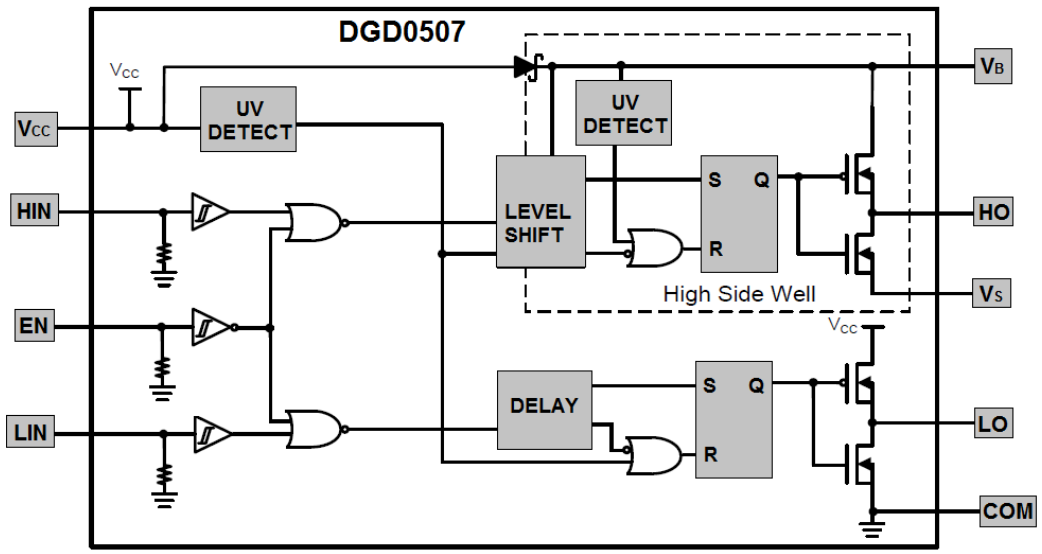


Top View: W-DFN3030-10 (Type TH)

Pin Descriptions

Pin Number	Pin Name	Function
1	V_{CC}	Low-Side and Logic Supply
2	NC	No Connect (No Internal Connection)
3	V_B	High-Side Floating Supply
4	HO	High-Side Gate Drive Output
5	V_S	High-Side Floating Supply Return
6	EN	Logic Input Enable, a Logic Low Turns off Gate Driver
7	HIN	Logic Input for High-Side Gate Driver, in Phase with HO
8	LIN	Logic Input for Low-Side Gate Driver, in Phase with LO
9	COM	Low-Side and Logic Return
10	LO	Low-Side Gate Drive Output
PAD	Substrate	Connect to COM on PCB

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
High-Side Floating Positive Supply Voltage	V_B	-0.3 to +50	V
High-Side Floating Negative Supply Voltage	V_S	V_B-14 to V_B+0.3	V
High-Side Floating Output Voltage	V_{HO}	V_S-0.3 to V_B+0.3	V
Offset Supply Voltage Transient	dV_S / dt	50	V/ns
Logic and Low-Side Fixed Supply Voltage	V_{CC}	-0.3 to +15	V
Low-Side Output Voltage	V_{LO}	-0.3 to V_{CC}+0.3	V
Logic Input Voltage (HIN, LIN and EN)	V_{IN}	-0.3 to 15	V

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation Linear Derating Factor (Note 5)	P_D	0.4	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	64	°C/W
Thermal Resistance, Junction to Case (Note 5)	$R_{\theta JC}$	42	°C/W
Operating Temperature	T_J	+150	°C
Lead Temperature (Soldering, 10s)	T_L	+300	
Storage Temperature Range	T_{STG}	-55 to +150	

Note: 5. When mounted on a standard JEDEC 2-layer FR-4 board.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
High-Side Floating Supply	V_B	V_S + 8	V_S + 14	V
High-Side Floating Supply Offset Voltage	V_S	(Note 6)	50 (Note 7)	V
High-Side Floating Output Voltage	V_{HO}	V_S	V_B	V
Logic and Low Side Fixed Supply Voltage	V_{CC}	8	14	V
Low-Side Output Voltage	V_{LO}	0	V_{CC}	V
Logic Input Voltage (HIN, LIN and EN)	V_{IN}	0	5	V
Ambient Temperature	T_A	-40	+125	°C

Notes: 6. Logic operation for V_S of -5V to +50V. Logic state held for V_S of -5V to -V_{BS}.
7. Provided V_B doesn't exceed absolute maximum rating of 50V.

DC Electrical Characteristics (V_{CC} = V_{BS} = 12V, COM = V_S = 0V, @T_A = +25°C, unless otherwise specified.) (Note 8)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Logic "1" Input Voltage	V_{IH}	2.4	–	–	V	–
Logic "0" Input Voltage	V_{IL}	–	–	0.8	V	–
Enable Logic "1" Input Voltage	V_{ENIH}	1.5	–	–	V	–
Enable Logic "0" Input Voltage	V_{ENIL}	–	–	0.7	V	–
Input Voltage Hysteresis	V_{INHYS}	–	0.6	–	V	–
Enable Input Voltage Hysteresis	$V_{ENINHYS}$	–	0.1	–	V	–
High Level Output Voltage, V_{BIAS} - V_O	V_{OH}	–	0.45	0.6	V	I_{O+} = 100mA
Low Level Output Voltage, V_O	V_{OL}	–	0.15	0.22	V	I_{O-} = 100mA
Offset Supply Leakage Current	I_{LK}	–	10	50	µA	V_B = V_S = 50V
V_{CC} Shutdown Supply Current	I_{CCSD}	–	0	1	µA	V_{IN} = 0V or 5V, V_{EN} = 0V
V_{CC} Quiescent Supply Current	I_{CCQ}	100	150	200	µA	V_{IN} = 0V or 5V
V_{CC} Operating Supply Current	I_{CCOP}	–	2.1	3.0	mA	fs = 500kHz
V_{BS} Quiescent Supply Current	I_{BSQ}	–	62	100	µA	V_{IN} = 0V or 5V
V_{BS} Operating Supply Current	I_{BSOP}	–	1.1	2.0	mA	fs = 500kHz
Logic "1" Input Bias Current	I_{IN+}	–	–	50	µA	V_{IN} = 5V
Logic "0" Input Bias Current	I_{IN-}	–	–	5	µA	V_{IN} = 0V
Enable Logic "1" Input Bias Current	I_{ENIN+}	–	43	60	µA	V_{IN} = 5V
Enable Logic "0" Input Bias Current	I_{ENIN-}	–	0	5	µA	V_{IN} = 0V
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	5.9	6.9	7.9	V	–
V_{BS} Supply Undervoltage Negative Going Threshold	V_{BSUV-}	5.6	6.6	7.6	V	–
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	5.9	6.9	7.9	V	–
V_{CC} Supply Undervoltage Negative Going Threshold	V_{CCUV-}	5.6	6.6	7.6	V	–
Output High Short Circuit Pulsed Current	I_{O+}	0.9	1.25	–	A	V_O = 0V, PW ≤ 10µs
Output Low Short Circuit Pulsed Current	I_{O-}	1.5	2.0	–	A	V_O = 15V, PW ≤ 10µs
Forward Voltage of Bootstrap Diode	V_{F1}	–	0.27	–	V	I_F = 100µA
Forward Voltage of Bootstrap Diode	V_{F2}	–	0.8	–	V	I_F = 100mA

Note: 8. The V_{IN} and I_{IN} parameters are applicable to the two logic pins: HIN, LIN and EN. The V_O and I_O parameters are applicable to the respective output pins: HO and LO.

AC Electrical Characteristics (V_{CC} = V_{BS} = 12V, COM = V_S = 0V, C_L = 1000pF, @T_A = +25°C, unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Turn-On Propagation Delay	t_{ON}	–	20	35	ns	–
Turn-Off Propagation Delay	t_{OFF}	–	23	56	ns	V_S = 50V
Delay Matching, HO & LO Turn-On	t_{DM}	–	–	5	ns	–
Turn-On Rise Time	t_R	–	23	35	ns	–
Turn-Off Fall Time	t_F	–	18	25	ns	–

Timing Waveforms

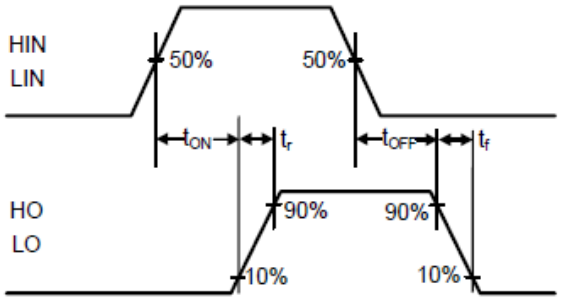


Figure 1. Switching Time Waveform Definitions

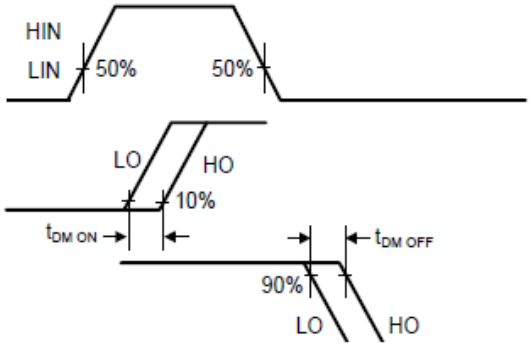


Figure 2. Delay Matching Waveform Definitions

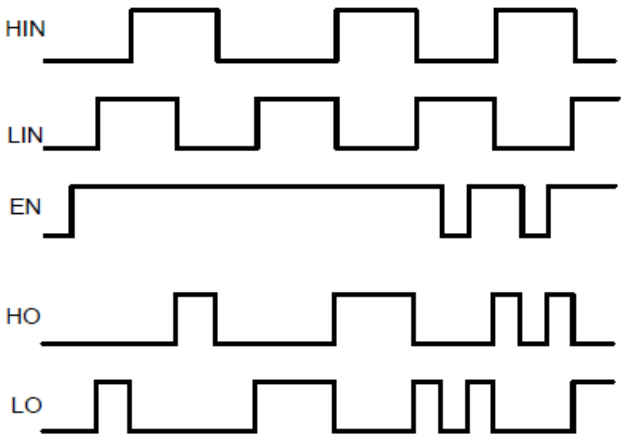


Figure 3. Input / Output Timing Diagram

Typical Performance Characteristics (@T_A = +25°C, unless otherwise specified.)

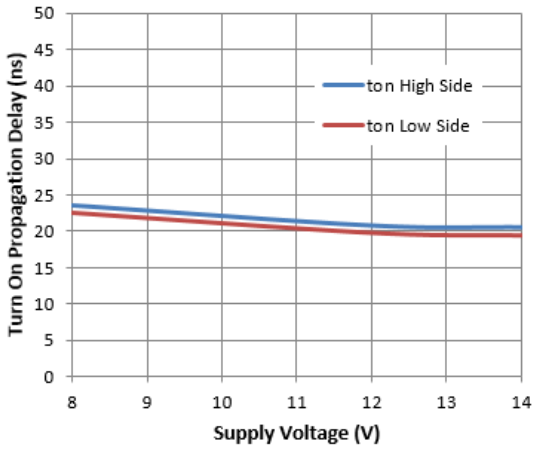


Figure 4. Turn-on Propagation Delay vs. Supply Voltage

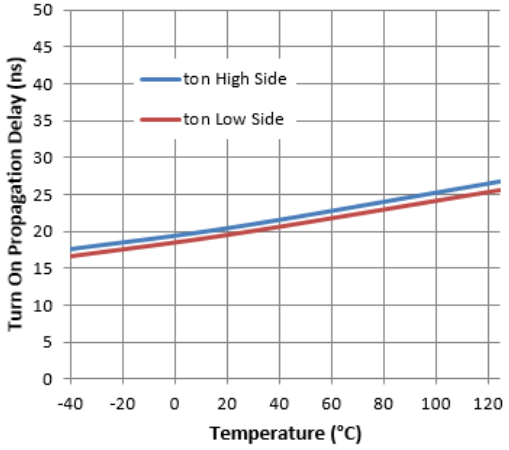


Figure 5. Turn-on Propagation Delay vs. Temperature

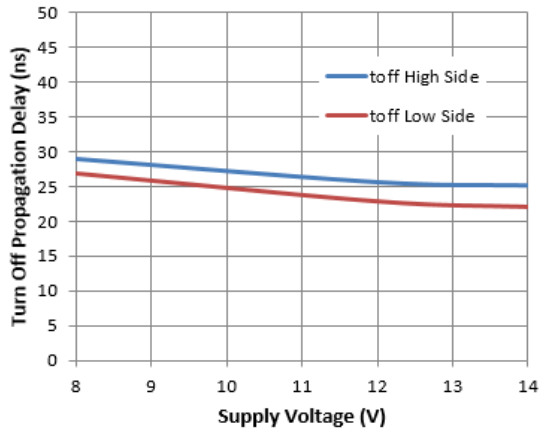


Figure 6. Turn-off Propagation Delay vs. Supply Voltage

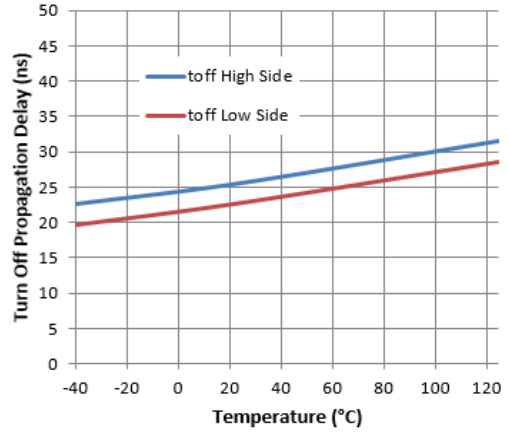


Figure 7. Turn-off Propagation Delay vs. Temperature

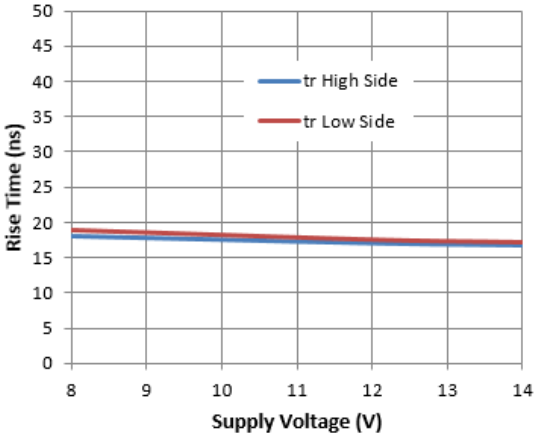


Figure 8. Rise Time vs. Supply Voltage

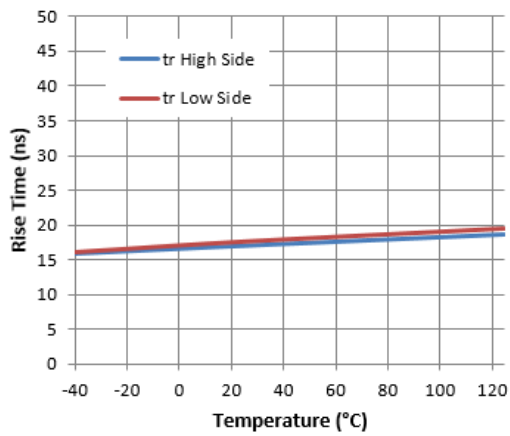


Figure 9. Rise Time vs. Temperature

Typical Performance Characteristics (Cont.)

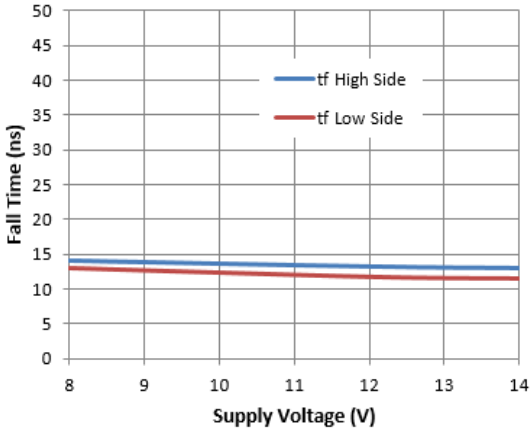


Figure 10. Fall Time vs. Supply Voltage

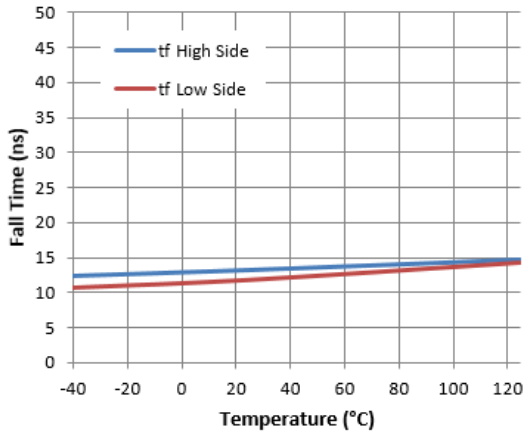


Figure 11. Fall Time vs. Temperature

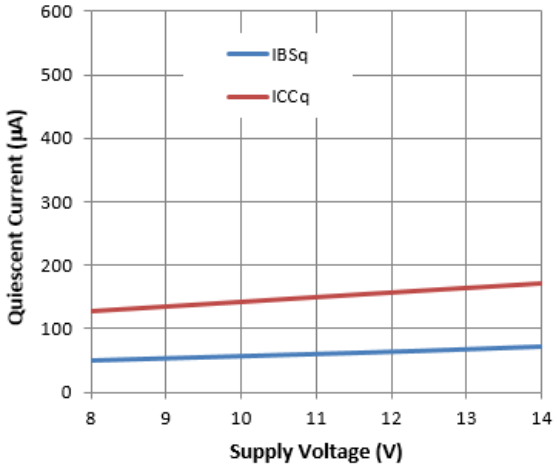


Figure 12. Quiescent Current vs. Supply Voltage

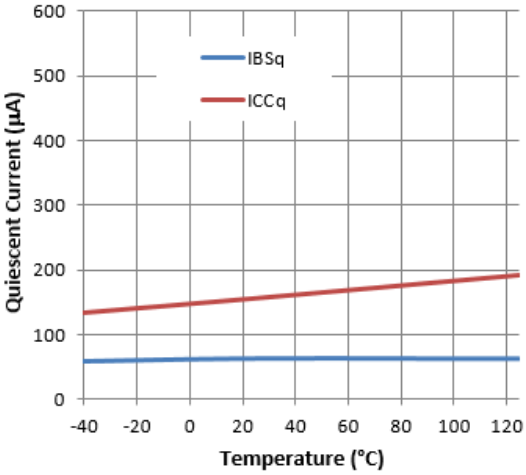


Figure 13. Quiescent Current vs. Temperature

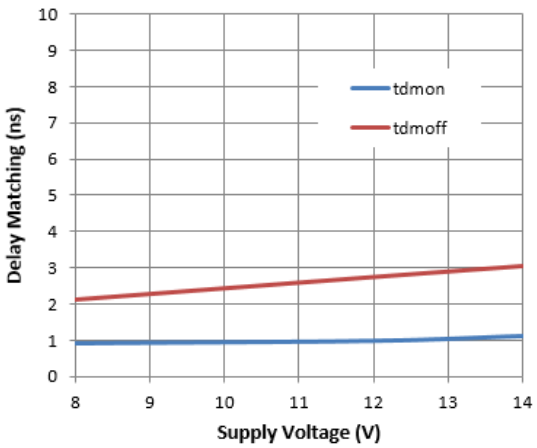


Figure 14. Delay Matching vs. Supply Voltage

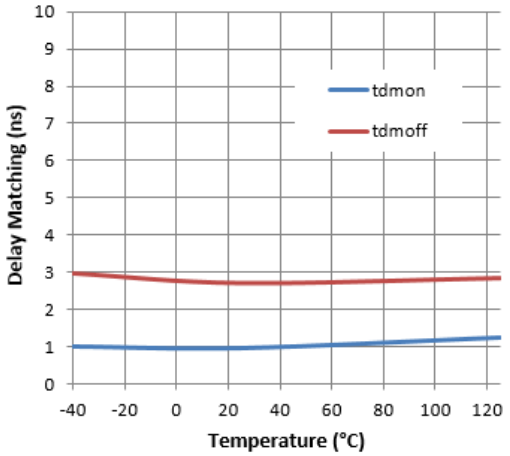


Figure 15. Delay Matching vs. Temperature

Typical Performance Characteristics (Cont.)

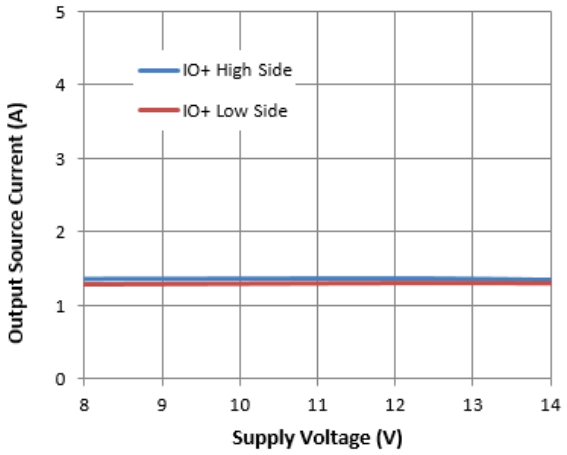


Figure 16. Output Source Current vs. Supply Voltage

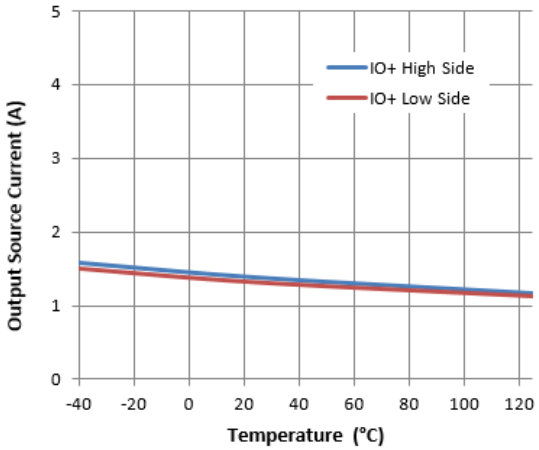


Figure 17. Output Source Current vs. Temperature

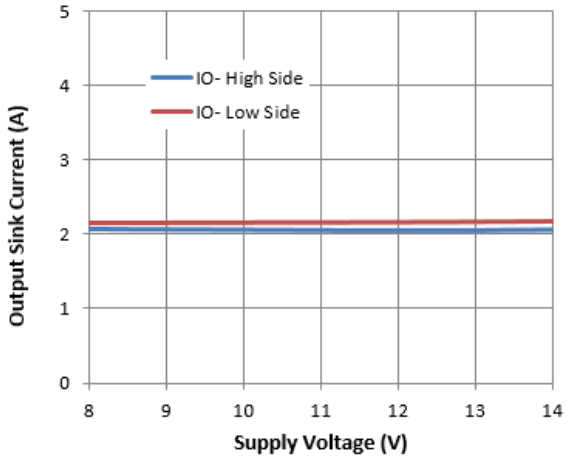


Figure 18. Output Sink Current vs. Supply Voltage

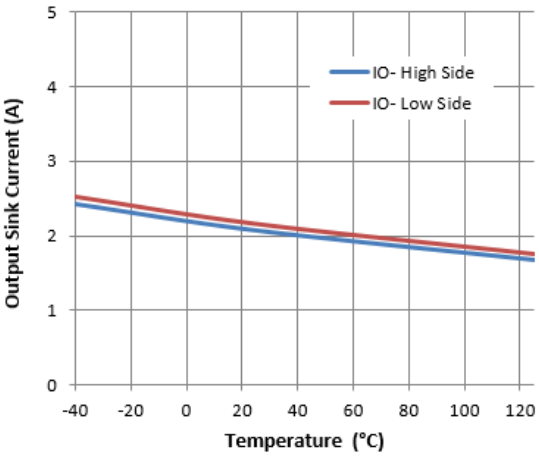


Figure 19. Output Sink Current vs. Temperature

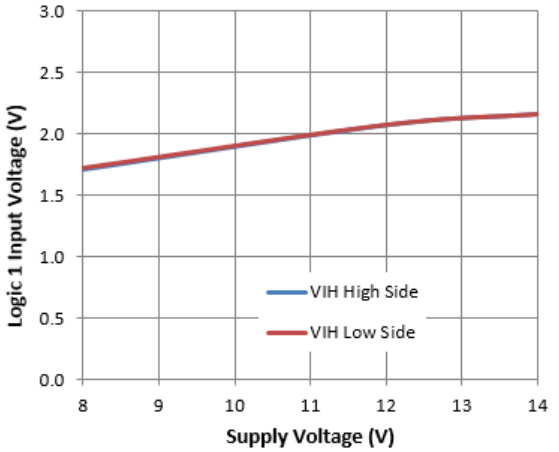


Figure 20. Logic 1 Input Voltage vs. Supply Voltage

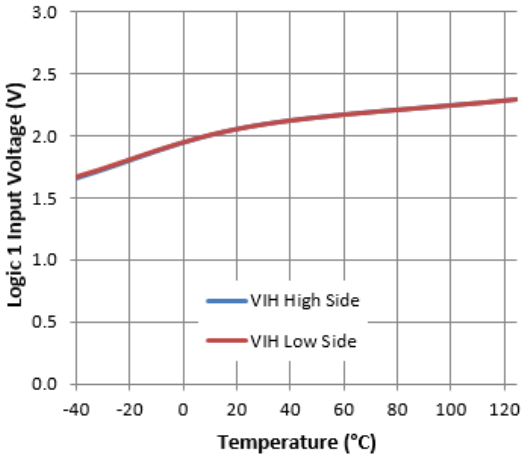


Figure 21. Logic 1 Input Voltage vs. Temperature

Typical Performance Characteristics (Cont.)

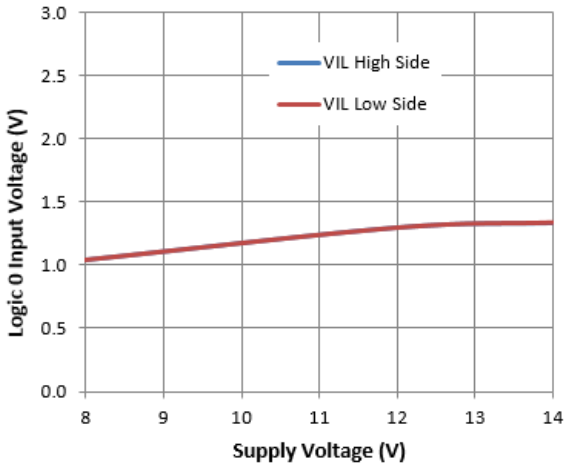


Figure 22. Logic 0 Input Voltage vs. Supply Voltage

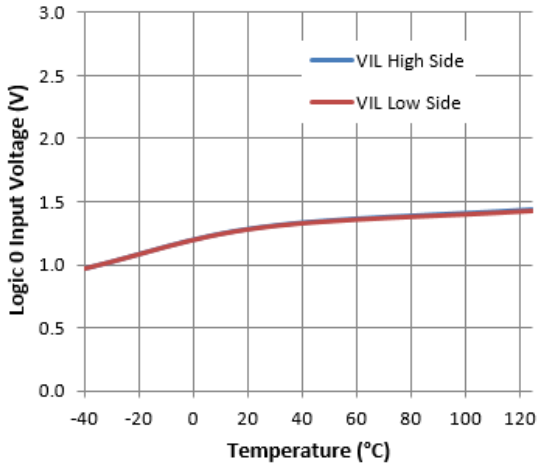


Figure 23. Logic 0 Input Voltage vs. Temperature

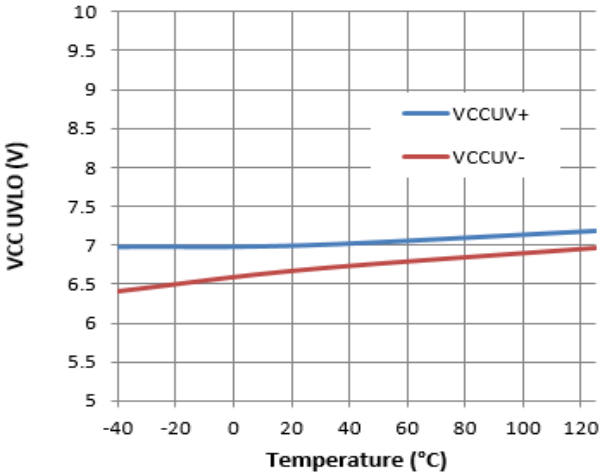


Figure 24. VCC UVLO vs. Temperature

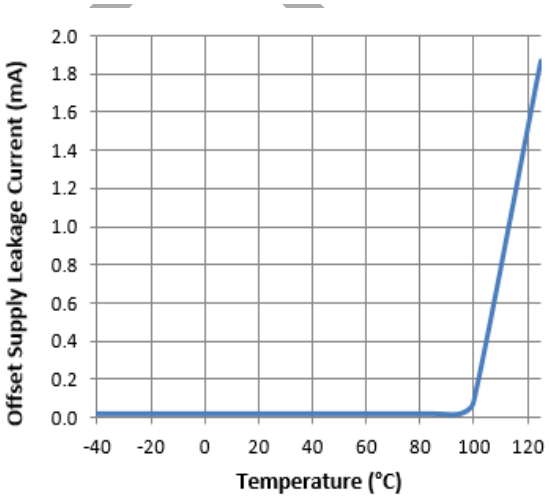
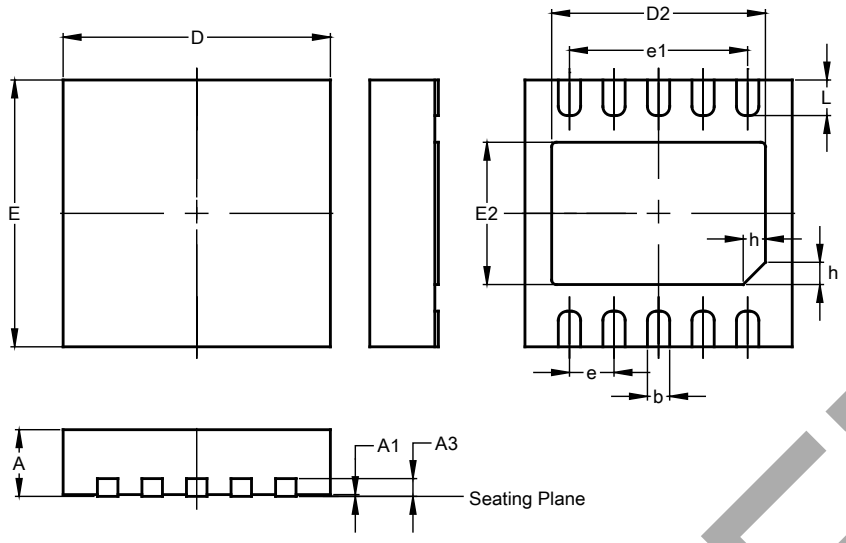


Figure 25. Offset Supply Leakage Current vs. Temperature

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-DFN3030-10 (Type TH)

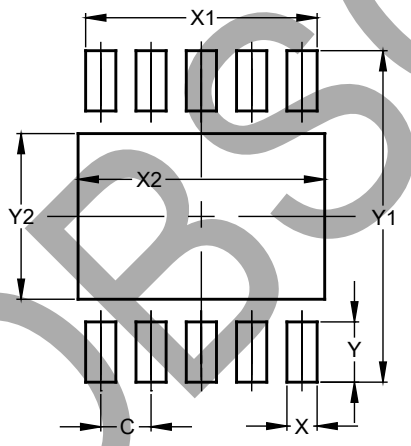


W-DFN3030-10 (Type TH)			
Dim	**Min**	**Max**	**Typ**
A	0.70	0.80	0.75
A1	--	0.05	0.02
A3	0.18	0.25	0.20
b	0.18	0.30	0.25
D	2.90	3.10	3.00
D2	2.40	2.60	2.50
e	0.50BSC		
e1	2.00BSC		
E	2.90	3.10	3.00
E2	1.45	1.65	1.55
h	0.20	0.30	0.25
L	0.30	0.50	0.40
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-DFN3030-10 (Type TH)



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	2.300
X2	2.600
Y	0.600
Y1	3.300
Y2	1.650

IMPORTANT NOTICE

1. DIODES INCORPORATED AND ITS SUBSIDIARIES ("DIODES") MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes products. Diodes products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of the Diodes products for their intended applications, (c) ensuring their applications, which incorporate Diodes products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.

3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes' websites, harmless against all damages and liabilities.

4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes' website) under this document.

5. Diodes products are provided subject to Diodes' Standard Terms and Conditions of Sale (https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

6. Diodes products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.

7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.

8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.

www.diodes.com