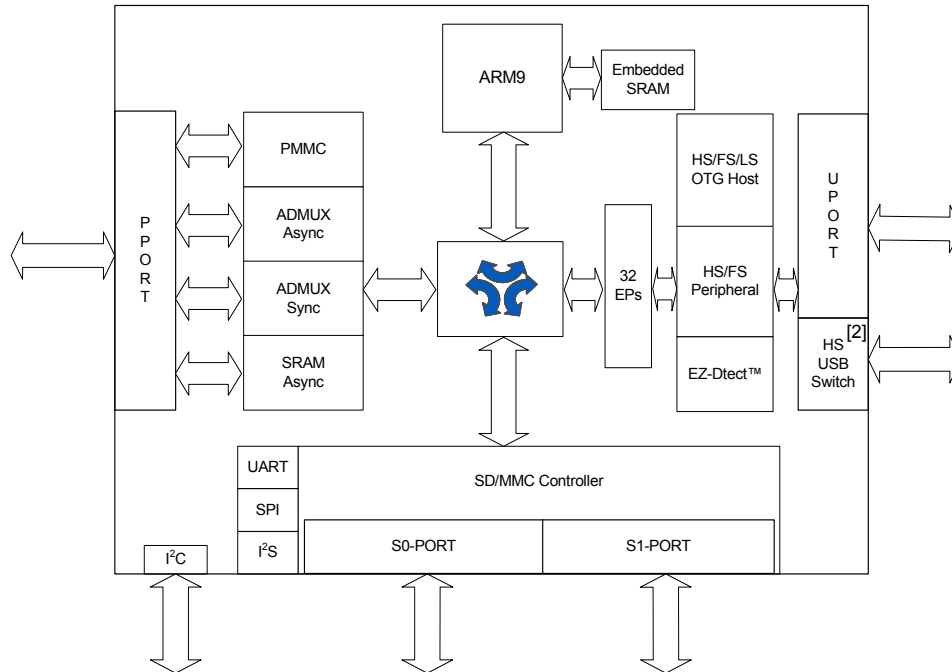


## Logic Block Diagram



### Note

2. Available only with the WLCSP package.

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## Functional Overview

West Bridge Bay™ is a Hi-Speed USB 2.0 West Bridge peripheral controller optimized for all sideloading and streaming applications. It supports the latest removable and embedded mass-storage devices. The SLIM II architecture, supervised by the ARM9 CPU core, enables simultaneous accesses among all the functional Bay ports without affecting the performance of each independent data path. The functional ports are as follows:

- USB port (U-Port) supporting USB 2.0 peripheral and USB 2.0 OTG host
- Mass storage port (S-Port) supporting two independent mass storage devices
- Processor port (P-Port) connecting to a host processor
- Low-performance peripheral port (LPP-Port) providing additional serial interfaces

Bay offers the following advantages:

- USB host (that is, PC) accessing mass storage attached to Bay (U-Port ↔ S-Port access) in a sideloading application. Bay acts as a USB 2.0 peripheral
- USB host exchanging data with the P-Port host processor (P-Port ↔ U-Port access) in a video streaming or tethered modem application. Bay acts as a USB 2.0 peripheral
- P-Port host processor accessing mass storage or I/O devices attached to Bay (P-Port ↔ S-Port access). Bay acts as a mass storage bridge
- P-Port host processor connecting to mass storage or HID attached to Bay's USB port (P-Port ↔ U-Port access). Bay acts as a USB 2.0 OTG host

Each of these access paths can operate independently or simultaneously in an interleaved manner. Bay also supports the USB composite device driver, enabling simultaneous enumeration of multiple independent USB device classes.

## Interface Description

### USB Interface (U-Port)

Bay supports USB peripheral functionality compliant with the USB 2.0 Specification.

- Bay is compliant with the USB OTG supplement revision 2.0. It supports high-speed, full-speed, and low-speed OTG dual-role device capability. As a peripheral, it is capable of high-speed and full-speed. As a host, it is capable of high-speed, full-speed, and low-speed
- Bay supports the Carkit Pass-Through UART functionality on USB D+/D– lines based on the CEA-936A specification

Bay supports up to 32 endpoints with fully configurable buffer sizes.

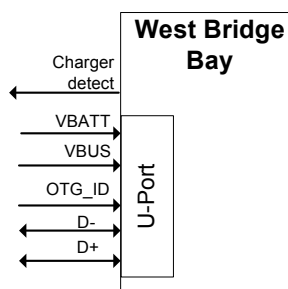
As a USB peripheral, Bay natively supports MSC and Media Transfer Protocol (MTP) USB peripheral classes. All other device classes are supported in pass-through mode. The external host processor, connected to the P-Port, handles enumeration.

As a USB OTG host, Bay natively supports MSC and HID device classes. All other device classes can be supported with custom firmware. Contact Cypress applications support for details.

When the USB port is not in use, the PHY and transceiver may be disabled for power savings.

The Cypress Vendor ID 0X04B4 is the default VID used for enumeration. This may be changed through firmware.

**Figure 1. U-Port Interface Signals**



### USB Switch

Bay integrates a high-speed USB 2.0 switch that allows a single USB connector to be shared with another device. The firmware can enable or disable this switch. When the switch is enabled, the USB D+/D– are connected to an external high-speed USB 2.0 PHY. After power-on-reset (POR) in the normal mode of operation, the USB switch is enabled by default. Note that this USB switch is only available with the WLCSP package, not with the BGA package.

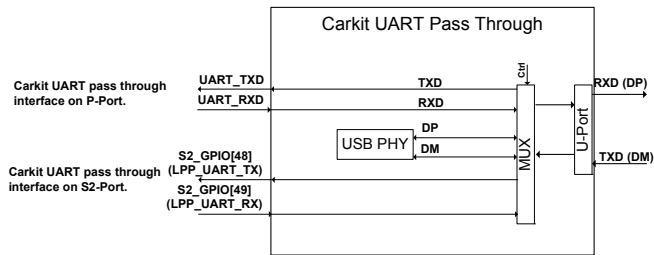
### Carkit UART Mode

The U-Port supports the Carkit UART mode (UART over D+/D–) for non-USB serial data transfer. This complies with the CEA-936A specification.

In the Carkit UART mode, the output signaling voltage is 3.3 V. The TXD of UART (output) is mapped to the D– line and the RXD of UART (input) is mapped to the D+ line.

Bay disables the USB transceiver and the D+ and D– pins function as pass-through pins to connect to the host processor UART. When the P-Port is configured to be in the asynchronous ADMux and PMMC modes, the Carkit UART signals are routed to the P-Port. In the asynchronous SRAM and synchronous ADMux modes, the Carkit UART signals are routed to S1-Port GPIOs as shown in Figure 2. Bay supports a baud rate of up to 9600 bps in this mode.

**Figure 2. Carkit UART Pass-Through Block Diagram**



### EZ-Dtect

Bay supports USB the charger and accessory detection mechanism (EZ-Dtect). The charger detection mechanism complies with the battery-charging specification, revision 1.1. Bay also provides hardware support to detect the resistance values on the ID pin.

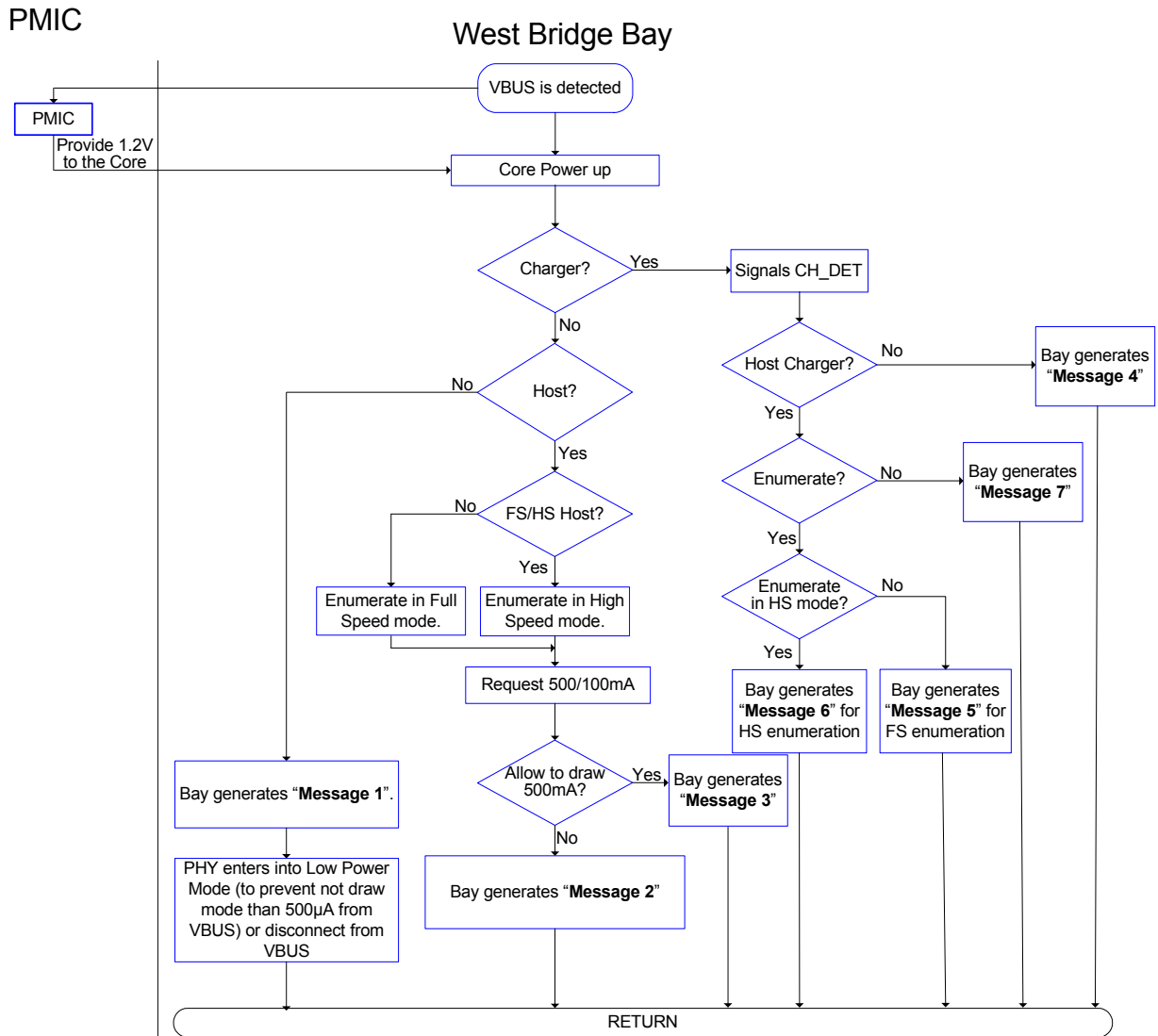
The Bay device detects the following resistance ranges:

- Less than 10  $\Omega$
- Less than 1 k $\Omega$
- 65 k $\Omega$  to 72 k $\Omega$
- 35 k $\Omega$  to 39 k $\Omega$
- 99.96 k $\Omega$  to 104.4 k $\Omega$  (102 k $\Omega \pm 2\%$ )
- 119 k $\Omega$  to 132 k $\Omega$
- Higher than 220 k $\Omega$
- 431.2 k $\Omega$  to 448.8 k $\Omega$  (440 k $\Omega \pm 2\%$ )

Bay's EZ-Dtect feature can identify a dedicated wall charger, host/hub charger, and host/hub.

Figure 3 shows the flowchart of the charger detection procedure that Bay uses. Table 1 on page 7 shows the messages that Bay may communicate over I<sup>2</sup>C to an external PMIC or processor.

Figure 3. Charger Detection Procedure



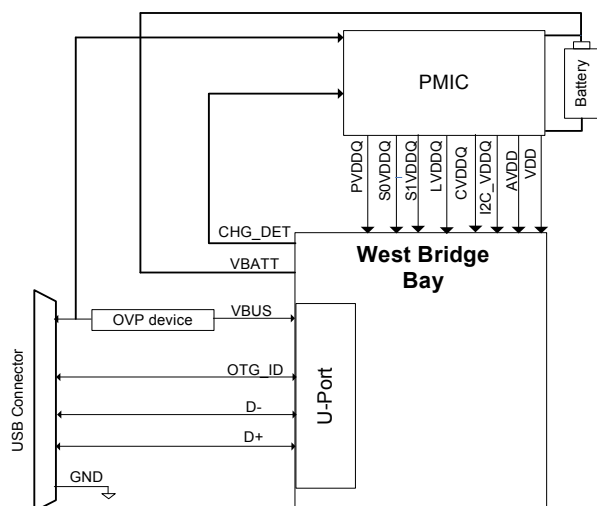
**Table 1. Charger Detect Messages**

| I <sup>2</sup> C to PMIC or External Processor | Description                                    |
|------------------------------------------------|------------------------------------------------|
| Message 1                                      | Fail negotiation                               |
| Message 2                                      | 100 mA available – Host only                   |
| Message 3                                      | 500 mA available – Host only                   |
| Message 4                                      | 1.8 A available – Wall charger                 |
| Message 5                                      | 1.5 A available – Host/hub charger in FS mode  |
| Message 6                                      | 900 mA available – Host/hub charger in HS mode |
| Message 7                                      | 1.5 A available – Host/hub charger             |

Note: Other messages can be customized in firmware.

#### VBUS Overvoltage Protection

Bay can withstand up to 6 V on the VBUS pin. In various failure scenarios, a charger may supply up to 12 V on VBUS. In this case, an external overvoltage protection (OVP) device prevents the failing charger from causing damage to the Bay device. [Figure 4](#) shows the system application diagram with an OVP device connected to VBUS. Bay is able to draw power from either the VBATT or VBUS voltage sources. Therefore, it is also possible to leave VBUS unconnected in the system and solely use VBATT as the power source. VBATT can be connected to the system battery or a stable 3.2–6-V voltage rail from the PMIC. In this case, Bay does not perform the charger detection function and this function is supported by the external PMIC. Refer to the [DC Specifications](#) for the operating range of VBUS and VBATT.

**Figure 4. System Diagram with OVP Device For VBUS**


#### On-The-Go (OTG)

The West Bridge Bay OTG performs the following functions:

- Complies with OTG revision 2.0 specification
- Supports both A and B device modes and supports control, interrupt, bulk, and isochronous data transfers
- Requires an external charge pump (either standalone or integrated with a PMIC) to power VBUS in OTG A-device mode
- The target peripheral list for OTG host implementation consists of MSC- and HID-class devices. Other devices may be supported with custom firmware. Contact Cypress Applications Support for details
- Bay does not support the attach detection protocol (ADP)

#### OTG Connectivity

In the OTG mode, Bay can be configured to be an A-, B-, or dual-role device. It can connect to the following:

- Targeted USB peripheral
- SRP-capable USB peripheral
- HNP-capable USB peripheral
- OTG host
- HNP-capable host
- OTG device

The Bay device supports ACA.

## Storage Port (S-Port)

Bay has two independent storage ports (S0-Port and S1-Port). Both storage ports comply with the following specifications:

- MMC system specification, MMCA Technical Committee, Version 4.4
- SD specification, Version 3.0
- SDIO host controller compliant with SDIO specification version 2.00 (Jan.30, 2007)

The following sections list the features that both the storage ports support.

### *SD/MMC Clock Stop*

Bay supports the stop clock feature that saves power if the internal buffer becomes full, when receiving data from the SD/MMC/SDIO.

### *SD\_CLK Output Clock Stop*

During the data transfer, the SD\_CLK clock can be enabled (on) or disabled (stopped) any time by the internal flow control mechanism.

You can dynamically configure the SD\_CLK output frequency using a clock divisor from a system clock. The clock choice for the divisor is user-configurable through a register. For example, the following frequencies may be configured:

- 400 kHz – For the SD/MMC card initialization
- 20 MHz – For a card with 0- to 20-MHz frequency
- 24 MHz – For a card with 0- to 26-MHz frequency
- 48 MHz – For a card with 0- to 52-MHz frequency (SD\_CLK supports 48-MHz frequency when the clock input to Bay is either 19.2 MHz or 38.4 MHz)
- 52 MHz – For a card with 0- to 52-MHz frequency (SD\_CLK supports 52-MHz frequency when the clock input to Bay is either 26 MHz or 52 MHz)
- 100 MHz – For a card with 0- to 100-MHz frequency

In the DDR mode, data is clocked on both the rising and falling edge of the SD clock. DDR clocks run up to 52 MHz.

### *Card Insertion and Removal Detection*

Bay supports two-card insertion and removal detection mechanisms.

- Use of SD\_D[3] data: During system design, this signal must have an external 470-k $\Omega$  pull-down resistor connected to SD\_D[3]. SD cards have an internal 10-k $\Omega$  pull-up resistor. When the card is inserted or removed from the SD/MMC connector, the voltage level at the SD\_D[3] pin changes and triggers an interrupt to the CPU. The older generations of MMC cards do not support this card detection mechanism.

- Use of S0/S1\_INS pin: Some SD/MMC connectors facilitate a micro switch for card insertion or removal of detection. This micro switch can be connected to S0/S1\_INS. When the card is inserted or removed from the SD/MMC connector, it turns the micro switch on and off. This causes a voltage-level change at the pin that triggers the interrupt to the CPU. The card-detect micro switch polarity is assumed to be the same as the write-protect micro switch polarity. A low indicates that the card is inserted. This S0/S1\_INS pin is shared between the two S-Ports. Register configuration determines which port gets to use this pin. This pin is mapped to the S1VDDQ power domain; if S0VDDQ and S1VDDQ are at different voltage levels, this pin cannot be used as S1\_INS.

### *Write Protection (WP)*

The S0\_WP/S1\_WP (SD Write Protection) on S-Port is used to connect to the WP micro switch of the SD/MMC card connector. This pin internally connects to a CPU-accessible GPIO for the firmware to detect the SD card Write Protection.

### *SDIO Interrupt*

The SDIO interrupt functionality is supported as specified in the SDIO specification version 2.00 (January 30, 2007).

### *SDIO Read-Wait Feature*

Bay supports the optional read-wait and suspend-resume features as defined in the SDIO specification Version 2.00 (January 30, 2007).

## Host Processor Interface (P-Port)

A dedicated interface enables communications with a host processor. Bay supports the following P-Port interfaces.

- 16-bit asynchronous non-multiplexed SRAM
- 16-bit asynchronous address/data multiplexed SRAM
- 32-bit synchronous address/data multiplexed SRAM
- MMC slave interface compatible with MMC system specification, MMCA Technical Committee, Version 4.2 with eMMC 4.3 and 4.4 Pass-Through boot

The following sections describe these P-Port interfaces.

### *Asynchronous SRAM*

This interface consists of standard asynchronous SRAM interface signals as shown in [Figure 5](#) on page 9. This interface is used to access the Bay device's configuration registers and buffer memory. Both single-cycle and burst accesses are supported by the asynchronous interface signals.

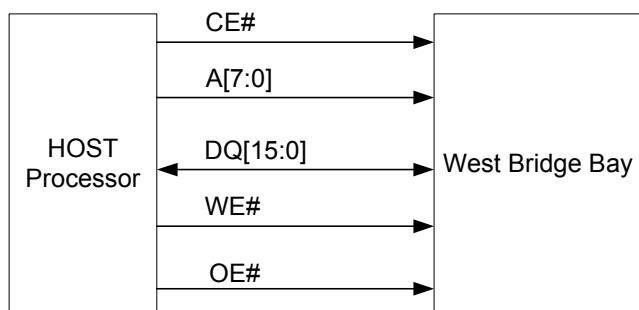
The most significant address bit, A[7], determines if configuration registers or buffer memory are accessed. When the configuration registers are selected by asserting the A[7] address bit, the address bus bits A[6:0] point to a configuration register. When A[7] is deasserted, the buffer memory is accessed as indicated by the P-Port DMA transfer register and the transfer size is determined by the P-Port DMA transfer size register.

Application processors, with a DMA controller that uses address auto-increment during DMA transfers, can override this by connecting any higher-order address line (such as A[15]/A[23]/A[31]) of the application processor to Bay's A[7].

In the asynchronous SRAM mode, when reading from a buffer memory, Bay supports two methods of reading out the next data from the buffer: read out on the rising edge of OE# or toggle the least significant address bit A[0].

In this mode, the P-Port interface works with a 32.5-ns minimum access cycle providing an interface data rate of up to 61.5 MB per second.

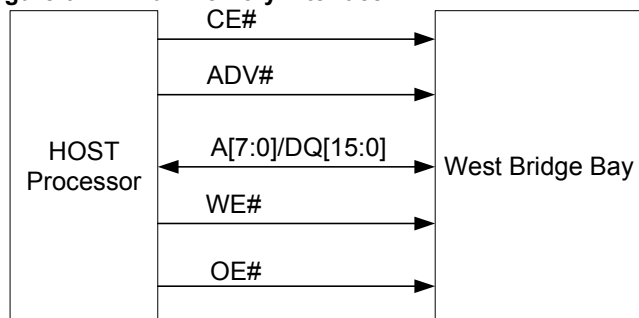
**Figure 5. Asynchronous SRAM Interface**



#### Asynchronous Address/Data Multiplexed

The physical ADMux memory interface consists of signals shown in Figure 6. This interface supports processors that implement a multiplexed address or data bus.

**Figure 6. ADMux Memory Interface**



The Bay device's ADMux interface supports a 16-bit time multiplexed address/data SRAM bus.

For read operations, both CE# and OE# must be asserted.

For write operations, both CE# and WE# are asserted. OE# is "Don't Care" during a write operation (during both address and data phase of the write cycle). Input data is latched on the rising edge of WE# or CE#, whichever occurs first. The addresses must be latched prior to the write operation by toggling Address Valid (ADV#). The Address Valid (ADV#) must be asserted during the address phase of the write operation, as shown in Figure 15 on page 34.

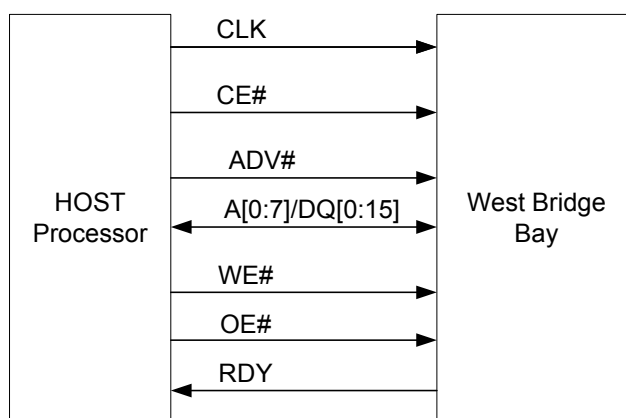
ADV# must be LOW during the Address phase of a read/write operation. ADV# must be HIGH during the data phase of a read/write operation, as shown in Figure 14 and Figure 15 on page 34.

#### Synchronous ADMux Interface

Bay's P-Port supports a synchronous address/data multiplexed interface. This interface operates at a frequency of up to 100 MHz and supports a 16-bit data bus.

The RDY output signal from the Bay device indicates a data valid for read transfers and is acknowledged for write transfers.

**Figure 7. Synchronous ADMux Interface**



See the synchronous ADMux interface timing diagrams for details.

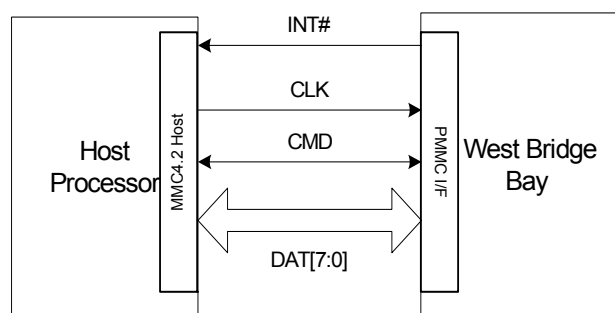
#### Processor MMC (PMMC) Slave Interface

Bay supports an MMC Slave interface on the P-Port called PMMC to distinguish it from the S-Port MMC interface.

Figure 8 illustrates the signals used to connect to the host processor.

The PMMC interface's GO\_IRQ\_STATE command allows West Bridge Bay to communicate asynchronous events without requiring the INT# signal. The use of the INT# signal is optional.

**Figure 8. PMMC Interface Configuration**



The MMC slave interface features are as follows:

- Interface operations are compatible with the MMC system specification, MMCA Technical Committee, Version 4.2
- Supports booting from an eMMC device connected to the S-Port. This feature is supported for eMMC devices operating at up to 52-MHz SDR
- Supports PMMC interface voltage ranges of 1.7 V to 1.95 V and 2.7 V to 3.6 V
- Supports open drain (both drive and receive open drain signals) on the CMD pin to allow GO\_IRQ\_STATE (CMD40) for PMMC
- Interface clock frequency range: 0 to 52 MHz
- Supports 1-bit, 4-bit, or 8-bit operation modes. This configuration is determined by the MMC initialization procedure
- Bay responds to standard initialization phase commands as specified for the MMC 4.2 slave device
- PMMC mode MMC 4.2 command classes: Class 0 (Basic), Class 2 (Block read), and Class 4 (Block write), Class 9 (I/O)

Bay supports the following PMMC commands:

- Class 0: Basic  
CMD0, CMD1, CMD2, CMD3, CMD4, CMD6, CMD7, CMD8, CMD9, CMD10, CMD12, CMD13, CMD15, CMD19, CMD5 (wake-up support)
- Class 2: Block Read  
CMD16, CMD17, CMD18, CMD23
- Class 4: Block Write  
CMD16, CMD23, CMD24, CMD25
- Class 9: I-O  
CMD39, CMD40

## Other Interfaces

Bay supports additional low-performance peripherals that include:

- UART
- I<sup>2</sup>C
- I<sup>2</sup>S
- SPI

The SPI, UART, and I<sup>2</sup>S interfaces are multiplexed on the S1-Port. The [WLCSP Pin List](#) on page 16 shows the details.

### UART Interface

The UART interface of Bay is intended for asynchronous serial communication with other UART devices.

The UART implementation supports full-duplex communication with a signaling format compatible with industry-standard UART. It includes the signals noted in [Table 2](#).

The UART is capable of generating a range of baud rates from 300 bps to 4608 Kbps selectable by the firmware. If flow control is enabled, then Bay's UART only transmits data when the CTS input is asserted. In addition to this, Bay's UART asserts the RTS output signal, when it is ready to receive data.

**Table 2. UART Interface Signals**

| Signal | Description   |
|--------|---------------|
| TX     | Output signal |
| RX     | Input signal  |
| CTS    | Flow control  |
| RTS    | Flow control  |

### I<sup>2</sup>C Interface

Bay has an I<sup>2</sup>C interface compatible with the I<sup>2</sup>C Bus Specification Revision 3. This I<sup>2</sup>C interface is only capable of operating as I<sup>2</sup>C master. Therefore, it may be used to communicate with other I<sup>2</sup>C slave devices. For example, Bay may boot from an EEPROM connected to the I<sup>2</sup>C interface, as a selectable boot option.

Bay's I<sup>2</sup>C master controller also supports the multi-master mode functionality.

The power supply for the I<sup>2</sup>C interface is I2CVDDQ, which is a separate power domain from the other serial peripherals. This gives the I<sup>2</sup>C interface the flexibility to operate at a different voltage than the other serial interfaces.

The bus frequencies supported by the I<sup>2</sup>C controller are 100 kHz, 400 kHz, and 1 MHz. When I2CVDDQ is 1.2 V, the maximum operating frequency supported is 100 kHz. When I2CVDDQ is 1.8 V, 2.5 V, or 3.3 V, the operating frequencies supported are 400 kHz and 1 MHz. The I<sup>2</sup>C controller supports the clock-stretching feature to enable slower devices to exercise flow control.

Both serial clock (SCL) and serial data (SDA) signals of the I<sup>2</sup>C interface require external pull-up resistors. The pull-up resistors must be connected to I2CVDDQ.

### I<sup>2</sup>S Interface

Bay has an I<sup>2</sup>S port to support external audio codec devices. It functions as I<sup>2</sup>S master only as a transmitter. The I<sup>2</sup>S interface consists of four signals: clock line (I2S\_CLK), serial data line (I2S\_SD), word select line (I2S\_WS), and master system clock (I2S\_MCLK). Bay can generate the system clock as an output on I2S\_MCLK or accept an external system clock input on I2S\_MCLK.

The I<sup>2</sup>S interface supports sampling frequencies of 32 kHz, 44.1 kHz, and 48 kHz.

### SPI Interface

Bay supports an SPI master interface on the S1-Port. The maximum operating frequency is 33 MHz.

The SPI controller supports the four modes of SPI communication (see [SPI Timing Specification](#) on page 41 for details on the modes) with a start-stop clock. The SPI controller is a single-master controller with a single automated SSN control. It supports transaction sizes ranging from 4 bits to 32 bits.

## Boot Options

Bay can load boot images from various sources, selected by the configuration of the PMODE pins. These include:

- Boot from eMMC (S0-Port)
- Boot from I<sup>2</sup>C
- Boot from asynchronous ADMux (P-Port)
- Boot from synchronous ADMux (P-Port)
- Boot from asynchronous non-multiplexed SRAM (P-Port)
- Boot from PMMC (P-Port)

USB boot can be enabled as a fallback boot option.

**Table 3. West Bridge Bay Booting Options**

| PMODE[2:0]         | Boot From                                                          |
|--------------------|--------------------------------------------------------------------|
| 000                | S0-Port (eMMC)<br>On failure, USB boot is enabled                  |
| 001                | PMMC pass-through<br>On failure, USB boot enabled                  |
| 010                | PMMC pass-through                                                  |
| 011                | PMMC_Relay (enables secure boot)                                   |
| 100                | S0-Port (eMMC)                                                     |
| 101                | Sync ADMux (16-bit data bus)                                       |
| 110                | PMMC legacy                                                        |
| 111                | USB Boot                                                           |
| 00F <sup>[3]</sup> | Async SRAM (16-bit data bus)                                       |
| 01F <sup>[3]</sup> | Async ADMux (16-bit data bus)                                      |
| 10F <sup>[3]</sup> | I <sup>2</sup> C<br>On failure, USB boot is enabled                |
| 11F <sup>[3]</sup> | I <sup>2</sup> C only                                              |
| 1F1 <sup>[3]</sup> | PMMC_Relay (enables secure boot)<br>On failure USB boot is enabled |
| Other Combinations | Reserved                                                           |

## Reset

### Hard Reset

A hard reset is initiated by asserting the RESET# pin on West Bridge Bay. The specific reset sequence and timing requirements are detailed in [Figure 23](#) on page 43 and [Figure 17](#) on page 42. All I/Os are tristated during a hard reset.

### Soft Reset

In a soft reset, the processor sets the appropriate bits in the PP\_INIT control register. There are two types of soft reset:

- CPU Reset - The CPU Program Counter is reset. Firmware does not need to be reloaded following a CPU Reset.
- Whole Device Reset - This reset is identical to hard reset. The firmware must be reloaded following a Whole Device Reset.

## Clocking

Bay allows either a crystal to be connected between the XTALIN and XTALOUT pins or an external clock to be connected at the CLKIN pin. The XTALIN, XTALOUT, CLKIN, and CLKIN\_32 pins can be left unconnected if not used.

Crystal frequency supported is 19.2 MHz, and the external clock frequencies supported are 19.2, 26, 38.4, and 52 MHz.

Bay has an on-chip oscillator circuit that uses an external 19.2-MHz (±100 ppm) crystal (when the crystal option is used). An appropriate load capacitance is required with a crystal. Refer to the specification of the crystal used to determine the appropriate load capacitance. The FSLC[2:0] pins must be configured appropriately to select the crystal- or clock-frequency option. The configuration options are shown in [Table 4](#) on page 11.

Clock inputs to Bay must meet the phase noise and jitter requirements specified in [Table 5](#) on page 12.

The input clock frequency is independent of the Bay core's clock/data rate or any of the device interfaces (including P-Port and S-Port). The internal PLL applies the appropriate clock multiply option depending on the input frequency.

**Table 4. Crystal/Clock Frequency Selection**

| FSLC[2] | FSLC[1] | FSLC[0] | Crystal/Clock Frequency |
|---------|---------|---------|-------------------------|
| 0       | 0       | 0       | 19.2-MHz crystal        |
| 1       | 0       | 0       | 19.2-MHz input CLK      |
| 1       | 0       | 1       | 26-MHz input CLK        |
| 1       | 1       | 0       | 38.4-MHz input CLK      |
| 1       | 1       | 1       | 52-MHz input CLK        |

### Note

3. F indicates Floating.

**Table 5. West Bridge Bay Input Clock Specifications**

| Parameter                   | Description    | Specification |      | Units |
|-----------------------------|----------------|---------------|------|-------|
|                             |                | Min           | Max  |       |
| Phase Noise                 | 100-Hz offset  | –             | –75  | dB    |
|                             | 1-kHz offset   | –             | –104 | dB    |
|                             | 10-kHz offset  | –             | –120 | dB    |
|                             | 100-kHz offset | –             | –128 | dB    |
|                             | 1-MHz offset   | –             | –130 | dB    |
| Maximum frequency deviation |                | –             | 150  | ppm   |
| Duty cycle                  |                | 30            | 70   | %     |
| Overshoot                   |                | –             | 3    | %     |
| Undershoot                  |                | –             | –3   | %     |
| Rise time/fall time         |                | –             | 3    | ns    |

### 32-kHz Watchdog Timer Clock Input

Bay includes a watchdog timer that can be used to interrupt the CPU, automatically wake up Bay in standby mode, and reset the CPU. The watchdog timer runs off a 32-kHz clock, which may optionally be supplied from an external source on a dedicated Bay pin.

The watchdog also periodically wakes up the processor in Standby mode for polling operations, if enabled. The firmware can disable the watchdog timer.

Requirements for the optional 32-kHz clock input are listed in [Table 6](#).

**Table 6. 32-kHz Clock Input Requirement**

| Parameter           | Min | Max  | Units |
|---------------------|-----|------|-------|
| Duty cycle          | 40  | 60   | %     |
| Frequency deviation | –   | ±200 | ppm   |
| Rise time/Fall time | –   | 200  | ns    |

### Power

Bay has the following main power supply domains:

■ **IO\_VDDQ**: This is a group of independent supply domains for digital I/Os. The voltage level on these supplies is 1.8 V to 3.3 V. Specifically, the separate I/O power domains are:

- PVDDQ: P-Port interface supply
- S0VDDQ: S0-Port supply
- S1VDDQ: S1-Port supply
- I2CVDDQ: I<sup>2</sup>C power supply (1.2 V to 3.3 V)
- LVDDQ: Low-performance peripherals power supply (UART/SPI/I<sup>2</sup>S)
- CVDDQ: Clock power supply

■ **V<sub>DD</sub>/AVDD**: Supply voltage for the logic core. The nominal supply voltage level is 1.2 V. This supplies the core logic circuits. The same supply must also be used for AVDD.

■ **VBATT**: This is the 3.2-V to 6-V battery power supply for the USB I/O and some analog circuits. This supply powers the USB transceiver through an internal voltage regulator. This supply is internally regulated to 3.3 V for the USB PHY.

■ **VBUS**: This is the 4.0-V to 6-V input from USB. When VBUS is greater than 3.7 V, it becomes the primary source of supply to the USB circuitry unless there is a software override.

## Power Modes

Bay supports the following power modes:

- **Normal mode:** This is the full-functional operating mode. In this mode the internal CPU clock and the internal PLLs are enabled.

Normal operating power consumption does not exceed the sum of  $I_{CC}$  core max and  $I_{CC}$  USB max (refer to [DC Specifications](#) for current consumption specifications).

The I/O power supplies S0VDDQ, S1VDDQ, LVDDQ, and I2CVDDQ can be turned off when the corresponding interface is not in use. PVDDQ cannot be turned off at any time if the P-port is used in the application.

- **Low-power modes** (see [Table 7](#)):

- Suspend mode
- Standby mode
- Core power-down mode

**Table 7. Summary for Methods of Entry/Exit for Low Power Modes**

| Power Mode   | Characteristics                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Method of Entry                                                                                                                                                                                                                                                                                                                                                | Method of Exit                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Suspend mode | <ul style="list-style-type: none"> <li>■ The power consumption in this mode does not exceed <math>ISB_{suspend}</math></li> <li>■ The clocks are shut off. The PLLs are disabled</li> <li>■ All I/Os maintain their previous state</li> <li>■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually</li> <li>■ The states of the configuration registers, buffer memory, and all internal RAM are maintained</li> <li>■ All transactions must be completed before Bay enters Suspend mode (state of outstanding transactions are not preserved)</li> <li>■ The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion). The program counter does not reset</li> </ul> | <ul style="list-style-type: none"> <li>■ Firmware executing on the internal ARM9 core can put West Bridge Bay into suspend mode. For example, on USB suspend condition, firmware may decide to put West Bridge Bay into suspend mode</li> <li>■ External Processor, through the use of mailbox registers, can put West Bridge Bay into suspend mode</li> </ul> | <ul style="list-style-type: none"> <li>■ D+ transitioning to LOW or HIGH</li> <li>■ D- transitioning to LOW or HIGH</li> <li>■ Impedance change on OTG_ID pin</li> <li>■ Detection of VBUS</li> <li>■ Level detect on UART_CTS (programmable polarity)</li> <li>■ P-port interface assertion of CE#</li> <li>■ Assertion of RESET#</li> <li>■ MMC CMD5 received over PMMC interface</li> <li>■ Insertion or removal of SD/MMC card detected on S0/S1_INS pin</li> <li>■ Level detect on S0_D1/S1_D1 (SDIO_INT; programmable polarity)</li> </ul> |

**Table 7. Summary for Methods of Entry/Exit for Low Power Modes (continued)**

| Power Mode           | Characteristics                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Method of Entry                                                                                                                                                                                                    | Method of Exit                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Standby mode         | <ul style="list-style-type: none"> <li>■ The power consumption in this mode does not exceed <math>ISB_{standby}</math></li> <li>■ All configuration register settings and program/data RAM contents are preserved. However, data in the buffers or other parts of the data path, if any, is not guaranteed. Therefore, the external processor must take care that the data needed is read before putting Bay into this Standby Mode</li> <li>■ The program counter is reset after waking up from Standby</li> <li>■ GPIO pins maintain their configuration</li> <li>■ Crystal oscillator is turned off</li> <li>■ Internal PLL is turned off</li> <li>■ USB transceiver is turned off</li> <li>■ ARM9 core is powered down. Upon wakeup, the core re-starts and runs the program stored in the program/data RAM</li> <li>■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually</li> </ul> | <ul style="list-style-type: none"> <li>■ Firmware executing on the internal ARM9 core or external processor sets the appropriate register</li> <li>■ MMC CMD5 (Sleep/Awake command) over PMMC interface</li> </ul> | <ul style="list-style-type: none"> <li>■ Detection of VBUS</li> <li>■ Insertion or removal of SD/MMC card detected on S0/S1_INS pin</li> <li>■ Level detect on S0_D1/S1_D1 (SDIO_INT; programmable polarity)</li> <li>■ Level detect on UART_CTS (Programmable Polarity)</li> <li>■ P-port interface assertion of CE# in SRAM/ADMux mode</li> <li>■ P-port interface activation of MMC_CLK in PMMC mode</li> <li>■ Assertion of RESET#</li> </ul> |
| Core power-down mode | <ul style="list-style-type: none"> <li>■ The power consumption in this mode does not exceed <math>ISB_{core}</math></li> <li>■ Core power is turned off</li> <li>■ All buffer memory, configuration registers, and the program RAM do not maintain state. After exiting this mode, reload the firmware</li> <li>■ In this mode, all other power domains can be turned on/off individually</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | <ul style="list-style-type: none"> <li>■ Turn off <math>V_{DD}</math></li> </ul>                                                                                                                                   | <ul style="list-style-type: none"> <li>■ Reapply <math>V_{DD}</math></li> <li>■ Assertion of RESET#</li> </ul>                                                                                                                                                                                                                                                                                                                                    |

## Configuration Options

Configuration options are available for specific usage models. Contact Cypress Applications/Marketing for details.

### Digital I/Os

Bay provides firmware-controlled pull-up or pull-down resistors internally on all digital I/O pins. The pins can be pulled HIGH through an internal 50-k $\Omega$  resistor or can be pulled LOW through an internal 10-k $\Omega$  resistor to prevent the pins from floating. An external 470-k $\Omega$  pull-down resistor is required on SD\_D[3] when this pin is used for SD card detection. The I/O pins may have the following states:

- Tristated (High-Z)
- Weak pull-up (through internal 50 k $\Omega$ )
- Pulled down (through internal 10 k $\Omega$ )
- Hold (I/O hold its value) when in low-power modes

All unused I/Os should be pulled high by using the internal pull-up resistors. All unused outputs should be left floating. All I/Os can be driven at full-strength, three-quarter strength, half-strength, or quarter-strength. These drive strengths are configured based on each interface.

### EMI

Bay meets the EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. It can also tolerate reasonable EMI, conducted by the aggressor, outlined by these specifications and continue to function as expected.

### System-level ESD

Bay has additional ESD protection on the D+, D-, OTG\_ID, VBUS, GND pins on the U-port and the S1\_D[0:7], S1\_CMD, S1\_CLK, S1\_WP and MMC1RST\_OUT pins on the S1-Port. The ESD protection levels provided on these ports are:

- $\pm 2.2$ -KV human body model (HBM) based on JESD22-A114 specification
- $\pm 6$ -KV contact discharge and  $\pm 8$ -KV air gap discharge based on IEC61000-4-2 level 3A
- $\pm 8$  KV contact discharge and  $\pm 15$  KV air gap discharge based on IEC61000-4-2 level 4C

This protection ensures that the device continues to function after ESD events up to the levels stated.

The S0/S1\_INS pin has up to  $\pm 2.2$ -KV HBM internal ESD protection.

**Figure 9. WLCSP Ball Map (Bottom View)<sup>[4]</sup>**

|   | 12          | 11          | 10          | 9           | 8           | 7          | 6            | 5          | 4          | 3          | 2            | 1         |
|---|-------------|-------------|-------------|-------------|-------------|------------|--------------|------------|------------|------------|--------------|-----------|
| A | VSS         | VSS         | NC          |             | NC          | FSLC[0]    | AVSS         | AVDD       | DP         | U2AFEVSSQ  | DM           | VDD       |
| B | L_GPIO[55]  | LVDDQ       | NC          | R_USB3      | NC          | FSLC[2]    | XTALIN       | XTALOUT    | SWDP       | R_USB2     | SWDM         | VDD       |
| C | L_GPIO[56]  | S1VDDQ      | VDD         | VSS         | VDD         | CVDDQ      | CLKIN_32     | CLKIN      | U2PLLVSQ   | OTG_ID     | TDO          | TRST#     |
| D | S1_GPIO[49] | S1_GPIO[50] | L_GPIO[53]  | L_GPIO[54]  | RESET#      | VDD        | I2C_GPIO[58] | TMS        | I2CVDDQ    | TCK        | I2C_GPIO[59] | VSS       |
| E | L_GPIO[57]  | S1_GPIO[48] | S1_GPIO[51] | S1_GPIO[52] | I2C_O[60]   | VSS        | VSS          | VSS        | VSS        | P_GPIO[3]  | VBATT        | VBUS      |
| F | VSS         | S1_GPIO[46] | S1_GPIO[47] | FSLC[1]     | TDI         | VDD        | VDD          | VDD        | VDD        | P_GPIO[4]  | P_GPIO[1]    | P_GPIO[0] |
| G | S0VDDQ      | S0_GPIO[43] | S0_GPIO[44] | S0_GPIO[45] | VSS         | VSS        | VDD          | VSS        | P_GPIO[9]  | P_GPIO[7]  | P_GPIO[6]    | P_GPIO[2] |
| H | VSS         | S0_GPIO[40] | S0_GPIO[41] | S0_GPIO[42] | S0_GPIO[39] | VSS        | P_GPIO[20]   | P_GPIO[18] | P_GPIO[14] | P_GPIO[12] | P_GPIO[8]    | PVDDQ     |
| J | S0VDDQ      | S0_GPIO[38] | S0_GPIO[37] | S0_GPIO[36] | P_GPIO[31]  | P_GPIO[27] | P_GPIO[25]   | P_GPIO[22] | P_GPIO[19] | P_GPIO[15] | P_GPIO[10]   | P_GPIO[5] |
| K | S0_GPIO[35] | S0_GPIO[34] | S0_GPIO[33] | P_GPIO[32]  | P_GPIO[28]  | P_GPIO[26] | P_GPIO[16]   | P_GPIO[21] | INT#       | P_GPIO[24] | P_GPIO[11]   | VSS       |
| L | VDD         | VSS         | VDD         | P_GPIO[30]  | P_GPIO[29]  | PVDDQ      | P_GPIO[23]   | VSS        | PVDDQ      | P_GPIO[17] | P_GPIO[13]   | VSS       |

**Figure 10. BGA Ball Map**

|   | 1           | 2           | 3           | 4           | 5           | 6          | 7          | 8          | 9            | 10           | 11         |
|---|-------------|-------------|-------------|-------------|-------------|------------|------------|------------|--------------|--------------|------------|
| A | VSS         | VDD         | NC          | NC          | NC          | NC         | AVDD       | VSS        | DP           | DM           | NC         |
| B | LVDDQ       | FSLC[0]     | NC          | FSLC[1]     | VDD         | CVDDQ      | AVSS       | VSS        | VSS          | VDD          | TRST#      |
| C | L_GPIO[54]  | L_GPIO[55]  | VDD         | L_GPIO[57]  | RESET#      | XTALIN     | XTALOUT    | R_USB2     | OTG_ID       | TDO          | I2CVDDQ    |
| D | S1_GPIO[50] | S1_GPIO[51] | S1_GPIO[52] | L_GPIO[53]  | L_GPIO[56]  | CLKIN_32   | CLKIN      | VSS        | I2C_GPIO[58] | I2C_GPIO[59] | O[60]      |
| E | S1_GPIO[47] | VSS         | S1VDDQ      | S1_GPIO[49] | S1_GPIO[48] | FSLC[2]    | TDI        | TMS        | VDD          | VBATT        | VBUS       |
| F | S0VDDQ      | S0_GPIO[45] | S0_GPIO[44] | S0_GPIO[41] | S1_GPIO[46] | TCK        | P_GPIO[2]  | P_GPIO[5]  | P_GPIO[1]    | P_GPIO[0]    | VDD        |
| G | VSS         | S0_GPIO[42] | S0_GPIO[43] | P_GPIO[30]  | P_GPIO[25]  | P_GPIO[22] | P_GPIO[21] | P_GPIO[15] | P_GPIO[4]    | P_GPIO[3]    | VSS        |
| H | VDD         | S0_GPIO[39] | S0_GPIO[40] | P_GPIO[31]  | P_GPIO[29]  | P_GPIO[26] | P_GPIO[20] | P_GPIO[24] | P_GPIO[7]    | P_GPIO[6]    | PVDDQ      |
| J | S0_GPIO[38] | S0_GPIO[36] | S0_GPIO[37] | S0_GPIO[34] | P_GPIO[28]  | P_GPIO[16] | P_GPIO[19] | P_GPIO[14] | P_GPIO[9]    | P_GPIO[8]    | VDD        |
| K | S0_GPIO[35] | S0_GPIO[33] | VSS         | VSS         | P_GPIO[27]  | P_GPIO[23] | P_GPIO[18] | P_GPIO[17] | P_GPIO[13]   | P_GPIO[12]   | P_GPIO[10] |
| L | VSS         | VSS         | VSS         | P_GPIO[32]  | VDD         | VSS        | VDD        | INT#       | PVDDQ        | P_GPIO[11]   | VSS        |

#### Note

4. No ball is populated at location A9.

## Pin Description

Table 8. WLCSP Pin List

| Pin |       | Power Domain | I/O | Name       | Description |              |              |         |
|-----|-------|--------------|-----|------------|-------------|--------------|--------------|---------|
|     |       |              |     |            | P-Port      |              |              |         |
|     |       |              |     |            | Async SRAM  | Async ADMux  | Sync ADMux   | PMMC    |
| F1  | PVDDQ | I/O          |     | P_GPIO[0]  | DQ[0]       | DQ[0]/A[0]   | DQ[0]/A[0]   | MMC_D0  |
| F2  | PVDDQ | I/O          |     | P_GPIO[1]  | DQ[1]       | DQ[1]/A[1]   | DQ[1]/A[1]   | MMC_D1  |
| G1  | PVDDQ | I/O          |     | P_GPIO[2]  | DQ[2]       | DQ[2]/A[2]   | DQ[2]/A[2]   | MMC_D2  |
| E3  | PVDDQ | I/O          |     | P_GPIO[3]  | DQ[3]       | DQ[3]/A[3]   | DQ[3]/A[3]   | MMC_D3  |
| F3  | PVDDQ | I/O          |     | P_GPIO[4]  | DQ[4]       | DQ[4]/A[4]   | DQ[4]/A[4]   | MMC_D4  |
| J1  | PVDDQ | I/O          |     | P_GPIO[5]  | DQ[5]       | DQ[5]/A[5]   | DQ[5]/A[5]   | MMC_D5  |
| G2  | PVDDQ | I/O          |     | P_GPIO[6]  | DQ[6]       | DQ[6]/A[6]   | DQ[6]/A[6]   | MMC_D6  |
| G3  | PVDDQ | I/O          |     | P_GPIO[7]  | DQ[7]       | DQ[7]/A[7]   | DQ[7]/A[7]   | MMC_D7  |
| H2  | PVDDQ | I/O          |     | P_GPIO[8]  | DQ[8]       | DQ[8]/A[8]   | DQ[8]/A[8]   | GPIO    |
| G4  | PVDDQ | I/O          |     | P_GPIO[9]  | DQ[9]       | DQ[9]/A[9]   | DQ[9]/A[9]   | GPIO    |
| J2  | PVDDQ | I/O          |     | P_GPIO[10] | DQ[10]      | DQ[10]/A[10] | DQ[10]/A[10] | GPIO    |
| K2  | PVDDQ | I/O          |     | P_GPIO[11] | DQ[11]      | DQ[11]/A[11] | DQ[11]/A[11] | GPIO    |
| H3  | PVDDQ | I/O          |     | P_GPIO[12] | DQ[12]      | DQ[12]/A[12] | DQ[12]/A[12] | GPIO    |
| L2  | PVDDQ | I/O          |     | P_GPIO[13] | DQ[13]      | DQ[13]/A[13] | DQ[13]/A[13] | GPIO    |
| H4  | PVDDQ | I/O          |     | P_GPIO[14] | DQ[14]      | DQ[14]/A[14] | DQ[14]/A[14] | GPIO    |
| J3  | PVDDQ | I/O          |     | P_GPIO[15] | DQ[15]      | DQ[15]/A[15] | DQ[15]/A[15] | GPIO    |
| K6  | PVDDQ | I/O          |     | P_GPIO[16] | CLK         | CLK          | CLK          | MMC_CLK |
| L3  | PVDDQ | I/O          |     | P_GPIO[17] | CE#         | CE#          | CE#          | GPIO    |
| H5  | PVDDQ | I/O          |     | P_GPIO[18] | WE#         | WE#          | WE#          | MMC_CMD |
| J4  | PVDDQ | I/O          |     | P_GPIO[19] | OE#         | OE#          | OE#          | GPIO    |
| H6  | PVDDQ | I/O          |     | P_GPIO[20] | DACK#       | DACK#        | DACK#        | GPIO    |
| K5  | PVDDQ | I/O          |     | P_GPIO[21] | DRQ#        | DRQ#         | DRQ#         | GPIO    |
| J5  | PVDDQ | I/O          |     | P_GPIO[22] | A[7]        | GPIO         | GPIO         | GPIO    |
| L6  | PVDDQ | I/O          |     | P_GPIO[23] | A[6]        | GPIO         | RDY          | GPIO    |
| K3  | PVDDQ | I/O          |     | P_GPIO[24] | A[5]        | GPIO         | GPIO         | GPIO    |
| J6  | PVDDQ | I/O          |     | P_GPIO[25] | A[4]        | GPIO         | GPIO         | GPIO    |
| K7  | PVDDQ | I/O          |     | P_GPIO[26] | A[3]        | GPIO         | GPIO         | GPIO    |
| J7  | PVDDQ | I/O          |     | P_GPIO[27] | A[2]        | ADV#         | ADV#         | GPIO    |

**Table 8. WLCSP Pin List (continued)**

| Pin            | Power Domain | I/O | Name        | Description   |                |               |                  |                      |
|----------------|--------------|-----|-------------|---------------|----------------|---------------|------------------|----------------------|
| K8             | PVDDQ        | I/O | P_GPIO[28]  | A[1]          | GPIO           | GPIO          | UART_RX          |                      |
| L8             | PVDDQ        | I/O | P_GPIO[29]  | A[0]          | GPIO           | GPIO          | UART_TX          |                      |
| L9             | PVDDQ        | I/O | P_GPIO[30]  | PMODE[0]      | PMODE[0]       | PMODE[0]      | PMODE[0]         |                      |
| J8             | PVDDQ        | I/O | P_GPIO[31]  | PMODE[1]      | PMODE[1]       | PMODE[1]      | PMODE[1]         |                      |
| K9             | PVDDQ        | I/O | P_GPIO[32]  | PMODE[2]      | PMODE[2]       | PMODE[2]      | PMODE[2]         |                      |
| K4             | PVDDQ        | O   | INT#        | INT#          | INT#           | INT#          | INT#             |                      |
| D8             | CVDDQ        | I   | RESET#      | RESET#        | RESET#         | RESET#        | RESET#           |                      |
| <b>S0-Port</b> |              |     |             |               |                |               |                  |                      |
|                |              |     |             | <b>8b MMC</b> | <b>SD+GPIO</b> |               | <b>GPIO</b>      |                      |
| K10            | SVDDQ        | I/O | S0_GPIO[33] | S0_SD0        | S0_SD0         |               | GPIO             |                      |
| K11            | SVDDQ        | I/O | S0_GPIO[34] | S0_SD1        | S0_SD1         |               | GPIO             |                      |
| K12            | SVDDQ        | I/O | S0_GPIO[35] | S0_SD2        | S0_SD2         |               | GPIO             |                      |
| J9             | SVDDQ        | I/O | S0_GPIO[36] | S0_SD3        | S0_SD3         |               | GPIO             |                      |
| J10            | SVDDQ        | I/O | S0_GPIO[37] | S0_SD4        | GPIO           |               | GPIO             |                      |
| J11            | SVDDQ        | I/O | S0_GPIO[38] | S0_SD5        | GPIO           |               | GPIO             |                      |
| H8             | SVDDQ        | I/O | S0_GPIO[39] | S0_SD6        | GPIO           |               | GPIO             |                      |
| H11            | SVDDQ        | I/O | S0_GPIO[40] | S0_SD7        | GPIO           |               | GPIO             |                      |
| H10            | SVDDQ        | I/O | S0_GPIO[41] | S0_CMD        | S0_CMD         |               | GPIO             |                      |
| H9             | SVDDQ        | I/O | S0_GPIO[42] | S0_CLK        | S0_CLK         |               | GPIO             |                      |
| G11            | SVDDQ        | I/O | S0_GPIO[43] | S0_WP         | S0_WP          |               | GPIO             |                      |
| G10            | SVDDQ        | I/O | S0_GPIO[44] | S0S1_INS      | S0S1_INS       |               | GPIO             |                      |
| G9             | SVDDQ        | I/O | S0_GPIO[45] | MMC0_RST_OUT  | GPIO           |               | GPIO             |                      |
| <b>S1-Port</b> |              |     |             |               |                |               |                  |                      |
|                |              |     |             | <b>8b MMC</b> | <b>SD+UART</b> | <b>SD+SPI</b> | <b>SD+GPIO</b>   | <b>GPIO</b>          |
| F11            | SVDDQ        | I/O | S1_GPIO[46] | S1_SD0        | S1_SD0         | S1_SD0        | S1_SD0           | GPIO                 |
| F10            | SVDDQ        | I/O | S1_GPIO[47] | S1_SD1        | S1_SD1         | S1_SD1        | S1_SD1           | GPIO                 |
| E11            | SVDDQ        | I/O | S1_GPIO[48] | S1_SD2        | S1_SD2         | S1_SD2        | S1_SD2           | GPIO                 |
| D12            | SVDDQ        | I/O | S1_GPIO[49] | S1_SD3        | S1_SD3         | S1_SD3        | S1_SD3           | GPIO                 |
| D11            | SVDDQ        | I/O | S1_GPIO[50] | S1_CMD        | S1_CMD         | S1_CMD        | S1_CMD           | GPIO                 |
| E10            | SVDDQ        | I/O | S1_GPIO[51] | S1_CLK        | S1_CLK         | S1_CLK        | S1_CLK           | GPIO                 |
| E9             | SVDDQ        | I/O | S1_GPIO[52] | S1_WP         | S1_WP          | S1_WP         | S1_WP            | GPIO                 |
|                |              |     |             |               |                |               | <b>4b SD+I2S</b> | <b>GPIO+UART+SPI</b> |
|                |              |     |             |               |                |               | S1_SD0           | GPIO                 |
|                |              |     |             |               |                |               | S1_SD1           | GPIO                 |
|                |              |     |             |               |                |               | S1_SD2           | GPIO                 |
|                |              |     |             |               |                |               | S1_SD3           | GPIO                 |
|                |              |     |             |               |                |               | S1_CMD           | I2S_CLK              |
|                |              |     |             |               |                |               | S1_CLK           | I2S_SD               |
|                |              |     |             |               |                |               | S1_WP            | I2S_WS               |
|                |              |     |             |               |                |               |                  | <b>UART+SPI+I2S</b>  |
|                |              |     |             |               |                |               |                  | UART_RTS             |
|                |              |     |             |               |                |               |                  | UART_CTS             |
|                |              |     |             |               |                |               |                  | UART_TX              |
|                |              |     |             |               |                |               |                  | UART_RX              |
|                |              |     |             |               |                |               |                  | I2S_CLK              |
|                |              |     |             |               |                |               |                  | I2S_SD               |
|                |              |     |             |               |                |               |                  | I2S_WS               |

**Table 8. WLCSP Pin List (continued)**

| Pin            |  |  |  | Power Domain | I/O | Name                      | Description                                           |          |          |      |      |          |          |          |
|----------------|--|--|--|--------------|-----|---------------------------|-------------------------------------------------------|----------|----------|------|------|----------|----------|----------|
| D10            |  |  |  | LVDDQ        | I/O | L_GPIO[53]                | S1_SD4                                                | UART_RTS | SPI_SCK  | GPIO | GPIO | UART_RTS | GPIO     | SPI_SCK  |
| D9             |  |  |  | LVDDQ        | I/O | L_GPIO[54]                | S1_SD5                                                | UART_CTS | SPI_SSN  | GPIO | GPIO | UART_CTS | GPIO     | SPI_SSN  |
| B12            |  |  |  | LVDDQ        | I/O | L_GPIO[55]                | S1_SD6                                                | UART_TX  | SPI_MISO | GPIO | GPIO | UART_TX  | GPIO     | SPI_MISO |
| C12            |  |  |  | LVDDQ        | I/O | L_GPIO[56]                | S1_SD7                                                | UART_RX  | SPI_MOSI | GPIO | GPIO | UART_RX  | GPIO     | SPI_MOSI |
| E12            |  |  |  | LVDDQ        | I/O | L_GPIO[57]                | MMC1_RST_OUT                                          | GPIO     | GPIO     | GPIO | GPIO | I2S_MCLK | I2S_MCLK | I2S_MCLK |
| U-Port         |  |  |  |              |     |                           |                                                       |          |          |      |      |          |          |          |
| C3             |  |  |  | VBUS/VBATT   | I   | OTG_ID                    | USB OTG Identification                                |          |          |      |      |          |          |          |
| A10            |  |  |  |              | I   | NC                        | No Connect                                            |          |          |      |      |          |          |          |
| B10            |  |  |  |              | I   | NC                        | No Connect                                            |          |          |      |      |          |          |          |
| A8             |  |  |  |              | O   | NC                        | No Connect                                            |          |          |      |      |          |          |          |
| B8             |  |  |  |              | O   | NC                        | No Connect                                            |          |          |      |      |          |          |          |
| A4             |  |  |  | VBUS/VBATT   | I/O | DP                        | USB (HS/FS) Data Plus                                 |          |          |      |      |          |          |          |
| A2             |  |  |  | VBUS/VBATT   | I/O | DM                        | USB (HS/FS) Data Minus                                |          |          |      |      |          |          |          |
| B4             |  |  |  | VBUS/VBATT   | I/O | SWDP                      | USB (HS/FS) Switch Interface Data Plus                |          |          |      |      |          |          |          |
| B2             |  |  |  | VBUS/VBATT   | I/O | SWDM                      | USB (HS/FS) Switch Interface Data Minus               |          |          |      |      |          |          |          |
| Crystal/Clocks |  |  |  |              |     |                           |                                                       |          |          |      |      |          |          |          |
| A7             |  |  |  | CVDDQ        | I   | FSLC[0]                   | Frequency Select 0                                    |          |          |      |      |          |          |          |
| B6             |  |  |  | AVDD         | I/O | XTALIN                    | Crystal Oscillator Input                              |          |          |      |      |          |          |          |
| B5             |  |  |  | AVDD         | I/O | XTALOUT                   | Crystal Oscillator Output                             |          |          |      |      |          |          |          |
| F9             |  |  |  | CVDDQ        | I   | FSLC[1]                   | Frequency Select 1                                    |          |          |      |      |          |          |          |
| B7             |  |  |  | CVDDQ        | I   | FSLC[2]                   | Frequency Select 2                                    |          |          |      |      |          |          |          |
| C5             |  |  |  | CVDDQ        | I   | CLKIN                     | External Clock Input                                  |          |          |      |      |          |          |          |
| C6             |  |  |  | CVDDQ        | I   | CLKIN_32                  | 32.76-kHz Clock Input for Watchdog Timer              |          |          |      |      |          |          |          |
| Other          |  |  |  |              |     |                           |                                                       |          |          |      |      |          |          |          |
| D6             |  |  |  | I2CVDDQ      | I/O | I <sup>2</sup> C_GPIO[58] | Serial Clock (SCL) for I <sup>2</sup> C Bus Interface |          |          |      |      |          |          |          |
| D2             |  |  |  | I2CVDDQ      | I/O | I <sup>2</sup> C_GPIO[59] | Serial Data (SDA) for I <sup>2</sup> C Bus Interface  |          |          |      |      |          |          |          |
| F8             |  |  |  | I2CVDDQ      | I   | TDI                       | Test Data In (TDI) for JTAG Interface                 |          |          |      |      |          |          |          |
| C2             |  |  |  | I2CVDDQ      | O   | TDO                       | Test Data Out (TDO) for JTAG Interface                |          |          |      |      |          |          |          |
| C1             |  |  |  | I2CVDDQ      | O   | TRST#                     | Test Reset (TRST) for JTAG Interface                  |          |          |      |      |          |          |          |
| D5             |  |  |  | I2CVDDQ      | O   | TMS                       | Test Mode Select (TMS) for JTAG Interface             |          |          |      |      |          |          |          |
| D3             |  |  |  | I2CVDDQ      | O   | TCK                       | Test Clock (TCK) for JTAG Interface                   |          |          |      |      |          |          |          |

**Table 8. WLCSP Pin List** (continued)

| Pin | Power Domain | I/O | Name      | Description                                      |
|-----|--------------|-----|-----------|--------------------------------------------------|
| E8  | I2CVDDQ      | O   | O[60]     | Charger Detect Output                            |
|     |              |     |           | <b>Power</b>                                     |
| E2  |              | PWR | VBATT     | USB Supply Voltage Input                         |
| B1  |              | PWR | VDD       | E-fuse Program Supply                            |
| A1  |              | PWR | VDD       | E-fuse Program Supply                            |
| C9  |              | PWR | VSS       | GND                                              |
| E1  |              | PWR | VBUS      | USB Supply Voltage Input                         |
| C4  |              | PWR | U2PLLVSQ  | USB2 Regulator GND                               |
| H1  |              | PWR | PVDDQ     | P-Port Supply Voltage Input                      |
| K1  |              | PWR | VSS       | GND                                              |
| L4  |              | PWR | PVDDQ     | P-Port Supply Voltage Input                      |
| L5  |              | PWR | VSS       | GND                                              |
| L7  |              | PWR | PVDDQ     | P-Port Supply Voltage Input                      |
| L1  |              | PWR | VSS       | GND                                              |
| J12 |              | PWR | S0VDDQ    | S0-Port Supply Voltage Input                     |
| H12 |              | PWR | VSS       | GND                                              |
| G12 |              | PWR | S0VDDQ    | S0- Port Supply Voltage Input                    |
| C11 |              | PWR | S1VDDQ    | S1-Port Supply Voltage Input                     |
| F12 |              | PWR | VSS       | GND                                              |
| B11 |              | PWR | LVDDQ     | Low-Performance Peripherals Supply Voltage Input |
| A11 |              | PWR | VSS       | GND                                              |
| A12 |              | PWR | VSS       | GND                                              |
| C7  |              | PWR | CVDDQ     | Clock-Supply Voltage Input                       |
| C8  |              | PWR | VDD       | Core-Supply Voltage Input                        |
| C10 |              | PWR | VDD       | Core-Supply Voltage Input                        |
| D4  |              | PWR | I2CVDDQ   | I2C- and JTAG-Supply Voltage Input               |
| A3  |              | PWR | U2AFEVSSQ | GND                                              |
| A5  |              | PWR | AVDD      | Analog-Supply Voltage Input                      |
| A6  |              | PWR | AVSS      | Analog GND                                       |
| F4  |              | PWR | VDD       | Core-Supply Voltage Input                        |
| D1  |              | PWR | VSS       | GND                                              |
| F5  |              | PWR | VDD       | Core-Supply Voltage Input                        |

**Table 8. WLCSP Pin List (continued)**

| Pin | Power Domain   | I/O | Name   | Description                                                                               |
|-----|----------------|-----|--------|-------------------------------------------------------------------------------------------|
| E4  |                | PWR | VSS    | GND                                                                                       |
| F6  |                | PWR | VDD    | Core-Supply Voltage Input                                                                 |
| E5  |                | PWR | VSS    | GND                                                                                       |
| F7  |                | PWR | VDD    | Core-Supply Voltage Input                                                                 |
| E6  |                | PWR | VSS    | GND                                                                                       |
| D7  |                | PWR | VDD    | Core-Supply Voltage Input                                                                 |
| E7  |                | PWR | VSS    | GND                                                                                       |
| G6  |                | PWR | VDD    | Core-Supply Voltage Input                                                                 |
| L10 |                | PWR | VDD    | Core-Supply Voltage Input                                                                 |
| L12 |                | PWR | VDD    | Core-Supply Voltage Input                                                                 |
| H7  |                | PWR | VSS    | GND                                                                                       |
| G7  |                | PWR | VSS    | GND                                                                                       |
| L11 |                | PWR | VSS    | GND                                                                                       |
| G8  |                | PWR | VSS    | GND                                                                                       |
| G5  |                | PWR | VSS    | GND                                                                                       |
| B3  | VBATT/<br>VBUS | I/O | R_USB2 | Precision Resistor for USB 2.0 (Connect a 6.04-kΩ ± 1% resistor between this pin and GND) |
| B9  |                | I/O | NC     | No Connect                                                                                |

**Table 9. BGA Pin List**

| Pin | Power Domain | I/O | Name      | Description         |
|-----|--------------|-----|-----------|---------------------|
|     |              |     |           | P-Port              |
| F10 | PVDDQ        | I/O | P_GPIO[0] | Async SRAM<br>DQ[0] |
| F9  | PVDDQ        | I/O | P_GPIO[1] | DQ[1]               |
| F7  | PVDDQ        | I/O | P_GPIO[2] | DQ[2]               |
| G10 | PVDDQ        | I/O | P_GPIO[3] | DQ[3]               |
| G9  | PVDDQ        | I/O | P_GPIO[4] | DQ[4]               |
| F8  | PVDDQ        | I/O | P_GPIO[5] | DQ[5]               |
| H10 | PVDDQ        | I/O | P_GPIO[6] | DQ[6]               |
|     |              |     |           | Async ADMux         |
|     |              |     |           | DQ[0]/A[0]          |
|     |              |     |           | DQ[1]/A[1]          |
|     |              |     |           | DQ[2]/A[2]          |
|     |              |     |           | DQ[3]/A[3]          |
|     |              |     |           | DQ[4]/A[4]          |
|     |              |     |           | DQ[5]/A[5]          |
|     |              |     |           | DQ[6]/A[6]          |
|     |              |     |           | Sync ADMux          |
|     |              |     |           | DQ[0]/A[0]          |
|     |              |     |           | DQ[1]/A[1]          |
|     |              |     |           | DQ[2]/A[2]          |
|     |              |     |           | DQ[3]/A[3]          |
|     |              |     |           | DQ[4]/A[4]          |
|     |              |     |           | DQ[5]/A[5]          |
|     |              |     |           | DQ[6]/A[6]          |
|     |              |     |           | PMMC                |
|     |              |     |           | MMC_D0              |
|     |              |     |           | MMC_D1              |
|     |              |     |           | MMC_D2              |
|     |              |     |           | MMC_D3              |
|     |              |     |           | MMC_D4              |
|     |              |     |           | MMC_D5              |
|     |              |     |           | MMC_D6              |

**Table 9. BGA Pin List**

| Pin | Power Domain | I/O | Name        | Description |              |              |          |
|-----|--------------|-----|-------------|-------------|--------------|--------------|----------|
| H9  | PVDDQ        | I/O | P_GPIO[7]   | DQ[7]       | DQ[7]/A[7]   | DQ[7]/A[7]   | MMC_D7   |
| J10 | PVDDQ        | I/O | P_GPIO[8]   | DQ[8]       | DQ[8]/A[8]   | DQ[8]/A[8]   | GPIO     |
| J9  | PVDDQ        | I/O | P_GPIO[9]   | DQ[9]       | DQ[9]/A[9]   | DQ[9]/A[9]   | GPIO     |
| K11 | PVDDQ        | I/O | P_GPIO[10]  | DQ[10]      | DQ[10]/A[10] | DQ[10]/A[10] | GPIO     |
| L10 | PVDDQ        | I/O | P_GPIO[11]  | DQ[11]      | DQ[11]/A[11] | DQ[11]/A[11] | GPIO     |
| K10 | PVDDQ        | I/O | P_GPIO[12]  | DQ[12]      | DQ[12]/A[12] | DQ[12]/A[12] | GPIO     |
| K9  | PVDDQ        | I/O | P_GPIO[13]  | DQ[13]      | DQ[13]/A[13] | DQ[13]/A[13] | GPIO     |
| J8  | PVDDQ        | I/O | P_GPIO[14]  | DQ[14]      | DQ[14]/A[14] | DQ[14]/A[14] | GPIO     |
| G8  | PVDDQ        | I/O | P_GPIO[15]  | DQ[15]      | DQ[15]/A[15] | DQ[15]/A[15] | GPIO     |
| J6  | PVDDQ        | I/O | P_GPIO[16]  | CLK         | CLK          | CLK          | MMC_CLK  |
| K8  | PVDDQ        | I/O | P_GPIO[17]  | CE#         | CE#          | CE#          | GPIO     |
| K7  | PVDDQ        | I/O | P_GPIO[18]  | WE#         | WE#          | WE#          | MMC_CMD  |
| J7  | PVDDQ        | I/O | P_GPIO[19]  | OE#         | OE#          | OE#          | GPIO     |
| H7  | PVDDQ        | I/O | P_GPIO[20]  | DACK#       | DACK#        | DACK#        | GPIO     |
| G7  | PVDDQ        | I/O | P_GPIO[21]  | DRQ#        | DRQ#         | DRQ#         | GPIO     |
| G6  | PVDDQ        | I/O | P_GPIO[22]  | A[7]        | GPIO         | GPIO         | GPIO     |
| K6  | PVDDQ        | I/O | P_GPIO[23]  | A[6]        | GPIO         | RDY          | GPIO     |
| H8  | PVDDQ        | I/O | P_GPIO[24]  | A[5]        | GPIO         | GPIO         | GPIO     |
| G5  | PVDDQ        | I/O | P_GPIO[25]  | A[4]        | GPIO         | GPIO         | GPIO     |
| H6  | PVDDQ        | I/O | P_GPIO[26]  | A[3]        | GPIO         | GPIO         | GPIO     |
| K5  | PVDDQ        | I/O | P_GPIO[27]  | A[2]        | ADV#         | ADV#         | GPIO     |
| J5  | PVDDQ        | I/O | P_GPIO[28]  | A[1]        | GPIO         | GPIO         | UART_RX  |
| H5  | PVDDQ        | I/O | P_GPIO[29]  | A[0]        | GPIO         | GPIO         | UART_TX  |
| G4  | PVDDQ        | I/O | P_GPIO[30]  | PMODE[0]    | PMODE[0]     | PMODE[0]     | PMODE[0] |
| H4  | PVDDQ        | I/O | P_GPIO[31]  | PMODE[1]    | PMODE[1]     | PMODE[1]     | PMODE[1] |
| L4  | PVDDQ        | I/O | P_GPIO[32]  | PMODE[2]    | PMODE[2]     | PMODE[2]     | PMODE[2] |
| L8  | PVDDQ        | I/O | INT#        | INT#        | INT#         | INT#         | INT#     |
| C5  | CVDDQ        | I   | RESET#      | RESET#      | RESET#       | RESET#       | RESET#   |
|     |              |     |             | S0-Port     |              |              |          |
|     |              |     |             | 8b MMC      | SD+GPIO      |              | GPIO     |
| K2  | S0VDDQ       | I/O | S0_GPIO[33] | S0_SD0      | S0_SD0       |              | GPIO     |
| J4  | S0VDDQ       | I/O | S0_GPIO[34] | S0_SD1      | S0_SD1       |              | GPIO     |

**Table 9. BGA Pin List**

| Pin | Power Domain | I/O | Name        | Description  |          |          |         |      |               |         |              |
|-----|--------------|-----|-------------|--------------|----------|----------|---------|------|---------------|---------|--------------|
| K1  | S0VDDQ       | I/O | S0_GPIO[35] | S0_SD2       | S0_SD2   |          |         |      |               |         | GPIO         |
| J2  | S0VDDQ       | I/O | S0_GPIO[36] | S0_SD3       | S0_SD3   |          |         |      |               |         | GPIO         |
| J3  | S0VDDQ       | I/O | S0_GPIO[37] | S0_SD4       | S0_SD4   |          |         |      |               |         | GPIO         |
| J1  | S0VDDQ       | I/O | S0_GPIO[38] | S0_SD5       | S0_SD5   |          |         |      |               |         | GPIO         |
| H2  | S0VDDQ       | I/O | S0_GPIO[39] | S0_SD6       | S0_SD6   |          |         |      |               |         | GPIO         |
| H3  | S0VDDQ       | I/O | S0_GPIO[40] | S0_SD7       | S0_SD7   |          |         |      |               |         | GPIO         |
| F4  | S0VDDQ       | I/O | S0_GPIO[41] | S0_CMD       | S0_CMD   |          |         |      |               |         | GPIO         |
| G2  | S0VDDQ       | I/O | S0_GPIO[42] | S0_CLK       | S0_CLK   |          |         |      |               |         | GPIO         |
| G3  | S0VDDQ       | I/O | S0_GPIO[43] | S0_WP        | S0_WP    |          |         |      |               |         | GPIO         |
| F3  | S0VDDQ       | I/O | S0_GPIO[44] | S0S1_INS     | S0S1_INS |          |         |      |               |         | GPIO         |
| F2  | S0VDDQ       | I/O | S0_GPIO[45] | MMC0_RST_OUT |          |          |         |      |               |         | GPIO         |
|     |              |     |             | S1-Port      |          |          |         |      |               |         |              |
|     |              |     |             | 8b MMC       | SD+UART  | SD+SPI   | SD+GPIO | GPIO | GPIO+UART+I2S | SD+I2S  | UART+SPI+I2S |
| F5  | S1VDDQ       | I/O | S1_GPIO[46] | S1_SD0       | S1_SD0   | S1_SD0   | S1_SD0  | GPIO | GPIO          | S1_SD0  | UART_RTS     |
| E1  | S1VDDQ       | I/O | S1_GPIO[47] | S1_SD1       | S1_SD1   | S1_SD1   | S1_SD1  | GPIO | GPIO          | S1_SD1  | UART_CTS     |
| E5  | S1VDDQ       | I/O | S1_GPIO[48] | S1_SD2       | S1_SD2   | S1_SD2   | S1_SD2  | GPIO | GPIO          | S1_SD2  | UART_TX      |
| E4  | S1VDDQ       | I/O | S1_GPIO[49] | S1_SD3       | S1_SD3   | S1_SD3   | S1_SD3  | GPIO | GPIO          | S1_SD3  | UART_RX      |
| D1  | S1VDDQ       | I/O | S1_GPIO[50] | S1_CMD       | S1_CMD   | S1_CMD   | S1_CMD  | GPIO | I2S_CLK       | S1_CMD  | I2S_CLK      |
| D2  | S1VDDQ       | I/O | S1_GPIO[51] | S1_CLK       | S1_CLK   | S1_CLK   | S1_CLK  | GPIO | I2S_SD        | S1_CLK  | I2S_SD       |
| D3  | S1VDDQ       | I/O | S1_GPIO[52] | S1_WP        | S1_WP    | S1_WP    | S1_WP   | GPIO | I2S_WS        | S1_WP   | I2S_WS       |
| D4  | LVDDQ        | I/O | L_GPIO[53]  | S1_SD4       | UART_RTS | SPI_SC   | GPIO    | GPIO | UART_RTS      | GPIO    | SPI_SCK      |
| C1  | LVDDQ        | I/O | L_GPIO[54]  | S1_SD5       | UART_CTS | SPI_SS   | GPIO    | GPIO | UART_CTS      | I2S_CLK | SPI_SSN      |
| C2  | LVDDQ        | I/O | L_GPIO[55]  | S1_SD6       | UART_TX  | SPI_MISO | GPIO    | GPIO | UART_TX       | I2S_SD  | SPI_MISO     |
| D5  | LVDDQ        | I/O | L_GPIO[56]  | S1_SD7       | UART_RX  | SPI_MOSI | GPIO    | GPIO | UART_RX       | I2S_WS  | SPI_MOSI     |

**Table 9. BGA Pin List**

| Pin | Power Domain | I/O | Name         | Description                         |      |      |      |          |          |          |
|-----|--------------|-----|--------------|-------------------------------------|------|------|------|----------|----------|----------|
| C4  | LVDDQ        | I/O | L_GPIO[57]   | MMC1_R<br>ST_OUT                    | GPIO | GPIO | GPIO | I2S_MCLK | I2S_MCLK | I2S_MCLK |
|     |              |     |              | USB Port (VBATT/VBUS Power Domain)  |      |      |      |          |          |          |
| C9  | VBUS/VBATT   | I   | OTG_ID       | OTG_ID                              |      |      |      |          |          |          |
|     |              |     |              | USB Port (VBATT/VBUS Power Domain)  |      |      |      |          |          |          |
| A3  |              | I   | NC           | No Connect                          |      |      |      |          |          |          |
| A4  |              | I   | NC           | No Connect                          |      |      |      |          |          |          |
| A6  |              | O   | NC           | No Connect                          |      |      |      |          |          |          |
| A5  |              | O   | NC           | No Connect                          |      |      |      |          |          |          |
| A9  | VBUS/VBATT   | I/O | DP           | D+                                  |      |      |      |          |          |          |
| A10 | VBUS/VBATT   | I/O | DM           | D-                                  |      |      |      |          |          |          |
| A11 |              |     | NC           | Do Not Connect                      |      |      |      |          |          |          |
|     |              |     |              | Crystal/Clocks (CVDDQ Power Domain) |      |      |      |          |          |          |
| B2  | CVDDQ        | I   | FSLC[0]      | FSLC[0]                             |      |      |      |          |          |          |
| C6  | AVDD         | I/O | XTALIN       | XTALIN                              |      |      |      |          |          |          |
| C7  | AVDD         | I/O | XTALOUT      | XTALOUT                             |      |      |      |          |          |          |
| B4  | CVDDQ        | I   | FSLC[1]      | FSLC[1]                             |      |      |      |          |          |          |
| E6  | CVDDQ        | I   | FSLC[2]      | FSLC[2]                             |      |      |      |          |          |          |
| D7  | CVDDQ        | I   | CLKIN        | CLKIN                               |      |      |      |          |          |          |
| D6  | CVDDQ        | I   | CLKIN_32     | CLKIN_32                            |      |      |      |          |          |          |
|     |              |     |              | I2C and JTAG (I2CVDDQ Power Domain) |      |      |      |          |          |          |
| D9  | I2CVDDQ      | I/O | I2C_GPIO[58] | I <sup>2</sup> C_SCL                |      |      |      |          |          |          |
| D10 | I2CVDDQ      | I/O | I2C_GPIO[59] | I <sup>2</sup> C_SDA                |      |      |      |          |          |          |
| E7  | I2CVDDQ      | I   | TDI          | TDI                                 |      |      |      |          |          |          |
| C10 | I2CVDDQ      | O   | TDO          | TDO                                 |      |      |      |          |          |          |
| B11 | I2CVDDQ      | I   | TRST#        | TRST#                               |      |      |      |          |          |          |
| E8  | I2CVDDQ      | I   | TMS          | TMS                                 |      |      |      |          |          |          |
| F6  | I2CVDDQ      | I   | TCK          | TCK                                 |      |      |      |          |          |          |
| D11 | I2CVDDQ      | O   | O[60]        | Charger detect output               |      |      |      |          |          |          |
|     |              |     |              | Power                               |      |      |      |          |          |          |

**Table 9. BGA Pin List**

| Pin | Power Domain | I/O | Name    | Description |
|-----|--------------|-----|---------|-------------|
| E10 |              | PWR | VBATT   |             |
| B10 |              | PWR | VDD     |             |
| A1  |              | PWR | VSS     |             |
| E11 |              | PWR | VBUS    |             |
| D8  |              | PWR | VSS     |             |
| H11 |              | PWR | PVDDQ   |             |
| E2  |              | PWR | VSS     |             |
| L9  |              | PWR | PVDDQ   |             |
| G1  |              | PWR | VSS     |             |
| F1  |              | PWR | S0VDDQ  |             |
| G11 |              | PWR | VSS     |             |
| E3  |              | PWR | S1VDDQ  |             |
| L1  |              | PWR | VSS     |             |
| B1  |              | PWR | LVDDQ   |             |
| L6  |              | PWR | VSS     |             |
| B6  |              | PWR | CVDDQ   |             |
| B5  |              | PWR | VDD     |             |
| A2  |              | PWR | VDD     |             |
| C11 |              | PWR | I2CVDDQ |             |
| L11 |              | PWR | VSS     |             |
| A7  |              | PWR | AVDD    |             |
| B7  |              | PWR | AVSS    |             |
| C3  |              | PWR | VDD     |             |
| B8  |              | PWR | VSS     |             |
| E9  |              | PWR | VDD     |             |
| B9  |              | PWR | VSS     |             |
| F11 |              | PWR | VDD     |             |
| H1  |              | PWR | VDD     |             |
| L7  |              | PWR | VDD     |             |
| J11 |              | PWR | VDD     |             |
| L5  |              | PWR | VDD     |             |
| K4  |              | PWR | VSS     |             |

**Table 9. BGA Pin List**

| Pin | Power Domain | I/O | Name   | Description                                                                                           |
|-----|--------------|-----|--------|-------------------------------------------------------------------------------------------------------|
| L3  |              | PWR | VSS    |                                                                                                       |
| K3  |              | PWR | VSS    |                                                                                                       |
| L2  |              | PWR | VSS    |                                                                                                       |
| A8  |              | PWR | VSS    |                                                                                                       |
|     |              |     |        | Precision Resistors                                                                                   |
| C8  | VBUS/VBATT   | I/O | R_usb2 | Precision Resistor for USB 2.0 (Connect a 6.04 k $\Omega$ $\pm$ 1% resistor between this pin and GND) |
| B3  |              | I/O | NC     | No Connect                                                                                            |

## Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device.

Storage temperature..... -65 °C to +150 °C

Ambient temperature with power supplied (Industrial)..... -40 °C to +85 °C

Supply voltage to ground potential

$V_{DD}$ ,  $A_{VDDQ}$ ..... 1.25 V

$P_{VDDQ}$ ,  $S0_{VDDQ}$ ,  $S1_{VDDQ}$ ,  $L_{VDDQ}$ ,

$C_{VDDQ}$ ,  $I^2C_{VDDQ}$ ..... 3.6 V

DC input voltage to any input pin..... VCC + 0.3

DC voltage applied to outputs in HIGH-Z state..... VCC + 0.3

(VCC is the corresponding IO voltage)

Static discharge voltage ESD protection levels:

■  $\pm 2.2$  KV HBM based on JESD22-A114

■ Additional ESD protection levels on D+, D-, OTG\_ID,  $V_{BUS}$ , GND pins U-port and S1\_D[0:7], S1\_CMD, S1\_CLK, S1\_WP, MMC1RST\_OUT pins S1-Port.

■  $\pm 6$  KV contact discharge,  $\pm 8$  KV air gap discharge based on IEC61000-4-2 level 3A,  $\pm 8$  KV Contact Discharge, and  $\pm 15$  KV air gap discharge based on IEC61000-4-2 level 4C

Latch-up current..... > 200 mA

Maximum output short-circuit current for all I/O configurations. ( $V_{out} = 0$  V)..... -100 mA

## Operating Conditions

Ambient temperature under bias ( $T_A$ )

Industrial..... -40 °C to +85 °C

$V_{DD}$ ,  $A_{VDDQ}$ , supply voltage..... 1.15 V to 1.25 V

$V_{BATT}$  supply voltage..... 3.2 V to 6 V

$P_{VDDQ}$ ,  $S0_{VDDQ}$ ,  $S1_{VDDQ}$ ,  $L_{VDDQ}$ ,  $C_{VDDQ}$  supply voltage..... 1.7 V to 3.6 V

$I^2C_{VDDQ}$  supply voltage..... 1.15 V to 3.6 V

## DC Specifications

| Parameter     | Description                | Min                   | Max                  | Units | Notes                                                                                                                         |
|---------------|----------------------------|-----------------------|----------------------|-------|-------------------------------------------------------------------------------------------------------------------------------|
| $V_{DD}$      | Core voltage supply        | 1.15                  | 1.25                 | V     | 1.2-V typical                                                                                                                 |
| $A_{VDD}$     | Analog voltage supply      | 1.15                  | 1.25                 | V     | 1.2-V typical                                                                                                                 |
| $P_{VDDQ}$    | P-Port I/O voltage supply  | 1.7                   | 3.6                  | V     | 1.8-, 2.5-, and 3.3-V typical                                                                                                 |
| $S0_{VDDQ}$   | S0 Port I/O voltage supply | 1.7                   | 3.6                  | V     | 1.8-, 2.5-, and 3.3-V typical                                                                                                 |
| $S1_{VDDQ}$   | S1 Port I/O voltage supply | 1.7                   | 3.6                  | V     | 1.8-, 2.5-, and 3.3-V typical                                                                                                 |
| $L_{VDDQ}$    | LPP I/O voltage supply     | 1.7                   | 3.6                  | V     | 1.8-, 2.5-, and 3.3-V typical                                                                                                 |
| $V_{BATT}$    | USB voltage supply         | 3.2                   | 6                    | V     | 3.7-V typical                                                                                                                 |
| $V_{BUS}$     | USB voltage supply         | 4.0                   | 6                    | V     | 5-V typical                                                                                                                   |
| $C_{VDDQ}$    | Clock voltage supply       | 1.7                   | 3.6                  | V     | 1.8-, 3.3-V typical                                                                                                           |
| $I^2C_{VDDQ}$ | $I^2C$ voltage supply      | 1.15                  | 3.6                  | V     | 1.2-, 1.8-, 2.5-, and 3.3-V typical                                                                                           |
| $V_{IH1}$     | Input HIGH voltage 1       | $0.625 \times V_{CC}$ | $V_{CC}+0.3$         | V     | For $2.0\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ (except USB port). VCC is the corresponding IO voltage supply.               |
| $V_{IH2}$     | Input HIGH voltage 2       | $V_{CC} - 0.4$        | $V_{CC}+0.3$         | V     | For $1.7\text{ V} \leq V_{CC} \leq 2.0\text{ V}$ (except USB port). VCC is the corresponding IO voltage supply.               |
| $V_{IL}$      | Input LOW voltage          | -0.3                  | $0.25 \times V_{CC}$ | V     | VCC is the corresponding I/O voltage supply.                                                                                  |
| $V_{OH}$      | Output HIGH voltage        | $0.9 \times V_{CC}$   | —                    | V     | $I_{OH}(\text{max}) = -100\text{ }\mu\text{A}$ tested at quarter drive strength. VCC is the corresponding I/O voltage supply. |
| $V_{OL}$      | Output LOW voltage         | —                     | $0.1 \times V_{CC}$  | V     | $I_{OL}(\text{min}) = +100\text{ }\mu\text{A}$ tested at quarter drive strength. VCC is the corresponding I/O voltage supply. |

**DC Specifications** (continued)

| Parameter       | Description                                        | Min | Max | Units   | Notes                                                                                                                                                                                |
|-----------------|----------------------------------------------------|-----|-----|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $I_{IX}$        | Input leakage current                              | -1  | 1   | $\mu A$ | All I/O signals held at $V_{DDQ}$<br>For I/Os with a pull-up/pull-down resistor connected, the leakage current increases by $V_{DDQ}/R_{pu}$ or $V_{DDQ}/R_{pd}$                     |
| $I_{OZ}$        | Output high-Z leakage current                      | -1  | 1   | $\mu A$ | All I/O signals held at $V_{DDQ}$                                                                                                                                                    |
| $I_{CC}$ Core   | Core and analog voltage operating current          | -   | 200 | mA      | Total current through $A_{VDD}$ , $V_{DD}$                                                                                                                                           |
| $I_{CC}$ USB    | USB voltage supply voltage operating current       | -   | 60  | mA      |                                                                                                                                                                                      |
| $ISB_{suspend}$ | Total suspend current during suspend mode          | -   | -   | mA      | Core current: 250 $\mu A$<br>I/O current: 20 $\mu A$<br>USB current: 1.2 mA<br>For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C.)    |
| $ISB_{standby}$ | Total standby current during standby mode          | -   | -   | $\mu A$ | Core current: 60 $\mu A$<br>I/O current: 20 $\mu A$<br>USB current: 40 $\mu A$<br>For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C.) |
| $ISB_{core}$    | Total standby current during core power-down mode  | -   | -   | $\mu A$ | Core current: 0 $\mu A$<br>I/O current: 20 $\mu A$<br>USB current: 40 $\mu A$<br>For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C.)  |
| $V_{RAMP}$      | Voltage ramp rate on core and I/O supplies         | 0.2 | 50  | V/ms    | Voltage ramp must be monotonic                                                                                                                                                       |
| $V_N$           | Noise level permitted on $V_{DD}$ and I/O supplies | -   | 100 | mV      | Max p-p noise level permitted on all supplies except $A_{VDD}$                                                                                                                       |
| $V_{N\_AVDD}$   | Noise level permitted on $A_{VDD}$ supply          | -   | 20  | mV      | Max p-p noise level permitted on $A_{VDD}$                                                                                                                                           |

## AC Timing Parameters

### Storage Port Timing

The S0-Port and S1-Port support the MMC specification Version 4.4 and SD Specification Version 3.0. [Table 10](#) lists the timing parameters for the Bay device's S-Port.

**Table 10. S-Port Timing Parameters<sup>[5]</sup>**

| Parameter     | Description                    | Min  | Max | Units |
|---------------|--------------------------------|------|-----|-------|
| <b>MMC-20</b> |                                |      |     |       |
| tSDIS CMD     | Host input setup time for CMD  | 4.8  | –   | ns    |
| tSDIS DAT     | Host input setup time for DAT  | 4.8  | –   | ns    |
| tSDIH CMD     | Host input hold time for CMD   | 4.4  | –   | ns    |
| tSDIH DAT     | Host input hold time for DAT   | 4.4  | –   | ns    |
| tSDOS CMD     | Host output setup time for CMD | 5    | –   | ns    |
| tSDOS DAT     | Host output setup time for DAT | 5    | –   | ns    |
| tSDOH CMD     | Host output hold time for CMD  | 5    | –   | ns    |
| tSDOH DAT     | Host output hold time for DAT  | 5    | –   | ns    |
| tSCLKR        | Clock rise time                | –    | 2   | ns    |
| tSCLKF        | Clock fall time                | –    | 2   | ns    |
| tSDCK         | Clock cycle time               | 50   | –   | ns    |
| SDFREQ        | Clock frequency                | –    | 20  | MHz   |
| tSDCLKOD      | Clock duty cycle               | 40   | 60  | %     |
| <b>MMC-26</b> |                                |      |     |       |
| tSDIS CMD     | Host input setup time for CMD  | 10   | –   | ns    |
| tSDIS DAT     | Host input setup time for DAT  | 10   | –   | ns    |
| tSDIH CMD     | Host input hold time for CMD   | 9    | –   | ns    |
| tSDIH DAT     | Host input hold time for DAT   | 9    | –   | ns    |
| tSDOS CMD     | Host output setup time for CMD | 3    | –   | ns    |
| tSDOS DAT     | Host output setup time for DAT | 3    | –   | ns    |
| tSDOH CMD     | Host output hold time for CMD  | 3    | –   | ns    |
| tSDOH DAT     | Host output hold time for DAT  | 3    | –   | ns    |
| tSCLKR        | Clock rise time                | –    | 2   | ns    |
| tSCLKF        | Clock fall time                | –    | 2   | ns    |
| tSDCK         | Clock cycle time               | 38.5 | –   | ns    |
| SDFREQ        | Clock frequency                | –    | 26  | MHz   |
| tSDCLKOD      | Clock duty cycle               | 40   | 60  | %     |
| <b>MC-HS</b>  |                                |      |     |       |
| tSDIS CMD     | Host input setup time for CMD  | 4    | –   | ns    |
| tSDIS DAT     | Host input setup time for DAT  | 4    | –   | ns    |
| tSDIH CMD     | Host input hold time for CMD   | 3    | –   | ns    |
| tSDIH DAT     | Host input hold time for DAT   | 3    | –   | ns    |
| tSDOS CMD     | Host output setup time for CMD | 3    | –   | ns    |
| tSDOS DAT     | Host output setup time for DAT | 3    | –   | ns    |
| tSDOH CMD     | Host output hold time for CMD  | 3    | –   | ns    |
| tSDOH DAT     | Host output hold time for DAT  | 3    | –   | ns    |
| tSCLKR        | Clock rise time                | –    | 2   | ns    |

**Table 10. S-Port Timing Parameters<sup>[5]</sup> (continued)**

| Parameter                       | Description                    | Min  | Max | Units |
|---------------------------------|--------------------------------|------|-----|-------|
| tSCLKF                          | Clock fall time                | –    | 2   | ns    |
| tSDCK                           | Clock cycle time               | 19.2 | –   | ns    |
| SDFREQ                          | Clock frequency                | –    | 52  | MHz   |
| tSDCLKOD                        | Clock duty cycle               | 40   | 60  | %     |
| <b>MMC-DDR52</b>                |                                |      |     |       |
| tSDIS CMD                       | Host input setup time for CMD  | 4    | –   | ns    |
| tSDIS DAT                       | Host input setup time for DAT  | 0.56 | –   | ns    |
| tSDIH CMD                       | Host input hold time for CMD   | 3    | –   | ns    |
| tSDIH DAT                       | Host input hold time for DAT   | 2.58 | –   | ns    |
| tSDOS CMD                       | Host output setup time for CMD | 3    | –   | ns    |
| tSDOS DAT                       | Host output setup time for DAT | 2.5  | –   | ns    |
| tSDOH CMD                       | Host output hold time for CMD  | 3    | –   | ns    |
| tSDOH DAT                       | Host output hold time for DAT  | 2.5  | –   | ns    |
| tSCLKR                          | Clock rise time                | –    | 2   | ns    |
| tSCLKF                          | Clock fall time                | –    | 2   | ns    |
| tSDCK                           | Clock cycle time               | 19.2 | –   | ns    |
| SDFREQ                          | Clock frequency                | –    | 52  | MHz   |
| tSDCLKOD                        | Clock duty cycle               | 45   | 55  | %     |
| <b>SD-Default Speed (SDR12)</b> |                                |      |     |       |
| tSDIS CMD                       | Host input setup time for CMD  | 24   | –   | ns    |
| tSDIS DAT                       | Host input setup time for DAT  | 24   | –   | ns    |
| tSDIH CMD                       | Host input hold time for CMD   | 2.5  | –   | ns    |
| tSDIH DAT                       | Host input hold time for DAT   | 2.5  | –   | ns    |
| tSDOS CMD                       | Host output setup time for CMD | 5    | –   | ns    |
| tSDOS DAT                       | Host output setup time for DAT | 5    | –   | ns    |
| tSDOH CMD                       | Host output hold time for CMD  | 5    | –   | ns    |
| tSDOH DAT                       | Host output hold time for DAT  | 5    | –   | ns    |
| tSCLKR                          | Clock rise time                | –    | 2   | ns    |
| tSCLKF                          | Clock fall time                | –    | 2   | ns    |
| tSDCK                           | Clock cycle time               | 40   | –   | ns    |
| SDFREQ                          | Clock frequency                | –    | 25  | MHz   |
| tSDCLKOD                        | Clock duty cycle               | 40   | 60  | %     |
| <b>SD-High-Speed(SDR25)</b>     |                                |      |     |       |
| tSDIS CMD                       | Host input setup time for CMD  | 4    | –   | ns    |
| tSDIS DAT                       | Host input setup time for DAT  | 4    | –   | ns    |
| tSDIH CMD                       | Host input hold time for CMD   | 2.5  | –   | ns    |
| tSDIH DAT                       | Host input hold time for DAT   | 2.5  | –   | ns    |
| tSDOS CMD                       | Host output setup time for CMD | 6    | –   | ns    |
| tSDOS DAT                       | Host output setup time for DAT | 6    | –   | ns    |
| tSDOH CMD                       | Host output hold time for CMD  | 2    | –   | ns    |
| tSDOH DAT                       | Host output hold time for DAT  | 2    | –   | ns    |
| tSCLKR                          | Clock rise time                | –    | 2   | ns    |

**Table 10. S-Port Timing Parameters<sup>[5]</sup> (continued)**

| Parameter       | Description                    | Min  | Max | Units |
|-----------------|--------------------------------|------|-----|-------|
| tSCLKF          | Clock fall time                | –    | 2   | ns    |
| tSDCK           | Clock cycle time               | 20   | –   | ns    |
| SDFREQ          | Clock frequency                | –    | 50  | MHz   |
| tSDCLKOD        | Clock duty cycle               | 40   | 60  | %     |
| <b>SD-SDR50</b> |                                |      |     |       |
| tSDIS CMD       | Host input setup time for CMD  | 1.5  | –   | ns    |
| tSDIS DAT       | Host input setup time for DAT  | 1.5  | –   | ns    |
| tSDIH CMD       | Host input hold time for CMD   | 2.5  | –   | ns    |
| tSDIH DAT       | Host input hold time for DAT   | 2.5  | –   | ns    |
| tSDOS CMD       | Host output setup time for CMD | 3    | –   | ns    |
| tSDOS DAT       | Host output setup time for DAT | 3    | –   | ns    |
| tSDOH CMD       | Host output hold time for CMD  | 0.8  | –   | ns    |
| tSDOH DAT       | Host output hold time for DAT  | 0.8  | –   | ns    |
| tSCLKR          | Clock rise time                | –    | 2   | ns    |
| tSCLKF          | Clock fall time                | –    | 2   | ns    |
| tSDCK           | Clock cycle time               | 10   | –   | ns    |
| SDFREQ          | Clock frequency                | –    | 100 | MHz   |
| tSDCLKOD        | Clock duty cycle               | 40   | 60  | %     |
| <b>SD-DDR50</b> |                                |      |     |       |
| tSDIS CMD       | Host input setup time for CMD  | 4    | –   | ns    |
| tSDIS DAT       | Host input setup time for DAT  | 0.92 | –   | ns    |
| tSDIH CMD       | Host input hold time for CMD   | 2.5  | –   | ns    |
| tSDIH DAT       | Host input hold time for DAT   | 2.5  | –   | ns    |
| tSDOS CMD       | Host output setup time for CMD | 6    | –   | ns    |
| tSDOS DAT       | Host output setup time for DAT | 3    | –   | ns    |
| tSDOH CMD       | Host output hold time for CMD  | 0.8  | –   | ns    |
| tSDOH DAT       | Host output hold time for DAT  | 0.8  | –   | ns    |
| tSCLKR          | Clock rise time                | –    | 2   | ns    |
| tSCLKF          | Clock fall time                | –    | 2   | ns    |
| tSDCK           | Clock cycle time               | 20   | –   | ns    |
| SDFREQ          | Clock frequency                | –    | 50  | MHz   |
| tSDCLKOD        | Clock duty cycle               | 45   | 55  | %     |

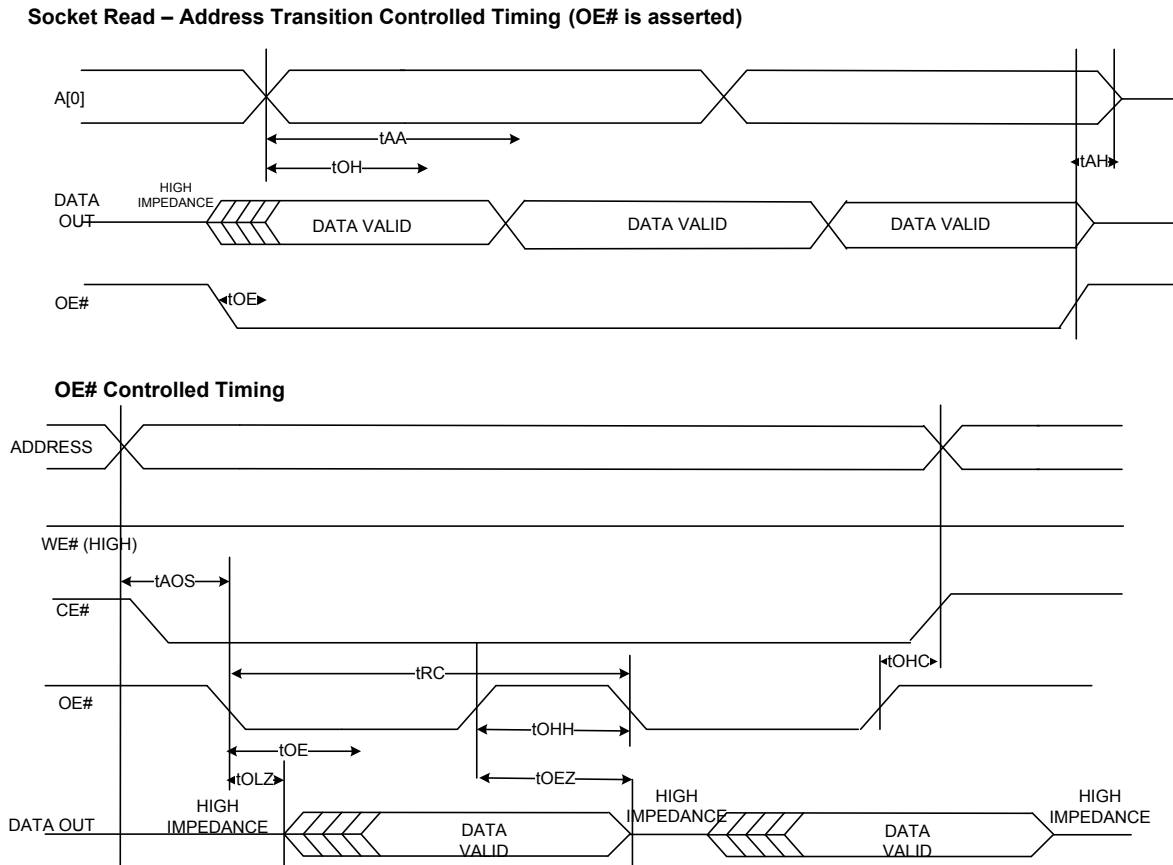
**Note**

5. All parameters guaranteed by design and validated through characterization.

## Host Processor Interface (P-Port) Timing

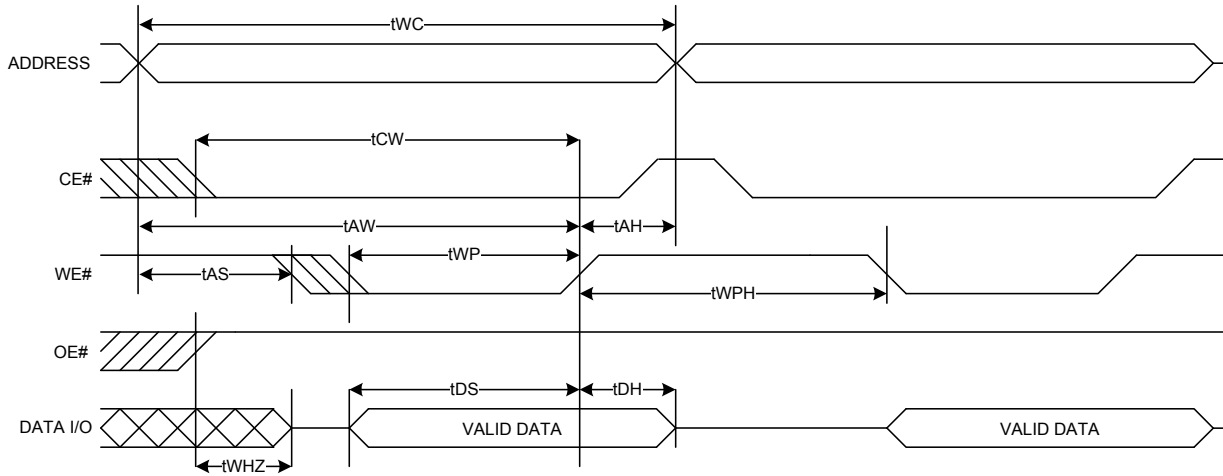
### Asynchronous SRAM Timing

**Figure 11. Non-multiplexed Asynchronous SRAM Read Timing**

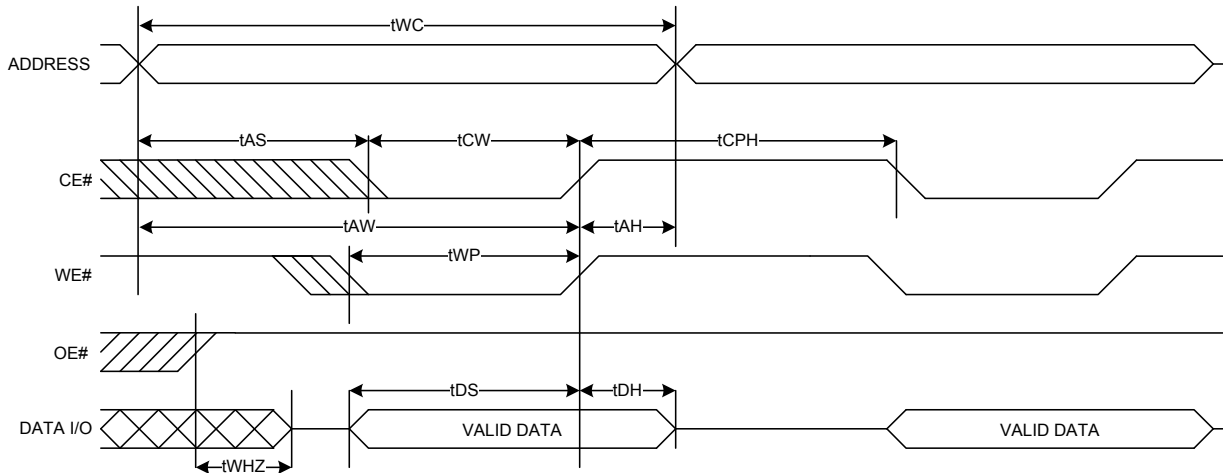


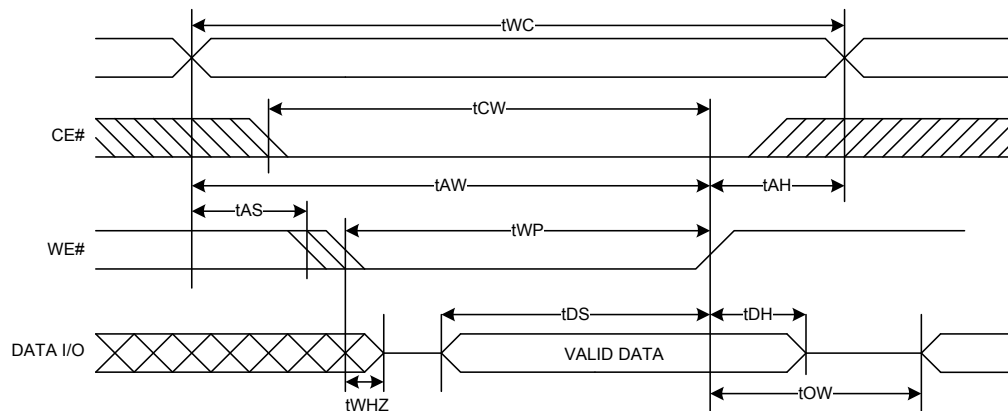
**Figure 12. Non-multiplexed Asynchronous SRAM Write Timing (WE# and CE# controlled)**

**Write Cycle 1 WE# Controlled, OE# High During Write**



**Write Cycle 2 CE# Controlled, OE# High During Write**



**Figure 13. Non-multiplexed Asynchronous SRAM Write Timing (WE# controlled, OE# LOW)**
**Write Cycle 3 WE# Controlled. OE# Low**


**Note:** tWP must be adjusted such that  $tWP > tWHZ + tDS$

**Table 11. Asynchronous SRAM Timing Parameters<sup>[6]</sup>**

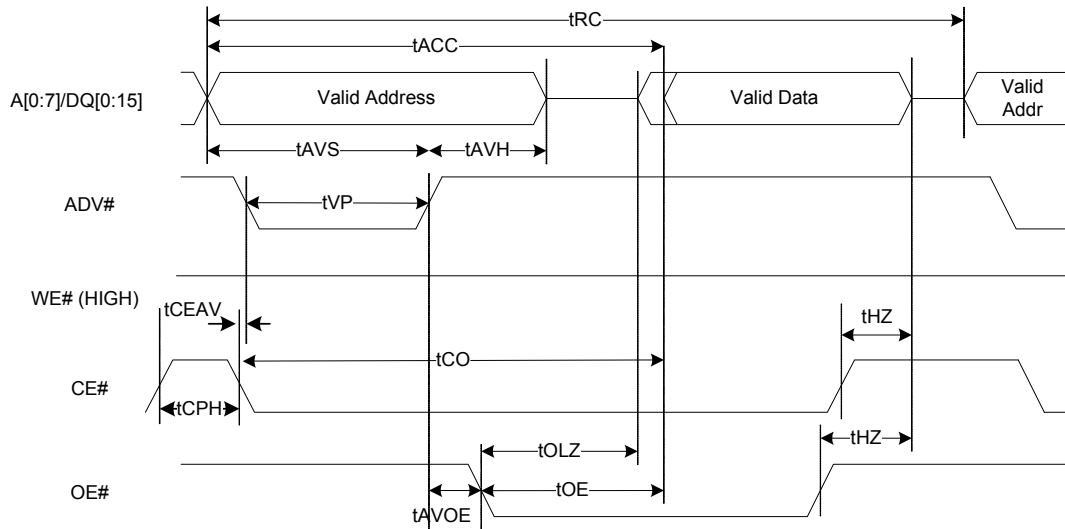
| Parameter | Description                          | Min  | Max  | Units | Notes |
|-----------|--------------------------------------|------|------|-------|-------|
|           | SRAM interface bandwidth             | –    | 61.5 | MBps  |       |
| tRC       | Read cycle time                      | 32.5 | –    | ns    |       |
| tAA       | Address to data valid                | –    | 30   | ns    |       |
| tAOS      | Address to OE# LOW setup time        | 7    | –    | ns    |       |
| tOH       | Data output hold from address change | 3    | –    | ns    |       |
| tOHH      | OE# HIGH hold time                   | 7.5  | –    | ns    |       |
| tOHC      | OE# HIGH to CE# HIGH                 | 2    | –    | ns    |       |
| tOE       | OE# LOW to data valid                | –    | 25   | ns    |       |
| tOLZ      | OE# LOW to LOW-Z                     | 0    | –    | ns    |       |
| tWC       | Write cycle time                     | 30   | –    | ns    |       |
| tCW       | CE# LOW to write end                 | 30   | –    | ns    |       |
| tAW       | Address valid to write end           | 30   | –    | ns    |       |
| tAS       | Address setup to write start         | 7    | –    | ns    |       |
| tAH       | Address hold time from CE# or WE#    | 2    | –    | ns    |       |
| tWP       | WE# pulse width                      | 20   | –    | ns    |       |
| tWPH      | WE# HIGH time                        | 10   | –    | ns    |       |
| tCPH      | CE# HIGH time                        | 10   | –    | ns    |       |
| tDS       | Data setup to write end              | 7    | –    | ns    |       |
| tDH       | Data hold to write end               | 2    | –    | ns    |       |
| tWHZ      | Write to DQ high-Z output            | –    | 22.5 | ns    |       |
| tOEZ      | OE# HIGH to DQ high-Z output         | –    | 22.5 | ns    |       |
| tOW       | End of write to low-Z output         | 0    | –    | ns    |       |

**Note**

6. All parameters guaranteed by design and validated through characterization.

*ADMux Timing for Asynchronous Access*

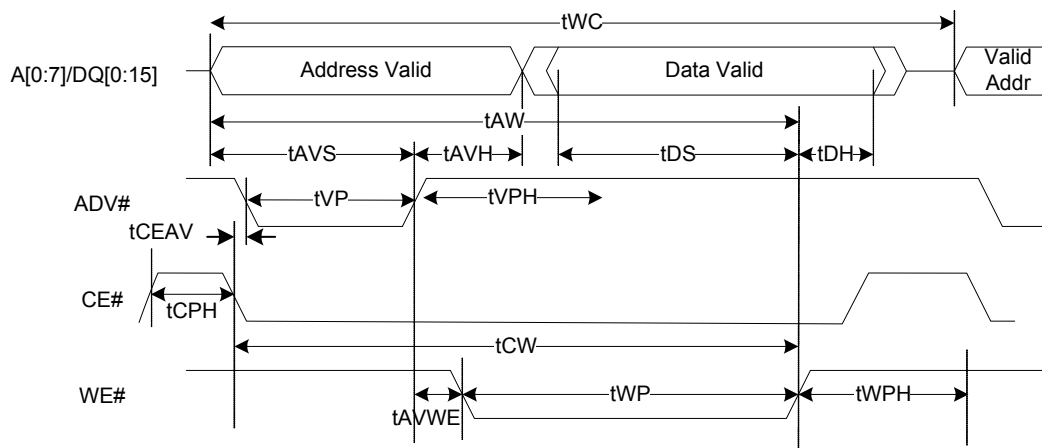
**Figure 14. ADMux Asynchronous Random Read**



**Note:**

1. Multiple read cycles can be executed while keeping CE# low.
2. Read operation ends with either de-assertion of either OE# or CE#, whichever comes earlier.

**Figure 15. ADMux Asynchronous Random Write**



**Note:**

1. Multiple write cycles can be executed while keeping CE# low.
2. Write operation ends with de-assertion of either WE# or CE#, whichever comes earlier.

Table 12. Asynchronous ADMux Timing Parameters<sup>[7]</sup>

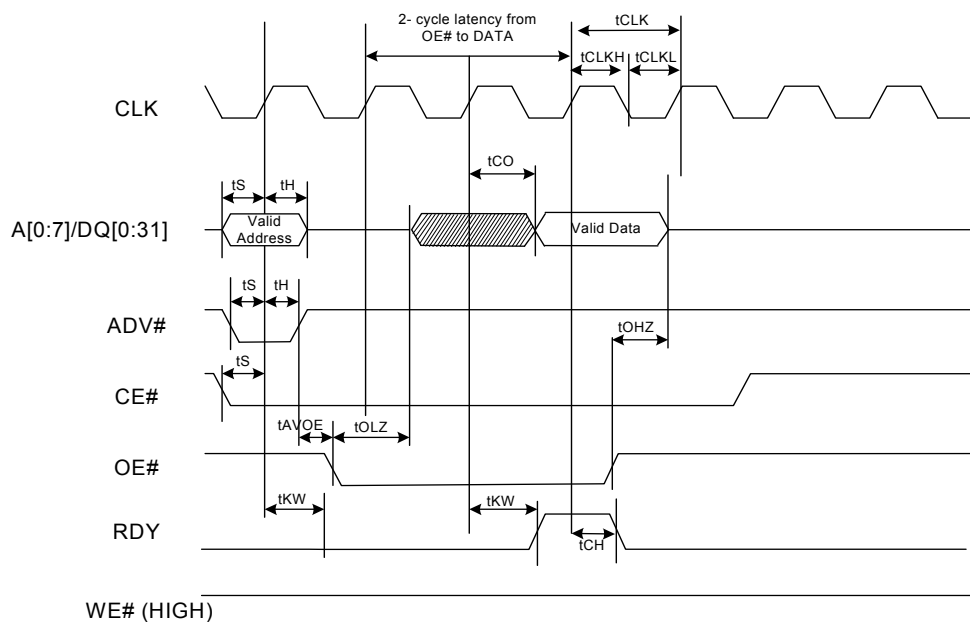
| Parameter                                                            | Description                                       | Min  | Max  | Units | Notes                                                                   |
|----------------------------------------------------------------------|---------------------------------------------------|------|------|-------|-------------------------------------------------------------------------|
| <b>ADMux Asynchronous READ Access Timing Parameters</b>              |                                                   |      |      |       |                                                                         |
| tRC                                                                  | Read cycle time (address valid to address valid)  | 54.5 | –    | ns    | This parameter is dependent on when the P-port processors deasserts OE# |
| tACC                                                                 | Address valid to data valid                       | –    | 32   | ns    |                                                                         |
| tCO                                                                  | CE# assert to data valid                          | –    | 34.5 | ns    |                                                                         |
| tAVOE                                                                | ADV# deassert to OE# assert                       | 2    | –    | ns    |                                                                         |
| tOLZ                                                                 | OE# assert to data LOW-Z                          | 0    | –    | ns    |                                                                         |
| tOE                                                                  | OE# assert to data valid                          | –    | 25   | ns    |                                                                         |
| tHZ                                                                  | Read cycle end to data HIGH-Z                     | –    | 22.5 | ns    |                                                                         |
| <b>ADMux Asynchronous WRITE Access Timing Parameters</b>             |                                                   |      |      |       |                                                                         |
| tWC                                                                  | Write cycle time (address valid to address valid) | –    | 52.5 | ns    |                                                                         |
| tAW                                                                  | Address valid to write end                        | 30   | –    | ns    |                                                                         |
| tCW                                                                  | CE# assert to write end                           | 30   | –    | ns    |                                                                         |
| tAVWE                                                                | ADV# deassert to WE# assert                       | 2    | –    | ns    |                                                                         |
| tWP                                                                  | WE# LOW pulse width                               | 20   | –    | ns    |                                                                         |
| tWPH                                                                 | WE# HIGH pulse width                              | 10   | –    | ns    |                                                                         |
| tDS                                                                  | Data valid setup to WE# deassert                  | 18   | –    | ns    |                                                                         |
| tDH                                                                  | Data valid hold from WE# deassert                 | 2    | –    | ns    |                                                                         |
| <b>ADMux Asynchronous Common READ/WRITE Access Timing Parameters</b> |                                                   |      |      |       |                                                                         |
| tAVS                                                                 | Address valid setup to ADV# deassert              | 5    | –    | ns    |                                                                         |
| tAVH                                                                 | Address valid hold from ADV# deassert             | 2    | –    | ns    |                                                                         |
| tVP                                                                  | ADV# LOW pulse width                              | 7.5  | –    | ns    |                                                                         |
| tCPH                                                                 | CE# HIGH pulse width                              | 10   | –    | ns    |                                                                         |
| tVPH                                                                 | ADV# HIGH pulse width                             | 15   | –    | ns    |                                                                         |
| tCEAV                                                                | CE# assert to ADV# assert                         | 0    | –    | ns    |                                                                         |

**Note**

7. All parameters guaranteed by design and validated through characterization.

## Synchronous ADMux Timing

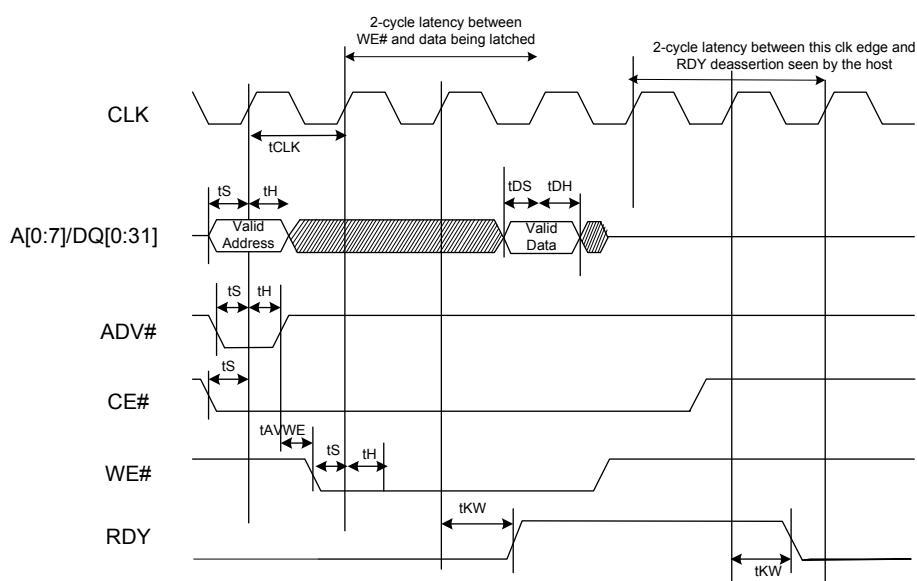
**Figure 16. Synchronous ADMux Interface – Read Cycle Timing**



Note:

- 1) External P-Port processor and West Bridge Benicia operate on the same clock edge
- 2) External processor sees RDY assert 2 cycles after OE # asserts and deasserts a cycle after the data appears on the output
- 3) Valid output data appears 2 cycle after OE # asserted. The data is held until OE # deasserts
- 4) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by bootloader)

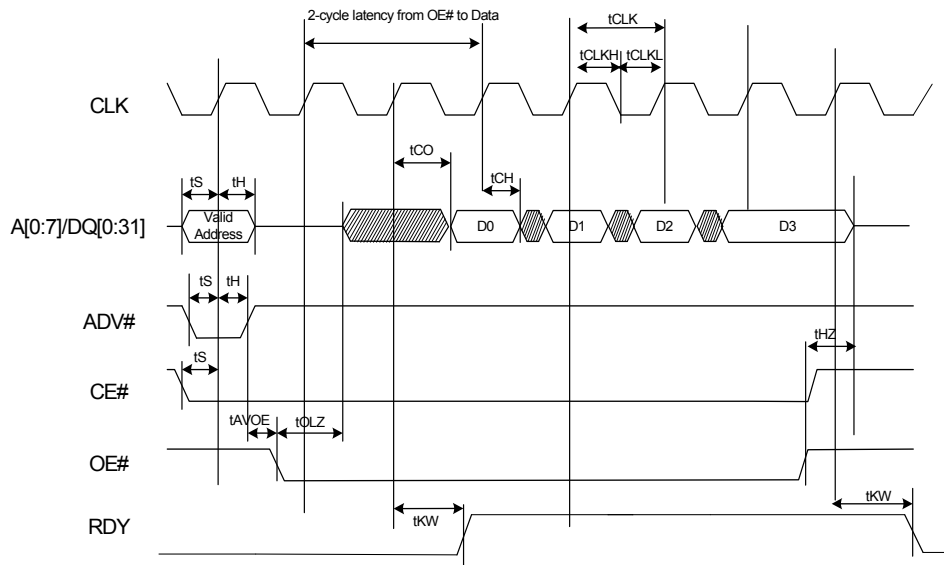
**Figure 17. Synchronous ADMux Interface – Write Cycle Timing**



Note:

- 1) External P-Port processor and West Bridge Benicia operate on the same clock edge
- 2) External processor sees RDY assert 2 cycles after WE # asserts and deasserts 3 cycles after the edge sampling the data.
- 3) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle at operations less than 50 MHz (this 1 cycle latency is not supported by bootloader)

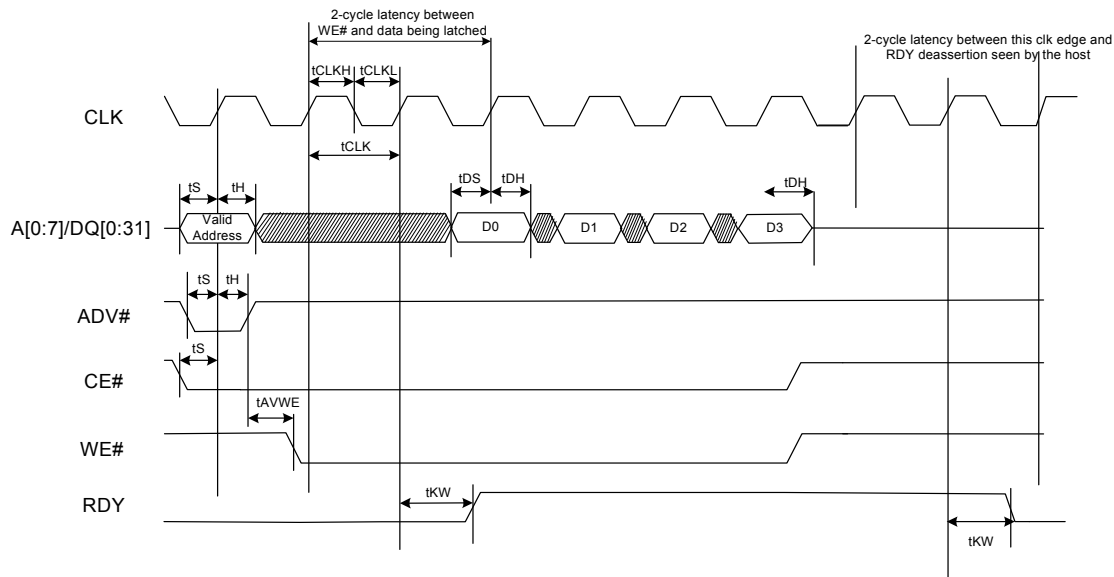
**Figure 18. Sync ADMux Interface - Burst Read Timing**



Note:

- 1) External P-Port processor and West Bridge Benicia work operate on the same clock edge
- 2) External processor sees RDY assert 2 cycles after OE # asserts and deasserts a cycle after the last burst data appears on the output
- 3) Valid output data appears 2 cycle after OE # asserts. The last burst data is held until OE # deasserts
- 4) Burst size of 4 is shown. Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst.
- 5) External processor cannot deassert OE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
- 6) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle at operations less than 50 MHz (this 1 cycle latency is not supported by bootloader)

**Figure 19. Sync ADMux Interface - Burst Write Timing**



Note:

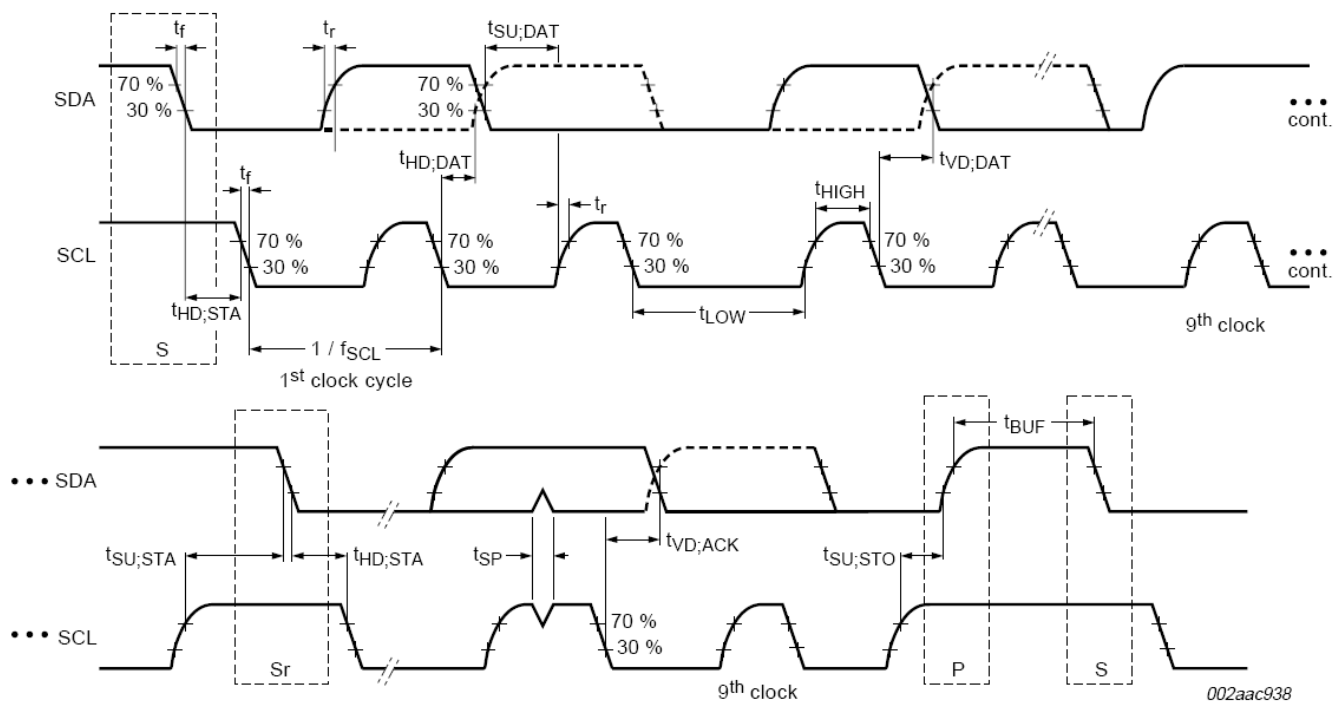
- 1) External P-Port processor and West Bridge Benicia operate on the same clock edge
- 2) External processor sees RDY assert 2 cycles after WE # asserts and deasserts 3 cycles after the edge sampling the last burst data.
- 3) Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst. Burst size of 4 is shown
- 4) External processor cannot deassert WE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
- 5) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle at operations less than 50 MHz (this 1 cycle latency is not supported by bootloader)

**Table 13. Synchronous ADMux Timing Parameters<sup>[8]</sup>**

| Parameter | Description                    | Min | Max | Unit |
|-----------|--------------------------------|-----|-----|------|
| FREQ      | Interface clock frequency      | –   | 100 | MHz  |
| tCLK      | Clock period                   | 10  | –   | ns   |
| tCLKH     | Clock HIGH time                | 4   | –   | ns   |
| tCLKL     | Clock LOW time                 | 4   | –   | ns   |
| tS        | CE#/WE#/DQ setup time          | 2   | –   | ns   |
| tH        | CE#/WE#/DQ hold time           | 0.5 | –   | ns   |
| tCH       | Clock to data output hold time | 0   | –   | ns   |
| tDS       | Data input setup time          | 2   | –   | ns   |
| tDH       | Clock to data input hold       | 0.5 | –   | ns   |
| tAVDOE    | ADV# HIGH to OE# LOW           | 0   | –   | ns   |
| tAVDWE    | ADV# HIGH to WE# LOW           | 0   | –   | ns   |
| tHZ       | CE# HIGH to Data HIGH-Z        | –   | 8   | ns   |
| tOHZ      | OE# HIGH to Data HIGH-Z        | –   | 8   | ns   |
| tOLZ      | OE# LOW to Data LOW-Z          | 0   | –   | ns   |
| tKW       | Clock to RDY valid             | –   | 8   | ns   |

### Low Performance Peripherals Timing

#### I<sup>2</sup>C Timing

**Figure 20. I<sup>2</sup>C Timing Definition**

**Note**

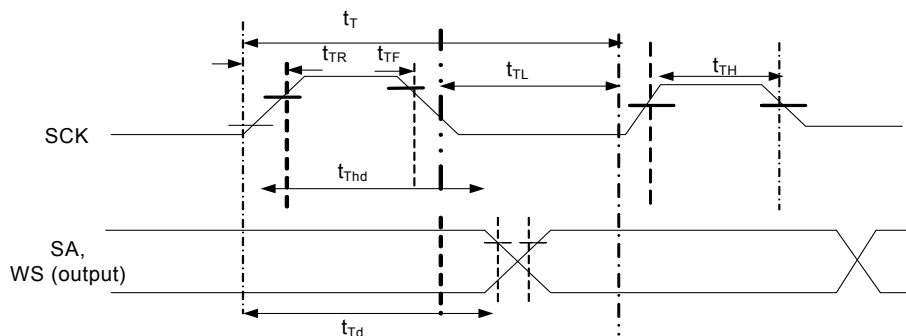
8. All parameters guaranteed by design and validated through characterization.

**Table 14. I<sup>2</sup>C Timing Parameters** <sup>[9]</sup>

| Parameter                                                                          | Description                                                   | Min  | Max  | Units | Notes |
|------------------------------------------------------------------------------------|---------------------------------------------------------------|------|------|-------|-------|
| <b>I<sup>2</sup>C Standard Mode Parameters</b>                                     |                                                               |      |      |       |       |
| fSCL                                                                               | SCL clock frequency                                           | 0    | 100  | kHz   |       |
| tHD:STA                                                                            | Hold time START condition                                     | 4    | –    | μs    |       |
| tLOW                                                                               | LOW period of the SCL                                         | 4.7  | –    | μs    |       |
| tHIGH                                                                              | HIGH period of the SCL                                        | 4    | –    | μs    |       |
| tSU:STA                                                                            | Setup time for a repeated START condition                     | 4.7  | –    | μs    |       |
| tHD:DAT                                                                            | Data hold time                                                | 0    | –    | μs    |       |
| tSU:DAT                                                                            | Data setup time                                               | 250  | –    | ns    |       |
| tr                                                                                 | Rise time of both SDA and SCL signals                         | –    | 1000 | ns    |       |
| tf                                                                                 | Fall time of both SDA and SCL signals                         | –    | 300  | ns    |       |
| tSU:STO                                                                            | Setup time for STOP condition                                 | 4    | –    | μs    |       |
| tBUF                                                                               | Bus free time between a STOP and START condition              | 4.7  | –    | μs    |       |
| tVD:DAT                                                                            | Data valid time                                               | –    | 3.45 | μs    |       |
| tVD:ACK                                                                            | Data valid ACK                                                | –    | 3.45 | μs    |       |
| tSP                                                                                | Pulse width of spikes that must be suppressed by input filter | –    | –    |       |       |
| <b>I<sup>2</sup>C Fast Mode Parameters</b>                                         |                                                               |      |      |       |       |
| fSCL                                                                               | SCL clock frequency                                           | 0    | 400  | kHz   |       |
| tHD:STA                                                                            | Hold time START condition                                     | 0.6  | –    | μs    |       |
| tLOW                                                                               | LOW period of the SCL                                         | 1.3  | –    | μs    |       |
| tHIGH                                                                              | HIGH period of the SCL                                        | 0.6  | –    | μs    |       |
| tSU:STA                                                                            | Setup time for a repeated START condition                     | 0.6  | –    | μs    |       |
| tHD:DAT                                                                            | Data hold time                                                | 0    | –    | μs    |       |
| tSU:DAT                                                                            | Data setup time                                               | 100  | –    | ns    |       |
| tr                                                                                 | Rise time of both SDA and SCL signals                         | –    | 300  | ns    |       |
| tf                                                                                 | Fall time of both SDA and SCL signals                         | –    | 300  | ns    |       |
| tSU:STO                                                                            | Setup time for STOP condition                                 | 0.6  | –    | μs    |       |
| tBUF                                                                               | Bus free time between a STOP and START condition              | 1.3  | –    | μs    |       |
| tVD:DAT                                                                            | Data valid time                                               | –    | 0.9  | μs    |       |
| tVD:ACK                                                                            | Data valid ACK                                                | –    | 0.9  | μs    |       |
| tSP                                                                                | Pulse width of spikes that must be suppressed by input filter | 0    | 50   | ns    |       |
| <b>I<sup>2</sup>C Fast Mode Plus Parameters (Not supported at I2CVDDQ = 1.2 V)</b> |                                                               |      |      |       |       |
| fSCL                                                                               | SCL clock frequency                                           | 0    | 1000 | kHz   |       |
| tHD:STA                                                                            | Hold time START condition                                     | 0.26 | –    | μs    |       |
| tLOW                                                                               | LOW period of the SCL                                         | 0.5  | –    | μs    |       |
| tHIGH                                                                              | HIGH period of the SCL                                        | 0.26 | –    | μs    |       |
| tSU:STA                                                                            | Setup time for a repeated START condition                     | 0.26 | –    | μs    |       |
| tHD:DAT                                                                            | Data hold time                                                | 0    | –    | μs    |       |
| tSU:DAT                                                                            | Data setup time                                               | 50   | –    | ns    |       |
| tr                                                                                 | Rise time of both SDA and SCL signals                         | –    | 120  | ns    |       |
| tf                                                                                 | Fall time of both SDA and SCL signals                         | –    | 120  | ns    |       |
| tSU:STO                                                                            | Setup time for STOP condition                                 | 0.26 | –    | μs    |       |
| tBUF                                                                               | Bus free time between a STOP and START condition              | 0.5  | –    | μs    |       |
| tVD:DAT                                                                            | Data valid time                                               | –    | 0.45 | μs    |       |
| tVD:ACK                                                                            | Data valid ACK                                                | –    | 0.55 | μs    |       |
| tSP                                                                                | Pulse width of spikes that must be suppressed by input filter | 0    | 50   | ns    |       |

**Note**

9. All parameters guaranteed by design and validated through characterization.

*I<sup>2</sup>S Timing Diagram*
**Figure 21. I<sup>2</sup>S Transmit Cycle**

**Table 15. I<sup>2</sup>S Timing Parameters<sup>[10]</sup>**

| Parameter | Description                                    | Min           | Max           | Units |
|-----------|------------------------------------------------|---------------|---------------|-------|
| $t_T$     | I <sup>2</sup> S transmitter clock cycle       | $T_{tr}$      | —             | ns    |
| $t_{TL}$  | I <sup>2</sup> S transmitter cycle LOW period  | $0.35 T_{tr}$ | —             | ns    |
| $t_{TH}$  | I <sup>2</sup> S transmitter cycle HIGH period | $0.35 T_{tr}$ | —             | ns    |
| $t_{TR}$  | I <sup>2</sup> S transmitter rise time         | —             | $0.15 T_{tr}$ | ns    |
| $t_{TF}$  | I <sup>2</sup> S transmitter fall time         | —             | $0.15 T_{tr}$ | ns    |
| $t_{Thd}$ | I <sup>2</sup> S transmitter data hold time    | 0             | —             | ns    |
| $t_{Td}$  | I <sup>2</sup> S transmitter delay time        | —             | $0.8 t_T$     | ns    |

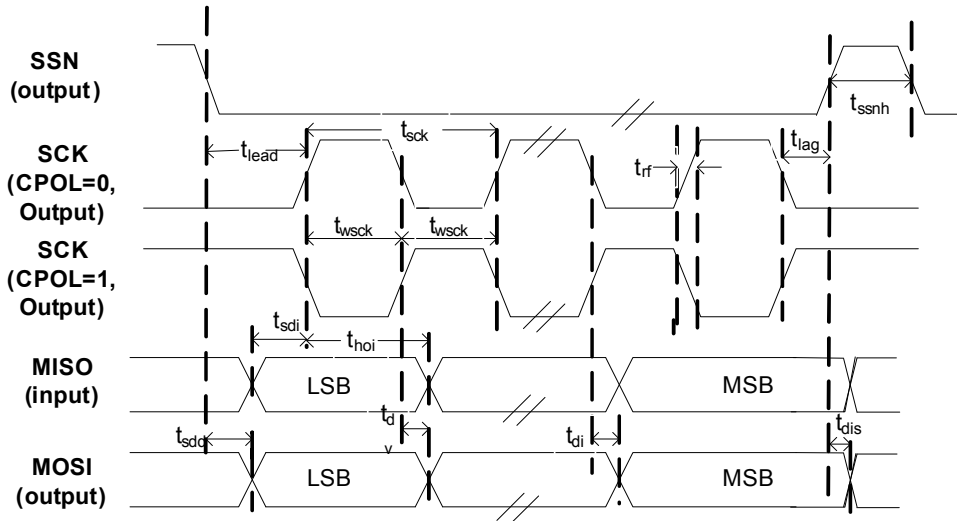
**Note**  $t_T$  is selectable through clock gears. Max  $T_{tr}$  is designed for 96-kHz codec at 32 bits to be 326 ns (3.072 MHz).

**Note**

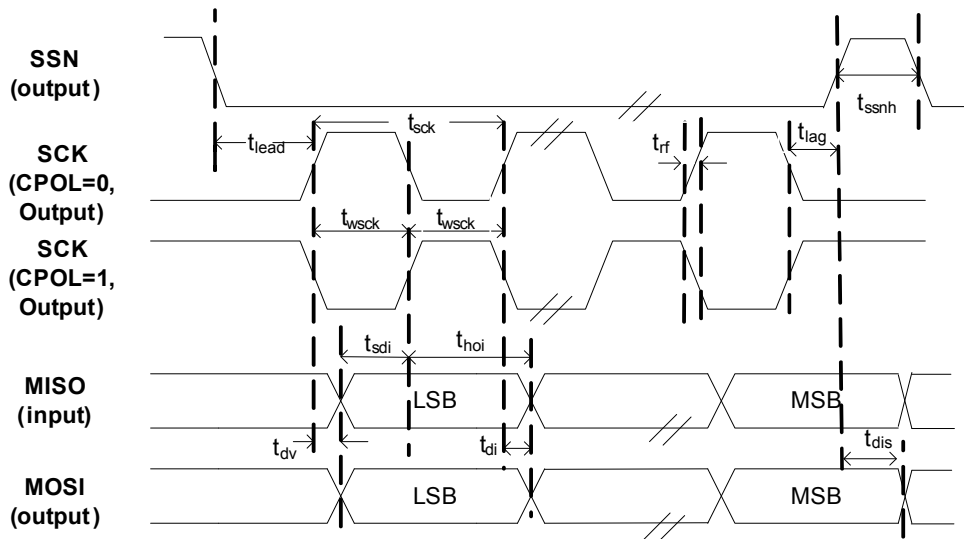
10. All parameters guaranteed by design and validated through characterization.

## SPI Timing Specification

**Figure 22. SPI Timing**



**SPI Master Timing for CPHA = 0**



**SPI Master Timing for CPHA = 1**

**Table 16. SPI Timing Parameters<sup>[11]</sup>**

| Parameter | Description                         | Min                           | Max                           | Units |
|-----------|-------------------------------------|-------------------------------|-------------------------------|-------|
| fop       | Operating frequency                 | 0                             | 33                            | MHz   |
| tsck      | Cycle time                          | 30                            | –                             | ns    |
| twscck    | Clock HIGH/LOW time                 | 13.5                          | –                             | ns    |
| tlead     | SSN-SCK lead time                   | $1/2 \text{ tsck}^{[12]} - 5$ | $1.5 \text{ tsck}^{[12]} + 5$ | ns    |
| tlag      | Enable lag time                     | 0.5                           | $1.5 \text{ tsck}^{[12]} + 5$ | ns    |
| trf       | Rise/fall time                      | –                             | 8                             | ns    |
| tsdd      | Output SSN to valid data delay time | –                             | 5                             | ns    |
| tdv       | Output data valid time              | –                             | 5                             | ns    |
| tdi       | Output data invalid                 | 0                             | –                             | ns    |
| tssnh     | Minimum SSN HIGH time               | 10                            | –                             | ns    |
| tsdi      | Data setup time input               | 8                             | –                             | ns    |
| thoi      | Data hold time input                | 0                             | –                             | ns    |
| tdis      | Disable data output on SSN HIGH     | 0                             | –                             | ns    |

## Reset Sequence

The hard reset sequence requirements for West Bridge Bay are specified in the following table.

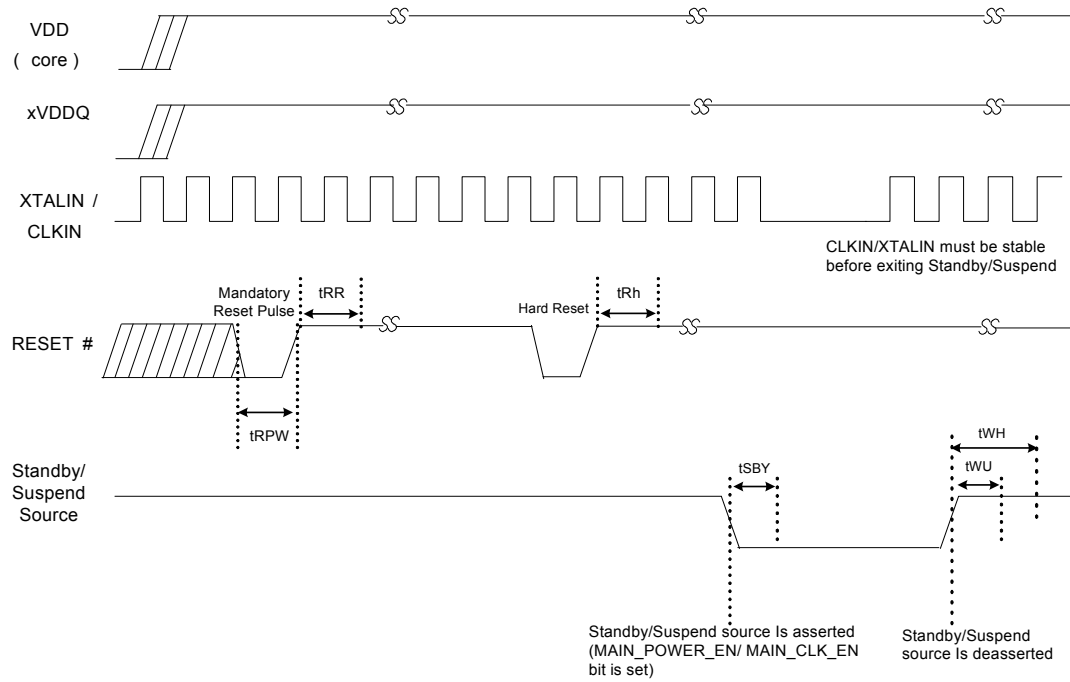
**Table 17. Reset and Standby Timing Parameters**

| Parameter | Description                                                                           | Conditions    | Min | Max | Units |
|-----------|---------------------------------------------------------------------------------------|---------------|-----|-----|-------|
| tRPW      | Minimum RESET# pulse width                                                            | Clock input   | 1   | –   | ms    |
|           |                                                                                       | Crystal input | 1   | –   | ms    |
| tRH       | Minimum HIGH on RESET#                                                                |               | 5   | –   | ms    |
| tRR       | Reset recovery time (after which boot loader begins firmware download)                | Clock input   | 1   | –   | ms    |
|           |                                                                                       | Crystal input | 5   |     | ms    |
| tSBY      | Time to enter standby/suspend (from the time MAIN_CLOCK_EN/ MAIN_POWER_EN bit is set) |               | –   | 1   | ms    |
| tWU       | Time to wakeup from standby                                                           | Clock input   | 1   | –   | ms    |
|           |                                                                                       | Crystal input | 5   | –   | ms    |
| tWH       | Minimum time before standby/suspend source is reasserted                              |               | 5   | –   | ms    |

### Notes

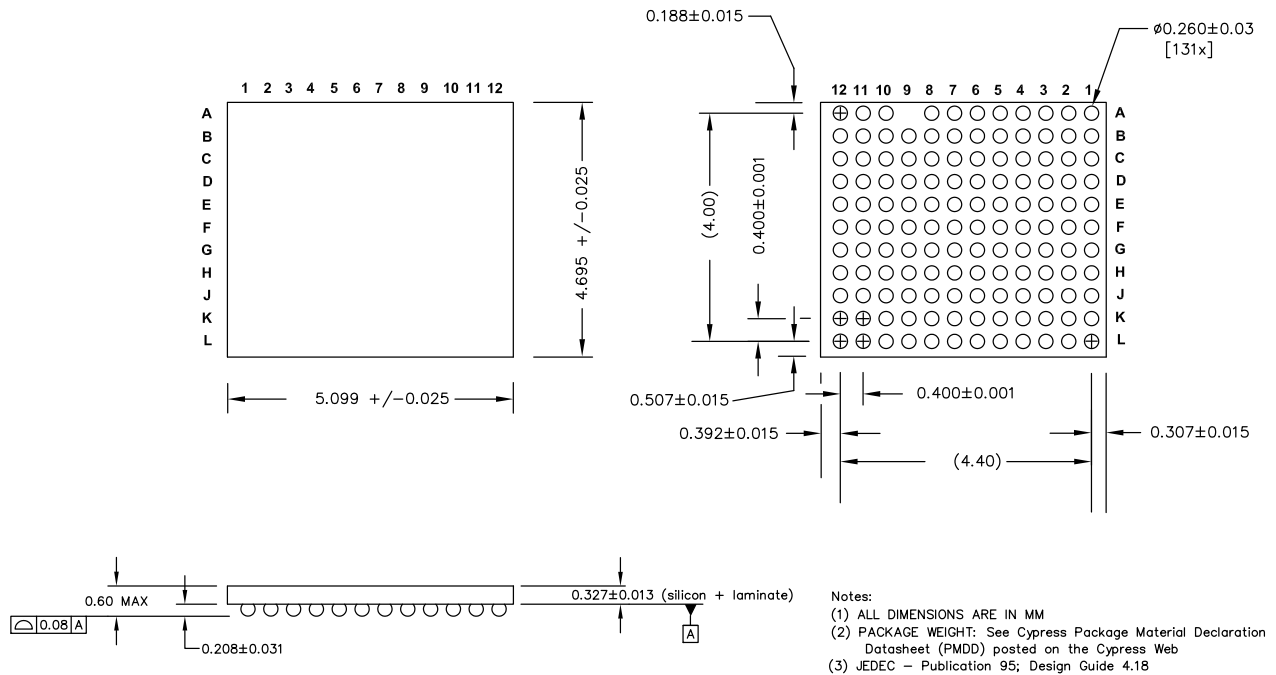
11. All parameters guaranteed by design and validated through characterization.  
12. Depends on LAG and LEAD setting in SPI\_CONFIG register.

**Figure 23. Reset Sequence**



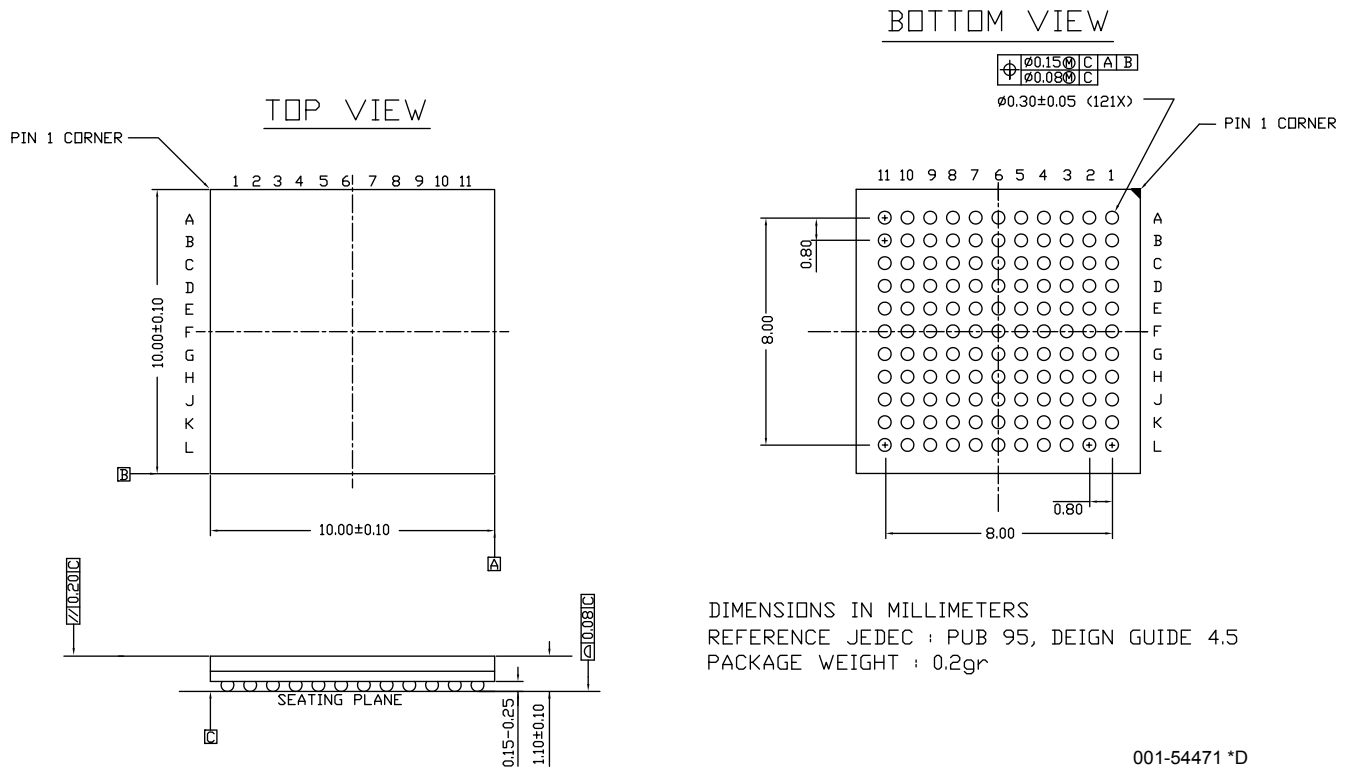
## Package Diagram

**Figure 24. 131-ball Benicia WLCSP (5.099 × 4.695 × 0.60 mm) Package Outline, 001-62221**



001-62221 \*C

**Figure 25. 121-Ball FBGA 10 × 10 × 1.2 Diagram**



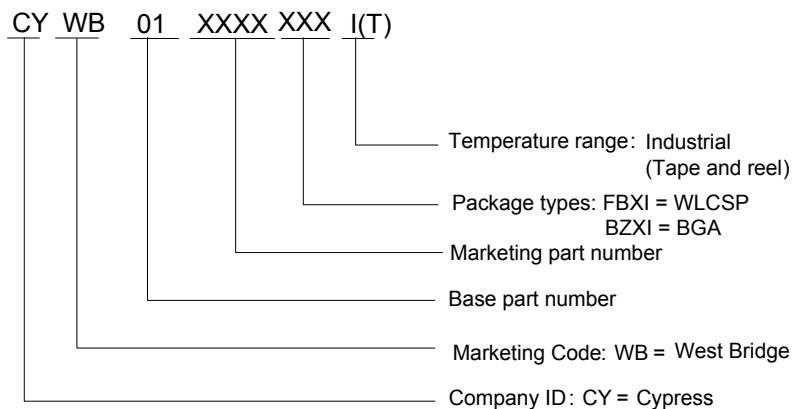
**Note** Underfill is required on the board design. Contact Cypress Applications for details.

## Ordering Information

Table 18. Ordering Information

| Ordering Code    | Package Type   | USB2.0 Integrated Switch |
|------------------|----------------|--------------------------|
| CYWB0163BB-FBXIT | 131-ball WLCSP | Yes                      |
| CYWB0164BB-BZXI  | 121-ball BGA   | No                       |

## Ordering Code Definitions



## Acronyms

| Acronym | Description                    |
|---------|--------------------------------|
| ACA     | Accessory Charger Adaptor      |
| ADP     | Attach Detection Protocol      |
| DMA     | Direct Memory Access           |
| HID     | Human Interface Device         |
| HNP     | Host Negotiation Protocol      |
| MMC     | Multimedia Card                |
| MSC     | Mass Storage Class             |
| MTP     | Media Transfer Protocol        |
| OTG     | On-The-Go                      |
| OVP     | Overvoltage Protection         |
| PLL     | Phase Locked Loop              |
| SCL     | Serial Clock                   |
| SD      | Secure Digital                 |
| SDA     | Serial Data                    |
| SDIO    | Secure Digital Input / Output  |
| SLC     | Single-Level Cell              |
| SPI     | Serial Peripheral Interface    |
| SRP     | Session Request Protocol       |
| USB     | Universal Serial Bus           |
| WP      | Write Protection               |
| WLCSP   | Wafer Level Chip Scale Package |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure      |
|--------|----------------------|
| °C     | degree Celsius       |
| μA     | microampere          |
| μs     | microsecond          |
| KHz    | kilohertz            |
| mA     | milliampere          |
| Mbps   | megabits per second  |
| MBps   | megabytes per second |
| MHz    | megahertz            |
| ms     | millisecond          |
| ns     | nanosecond           |
| Ω      | ohm                  |
| pF     | picofarad            |
| V      | volt                 |

## Errata

This section describes the errata for West Bridge Bay and Benicia, CYWB0163BB-FBXI and CYWB0263BB-FBXI. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

### Part Numbers Affected

| Part Number     |
|-----------------|
| CYWB0163BB-FBXI |
| CYWB0263BB-FBXI |

### Bay and Benicia, USB and Mass Storage Peripheral Controller Qualification Status

Product Status: Sampling

### Bay and Benicia, USB and Mass Storage Peripheral Controller Errata Summary

This table defines the errata applicable to Bay and Benicia, USB and Mass Storage Peripheral Controller family devices.

**Note:** Errata items in the table below are hyperlinked. Click on any item entry to jump to its description.

| Items                                     | Part Number                        | Silicon Revision | Fix Status                                               |
|-------------------------------------------|------------------------------------|------------------|----------------------------------------------------------|
| 1. <a href="#">USB Boot Is Not Stable</a> | CYWB0163BB-FBXI<br>CYWB0263BB-FBXI | ES               | 1. Workaround provided.<br>2. Fix in Production Silicon. |
| 2. <a href="#">P-Port Clock Stop</a>      | CYWB0163BB-FBXI<br>CYWB0263BB-FBXI | ES               | 1. Workaround provided.                                  |

#### 1. USB Boot Is Not Stable

##### ■ Problem Definition

Bay and Benicia may not enumerate with the USB host (for example: PC) and fail to boot from the USB port if after reset the PMODE pins are selected or configured to boot from USB.

##### ■ Parameters Affected

NA

##### ■ Trigger Condition(S)

This condition is triggered when PMODE pins is configured to boot from the USB port.

##### ■ Scope of Impact

Fail to boot from USB Port.

##### ■ Workaround

Select alternate boot option like I2C and P-Port etc. boot

##### ■ Fix Status

Fix in production silicon

## 2. P-Port Clock Stop

### ■ Problem Definition

Bay and Benicia require a free running clock on the P-Port in synchronous mode. In cases where free running clocks are not available P-Port DMA transfers will not work.

### ■ Parameters Affected

NA

### ■ Trigger Condition(S)

This condition is triggered when P-Port is configured to synchronous interface (for example synchronous ADMux interface).

### ■ Scope of Impact

In cases where free running clocks are not available P-Port DMA transfers will not work.

### ■ Workaround

Provide a free running clock or provide at least 150 clock edges before the clock stops.

### ■ Fix Status

No fix. Workaround is required.

## Document History Page

| Document Title: CYWB0163BB/CYWB0164BB, West Bridge® Bay™ USB and Mass Storage Controller<br>Document Number: 001-45550 |         |                 |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------------------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Revision                                                                                                               | ECN     | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| **                                                                                                                     | 2669072 | VSO / PYRS      | 03/05/09        | New data sheet                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| *A                                                                                                                     | 2754304 | VSO             | 08/21/09        | Updated the part number (in title).<br>The whole Features section has been updated.<br>The whole Applications section has been updated.<br>Updated the block diagram.<br>The Functional Overview section has been updated.<br>The Processor Interface section and sub-sections have been updated.<br>Added Boot Options section. Added a section of Power.<br>Added a section of Pin Description.<br>Added Table 1. Pin List.                                                                                                                                                                                          |
| *B                                                                                                                     | 2823531 | OSG             | 12/08/09        | Added data sheet to the USB 3.0 EROS spec 001-51884. No technical updates.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| *C                                                                                                                     | 3080927 | OSG             | 11/08/2010      | Changed status from Advance to Preliminary<br>Changed part number from CYWB0101BB to CYWB0163BB<br>Added the following sections: <a href="#">Power</a> , <a href="#">Configuration Options</a> , <a href="#">Digital I/Os</a> , <a href="#">EMI</a> , <a href="#">System-level ESD</a> , <a href="#">Absolute Maximum Ratings</a> , <a href="#">AC Timing Parameters</a> , <a href="#">Reset Sequence</a><br>Added <a href="#">DC Specifications</a> table<br>Updated Pin List<br>Updated block diagram                                                                                                                |
| *D                                                                                                                     | 3204393 | OSG             | 03/24/2011      | Changed Async SRAM tOE parameter<br>Changed Async SRAM tRC parameter<br>Changed Async ADMux tOE parameter<br>Changed Async ADMux tRC parameter<br>Changed Async ADMux tACC parameter<br>Changed Async ADMux tCO parameter<br>Changed Async SRAM max interface throughput<br>Updated dimensions of WLCSP package<br>Updated Pin List<br>Added description for Clock Stop Enable feature for Sync ADMux interface.                                                                                                                                                                                                       |
| *E                                                                                                                     | 3217917 | OSG             | 04/06/2011      | Changed value of R_USB2<br>Updated Async SRAM A0 Controlled Read timing diagram<br>Removed Sync ADMux Clock Stop support<br>Updated Sync ADMux interconnect diagram.                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| *F                                                                                                                     | 3369042 | OSG             | 12/06/2011      | Updated tRR and tRPW for crystal input<br>Removed tWZ parameter from Sync ADMux timing<br>Updated SPI timing diagram<br>Updated I2S Timing diagram and tTd parameter<br>Added Note in the Package Diagram section.<br>Corrected ADV# pin mapping in the Pin List<br>Updated Absolute Maximum Ratings<br>In Power Modes description, stated that PVDDQ cannot be turned off at any time if the P-port is used in the application.<br>Added clarification regarding VCC in DC Specifications table<br>Updated I2C interface tVD:ACK parameter for 1 MHz operation<br>Changed datasheet status from Preliminary to Final. |
| *G                                                                                                                     | 3649782 | OSG             | 08/16/2012      | Added note about the I <sup>2</sup> C controller support for clock stretching.<br>Updated Clocking and Hard Reset sections.<br>Modified V <sub>BUS</sub> min value.<br>Updated Rise/fall time max value.                                                                                                                                                                                                                                                                                                                                                                                                               |

**Document History Page** (continued)

| Document Title: CYWB0163BB/CYWB0164BB, West Bridge® Bay™ USB and Mass Storage Controller<br>Document Number: 001-45550 |         |                 |                 |                                                                                                                                                                     |
|------------------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Revision                                                                                                               | ECN     | Orig. of Change | Submission Date | Description of Change                                                                                                                                               |
| *H                                                                                                                     | 3848148 | OSG             | 12/20/2012      | Added BGA Pin List and package diagram.<br>Added BGA ball map.<br>Updated ordering information and ordering code diagram.                                           |
| *I                                                                                                                     | 4016006 | OSG             | 05/31/2013      | No content update.                                                                                                                                                  |
| *J                                                                                                                     | 4354719 | DBIR            | 04/21/2014      | Updated <a href="#">Package Diagram</a> :<br>spec 001-62221 – Changed revision from *B to *C.<br><br>Added <a href="#">Errata</a> .<br><br>Updated in new template. |

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