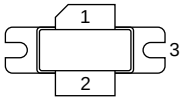
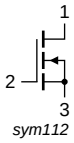
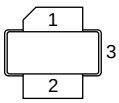
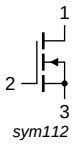
1.3 Applications

- L-band power amplifiers for radar applications in the 1.2 GHz to 1.4 GHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLL6H1214L-250 (SOT502A)				
1	drain			
2	gate			
3	source	[1]		
BLL6H1214LS-250 (SOT502B)				
1	drain			
2	gate			
3	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLL6H1214L-250	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLL6H1214LS-250	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	100	V
V_{GS}	gate-source voltage		−0.5	+13	V
I_D	drain current		-	42	A
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		-	200	°C

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5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_{case} = 85 °C; P_L = 250 W		
		t_p = 100 μs; δ = 10 %	0.10	K/W
		t_p = 200 μs; δ = 10 %	0.13	K/W
		t_p = 300 μs; δ = 10 %	0.15	K/W
		t_p = 100 μs; δ = 20 %	0.14	K/W
		t_p = 500 μs; δ = 20 %	0.20	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.7 mA	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 270 mA	1.3	1.8	2.25	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	32	42	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 270 mA	1.6	2.3	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 9.5 A	-	100	169	mΩ

Table 7. RF characteristics

Mode of operation: pulsed RF; t_p = 300 μs; δ = 10 %; RF performance at V_{DS} = 50 V; I_{Dq} = 100 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_L	output power		250	-	-	W
V_{DS}	drain-source voltage	P_L = 250 W	-	-	50	V
G_p	power gain	P_L = 250 W	15	17	-	dB
t_p	pulse duration	P_L = 250 W	-	300	500	μs
δ	duty cycle	P_L = 250 W	-	10	20	%
RL_{in}	input return loss	P_L = 250 W	-	10	-	dB
$P_{L(1dB)}$	output power at 1 dB gain compression		-	300	-	W
η_D	drain efficiency	P_L = 250 W	49	55	-	%
$P_{droop(pulse)}$	pulse droop power	P_L = 250 W	-	0	0.3	dB
t_r	rise time	P_L = 250 W	-	15	-	ns
t_f	fall time	P_L = 250 W	-	5	-	ns

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6.1 Ruggedness in class-AB operation

The BLL6H1214L-250 and BLL6H1214LS-250 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 100 mA; P_L = 250 W; t_p = 300 μs; δ = 10 %.

7. Application information

7.1 Impedance information

Table 8. Typical impedance

Typical values unless otherwise specified.

f	Z_S	Z_L
GHz	Ω	Ω
1.2	1.268 – j2.623	2.987 – j1.664
1.3	2.193 – j2.457	2.162 – j1.326
1.4	2.359 – j2.052	1.604 – j1.887

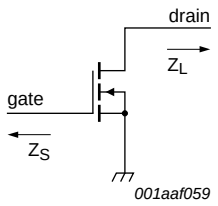

Fig 1. Definition of transistor impedance

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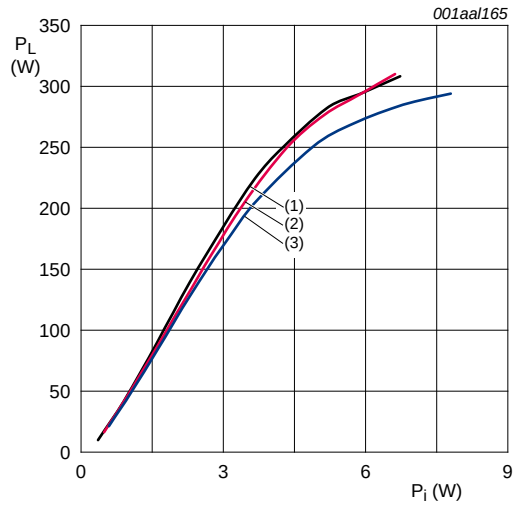
7.2 RF performance



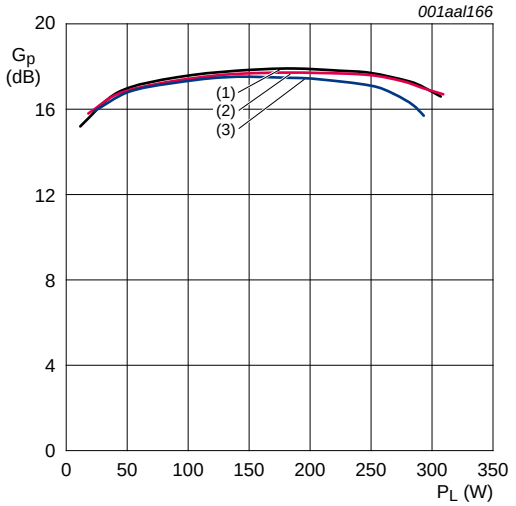
V_{DS} = 50 V; t_p = 300 μs; δ = 10 %; I_{Dq} = 100 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 2. Output power as a function of input power; typical values



V_{DS} = 50 V; t_p = 300 μs; δ = 10 %; I_{Dq} = 100 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 3. Power gain as a function of load power; typical values

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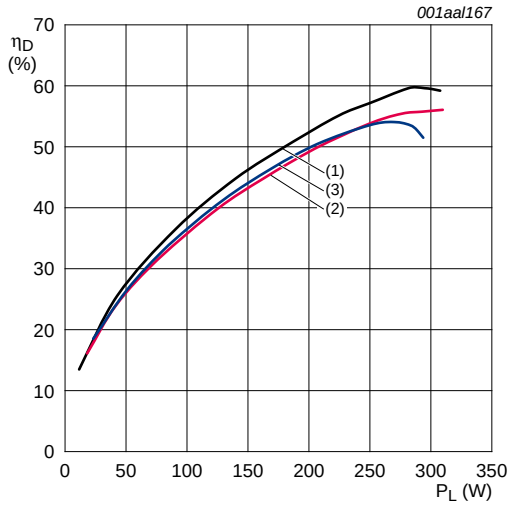


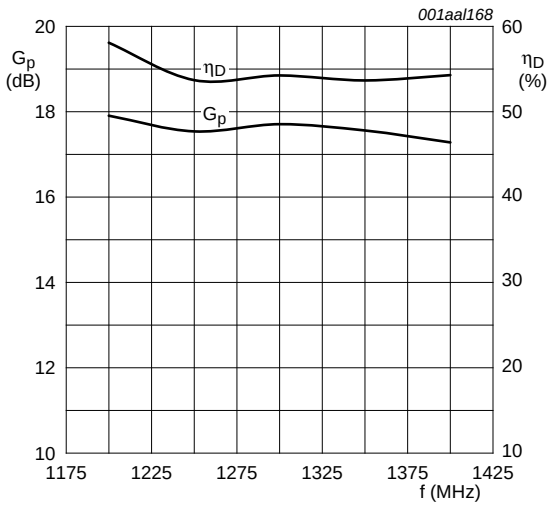
V_{DS} = 50 V; t_p = 300 μs; δ = 10 %; I_{Dq} = 100 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

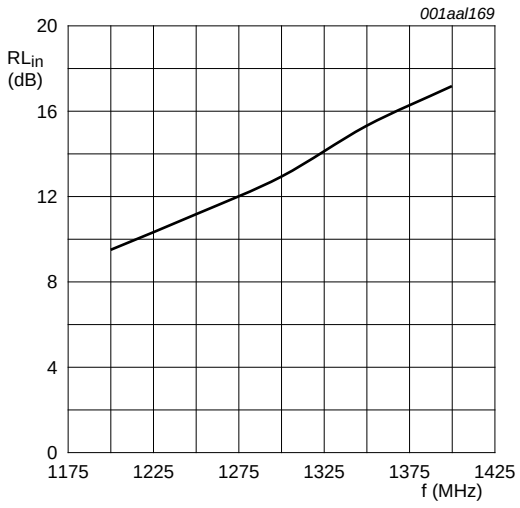
(3) f = 1400 MHz

Fig 4. Drain efficiency as a function of load power; typical values



P_L = 250 W; V_{DS} = 50 V; t_p = 300 μs; δ = 10 %; I_{Dq} = 100 mA.

Fig 5. Power gain and drain efficiency as function of frequency; typical values



P_L = 250 W; V_{DS} = 50 V; t_p = 300 μs; δ = 10 %; I_{Dq} = 100 mA.

Fig 6. Input return loss as a function of frequency; typical value

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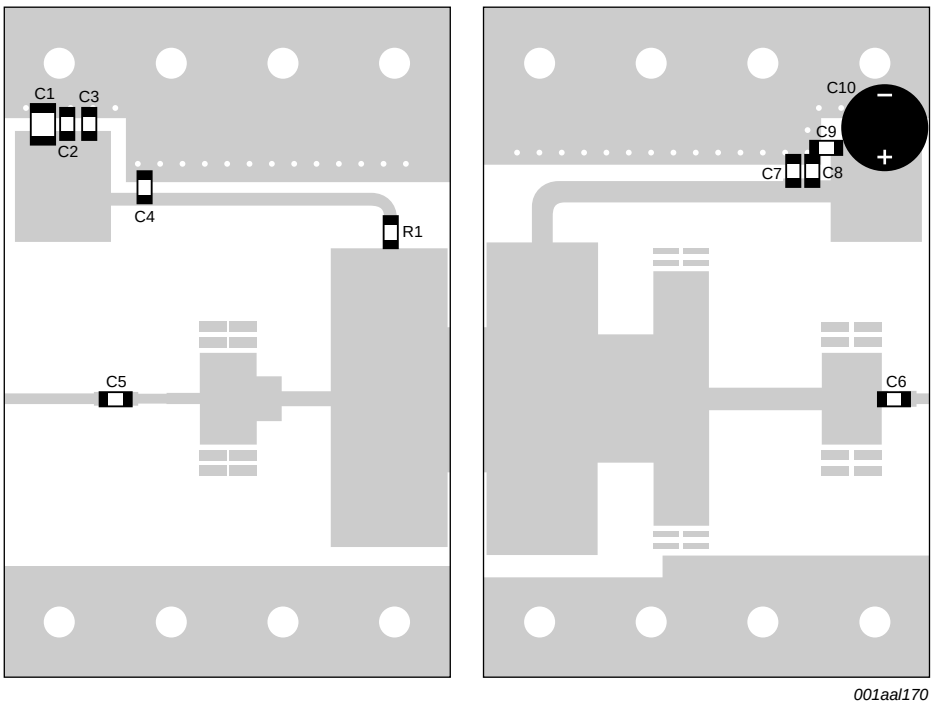
7.3 Application circuit



See Table 9 for list of components.

Fig 7. Component layout for class-AB application circuit

Table 9. List of components

See Figure 7.

Striplines are on a Rodgers Duroid 6006 Printed-Circuit Board (PCB); ε_r = 6.15 F/m; thickness = 0.64 mm

Component	Description	Value		Remarks
C1	multilayer ceramic chip capacitor	10 μF; 35 V	[1]	
C2, C4	multilayer ceramic chip capacitor	51 pF	[2]	
C3, C8	multilayer ceramic chip capacitor	1 nF	[2]	
C5	multilayer ceramic chip capacitor	82 pF	[3]	
C6, C7	multilayer ceramic chip capacitor	56 pF	[3]	
C9	multilayer ceramic chip capacitor	100 pF	[3]	
C10	electrolytic capacitor	47 μF; 63 V		
R1	SMD resistor	10 Ω		0603

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

[3] American Technical Ceramics type 800B or capacitor of same quality.

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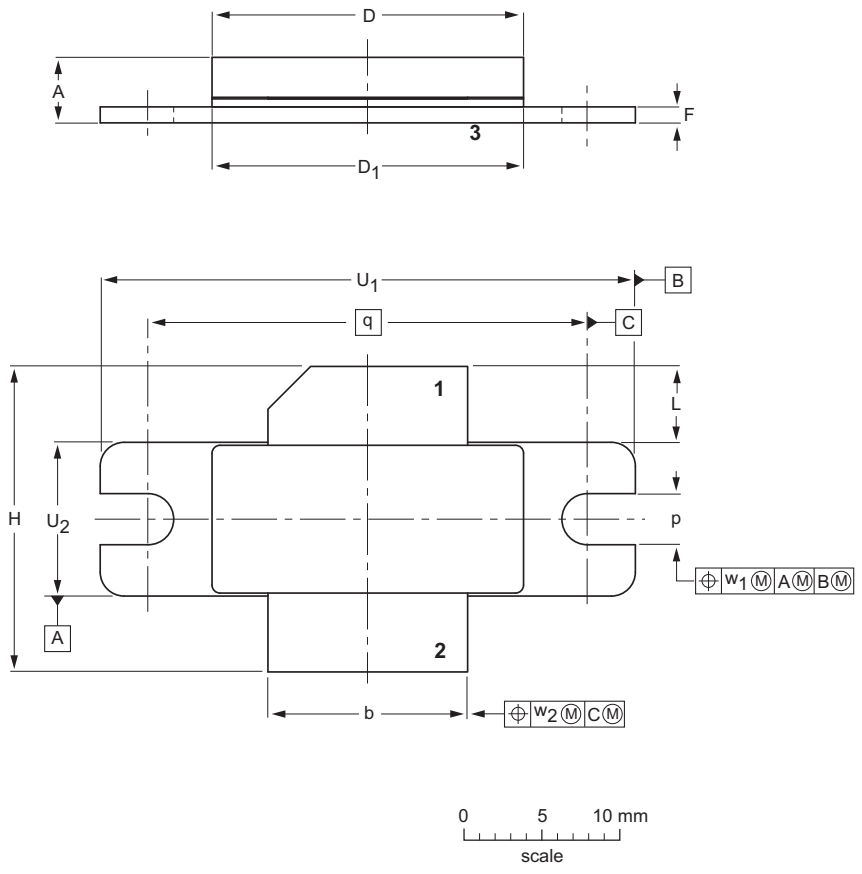
8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT502A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~03-01-10~~ 12-05-02

Fig 8. Package outline SOT502A

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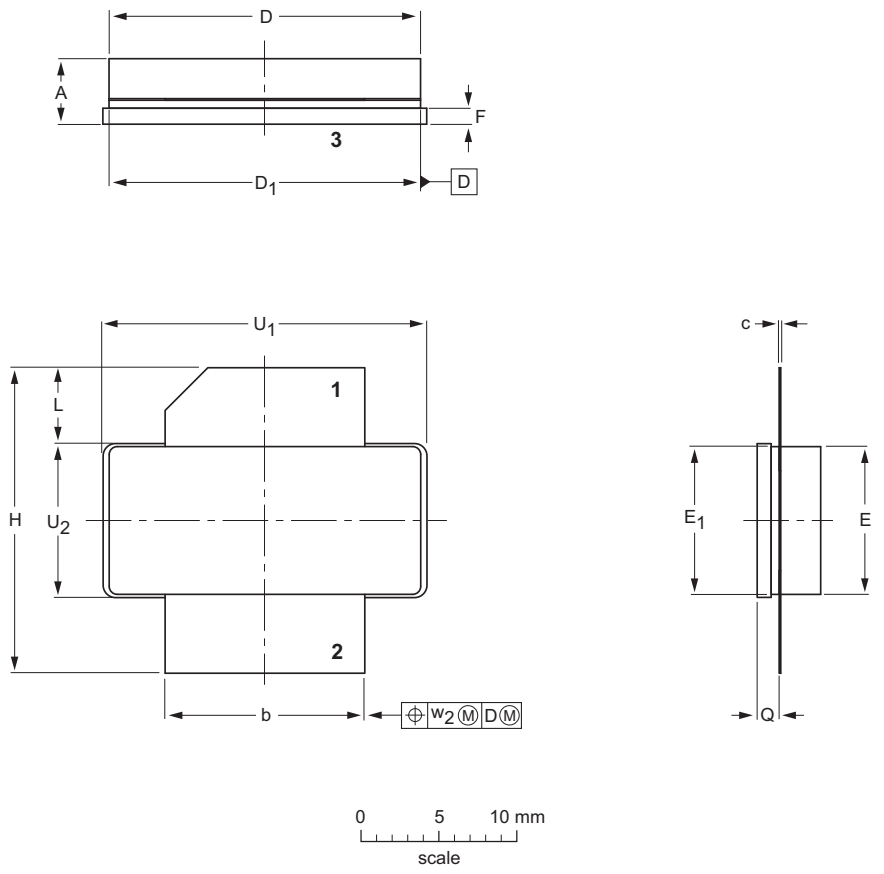
Earless flanged ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~07-05-09~~ 12-05-02

Fig 9. Package outline SOT502B

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9. Abbreviations

Table 10. Abbreviations

Acronym	Description
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

10. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLL6H1214L-250_1214LS-250#4	20150901	Product data sheet		BLL6H1214L-250_1214LS-250#3
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLL6H1214L-250_1214LS-250#3	20100714	Product data sheet	-	BLL6H1214L-250_1214LS-250#2
BLL6H1214L-250_1214LS-250#2	20100302	Objective data sheet	-	BLL6H1214L-250_1214LS-250#1
BLL6H1214L-250_1214LS-250#1	20091211	Objective data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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