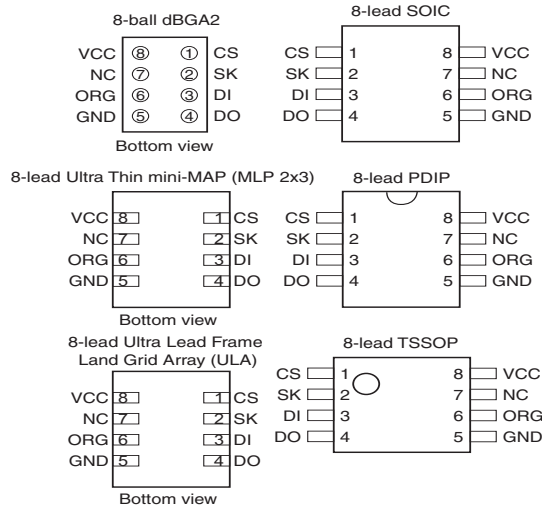


Table 2-1. Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
VCC	Power Supply
ORG	Internal Organization
NC	No Connect

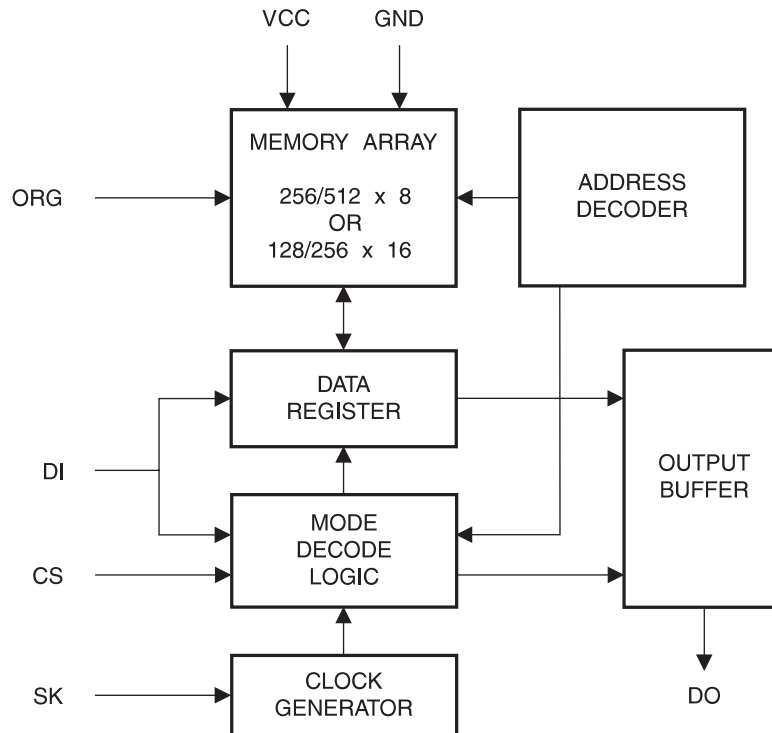


3. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current.....	5.0 mA

***NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Figure 3-1. Block Diagram



Note: When the ORG pin is connected to VCC, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1 Meg ohm pullup, then the x 16 organization is selected.

Table 3-1. Pin Capacitance^(Note:)

 Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$, $V_{CC} = +5.0\text{V}$ (unless otherwise noted)

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	$V_{OUT} = 0\text{V}$
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

Table 3-2. DC Characteristics

 Applicable over recommended operating range from: $T_{AI} = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$ (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.7		5.5	V
V_{CC3}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current	$V_{CC} = 5.0\text{V}$	READ at 1.0 MHz	0.5	2.0	mA
			WRITE at 1.0 MHz	0.5	2.0	mA
I_{SB1}	Standby Current	$V_{CC} = 1.8\text{V}$	CS = 0V	0.4	1.0	μA
I_{SB2}	Standby Current	$V_{CC} = 2.7\text{V}$	CS = 0V	6.0	10.0	μA
I_{SB3}	Standby Current	$V_{CC} = 5.0\text{V}$	CS = 0V	10.0	15.0	μA
I_{IL}	Input Leakage	$V_{IN} = 0\text{V}$ to V_{CC}		0.1	3.0	μA
I_{OL}	Output Leakage	$V_{IN} = 0\text{V}$ to V_{CC}		0.1	3.0	μA
V_{IL1} ^(Note:) V_{IH1} ^(Note:)	Input Low Voltage Input High Voltage	$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$		-0.6 2.0	0.8 $V_{CC} + 1$	V
V_{IL2} ^(Note:) V_{IH2} ^(Note:)	Input Low Voltage Input High Voltage	$1.8\text{V} \leq V_{CC} \leq 2.7\text{V}$		-0.6 $V_{CC} \times 0.7$	$V_{CC} \times 0.3$ $V_{CC} + 1$	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	$I_{OL} = 2.1\text{ mA}$		0.4	V
			$I_{OH} = -0.4\text{ mA}$	2.4		V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	$1.8\text{V} \leq V_{CC} \leq 2.7\text{V}$	$I_{OL} = 0.15\text{ mA}$		0.2	V
			$I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$		V

 Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 3-3. AC Characteristics

Applicable over recommended operating range from $T_{AI} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = \text{As Specified}$,
 $CL = 1$ TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	$4.5V \leq V_{CC} \leq 5.5V$ $2.7V \leq V_{CC} \leq 5.5V$ $1.8V \leq V_{CC} \leq 5.5V$	0 0 0		2 1 0.25	MHz
t_{SKH}	SK High Time	$2.7V \leq V_{CC} \leq 5.5V$ $1.8V \leq V_{CC} \leq 5.5V$	250 1000			ns
t_{SKL}	SK Low Time	$2.7V \leq V_{CC} \leq 5.5V$ $1.8V \leq V_{CC} \leq 5.5V$	250 1000			ns
t_{CS}	Minimum CS Low Time	$2.7V \leq V_{CC} \leq 5.5V$ $1.8V \leq V_{CC} \leq 5.5V$	250 1000			ns
t_{CSS}	CS Setup Time	Relative to SK $2.7V \leq V_{CC} \leq 5.5V$ $1.8V \leq V_{CC} \leq 5.5V$	50 200			ns
t_{DIS}	DI Setup Time	Relative to SK $2.7V \leq V_{CC} \leq 5.5V$ $1.8V \leq V_{CC} \leq 5.5V$	100 400			ns
t_{CSH}	CS Hold Time	Relative to SK	0			ns
t_{DIH}	DI Hold Time	Relative to SK $2.7V \leq V_{CC} \leq 5.5V$ $1.8V \leq V_{CC} \leq 5.5V$	100 400			ns
t_{PD1}	Output Delay to "1"	AC Test $2.7V \leq V_{CC} \leq 5.5V$ $1.8V \leq V_{CC} \leq 5.5V$			250 1000	ns
t_{PD0}	Output Delay to "0"	AC Test $2.7V \leq V_{CC} \leq 5.5V$ $1.8V \leq V_{CC} \leq 5.5V$			250 1000	ns
t_{SV}	CS to Status Valid	AC Test $2.7V \leq V_{CC} \leq 5.5V$ $1.8V \leq V_{CC} \leq 5.5V$			250 1000	ns
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL} $2.7V \leq V_{CC} \leq 5.5V$ $1.8V \leq V_{CC} \leq 5.5V$			150 400	ns
t_{WP}	Write Cycle Time	$1.8V \leq V_{CC} \leq 5.5V$	0.1	3	10	ms
Endurance ^(Note:)	5.0V, 25°C		1M			Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

Table 3-4. Instruction Set for the AT93C56A and AT93C66A

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	$A_8 - A_0$	$A_7 - A_0$			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXXXX	11XXXXXXX			Write enable must precede all programming modes.
ERASE	1	11	$A_8 - A_0$	$A_7 - A_0$			Erases memory location $A_n - A_0$.
WRITE	1	01	$A_8 - A_0$	$A_7 - A_0$	$D_7 - D_0$	$D_{15} - D_0$	Writes memory location $A_n - A_0$.
ERAL	1	00	10XXXXXXXX	10XXXXXXX			Erases all memory locations. Valid only at $V_{CC} = 4.5V$ to $5.5V$.
WRAL	1	00	01XXXXXXXX	01XXXXXXX	$D_7 - D_0$	$D_{15} - D_0$	Writes all memory locations. Valid only at $V_{CC} = 5.0V \pm 10\%$ and Disable Register cleared.
EWDS	1	00	00XXXXXXXX	00XXXXXXX			Disables all programming instructions.

Note: The X's in the address field represent don't care values and must be clocked.

4. Functional Description

The AT93C56A/66A is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. **A valid instruction starts with a rising edge of CS** and consists of a Start Bit (logic “1”) followed by the appropriate Op Code and the desired memory address location.

READ (READ): The Read (READ) instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic “0”) precedes the 8- or 16-bit data output string. The AT93C56A/66A supports sequential read operations. The device will automatically increment the internal address pointer and clock out the next memory location as long as Chip Select (CS) is held high. In this case, the dummy bit (logic “0”) will not be clocked out between memory locations, thus allowing for a continuous stream of data to be read.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or V_{CC} power is removed from the part.

ERASE (ERASE): The Erase instruction programs all bits in the specified memory location to the logical “1” state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic “1” at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle t_{WP} starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic “0” at DO indicates that programming is still in progress. A logic “1” indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. **A READY/BUSY status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle t_{WP} .**

ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic “1” state and is primarily used for testing purposes. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at $V_{CC} = 5.0V \pm 10\%$.

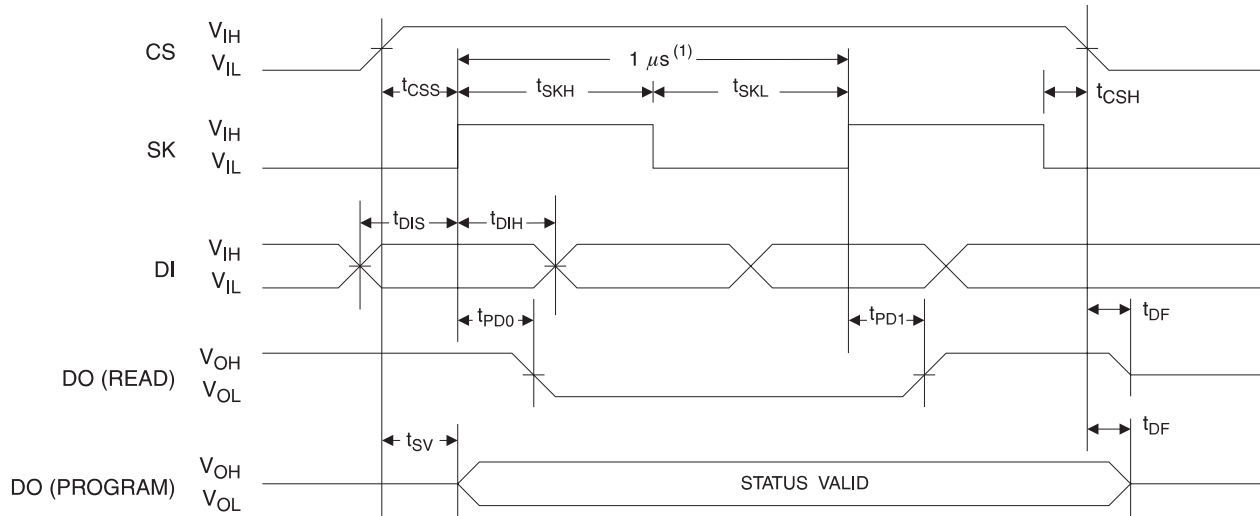
WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at $V_{CC} = 5.0V \pm 10\%$.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.



5. Timing Diagrams

Figure 5-1. Synchronous Data Timing



Note: 1. This is the minimum SK period.

Table 5-1. Organization Key for Timing Diagrams

I/O	AT93C56A (2K)		AT93C66A (4K)	
	x 8	x 16	x 8	x 16
A_N	$A_8^{(1)}$	$A_7^{(2)}$	A_8	A_7
D_N	D_7	D_{15}	D_7	D_{15}

Notes: 1. A_8 is a DON'T CARE value, but the extra clock is required.
 2. A_7 is a DON'T CARE value, but the extra clock is required.

Figure 5-2. READ Timing

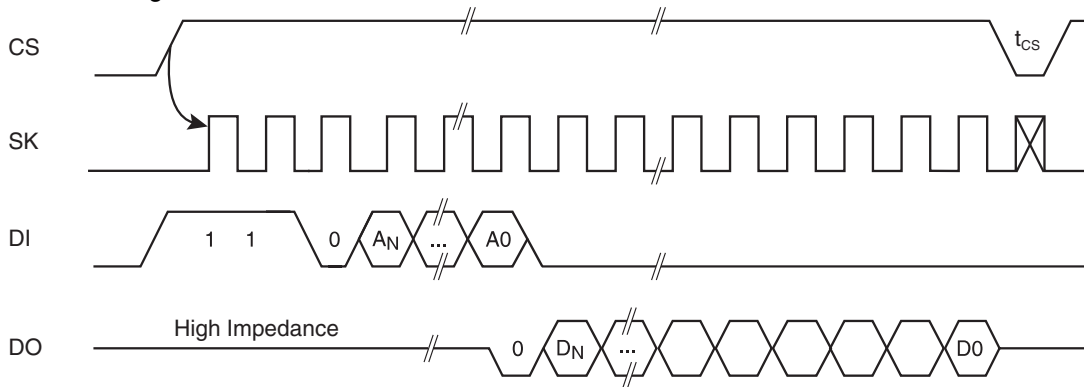


Figure 5-3. EWEN Timing

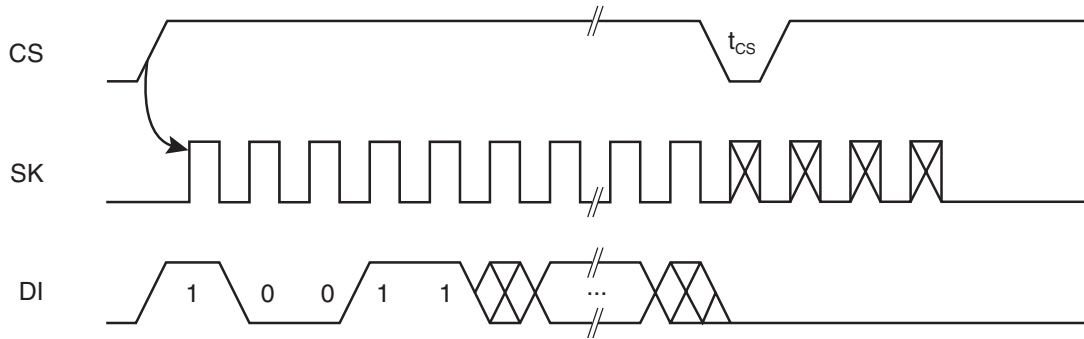


Figure 5-4. EWDS Timing

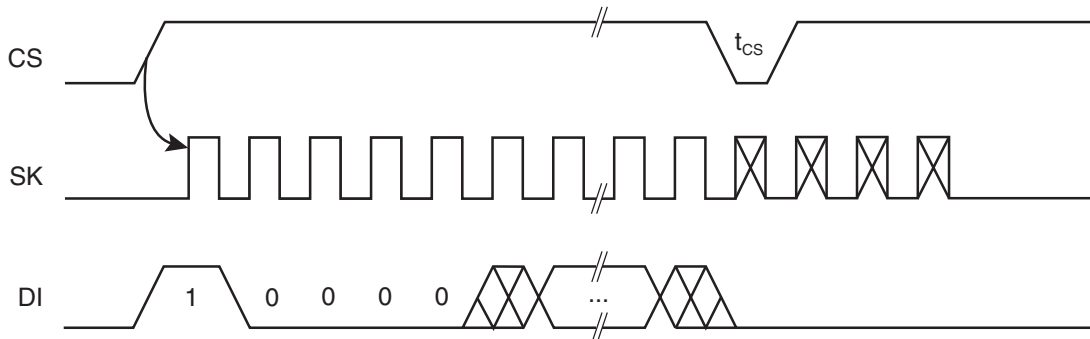


Figure 5-5. WRITE Timing

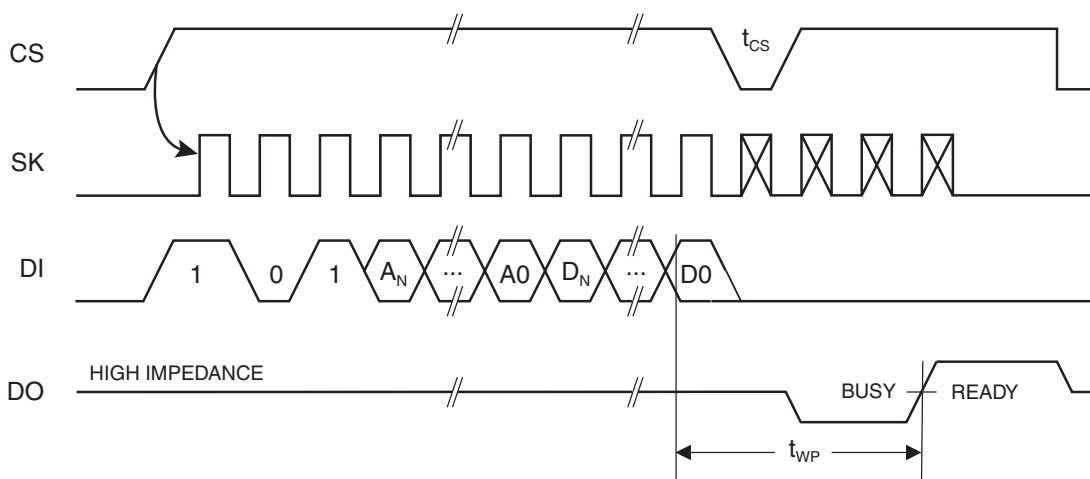
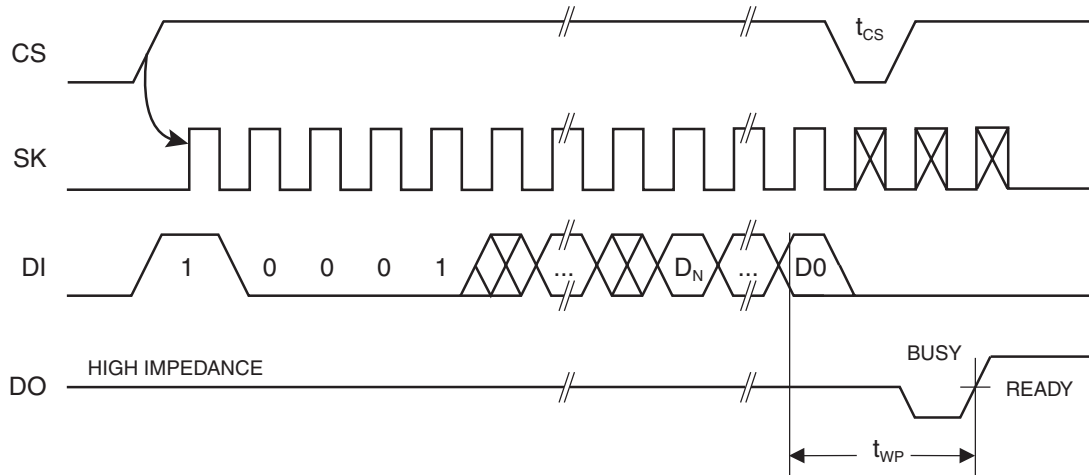


Figure 5-6. WRAL Timing⁽¹⁾



Note: 1. Valid only at $V_{CC} = 4.5V$ to $5.5V$.

Figure 5-7. ERASE Timing

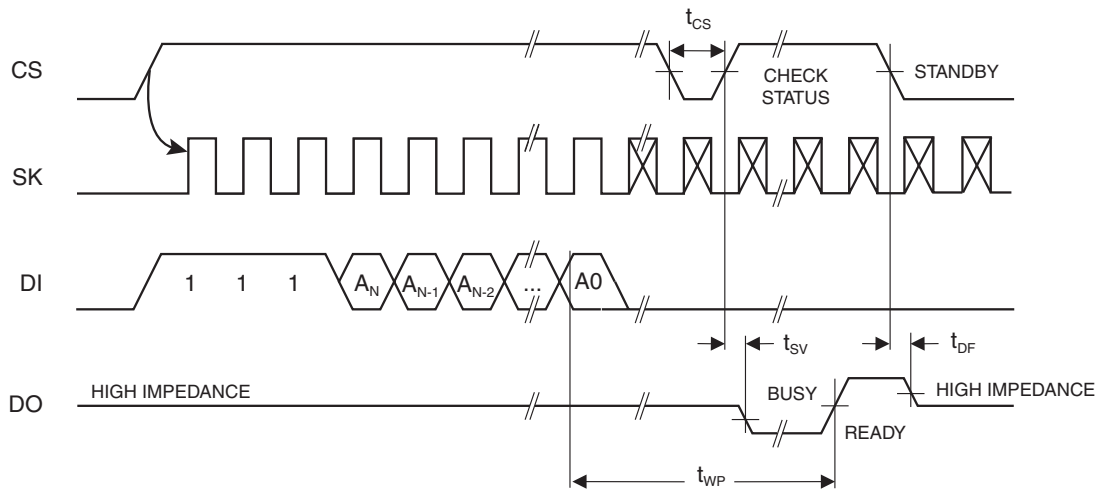
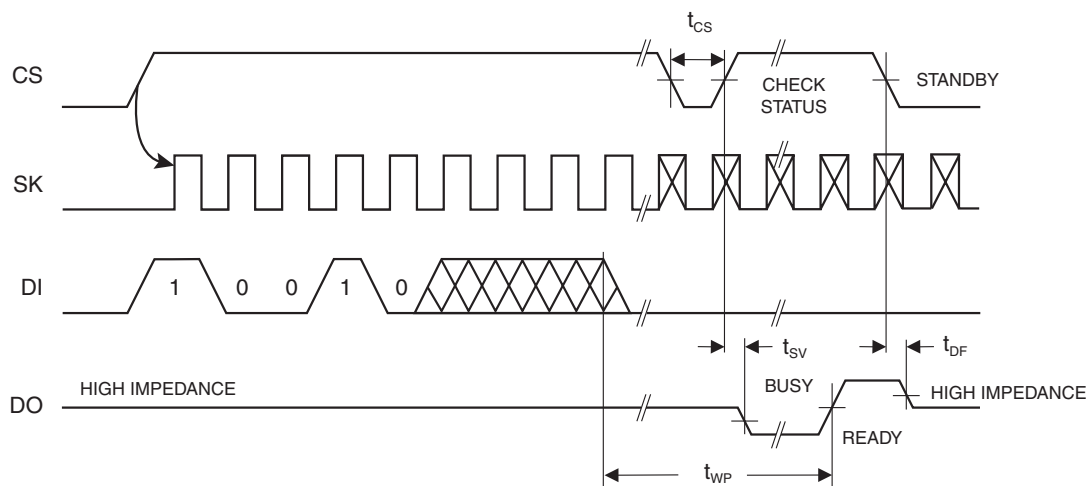


Figure 5-8. ERAL Timing⁽¹⁾



Note: 1. Valid only at $V_{CC} = 4.5V$ to $5.5V$.

6. AT93C56A Ordering Information⁽¹⁾

Ordering Code	Package	Operation Range
AT93C56A-10PU-2.7 ⁽²⁾	8P3	Lead-free/Halogen-free/ Industrial Temperature (-40°C to 85°C)
AT93C56A-10PU-1.8 ⁽²⁾	8P3	
AT93C56A-10SU-2.7 ⁽²⁾	8S1	
AT93C56A-10SU-1.8 ⁽²⁾	8S1	
AT93C56AW-10SU-2.7 ⁽²⁾	8S2	
AT93C56AW-10SU-1.8 ⁽²⁾	8S2	
AT93C56A-10TU-2.7 ⁽²⁾	8A2	
AT93C56A-10TU-1.8 ⁽²⁾	8A2	
AT93C56AU3-10UU-1.8 ⁽²⁾	8U3-1	
AT93C56AD3-10DH-1.8 ⁽³⁾	8D3	
AT93C56AY1-10YU-1.8 ⁽²⁾ (Not recommended for new design)	8Y1	
AT93C56AY6-10YH-1.8 ⁽³⁾	8Y6	
AT93C56A-W1.8-11 ⁽⁴⁾	Die Sales	Industrial Temperature (-40°C to 85°C)

- Notes:
1. For 2.7V devices used in the 4.5V to 5.5V range, please refer to performance values in the AC and DC characteristics table.
 2. "U" designates Green package + RoHS compliant.
 3. "H" designates Green package + RoHS compliant, with NiPdAu Lead Finish.
 4. Available in waffle pack and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial Marketing.

Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8A2	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
8U3-1	8-ball, die Ball Grid Array Package (dBGAA2)
8Y1	8-lead, 4.90 mm x 3.00 mm Body, Dual Footprint, Non-leaded, Miniature Array Package (MAP)
8Y6	8-lead, 2.00 mm x 3.00 mm Body, 0.50 mm Pitch, Ultra Thin Mini-MAP, Dual No Lead package (DFN), (MLP 2x3 mm)
8D3	8-lead, 1.80 mm x 2.20 mm Body, Ultra Lead Frame Land Grid Array (ULA)
Options	
-2.7	Low-voltage (2.7V to 5.5V)
-1.8	Low-voltage (1.8V to 5.5V)

7. AT93C66A Ordering Information⁽¹⁾

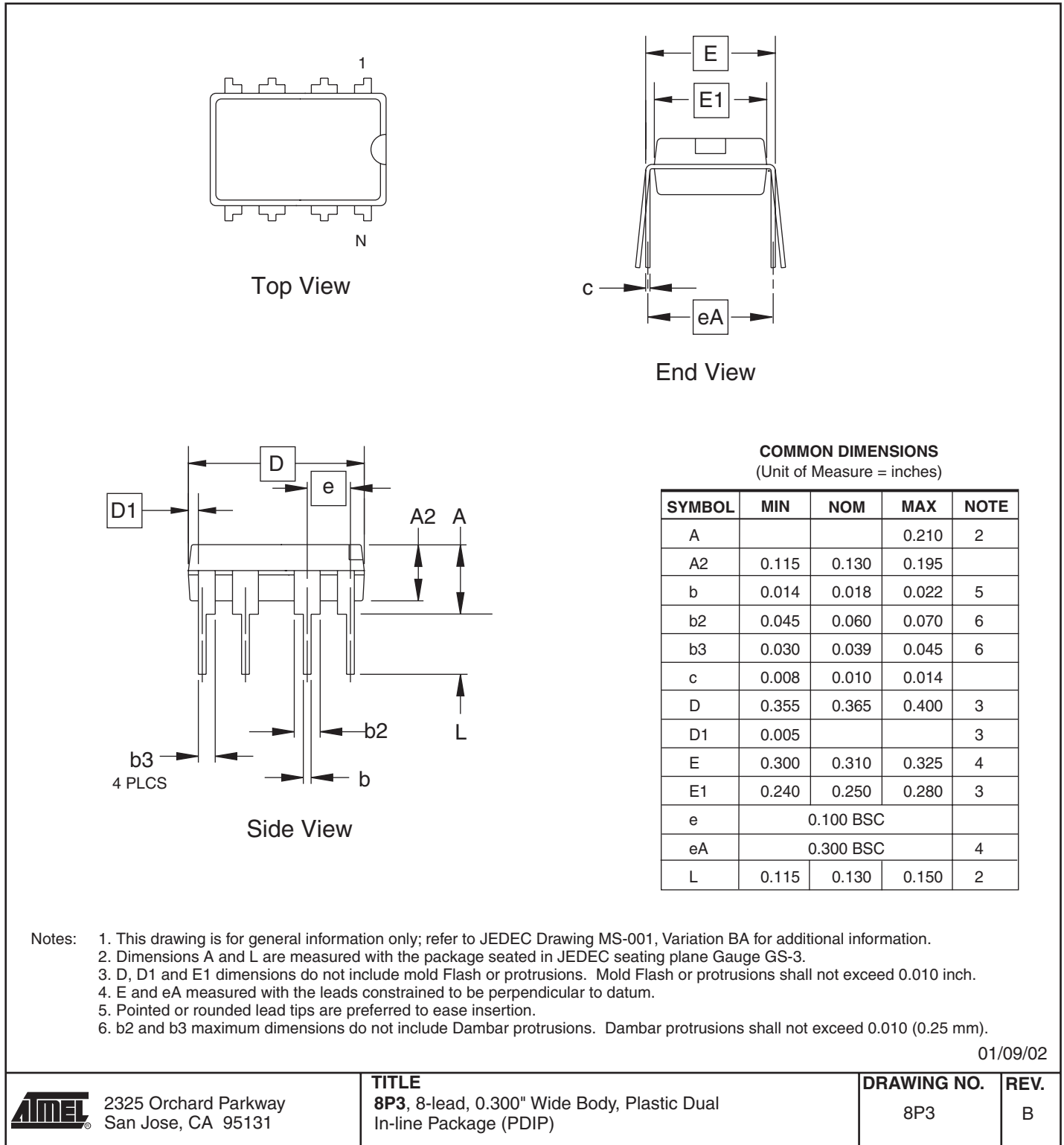
Ordering Code	Package	Operation Range
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AT93C66A-10PU-1.8 ⁽²⁾	8P3	
AT93C66A-10SU-2.7 ⁽²⁾	8S1	
AT93C66A-10SU-1.8 ⁽²⁾	8S1	
AT93C66AW-10SU-2.7 ⁽²⁾	8S2	
AT93C66AW-10SU-1.8 ⁽²⁾	8S2	
AT93C66A-10TU-2.7 ⁽²⁾	8A2	
AT93C66A-10TU-1.8 ⁽²⁾	8A2	
AT93C66AU3-10UU-1.8 ⁽²⁾	8U3-1	
AT93C66AD3-10DH-1.8 ⁽³⁾	8D3	
AT93C66AY1-10YU-1.8 ⁽²⁾ (Not recommended for new design)	8Y1	
AT93C66AY6-10YH-1.8 ⁽³⁾	8Y6	
AT93C66A-W1.8-11 ⁽⁴⁾	Die Sale	Industrial Temperature (-40°C to 85°C)

- Notes:
1. For 2.7V devices used in the 4.5V to 5.5V range, please refer to performance values in the AC and DC characteristics table.
 2. "U" designates Green package + RoHS compliant.
 3. "H" designates Green package + RoHS compliant, with NiPdAu Lead Finish.
 4. Available in waffle pack and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial EEPROM Marketing.

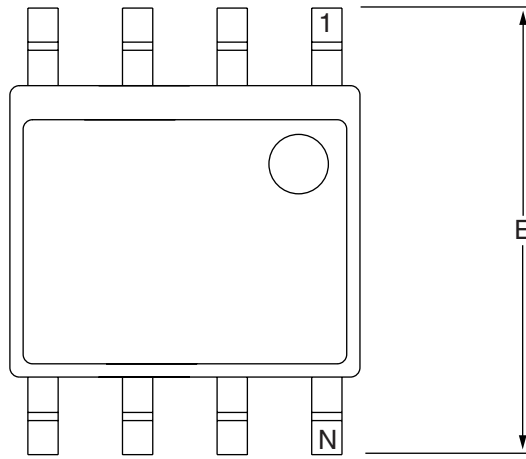
Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8A2	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
8U3-1	8-ball, die Ball Grid Array Package (dBGAA2)
8Y1	8-lead, 4.90 mm x 3.00 mm Body, Dual Footprint, Non-leaded, Miniature Array Package (MAP)
8Y6	8-lead, 2.00 mm x 3.00 mm Body, 0.50 mm Pitch, Ultra Thin Mini-MAP, Dual No Lead package (DFN), (MLP 2x3 mm)
8D3	8-lead, 1.80 mm x 2.20 mm Body, Ultra Lead Frame Land Grid Array (ULA)
Options	
-2.7	Low-voltage (2.7V to 5.5V)
-1.8	Low-voltage (1.8V to 5.5V)

8. Packaging Information

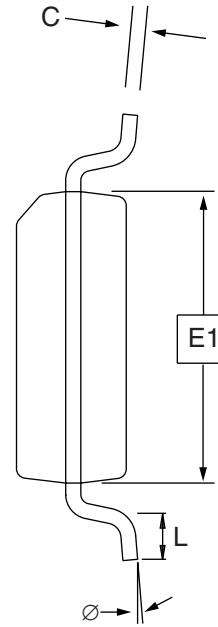
8.1 8P3 – PDIP



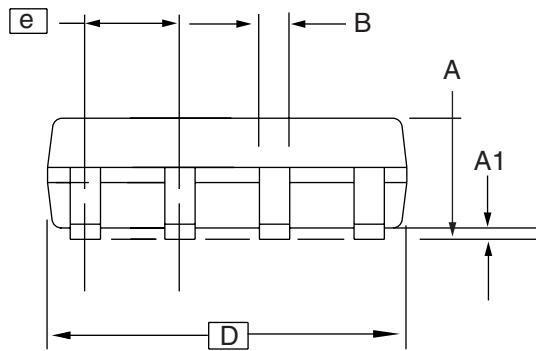
8.2 8S1 – JEDEC SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.00	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
∅	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

10/7/03



1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906

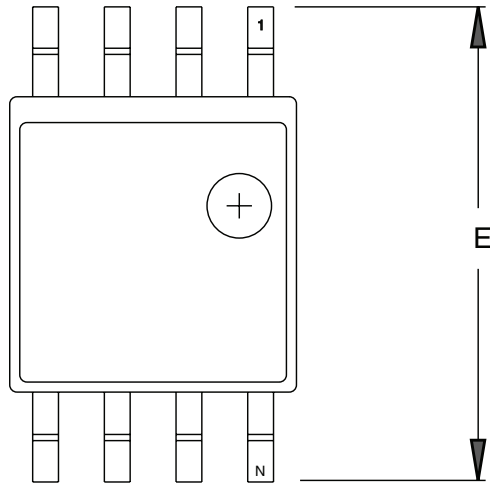
TITLE
8S1, 8-lead (0.150" Wide Body), Plastic Gull Wing
Small Outline (JEDEC SOIC)

DRAWING NO.
8S1

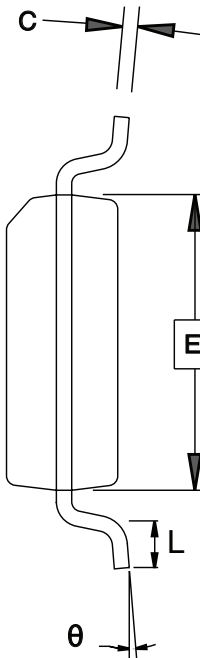
REV.
B



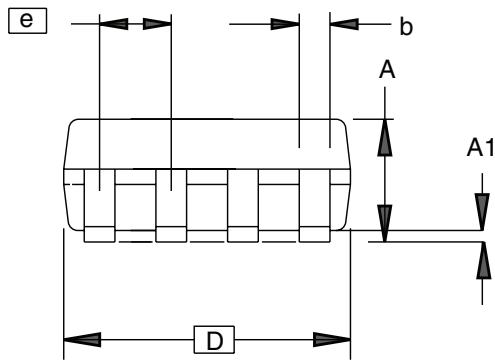
8.3 8S2 – EIAJ SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	5
C	0.15		0.35	5
D	5.13		5.35	
E1	5.18		5.40	2, 3
E	7.70		8.26	
L	0.51		0.85	
θ	0°		8°	
e	1.27 BSC			4

- Notes: 1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
 2. Mismatch of the upper and lower dies and resin burrs aren't included.
 3. It is recommended that upper and lower cavities be equal. If they are different, the larger dimension shall be regarded.
 4. Determines the true geometric position.
 5. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021 mm.

04/07/06

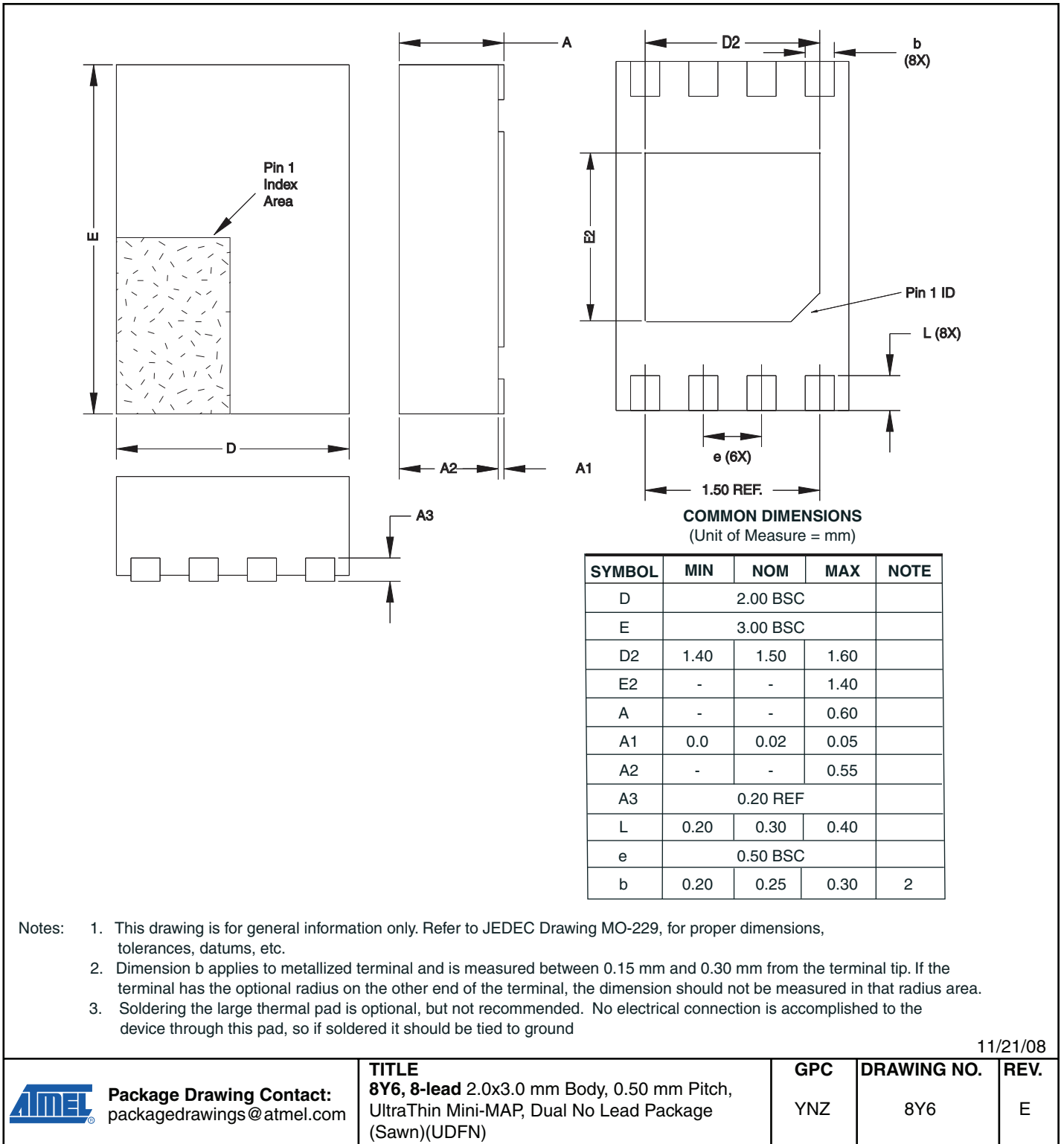


2325 Orchard Parkway
San Jose, CA 95131

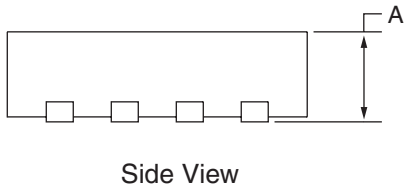
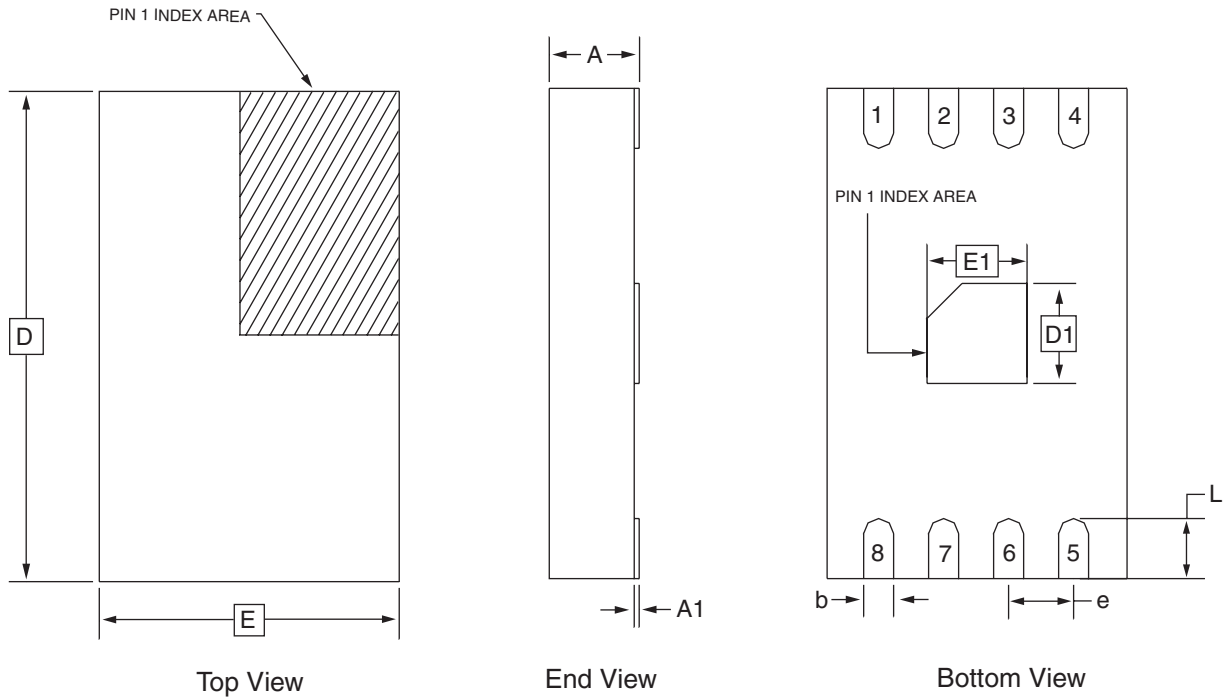
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Outline Package (EIAJ)

DRAWING NO.	REV.
8S2	D

8.4 8Y6 – MiniMap (MLP 2x3)



8.5 8Y1 – Map



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.90	
A1	0.00	–	0.05	
D	4.70	4.90	5.10	
E	2.80	3.00	3.20	
D1	0.85	1.00	1.15	
E1	0.85	1.00	1.15	
b	0.25	0.30	0.35	
e	0.65 TYP			
L	0.50	0.60	0.70	

2/28/03



2325 Orchard Parkway
San Jose, CA 95131

TITLE

8Y1, 8-lead (4.90 x 3.00 mm Body) MSOP Array Package
(MAP) Y1

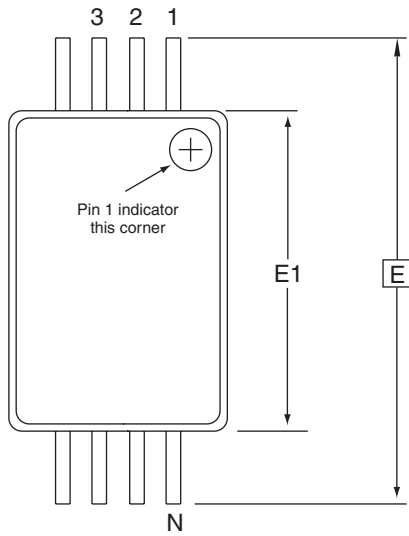
DRAWING NO.

8Y1

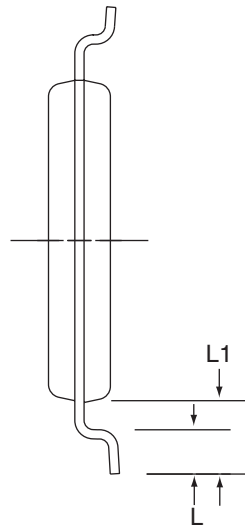
REV.

C

8.6 8A2 – TSSOP



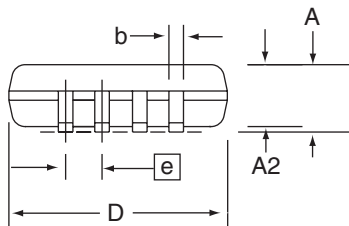
Top View



End View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E	6.40 BSC			
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e	0.65 BSC			
L	0.45	0.60	0.75	
L1	1.00 REF			



Side View

- Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
 2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
 3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
 4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
 5. Dimension D and E1 to be determined at Datum Plane H.

5/30/02



2325 Orchard Parkway
San Jose, CA 95131

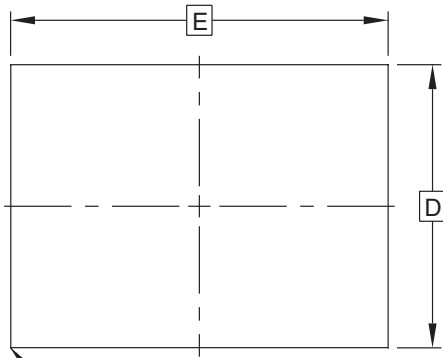
TITLE
8A2, 8-lead, 4.4 mm Body, Plastic
Thin Shrink Small Outline Package (TSSOP)

DRAWING NO.
8A2

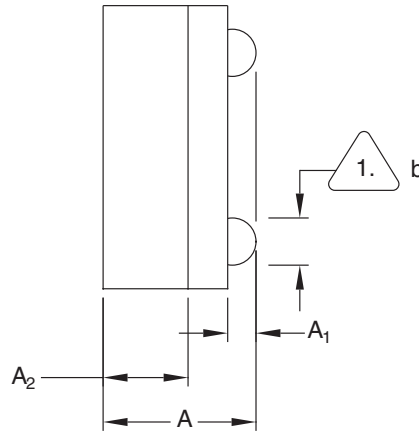
REV.
B



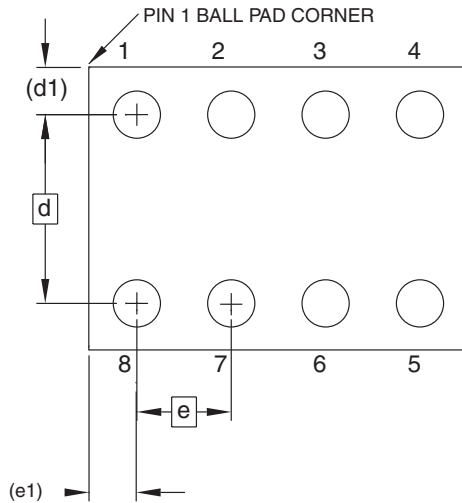
8.7 8U3-1 – dBGA2



Top View



Side View



Bottom View
8 Solder Balls

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.713	0.79	0.85	
A1	0.09	0.14	0.19	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	2
D	1.50 BSC			
E	2.00 BSC			
e	0.50 BSC			
e1	0.25 REF			
d	1.00 BSC			
d1	0.25 REF			

1. This drawing is for general information only.
2. Dimension 'b' is measured at maximum solder ball diameter

5/3/05



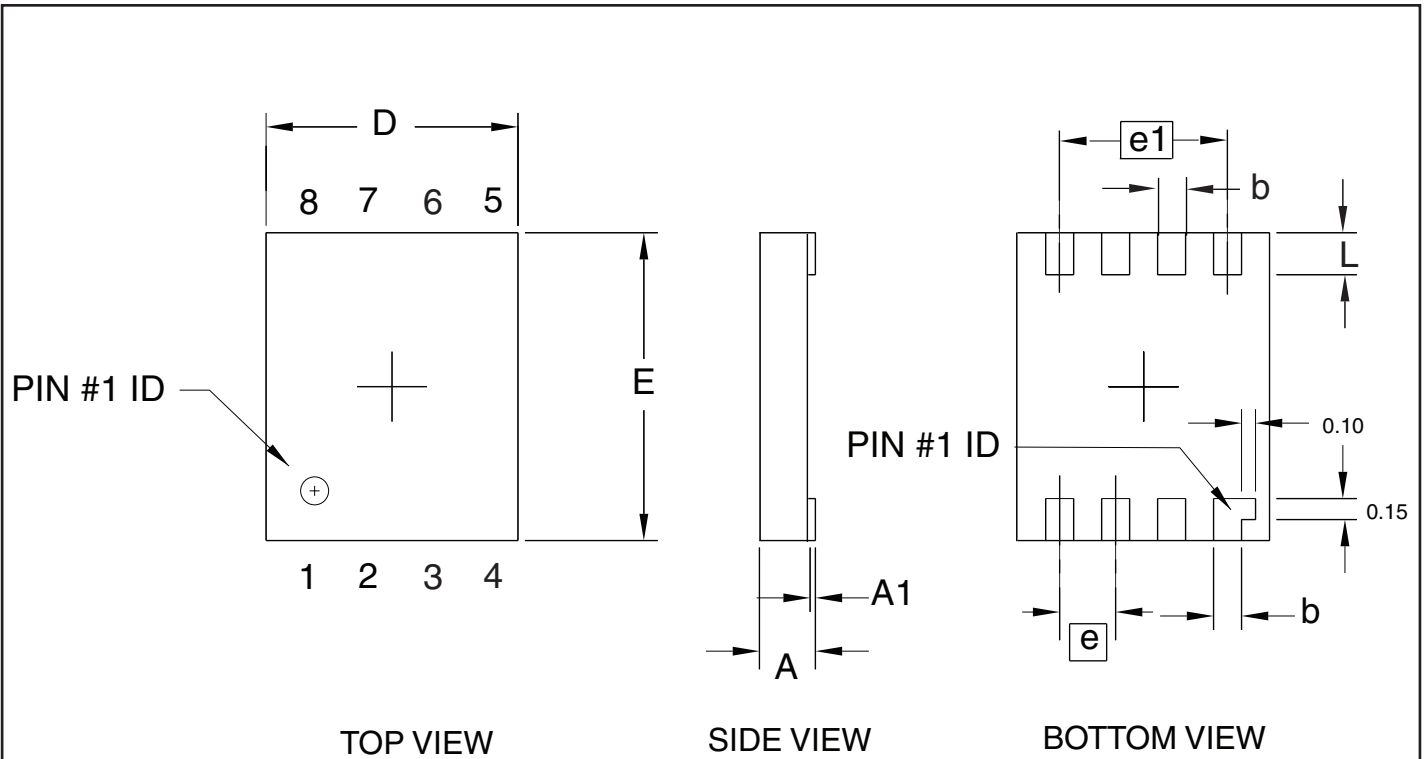
1150E Cheyenne Mt. Blvd
Colorado Springs, CO 80906

TITLE
8U3-1, 8-ball, 1.50 x 2.00 mm Body, 0.50 mm pitch,
Small Die Ball Grid Array Package (dBGA2)

DRAWING NO.
PO8U3-1

REV.
b

8.8 8D3 - ULA



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	0.40	
A1	0.00	-	0.05	
D	1.70	1.80	1.90	
E	2.10	2.20	2.30	
b	0.15	0.20	0.25	
e		0.40 TYP		
e1		1.20 REF		
L	0.25	0.30	0.35	

11/15/05



1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906

TITLE

8D3, 8-lead (1.80 x 2.20 mm Body) Ultra Leadframe
Land Grid Array (ULLGA) D3

DRAWING NO.

8D3

REV.

0



9. Revision History

Revision No.	Date	Comments
3378O	11/2009	Added 8S2 package drawing
3378N	1/2009	Updated 8Y6 package drawing
3378M	7/2008	Updated Ordering Codes
3378L	11/2007	Updated to new template Added ULA package offering
3378K	12/2006	Removed DC/Don't Connect and replaced with NC/No Conenct Adjusted size of Block diagram on pg. 2 Made all diagrams on pages 6-9 consistently the same size Corrected 8U3-1



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