

Single Phase Synchronous Buck PWM Controller

AP3586A/B/C

Pin Configuration

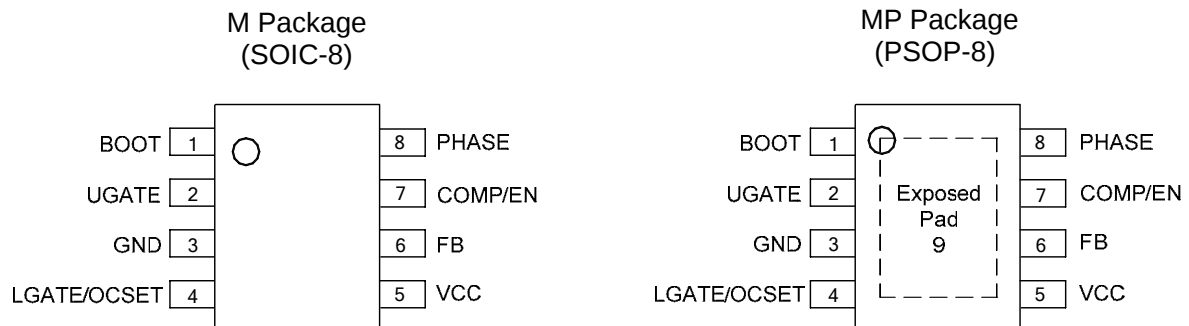


Figure 2. Pin Configuration of AP3586A/B/C (Top View)

Pin Description

Pin Number		Pin Name	Function
SOIC-8	PSOP-8		
1	1	BOOT	Bootstrap pin. Connect a bootstrap capacitor from this pin to PHASE for creating a BOOT voltage suitable to drive a standard N-Channel MOSFET.
2	2	UGATE	Upper-gate drive pin. Connect this pin to the upper MOSFET gate providing the gate drive. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
3	3	GND	Ground for the IC. All voltage levels are measured with respect to this pin. Connect this pin directly to the low side MOSFET source and ground plane with the lowest impedance. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
4	4	LGATE/OCSET	Low-side Gate Driver Output and Over-Current Setting Input. This pin is the gate driver for low-side MOSFET. It is also used to set the maximum inductor current. Refer to the section in “Function Description” for detail.
5	5	VCC	Bias supply pin. Provides a 5V or 12V bias supply for the chip from this pin. The pin should be bypassed with a capacitor to GND.
6	6	FB	Feedback pin. This pin is the inverting input of the internal error amplifier. Use FB pin, in combination with the COMP pin, to compensate the voltage control feedback loop of the converter. A resistor divider from output to GND is used to set the output voltage.
7	7	COMP/EN	Compensation and disable pin. This pin is the output of the Error Amplifier. Pull COMP pin low will shut down the IC.
8	8	PHASE	This pin connects to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
	9	Exposed Pad	Exposed Pad as ground pin.

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Functional Block Diagram

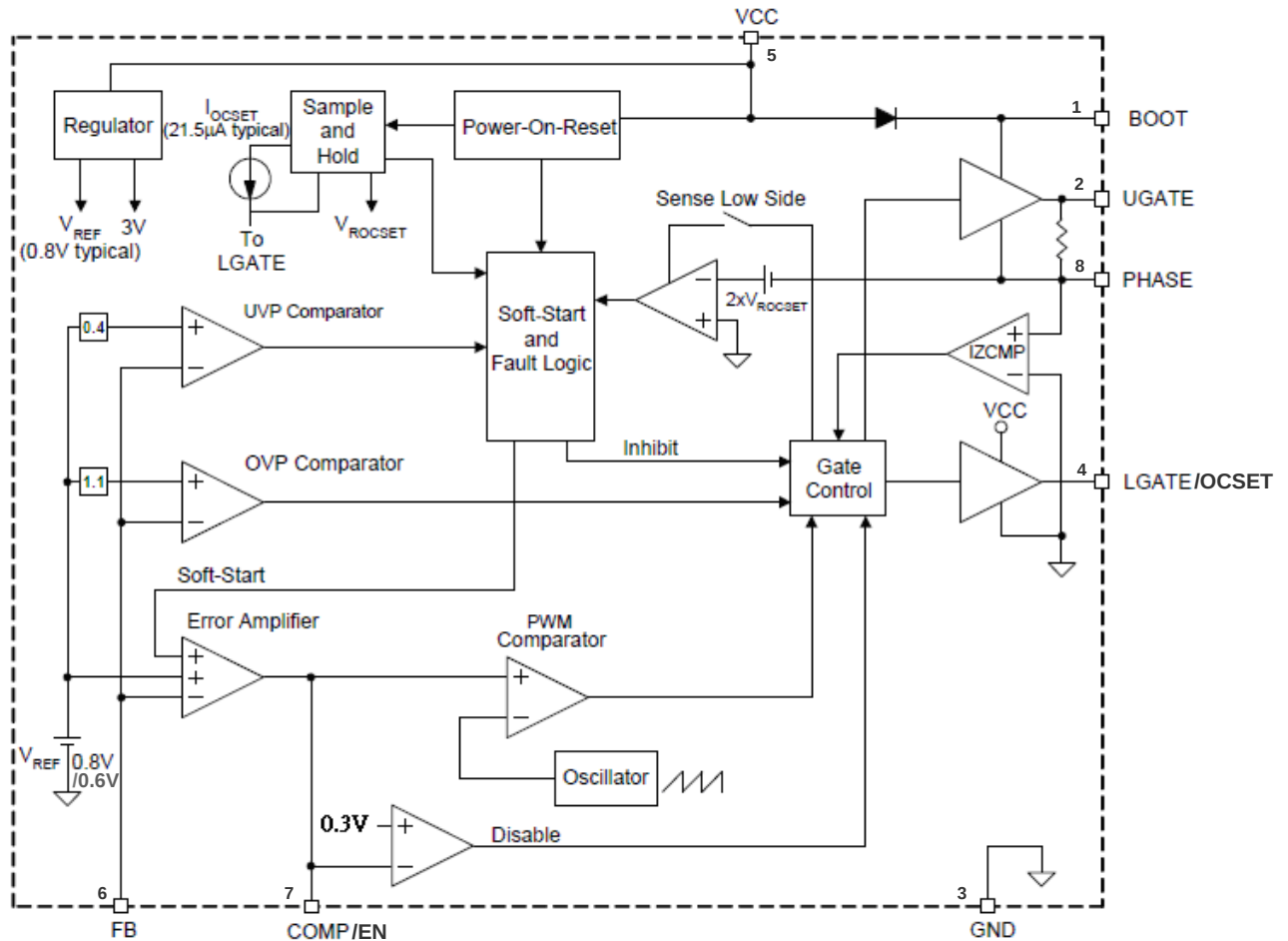
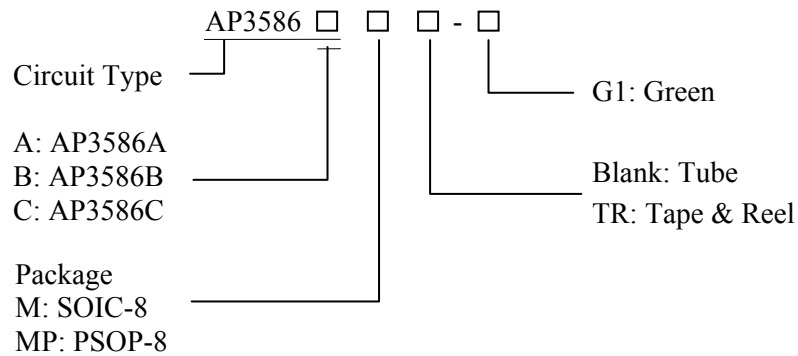


Figure 3. Functional Block Diagram of AP3586A/B/C

**Single Phase Synchronous Buck PWM Controller****AP3586A/B/C****Ordering Information**

Package	Temperature Range	Part Number	Marking ID	Packing Type
SOIC-8	-40 to 85°C	AP3586AM-G1	3586AM-G1	Tube
		AP3586AMTR-G1	3586AM-G1	Tape & Reel
		AP3586BM-G1	3586BM-G1	Tube
		AP3586BMTR-G1	3586BM-G1	Tape & Reel
		AP3586CM-G1	3586CM-G1	Tube
		AP3586CMTR-G1	3586CM-G1	Tape & Reel
PSOP-8		AP3586AMP-G1	3586AMP-G1	Tube
		AP3586AMPTR-G1	3586AMP-G1	Tape & Reel
		AP3586BMP-G1	3586BMP-G1	Tube
		AP3586BMPTR-G1	3586BMP-G1	Tape & Reel
		AP3586CMP-G1	3586CMP-G1	Tube
		AP3586CMPTR-G1	3586CMP-G1	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "G1" suffix in the part number, are RoHS compliant and green.

**Single Phase Synchronous Buck PWM Controller****AP3586A/B/C****Absolute Maximum Ratings (Note 1)**

Parameter	Symbol	Value	Unit
Supply Input Voltage	V_{CC}	-0.3 to 15	V
BOOT Voltage	V_{BOOT}	-0.3 to $V_{PHASE} + 15$	V
UGATE to PHASE Voltage	V_{UGATE}	-0.3 to 15	V
PHASE, LGATE to GND Voltage	$V_{PHASE},$ V_{LGATE}	-1 to 15	V
Other Pin Voltage		-0.3 to 6	V
Power Dissipation	P_D	TBD	mW
Thermal Resistance	θ_{JA}	50	°C/W
Operating Junction Temperature	T_J	-40 to 125	°C
Storage Temperature	T_{STG}	-65 to 150	°C
Lead Temperature (Soldering, 10 sec)	T_{LEAD}	260	°C
ESD (Human Body Model) (Note 2)		2000	V
ESD (Machine Model) (Note 2)		200	V

Note 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Note 2: Devices are ESD sensitive. Handling precaution is recommended.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Input Voltage	V_{CC}	5	12	V
Operating Ambient Temperature	T_A	-40	85	°C

**Single Phase Synchronous Buck PWM Controller****AP3586A/B/C****Electrical Characteristics** $V_{CC}=12V$, $T_A=25^{\circ}C$, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY INPUT						
Supply Current	I_{CC}	UGATE and LGATE Pins Open; Switching		5		mA
Quiescent Supply Current	I_{CC_Q}	$V_{FB}=V_{REF}+0.1V$, No Switching		4		mA
Power Input Voltage	V_{IN}		3.0		13.2	V
POWER ON RESET						
V_{CC} Rising Threshold	V_{POR}	V_{CC} Rising	4.0	4.2	4.4	V
V_{CC} Threshold Hysteresis	V_{POR_HYS}			500		mV
OSCILLATOR						
Oscillator Frequency	f_{OSC}	For AP3586A/B	270	300	330	kHz
		For AP3586C	180	200	220	kHz
Ramp Amplitude	ΔV_{OSC}			1.4		V_{P-P}
ERROR AMPLIFIER						
Open Loop DC Gain	G_{DC_OL}		55	70		dB
Gain-bandwidth Product	G_{BW}			10		MHz
Slew Rate	SR		3	6		V/ μs
Transconductance				800	1100	$\mu A/V$
Output Source Current		$V_{FB}<V_{REF}$	80	120		μA
Output Sink Current		$V_{FB}>V_{REF}$	80	120		μA
PWM CONTROLLER GATE DRIVERS						
Upper Gate Source Current	I_{UG_SRC}	$V_{BOOT}-V_{PHASE}=12V$, $V_{BOOT}-V_{UGATE}=6V$		-1.0		A
Upper Gate Sink Current	I_{UG_SNK}	$V_{BOOT}-V_{PHASE}=12V$, $V_{BOOT}-V_{UGATE}=6V$		1.5		A
Upper Gate Sink Resistance	R_{UGATE}	50mA Source Current		2	4	Ω
Lower Gate Source Current	I_{LG_SRC}	$V_{CC}-V_{LGATE}=6V$		-1		A
Lower Gate Sink Current	I_{LG_SNK}	$V_{LGATE}=6V$		1.5		A
Lower Gate Sink Resistance	R_{LGATE}	50mA Source Current		1	2	Ω
PHASE Falling to LGATE Rising Delay		$V_{PHASE}<1.2V$ to $V_{LGATE}>1.2V$		50		ns
LGATE Falling to UGATE Rising Delay		$V_{LGATE}<1.2V$ to $(V_{UGATE}-V_{PHASE})>1.2V$		50		ns

**Single Phase Synchronous Buck PWM Controller****AP3586A/B/C****Electrical Characteristics (Continued)** $V_{CC}=12V$, $T_A=25^{\circ}C$, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Minimum Duty Cycle				0		%
Maximum Duty Cycle			75	82	89	%
REFERENCE VOLTAGE						
Feedback Voltage	V_{FB}	AP3586A	0.591	0.6	0.609	V
		AP3586B/C	0.788	0.8	0.812	V
Feedback Bias Current	I_{FB}	$V_{FB}=5V$		10	50	nA
PROTECTION						
Under Voltage Protection	V_{FB_UVP}		0.3	0.4	0.5	V
Over Voltage Protection	V_{FB_OVP}			1.1		V
OC Current Source	I_{OPS}		19.5	21.5	23.5	μA
Built-in Maximum OCP Voltage	V_{OCP_MAX}			0.3		V
Soft-start Interval	t_{SS}	AP3586A		2		ms
		AP3586B		2.7		
		AP3586C		3.6		
Enable Threshold	$V_{COMP/EN}$		0.25	0.30	0.35	V
Thermal Shutdown	T_{OTSD}			160		$^{\circ}C$
Thermal Shutdown Hysteresis	T_{HYS}			20		$^{\circ}C$

Single Phase Synchronous Buck PWM Controller

AP3586A/B/C

Typical Performance Characteristics

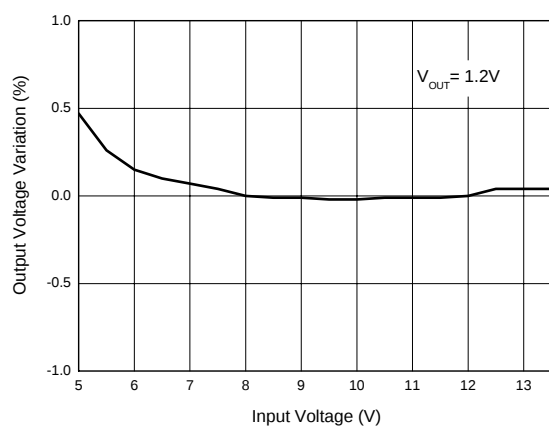


Figure 4. Line Regulation

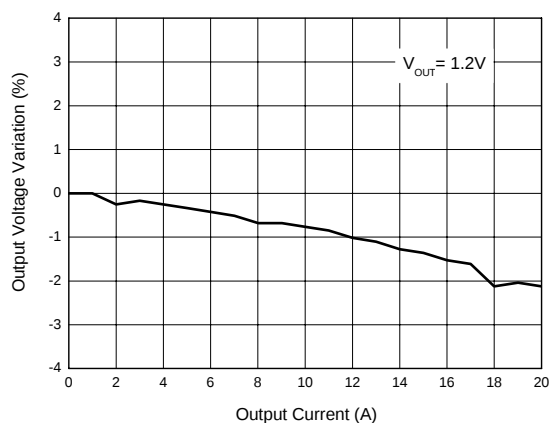


Figure 5. Load Regulation

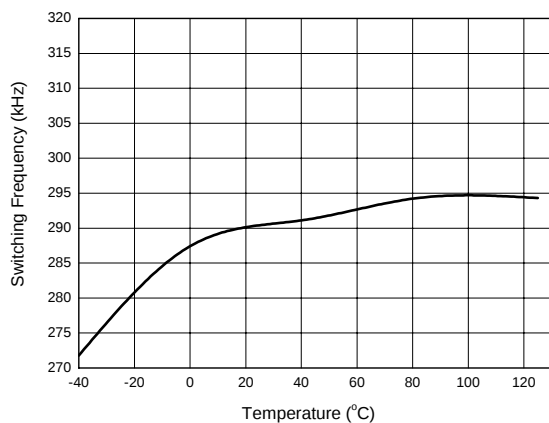


Figure 6. Switching Frequency vs. Temperature

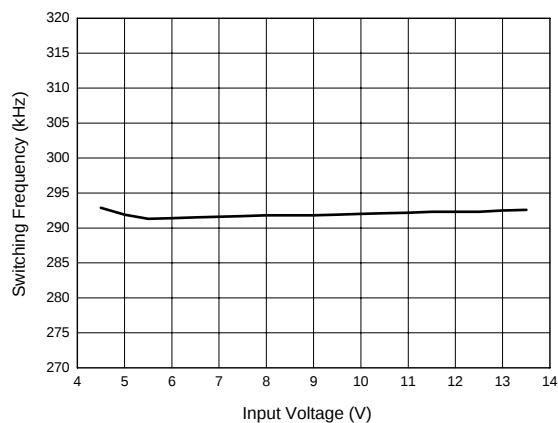


Figure 7. Switching Frequency vs. Input Voltage

Single Phase Synchronous Buck PWM Controller

AP3586A/B/C

Typical Performance Characteristics (Continued)

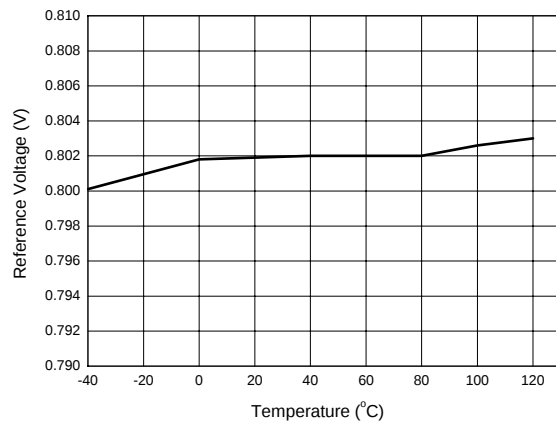


Figure 8. Reference Voltage vs. Temperature

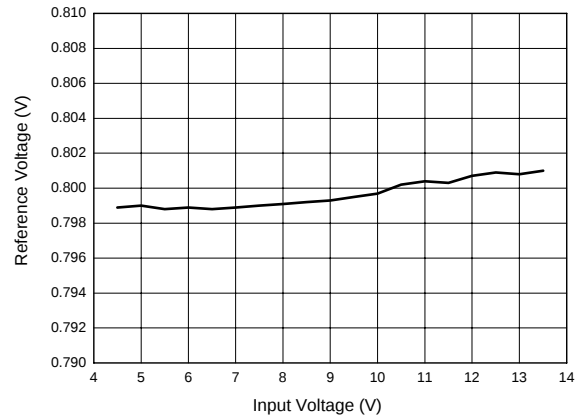
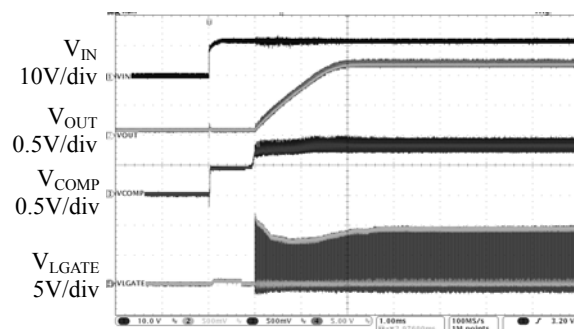
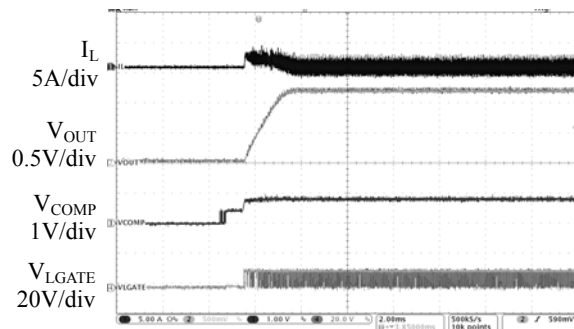


Figure 9. Reference Voltage vs. Input Voltage



Time 1ms/div

Figure 10. Power-on Waveform
($V_{IN}=12V$, $V_{OUT}=1.2V$, $I_{OUT}=0A$)


Time 2ms/div

Figure 11. Enable Waveform
($V_{IN}=12V$, $V_{OUT}=1.2V$, $I_{OUT}=0A$)

Single Phase Synchronous Buck PWM Controller

AP3586A/B/C

Typical Performance Characteristics (Continued)

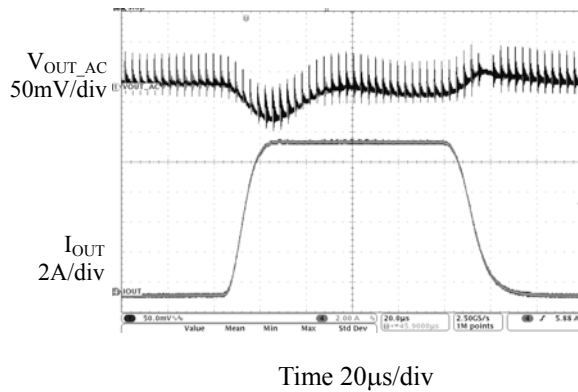


Figure 12. Load Transient Response
($V_{IN}=12V$, $V_{OUT}=1.2V$, $I_{OUT}=0A$ to $10A$)

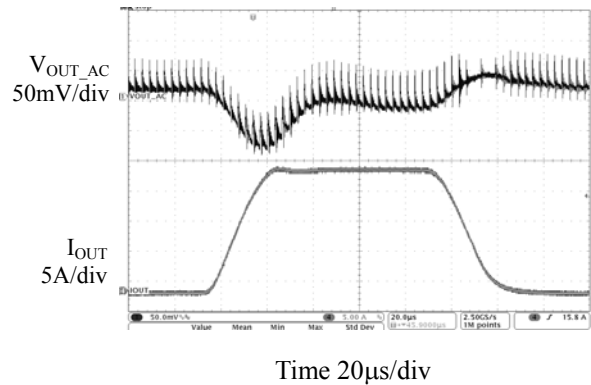


Figure 13. Load Transient Response
($V_{IN}=12V$, $V_{OUT}=1.2V$, $I_{OUT}=0A$ to $20A$)

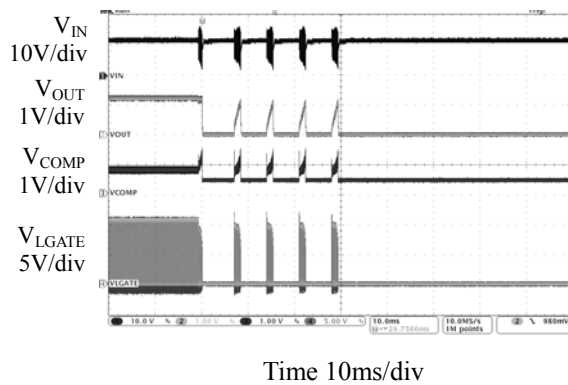


Figure 14. Over Current Protection
($V_{IN}=12V$, $V_{OUT}=1.2V$, $I_{OUT}=20A$)

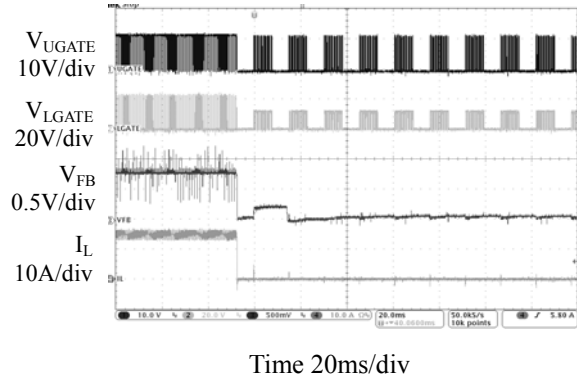


Figure 15. Under Voltage Protection
($V_{IN}=12V$, $V_{OUT}=1.2V$, $I_{OUT}=20A$)

Single Phase Synchronous Buck PWM Controller

AP3586A/B/C

Typical Application

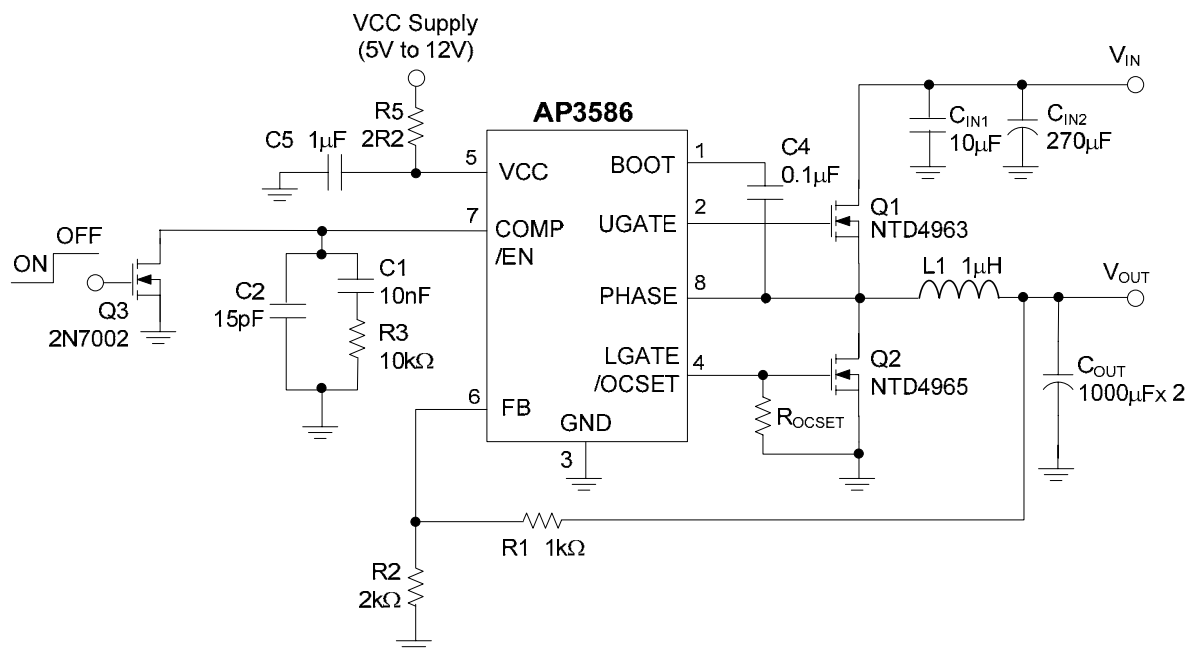


Figure 16. Typical Application Circuit of AP3586A/B/C

Single Phase Synchronous Buck PWM Controller

AP3586A/B/C

Function Description

The AP3586A/B/C is a voltage-mode single phase synchronous buck controller with embedded MOSFET drivers. This part provides complete protection functions such as over voltage protection, under voltage protection and over current protection. Inductor current information is sensed by $R_{DS(ON)}$ of the low side MOSFET. The over current protection threshold can be simply programmed by a resistor.

Power on Reset and Chip Enable

A power on reset (POR) circuitry continuously monitors the supply voltage at VCC pin. Once the rising POR threshold is exceeded, the AP3586A/B/C sets itself to active state and is ready to accept chip enable command. The rising POR threshold is typically 4.2V at VCC rising.

The COMP/EN is a multifunctional pin: control loop compensation and chip enable as shown in Figure 17. An Enable Comparator monitors the COMP/EN pin voltage for chip enable. A signal level transistor is adequate to pull this pin down to ground and shut down AP3586. A 120 μ A current source charges the external compensation network with 0.45V ceiling when this pin is released. If the voltage at COMP/EN pin exceeds 0.3V, the AP3586A/B/C initiates its soft start cycle.

The 120 μ A current source keeps charging the COMP pin to its ceiling until the feedback loop boosts the COMP pin higher than 0.45V according to the feedback signal. The current source is cut off when V_{COMP} is higher than 0.45V during normal operation.

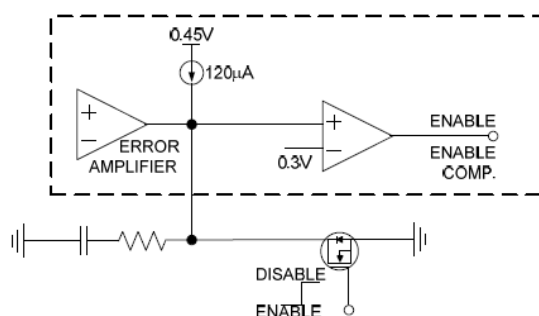


Figure 17. Chip Enable Function

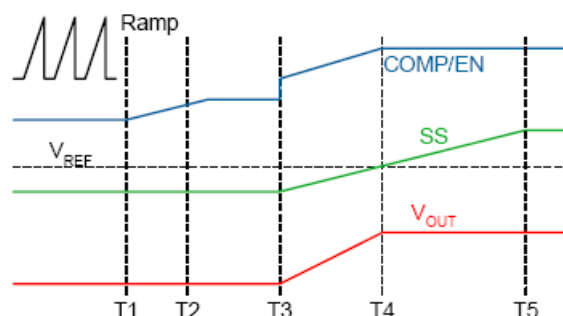
Soft Start

A built-in Soft Start is used to prevent surge current

from power supply input V_{IN} during turn-on (Referring to the Functional Block Diagram). The error amplifier is a three-input device. Reference voltage V_{REF} or the internal soft start voltage SS whichever is smaller dominates the behavior of the non-inverting inputs of the error amplifier. SS internally ramps up to 0.6V in 2ms for AP3586A (to 0.8V in 2.7ms for AP3586B; to 0.8V in 3.6ms for AP3586C) after the soft start cycle is initiated. The ramp is created digitally, so there will be 100 small discrete steps. Accordingly, the output voltage will follow the SS signal and ramp up smoothly to its target level.

The SS signal keeps ramping up after it exceeds the internal 0.6V (0.8V for AP3586B/C) reference voltage. However, the internal 0.6V(0.8V for AP3586B/C) reference voltage takes over the behavior of error amplifier after $SS > V_{REF}$. When the SS signal climbs to its ceiling voltage (4.2V), AP3586A/B/C claims the end of soft start cycle and enables the under voltage protection of the output voltage.

Figure 18 shows a typical start up interval for AP3586A/B/C where the COMP/EN pin has been released from a grounded (system shutdown) state. The internal 120 μ A current source starts charge the compensation network after the COMP/EN pin is released from ground at T1. The COMP/EN exceeds 0.3V and enables the AP3586A/B/C at T2. The COMP/EN continues ramping up the stays at 0.45V before the SS starts ramping at T3. The output voltage follows the internal SS and ramps up to its final level during T3 and T4. At T4, the reference voltage V_{REF} takes over the behavior of the error amplifier as the internal SS crosses V_{REF} . The internal SS keeps ramping up and stays at 4.2V at T5, where AP3586A/B/C asserts the end of soft start cycle.



Single Phase Synchronous Buck PWM Controller

AP3586A/B/C

Function Description (Continued)

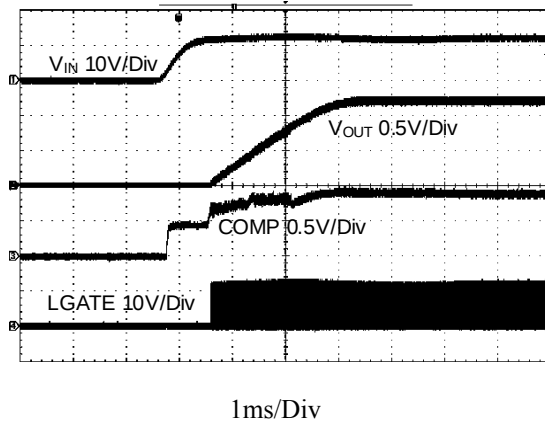


Figure 18. Soft Start Behavior of AP3586A/B/C

Power Input Detection

The AP3586A/B/C detects PHASE voltage for the present of power input V_{IN} when UGATE turns on the first time. If the PHASE voltage does not exceed 2.0V when UGATE turns on, AP3586A/B/C asserts that V_{IN} is not ready and stops the soft start cycle. However, the internal SS continues ramping up to V_{DD} . Another soft start is initiated after SS ramps up to V_{DD} . The hiccup period is about 1ms. Figure 19 shows the start-up waveform where V_{IN} does not present initially.

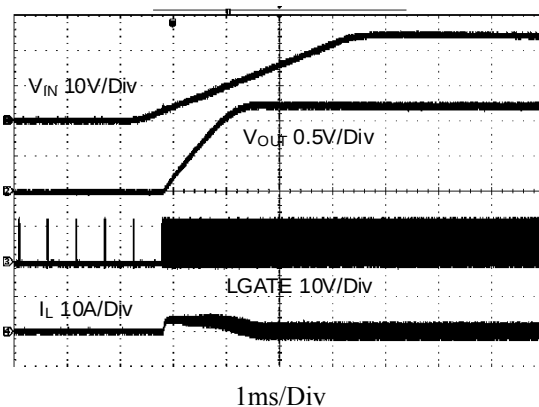


Figure 19. Soft Start Where V_{IN} Does Not Present Initially

Over Current Protection (OCP)

A resistor R_{OCSET} connected from LGATE pin sets the threshold. An internal current source I_{OC} (21.5 μ A typically), flowing through R_{OCSET} determines the OCP trigger point, which can be calculated using the

following equation:

$$I_{LIMIT} = \frac{2 \times I_{OCSET} \times R_{OCSET}}{R_{DS(ON)} \text{ of the low side MOSFET}}$$

Because the $R_{DS(ON)}$ of MOSFET increases with temperature, it is necessary to take this thermal effect into consideration in calculating OCP point.

When OCP is triggered, both UGATE and LGATE will go low to stop the energy transfer to the load. Controller will try to restart in a hiccupped way. Figure 20 shows the hiccupped over current protection. Only four times of hiccup is allowed in over current protection. If over current condition still exists after four times of hiccup, controller will be latched.

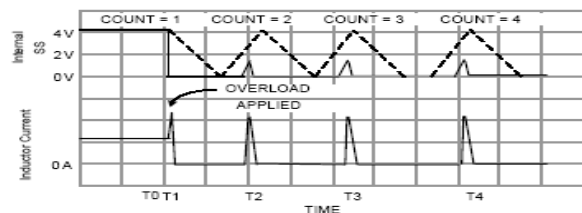


Figure 20. Hiccupped Over Current Protection

Over Voltage Protection (OVP)

The feedback voltage is continuously monitored for over voltage protection. When OVP is triggered, LGATE will go high and UGATE will go low to discharge the output capacitor.

The AP3586A/B/C provides full-time over voltage protection whenever soft start completes or not. The typical OVP threshold is 137.5% of the internal reference voltage V_{REF} . AP3586A/B/C provides non-latched OVP. The controller will return to normal operation if over voltage condition is removed.

Under Voltage Protection (UVP)

The feedback voltage is also monitored for under voltage protection. The under voltage protection has 15 μ s triggered delay. When UVP is triggered, both UGATE and LGATE will go low. Unlike OCP, UVP is not a latched protection; controller will always try to restart in a hiccupped way.

Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of 160 $^{\circ}$ C, the PWM and the

Single Phase Synchronous Buck PWM Controller**AP3586A/B/C****Function Description (Continued)**

oscillator are turned off and UGATE and LGATE are driven low, turning off both MOSFETs. When the junction cools to the required level (140°C nominal), the PWM initiates soft start as during a normal power-up cycle.

Output Voltage Selection

The output voltage can be programmed to any level between the 0.6V internal reference (0.8V for AP3586B/C) to the 82% of V_{IN} supply. The lower limitation of output voltage is caused by the internal reference. The upper limitation of the output voltage is caused by the maximum available duty cycle (82%). This is to leave enough time for over-current detection. Output voltage out of this range is not allowed.

A voltage divider sets the output voltage (Refer to the typical application circuit). In real applications, choose R1 in 100Ω to 10kΩ range and choose appropriate R2 according to the desired output voltage.

$$V_{OUT} = 0.6V \times \frac{R1 + R2}{R2} \quad \text{AP3586A}$$

$$V_{OUT} = 0.8V \times \frac{R1 + R2}{R2} \quad \text{AP3586B/C}$$

PCB Layout Considerations

High speed switching and relatively large peak currents in a synchronous-rectified buck converter make the PCB layout a very important part of design. Switching current from one power device to another can generate voltage spikes across the impedances of the interconnecting bond wires and circuit traces. The voltage spikes can degrade efficiency and radiate noise, that results in over-voltage stress on devices. Careful component placement layout a printed circuit design can minimize the voltage spikes induced in the converter.

Follow the below layout guidelines for optimal performance of AP3586A/B/C.

- 1) The turn-off transition of the upper MOSFET prior to turn-off, the upper MOSFET was carrying the full load current. During turn-off, current stops flowing in the upper MOSFET and is picked up by the low side MOSFET. Any inductance in the switched path generates a large voltage spike during the switching interval. Careful component selections, layout of the critical components, and use shorter and wider PCB traces help in minimizing the magnitude of voltage spikes.
- 2) The power components and the PWM controller should be placed firstly. Place the input capacitors, especially the high-frequency ceramic decoupling capacitors, close to the power switches. Place the output inductor and output capacitors between the MOSFETs and the load. Also locate the PWM controller near MOSFETs.
- 3) Use a dedicated grounding plane and use vias to ground all critical components to this layer. Use an immediate via to connect the component to ground plane including GND of AP3586A/B/C.
- 4) Apply another solid layer as a power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the PHASE node.
- 5) The PHASE node is subject to very high dV/dt voltages. Stray capacitance between this island and the surrounding circuitry tend to induce current spike and capacitive noise coupling. Keep the sensitive circuit away from the PHASE node and keep the PCB area small to limit the capacitive coupling. However, the PCB area should be kept moderate since it also acts as main heat convection path of the lower MOSFET.
- 6) The PCB traces between the PWM controller and the gate of MOSFET and also the traces connecting source of MOSFETs should be sized to carry 2A peak currents.

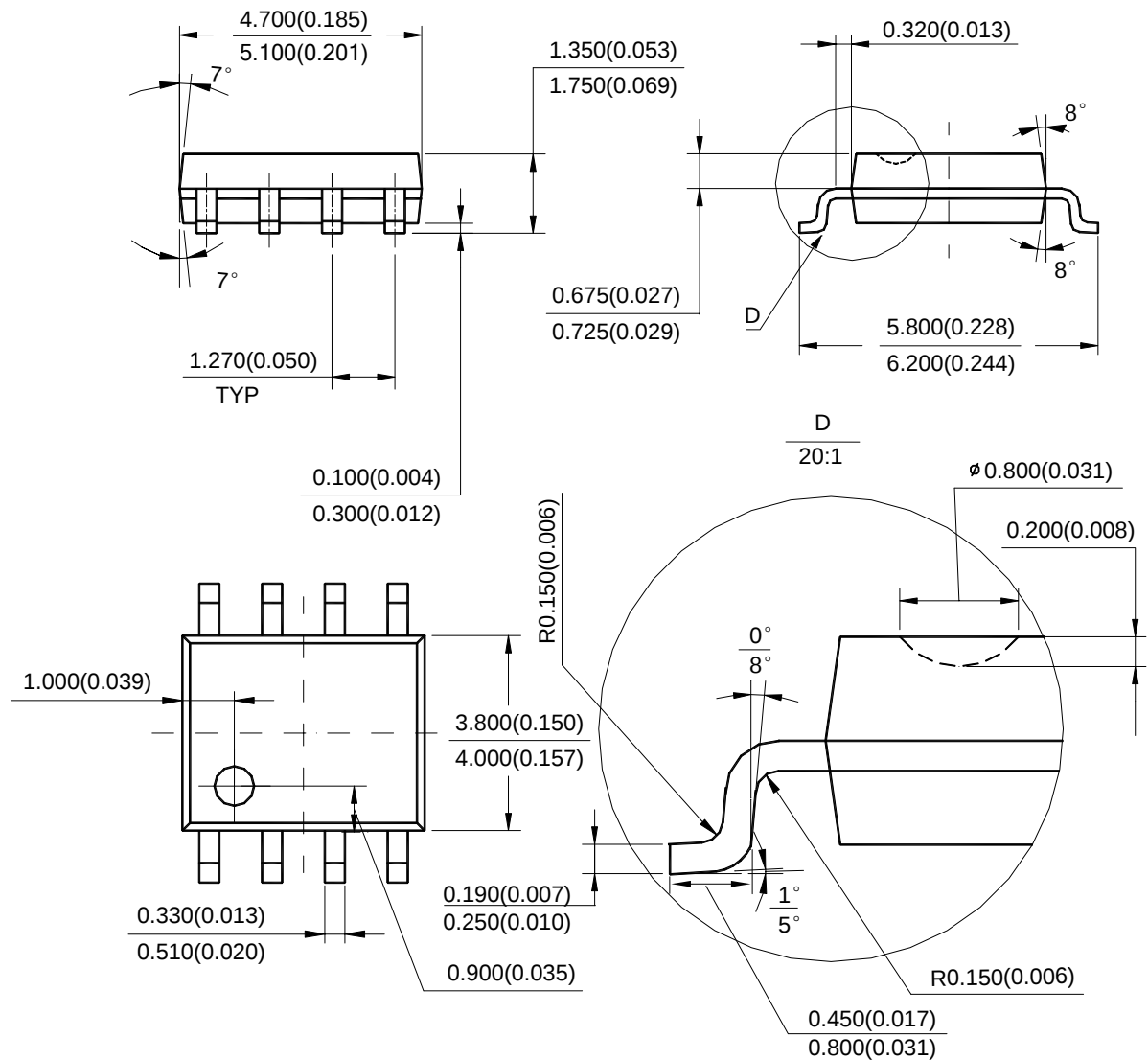
Single Phase Synchronous Buck PWM Controller

AP3586A/B/C

Mechanical Dimensions

SOIC-8

Unit: mm(inch)



Note: Eject hole, oriented hole and mold mark is optional.

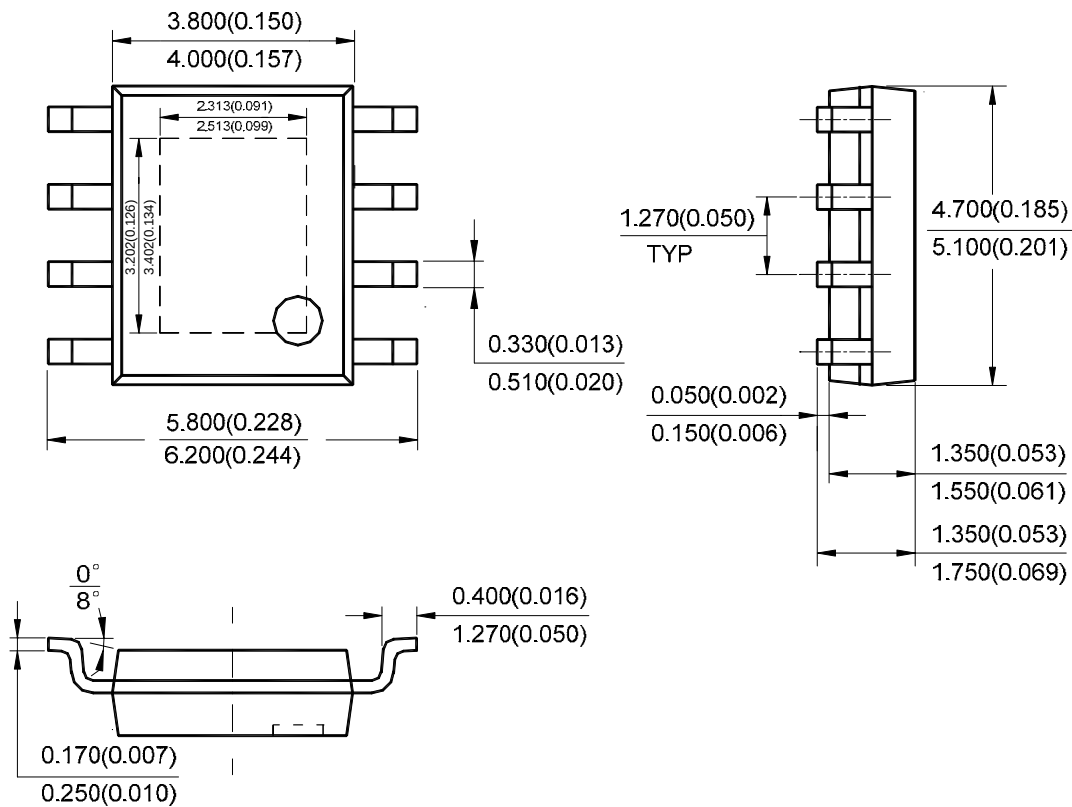
Single Phase Synchronous Buck PWM Controller

AP3586A/B/C

Mechanical Dimensions (Continued)

PSOP-8

Unit: mm(inch)



Note: Eject hole, oriented hole and mold mark is optional.



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