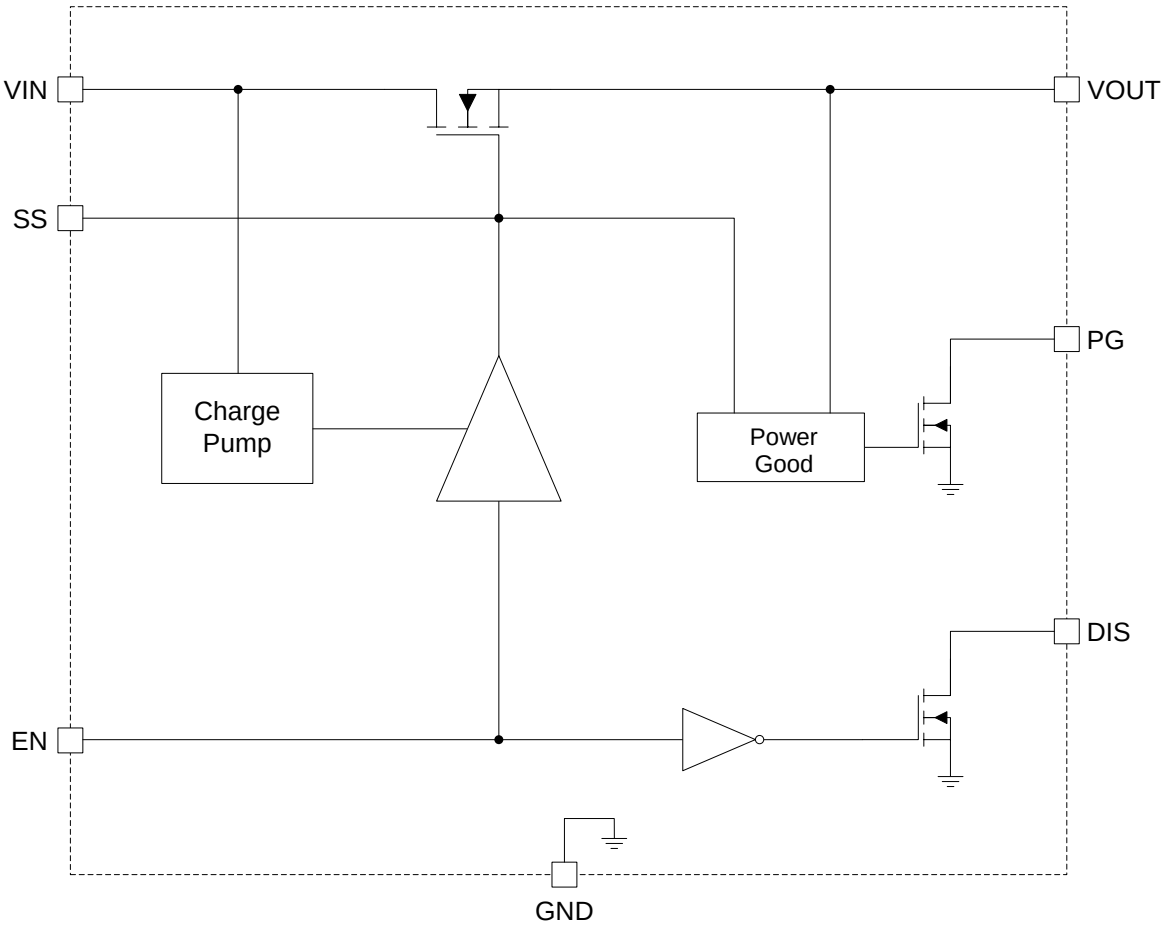
NEW PRODUCT

Pin Descriptions

Pin Name	Pin Number	Function
VIN	1, 2	Input Voltage.
EN	3	Enable Input, Active High.
SS	4	Soft-Start Adjust. An external capacitor connected to this pin will set the ramp-up time of VOUT.
PG	5	Power Good. Open-drain output to indicate when the switch is fully enhanced.
DIS	6	Output Discharge. An external resistor between DIS and VOUT sets the discharge rate at VOUT when EN goes low.
VOUT	7, 8	Output Voltage. This pin connects to the Source of the N-channel MOSFET.
GND	PAD	Ground.

Functional Block Diagram



NEW PRODUCT

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter		Ratings	Units
ESD HBM	Human Body ESD Protection		2000	V
ESD MM	Machine Model ESD Protection		200	V
V_{IN}	Input Voltage		6.0	V
V_{OUT}	Output Voltage		6.0	V
V_{EN}	Enable Voltage		6.0	V
I_L	Load Current		4.0	A
$T_{J(max)}$	Maximum Junction Temperature		+125	°C
T_{ST}	Storage Temperature		-55 to +150	°C
P_D	Power Dissipation	(Note 5)	0.35	W
		(Note 6)	1.42	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 5)	290	°C/W
		(Note 6)	71	
$R_{\theta JC}$	Thermal Resistance, Junction to Case		8.5	°C/W

Notes:
4. Stresses greater than the 'Absolute Maximum Ratings' specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. For a device surface mounted on minimum recommended pad layout, in still air conditions; the device is measured when operating in a steady state condition.
6. For a device surface mounted on 25mm by 25mm by 1.6mm FR4 PCB with high coverage of single sided 2oz copper, in still air conditions; the device is measured when operating in a steady state condition.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Units
V_{IN}	Input Voltage Range	1.5	5.5	V
V_{EN}	Enable Voltage Range	0	5.5	V
V_{PG}	Power Good Voltage Range	0	5.5	V
T_A	Operating Ambient Temperature	-40	+85	°C

NEW PRODUCT

Electrical Characteristics (@T_A = +25°C, C_{IN} = 1µF, C_L = 100nF, unless otherwise specified.)

V_{IN} = 5.0V						
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
I_{IN_Q}	Input Quiescent Current	V_{EN} = V_{IN}, I_{OUT} = 0A	–	21	35	µA
I_{IN_SD}	Input Shutdown Current	V_{EN} = 0V, I_{OUT} = 0A, R_{DIS} = 240Ω	–	0.05	0.5	µA
$R_{DS(ON)}$	Load Switch On-Resistance	V_{EN} = V_{IN}, I_{OUT} = −1A	–	16	21	mΩ
V_{IH_EN}	EN Input Logic High Voltage	–	1.0	–	–	V
V_{IL_EN}	EN Input Logic Low Voltage	–	–	–	0.5	V
I_{LEAK_EN}	EN Input Leakage	V_{EN} = V_{IN}	–	–	0.1	µA
R_{DS_DIS}	Discharge FET On-Resistance	V_{EN} = 0V, I_{DIS} = 10mA	–	4	6	Ω
V_{OL_PG}	Power Good Output Low Level	I_{OL_PG} = 100µA, V_{EN} = 0V	–	–	0.2	V
I_{OZ_PG}	Power Good High-Impedance Current	V_{PG} = V_{IN}, V_{EN} = V_{IN}	–	–	0.05	µA
t_{RISE}	Output Rise Time	R_L = 10Ω, C_{SS} = 10nF	–	130	–	µs
t_{ON}	Output Turn-ON Delay Time	R_L = 10Ω, C_{SS} = 10nF	–	90	–	µs
t_{FALL}	Output Fall Time	R_L = Open, R_{DIS} = 240Ω, C_{SS} = 10nF	–	55	–	µs
t_{OFF}	Output Turn-OFF Delay Time	R_L = Open, R_{DIS} = 240Ω, C_{SS} = 10nF	–	21	–	µs
t_D	Output Start Delay Time	R_L = 10Ω, C_{SS} = 10nF (Note 7)	–	20	–	µs
t_{PG}	Power Good Delay Time	R_L = 10Ω, C_{SS} = 10nF	–	410	–	µs

V_{IN} = 3.3V						
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
I_{IN_Q}	Input Quiescent Current	V_{EN} = V_{IN}, I_{OUT} = 0A	–	13	23	µA
I_{IN_SD}	Input Shutdown Current	V_{EN} = 0V, I_{OUT} = 0A, R_{DIS} = 240Ω	–	0.04	0.2	µA
$R_{DS(ON)}$	Load Switch On-Resistance	V_{EN} = V_{IN}, I_{OUT} = −1A	–	17	22	mΩ
V_{IH_EN}	EN Input Logic High Voltage	–	1.0	–	–	V
V_{IL_EN}	EN Input Logic Low Voltage	–	–	–	0.5	V
I_{LEAK_EN}	EN Input Leakage	V_{EN} = V_{IN}	–	–	0.1	µA
R_{DS_DIS}	Discharge FET On-Resistance	V_{EN} = 0V, I_{DIS} = 10mA	–	5	8	Ω
V_{OL_PG}	Power Good Output Low Level	I_{OL_PG} = 100µA, V_{EN} = 0V	–	–	0.2	V
I_{OZ_PG}	Power Good High-Impedance Current	V_{PG} = V_{IN}, V_{EN} = V_{IN}	–	–	0.05	µA
t_{RISE}	Output Rise Time	R_L = 10Ω, C_{SS} = 10nF	–	130	–	µs
t_{ON}	Output Turn-ON Delay Time	R_L = 10Ω, C_{SS} = 10nF	–	90	–	µs
t_{FALL}	Output Fall Time	R_L = Open, R_{DIS} = 240Ω, C_{SS} = 10nF	–	55	–	µs
t_{OFF}	Output Turn-OFF Delay Time	R_L = Open, R_{DIS} = 240Ω, C_{SS} = 10nF	–	21	–	µs
t_D	Output Start Delay Time	R_L = 10Ω, C_{SS} = 10nF (Note 7)	–	25	–	µs
t_{PG}	Power Good Delay Time	R_L = 10Ω, C_{SS} = 10nF	–	340	–	µs

NEW PRODUCT

Electrical Characteristics (Cont. @ T_A = +25°C, C_{IN} = 1µF, C_L = 100nF, unless otherwise specified.)

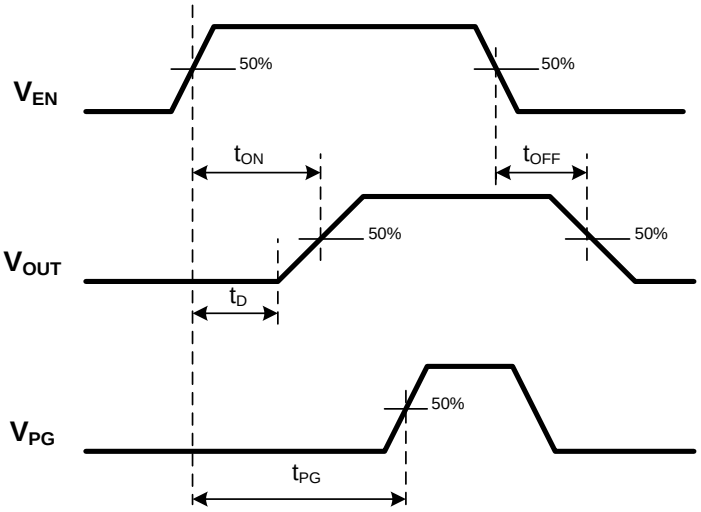
V_{IN} = 2.5V						
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
I_{IN_Q}	Input Quiescent Current	V_{EN} = V_{IN}, I_{OUT} = 0A	–	11	19	µA
I_{IN_SD}	Input Shutdown Current	V_{EN} = 0V, I_{OUT} = 0A, R_{DIS} = 240Ω	–	0.04	0.2	µA
$R_{DS(ON)}$	Load Switch On-Resistance	V_{EN} = V_{IN}, I_{OUT} = −1A	–	19	24	mΩ
V_{IH_EN}	EN Input Logic High Voltage	–	1.0	–	–	V
V_{IL_EN}	EN Input Logic Low Voltage	–	–	–	0.5	V
I_{LEAK_EN}	EN Input Leakage	V_{EN} = V_{IN}	–	–	0.1	µA
R_{DS_DIS}	Discharge FET On-Resistance	V_{EN} = 0V, I_{DIS} = 10mA	–	6	9	Ω
V_{OL_PG}	Power Good Output Low Level	I_{OL_PG} = 100µA, V_{EN} = 0V	–	–	0.2	V
I_{OZ_PG}	Power Good High-Impedance Current	V_{PG} = V_{IN}, V_{EN} = V_{IN}	–	–	0.05	µA
t_{RISE}	Output Rise Time	R_L = 10Ω, C_{SS} = 10nF	–	125	–	µs
t_{ON}	Output Turn-ON Delay Time	R_L = 10Ω, C_{SS} = 10nF	–	95	–	µs
t_{FALL}	Output Fall Time	R_L = Open, R_{DIS} = 240Ω, C_{SS} = 10nF	–	56	–	µs
t_{OFF}	Output Turn-OFF Delay Time	R_L = Open, R_{DIS} = 240Ω, C_{SS} = 10nF	–	21	–	µs
t_D	Output Start Delay Time	R_L = 10Ω, C_{SS} = 10nF (Note 7)	–	30	–	µs
t_{PG}	Power Good Delay Time	R_L = 10Ω, C_{SS} = 10nF	–	310	–	µs

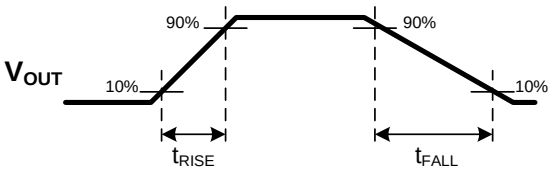
V_{IN} = 1.8V						
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
I_{IN_Q}	Input Quiescent Current	V_{EN} = V_{IN}, I_{OUT} = 0A	–	9	16	µA
I_{IN_SD}	Input Shutdown Current	V_{EN} = 0V, I_{OUT} = 0A, R_{DIS} = 240Ω	–	0.03	0.2	µA
$R_{DS(ON)}$	Load Switch On-Resistance	V_{EN} = V_{IN}, I_{OUT} = −1A	–	22	28	mΩ
V_{IH_EN}	EN Input Logic High Voltage	–	0.9	–	–	V
V_{IL_EN}	EN Input Logic Low Voltage	–	–	–	0.4	V
I_{LEAK_EN}	EN Input Leakage	V_{EN} = V_{IN}	–	–	0.1	µA
R_{DS_DIS}	Discharge FET On-Resistance	V_{EN} = 0V, I_{DIS} = 10mA	–	8	12	Ω
V_{OL_PG}	Power Good Output Low Level	I_{OL_PG} = 100µA, V_{EN} = 0V	–	–	0.2	V
I_{OZ_PG}	Power Good High-Impedance Current	V_{PG} = V_{IN}, V_{EN} = V_{IN}	–	–	0.05	µA
t_{RISE}	Output Rise Time	R_L = 10Ω, C_{SS} = 10nF	–	130	–	µs
t_{ON}	Output Turn-ON Delay Time	R_L = 10Ω, C_{SS} = 10nF	–	100	–	µs
t_{FALL}	Output Fall Time	R_L = Open, R_{DIS} = 240Ω, C_{SS} = 10nF	–	56	–	µs
t_{OFF}	Output Turn-OFF Delay Time	R_L = Open, R_{DIS} = 240Ω, C_{SS} = 10nF	–	21	–	µs
t_D	Output Start Delay Time	R_L = 10Ω, C_{SS} = 10nF (Note 7)	–	40	–	µs
t_{PG}	Power Good Delay Time	R_L = 10Ω, C_{SS} = 10nF	–	300	–	µs

Note: 7. Guaranteed by design

NEW PRODUCT

Test Circuit and t_{ON}/t_{OFF} Waveforms

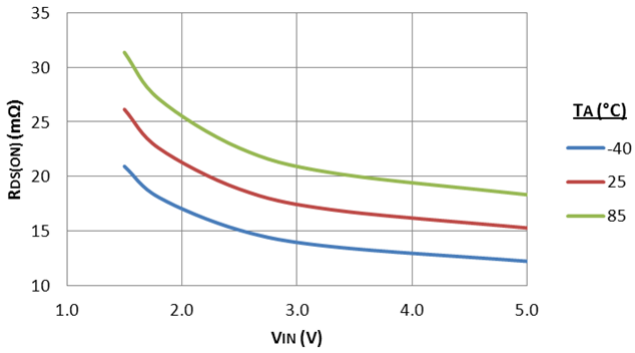




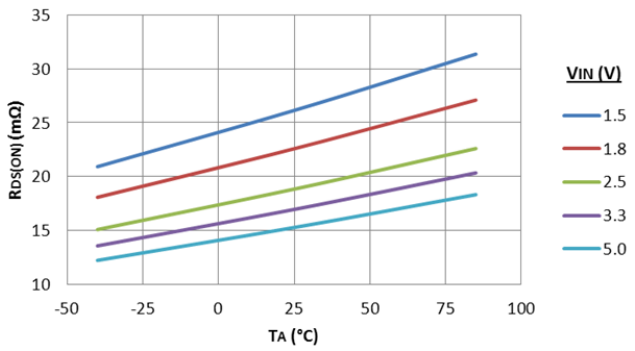
NEW PRODUCT

Performance Characteristics (@T_A = +25°C, V_{IN} = 5V, unless otherwise specified.)

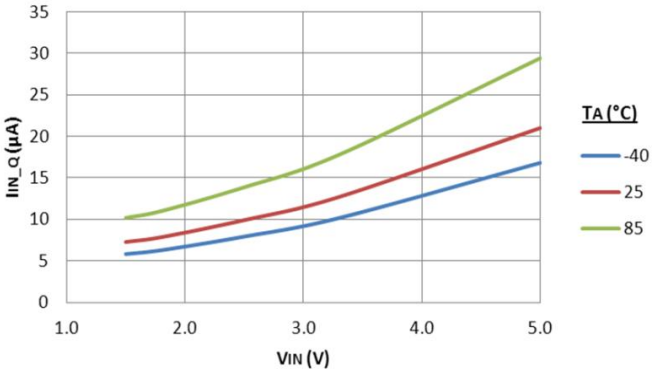
$R_{DS(ON)}$ vs. V_{IN} (I_{OUT}=200mA)



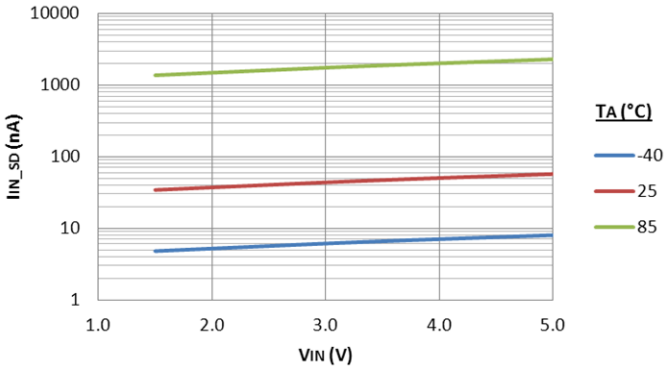
$R_{DS(ON)}$ vs. Ambient Temperature (I_{OUT}=200mA)



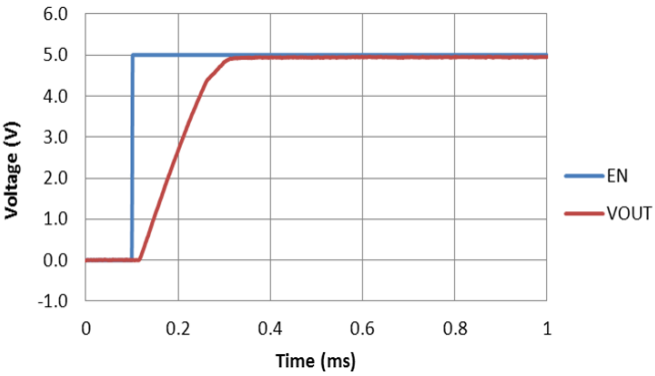
Input Quiescent Current vs. V_{IN}



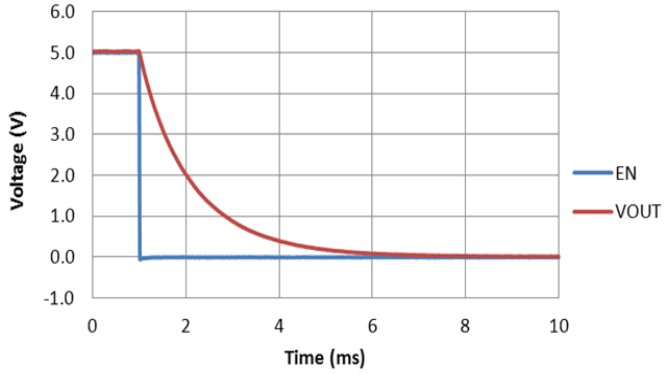
Input Shutdown Current vs. V_{IN}



Turn On Response Time
(V_{IN}=5V, T_A=+25°C, R_L=10Ω, C_{SS}=10nF, C_L=1μF, C_{IN}=1μF)



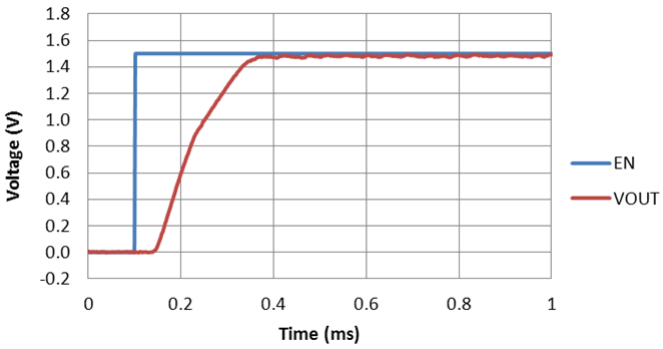
Turn Off Response Time
(V_{IN}=5V, T_A=+25°C, R_{DIS}=1kΩ, C_{SS}=10nF, C_L=1μF, C_{IN}=1μF)



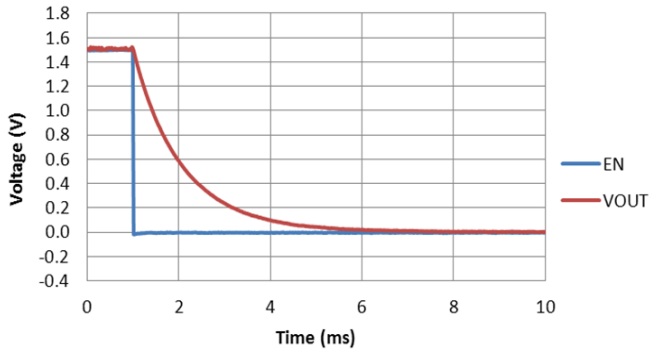
NEW PRODUCT

Performance Characteristics (Cont. @ T_A = +25°C, V_{IN} = 5V, unless otherwise specified.)

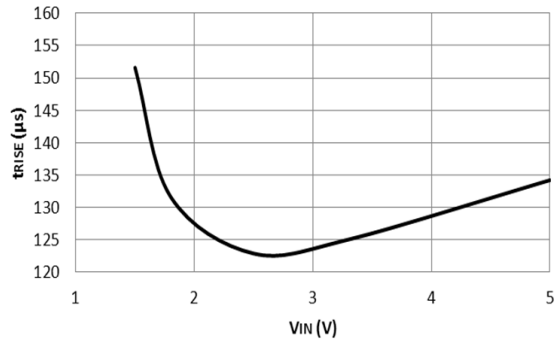
Turn On Response Time
(V_{IN}=1.5V, R_L=10Ω, C_{SS}=10nF, C_L=1μF, C_{IN}=1μF)



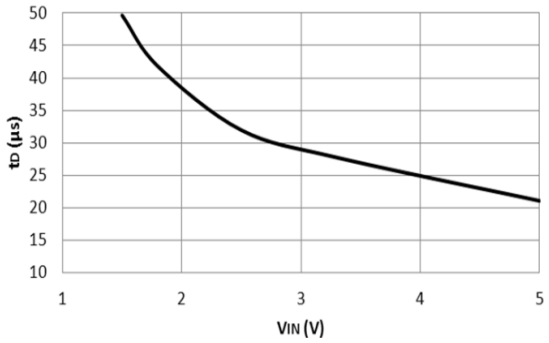
Turn Off Response Time
(V_{IN}=1.5V, T_A=+25°C, R_{DIS}=1kΩ, C_{SS}=10nF, C_L=1μF, C_{IN}=1μF)



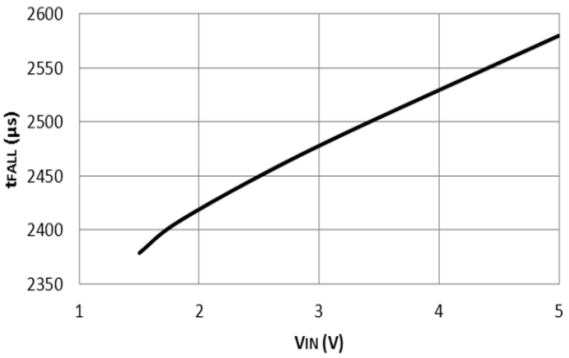
t_{RISE} vs. V_{IN}
(T_A=+25°C, R_L=10Ω, C_{SS}=10nF, C_L=1μF, C_{IN}=1μF)



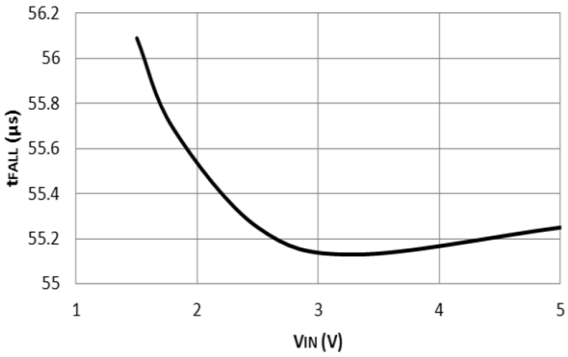
t_D vs. V_{IN}
(T_A=+25°C, R_L=10Ω, C_{SS}=10nF, C_L=1μF, C_{IN}=1μF)



t_{FALL} vs. V_{IN}
(T_A=+25°C, R_{DIS}=1kΩ, C_{SS}=10nF, C_L=1μF, C_{IN}=1μF)



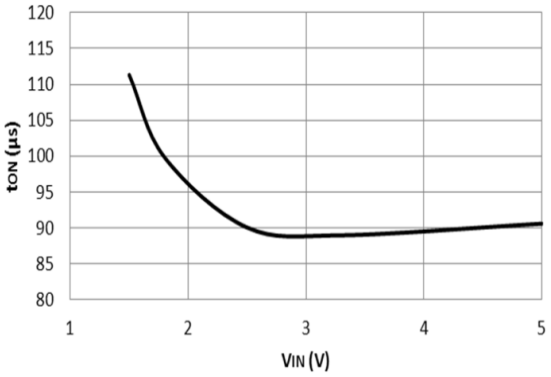
t_{FALL} vs. V_{IN}
(T_A=+25°C, R_{DIS}=240Ω, C_{SS}=10nF, C_L=0.1μF, C_{IN}=1μF)



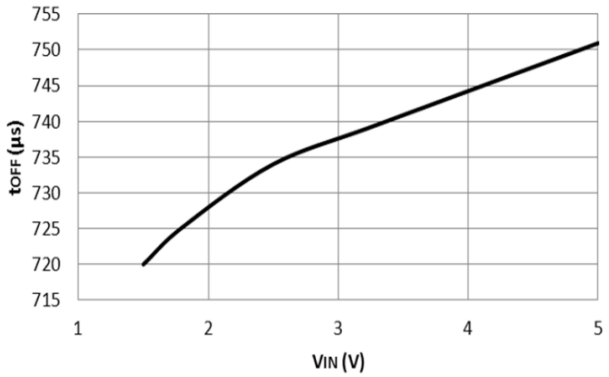
NEW PRODUCT

Performance Characteristics (Cont. @ T_A = +25°C, V_{IN} = 5V, unless otherwise specified.)

t_{ON} vs. V_{IN}
(T_A=+25°C, R_L=10Ω, C_{SS}=10nF, C_L=1µF, C_{IN}=1µF)



t_{OFF} vs. V_{IN}
(T_A=+25°C, R_{DIS}=1kΩ, C_{SS}=10nF, C_L=1µF, C_{IN}=1µF)



Application Information

Theory of Operation

The AP22800 is a load switch that can be used to isolate or power-down part of a system in order to reduce power consumption, particularly in battery-powered devices. The NMOS pass element in the AP22800 is turned on when EN pin is pulled high. This enables the internal charge pump, which then increases the voltage on the SS pin and provides an overdrive on the gate of the N-channel pass switch.

When the voltage on the gate of the pass switch is around 1.6 times greater than VIN, power is deemed to be good, and the Power Good (PG) output is pulled high via an external pull-up resistor. The rise-time of the switch is controlled by the value of the capacitor on the SS pin.

When EN is pulled low, the NMOS pass switch turns off and isolates VOUT from VIN. In addition, PG is pulled to ground to indicate that the power is no longer good. The DIS pin keeps VOUT grounded while EN is low. The fall time on VOUT is largely controlled by the value of the discharge resistor and the capacitance on the output.

Input and Output Voltage

The Input Voltage (VIN) should be between 1.5V and 5.5V. With the switch activated, the Output Voltage (VOUT) will be the input voltage minus the voltage drop across the device.

Enable

The GPIO compatible EN input allows the output current to be switched on and off. A high signal (switch on) should be at least 1V, and a low signal (switch off) no higher than 0.5V. The EN pin should not be left floating. It is advisable to hold EN low when applying or removing power.

Power Good

The PG output is an open drain output that indicates when the pass switch is enhanced enough to deliver current to the load. When the gate voltage rises to VIN × 1.6, PG is pulled high via the external pull-up resistor. For example, if V_{IN} = 5V, then PG goes high when the gate voltage of the pass switch reaches 8V, thus, providing an overdrive of 3V. PG is pulled low when power is deemed not to be good.

PG can be pulled up to any voltage to a maximum of 5.5V, although it is recommended to utilize VOUT with a resistor greater than 50kΩ. The advantage of pulling up PG to VOUT is that when EN is low, VOUT is also grounded. Thus, no power is wasted in the pull-up resistor.

If this feature is not required, then PG pin can be left floating.

Input and Output Capacitors

The input and output capacitors should be placed as close to VIN and VOUT pins as possible. The output capacitor should not be greater than the input capacitor, otherwise, current may flow backwards through the device after turn off. Typically, a 10µF input capacitor and a 1µF output capacitor should be placed close to VIN and VOUT pins.

NEW PRODUCT

Application Information (Cont.)

For heavier loads, it is recommended that the VIN and VOUT trace lengths be kept to a minimum. In addition, a bulk capacitor (≥ 10µF) may also be placed close to the VOUT pin. If using a bulk capacitor on VOUT, it is important to control the inrush current by choosing an appropriate soft-start time in order to minimize the droop on the input supply.

Adjustable Slew Rate/Soft-Start

The SS pin allows the output ramp time of the switch to be controlled using an external capacitor (C_{SS}). The capacitor voltage rises to approximately twice the value of VIN. Table 1 shows typical rise times (in µs) associated with various timing capacitors at different VIN values.

Output Voltage Rise Time (in µs) Measured at +25°C Using 0805 X7R 10% 25V Ceramic Capacitors				
V_{IN}	**1.8V**	**2.5V**	**3.3V**	**5.0V**
V_{SS} / C_{SS}	**3.5V**	**4.8V**	**6.4V**	**9.7V**
470pF	6.9	7.0	7.1	7.3
1nF	12.0	12.1	12.3	14.3
10nF	120	127	135	145
47nF	626	636	652	692
100nF	1305	1320	1340	1420
470nF	6320	6400	6660	7020
1000nF	13400	13040	13120	13800

Table 1. Timing Capacitors and Rise Times

Extra capacitance will allow further increase in rise time if desired. The timing capacitor should have a breakdown voltage of at least 25V to allow for a high voltage on this pin.

Adjustable Discharge

When EN goes low, VOUT is discharged to ground through the discharge resistor (R_{DIS}). The discharge/fall time on VOUT is largely controlled by R_{DIS} and by the output capacitor. The data in Table 2 shows typical fall times associated with various discharge resistors with C_L = 1µF, for different values of V_{IN}.

1206 250mW 1% Discharge Resistor (Ω)	**Fall Time (in ms) Measured at +25°C, with C_L = 1µF, R_L = Open**			
	1.8V	**2.5V**	**3.3V**	**5V**
100	0.25	0.26	0.26	0.27
470	1.07	1.09	1.12	1.18
1000	2.28	2.32	2.40	2.54
4700	10.42	10.65	10.90	11.50
10000	23.33	24.30	24.50	25.05

Table 2. Discharge Resistors and Output Voltage Fall Times

NEW PRODUCT

Board Layout and Thermal Considerations

Due to the high current capacity of the load switch, PCB layout needs to ensure good thermal distribution during operation. The top and bottom of AP22800EV1, the evaluation board for the AP22800, can be seen below.

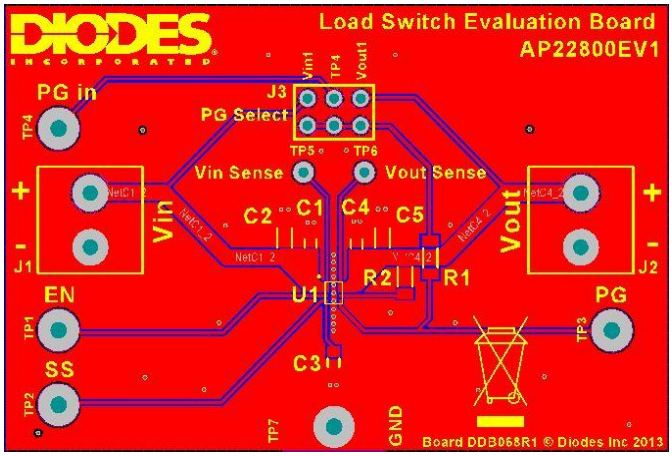


Figure 1. PCB Copper Layout & Silk Screen – Top

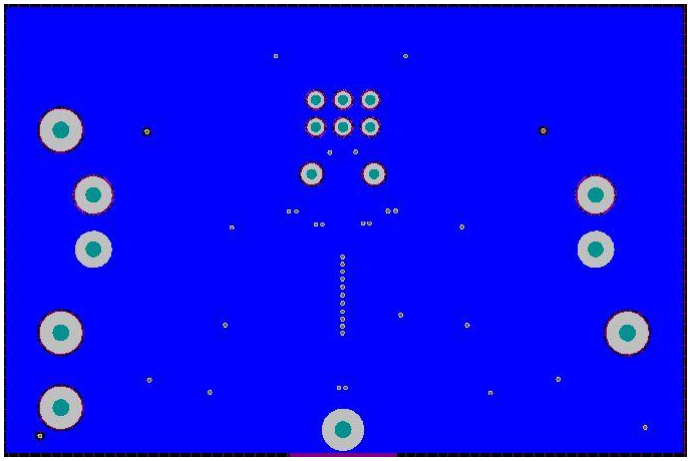


Figure 2. PCB Copper Layout & Silk Screen – Bottom

Thermal vias are used directly underneath the chip to help distribute the heat from the device. The ground plane on the underside of the board effectively acts as a large heatsink. The widths of the tracks carrying VIN and VOUT are kept wide. Vias are also distributed around the board to aid thermal conduction and to ensure a consistent potential, particularly around the ground connections of the capacitors. All capacitors used are located as close as possible to the AP22800 to minimize any parasitic effects.

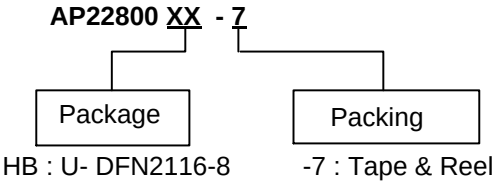
The maximum junction temperature of the AP22800 is +125°C. To ensure that this is not exceeded, the following equation can be used to give an approximation of junction temperature. Temperature readings taken with a thermal camera can also give a good approximation of power dissipation with the use of this equation. The board layout has a major influence on the parameter θ_{JA}.

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where, T_J = Junction temperature (°C)
T_A = Ambient temperature (°C)
θ_{JA} = Junction to ambient thermal impedance (°C/W)
P_D = Power dissipation (voltage drop across device × output current) (W)

NEW PRODUCT

Ordering Information

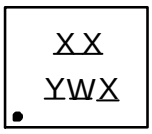


Part Number	Package Code	Packaging	7" Tape and Reel	
			Quantity	Part Number Suffix
AP22800HB-7	HB	U-DFN2116-8	3000/Tape & Reel	-7

Marking Information

U-DFN2116-8

(Top View)



XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 Week;
a~z : 27~52 Week; z Represents
52 and 53 Week
X : Internal Code

Part Number	Package	Identification Code
AP22800HB-7	U-DFN2116-8	WA

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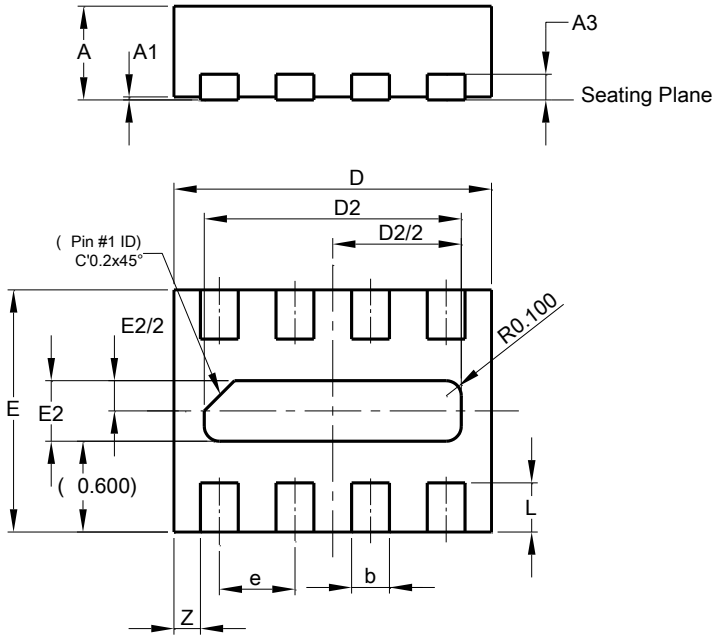
Package Outline Dimensions (All dimensions in mm.)

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

(1) Package Type: U-DFN2116-8

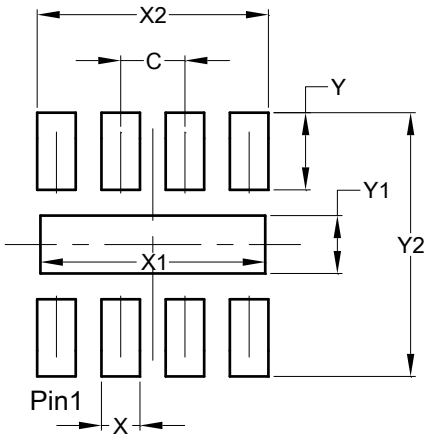


U-DFN2116-8			
Dim	**Min**	**Max**	**Typ**
A	0.545	0.605	0.575
A1	0.000	0.050	0.020
A3	-	-	0.130
b	0.200	0.300	0.250
D	2.050	2.175	2.100
D2	1.600	1.800	1.700
E	1.550	1.675	1.600
E2	0.300	0.500	0.400
e	-	-	0.500
L	0.275	0.375	0.325
Z	-	-	0.175
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

(1) Package Type: U-DFN2116-8



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	1.750
X2	1.800
Y	0.600
Y1	0.450
Y2	2.050

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