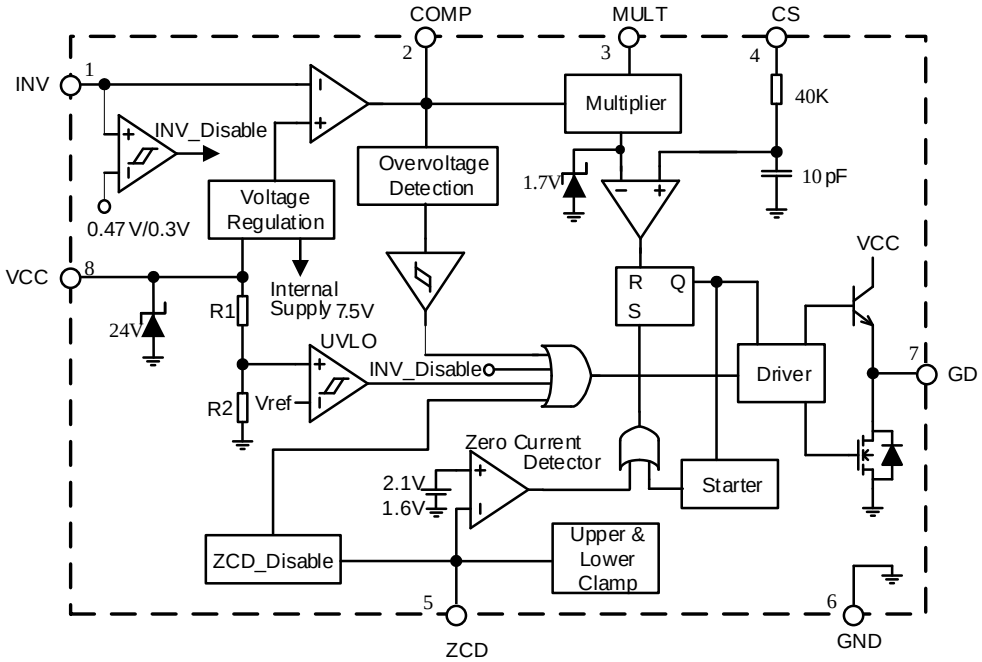
NEW PRODUCT

Pin Descriptions

Pin Number	Pin Name	Brief Description
1	INV	Inverting Input Pin of the Internal Error Amplifier. This pin is connected externally via a resistor divider from the regulated output voltage. It can provide input to inverting input of internal error amplifier. This pin can also be used as ENABLE/DISABLE control input.
2	COMP	Output from Error Amplifier. A feedback compensation network consisting of resistor and capacitor connects between INV (Pin1) and this pin to reduce the bandwidth and achieve stability of the voltage control loop and ensure high power factor and low THD.
3	MULT	Input to the Internal Multiplier. This pin connects to the rectified mains voltage through external resistor divider to provide a sinusoidal voltage reference for the control current loop.
4	CS	Current Sense Connecting to External Resistor for Current Feedback. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference generated by the multiplier to determine MOSFET's turn-off. This pin has an internal Leading-Edge-Blanking of about 200 nanoseconds to improve noise immunity.
5	ZCD	Zero Current Detection. This pin takes input from inductor's demagnetization sensing to achieve zero current detection, required for Transition Mode (TM) operation. A negative-going edge triggers turn-on of MOSFET.
6	GND	System Ground. Ground for circuit. Current return for both the signal circuitry and the gate drive stage.
7	GD	Gate Driver Output. This pin is able to drive external MOSFET. The totem-pole output stage is able to drive MOSFET with a peak current of 600mA/800mA for source and sink capability respectively. The high level voltage of this pin is internally clamped at about 12V to avoid excessive gate voltage in case V_{CC} pin is supplied by a higher voltage.
8	V_{CC}	System Power Input Pin. This pin is for supply voltage of both the signal part and gate driver of the IC. Upper limit is extended to a maximum of 22V to provide more headroom for supply voltage changes. This pin has an internal 25V Zener to protect the IC itself from overvoltage transients.

Functional Block Diagram



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Absolute Maximum Ratings (Note 4)

Symbol	Description	Value	Unit
V_{CC}	IC Supply Voltage	Self Limited	V
Icc	Operating Supply Current	30	mA
V_{INV},V_{COMP},V_{MULT}	Input/Output of Error Amplifier, Input of Multiplier	-0.3 to 7	V
I_{ZCD} (Note 5)	Zero Current Detector Max. Current	Source: -50 Sink: 10	mA mA
ESD(HBM)	ESD (Human Body Model)	3000	V
ESD(MM)	ESD (Machine Model)	200	V
T_J	Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
P_{TOT}	Power Dissipation	0.65	W
$R_{\theta JA}$	Thermal Resistance (Junction – Ambient)	150	°C/W
T_{LEAD}	Lead Temperature (Soldering, 10 sec)	+260	°C

Notes: 4. Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

5. Currents flowing into device pins are considered as positive and out of device pins are considered as negative.

NEW PRODUCT

Electrical Characteristics

(Over recommended operating conditions unless otherwise specified V_{CC} = 12.0V, T_J = -25°C to +125°C, C_O = 1nF)

Symbol	Parameter	Conditions	Min	Typ.	Max	Units
SUPPLY VOLTAGE						
V_{CC}	IC Supply Voltage	After turn-on	10.3	—	22	V
$V_{CC\ ON}$	Turn-On Threshold	—	11.0	12.0	13.0	V
$V_{CC\ OFF}$	Turn-Off Threshold	—	8.7	9.5	10.3	V
V_{CC-HYS}	Hysteresis	—	2.2	2.5	2.8	V
V_Z	Zener Voltage	I_{CC} = 20 mA	22	24	—	V
SUPPLY CURRENT						
$I_{start-up}$	Start-Up Current	Before turn-on, V_{CC}=11V	—	40	70	µA
I_Q	Quiescent Current	After turn-on	—	2.5	3.75	mA
I_{CC}	Operating Supply Current	@ 70kHz In OVP condition, V_{INV} = 2.7V	— —	3.5 1.4	5 2.2	mA mA
I_Q	Quiescent Current	V_{ZCD}≤150mV, V_{CC}>V_{CC-OFF} V_{ZCD}≤150mV, V_{CC}<V_{CC-OFF}	 20	 50	2.2 90	mA µA
ERROR AMPLIFIER						
V_{INV}	Voltage Feedback Input Threshold	T_J = +25°C 10.3V < V_{CC} < 22V	2.465 2.44	2.5 —	2.535 2.56	V
	Line Regulation	V_{CC} = 10.3V to 22V (Note 6)	—	2	5	mV
I_{INV}	Input Bias Current	V_{INV} = 0 to 3V	—	-0.1	-1	µA
G_V	Voltage Gain (Note 6)	OPEN LOOP	60	80	—	dB
GB	Gain-Bandwidth (Note 6)	—	—	1	—	MHz
I_{COMP}	Source Current	V_{COMP} = 4V, V_{INV} = 2.4V	-2	-4.0	-8	mA
	Sink Current	V_{COMP} = 4V, V_{INV} = 2.6V	2.5	4.5	—	mA
V_{COMP}	Upper Clamp Voltage	I_{SOURCE} = 0.5 mA	—	5.8	—	V
	Lower Clamp Voltage	I_{SINK} = 0.5 mA	2.1	2.25	2.4	V
V_{INVdis}	Disable Threshold (Note 6)	—	250	300	350	mV
V_{INVen}	Restart Threshold	—	400	480	600	mV
MULTIPLIER INPUT						
V_{MULT}	Linear Operation Range	—	0 - 3	0 – 3.5	—	V
$\frac{\Delta V_{CS}}{\Delta V_{MULT}}$	Output Maximum Slope	V_{MULT} = 0 to 0.5V, V_{COMP} = upper clamp	1.65	1.9	—	V/V
K	Gain (Note 7)	V_{MULT} = 1V,V_{COMP} = 4V	0.6	0.75	0.9	1/V
ZERO CURRENT DETECTOR						
V_{ZCDH}	Upper Clamp Voltage	I_{ZCD} = 3mA	4.7	5.2	6.1	V
V_{ZCDL}	Lower Clamp Voltage	I_{ZCD} = -3mA	0.3	0.65	1.0	V
V_{ZCDA}	Arming Voltage	Positive-going edge	—	2.1	—	V
V_{ZCDT}	Triggering Voltage	Negative-going edge	—	1.6	—	V
I_{ZCDb}	Input Bias Current	V_{ZCD} =1 to 4.5V	—	2	—	µA
I_{ZCDsrc}	Source Current Capability (Note 6)	—	-2.5	—	-10	mA
I_{ZCDsnk}	Sink Current Capability (Note 6)	—	3.0	—	—	mA
V_{ZCDdis}	Disable Threshold	—	150	200	250	mV
V_{ZCDhys}	Restart hysteresis Threshold	—	20	100	165	mV
I_{ZCDres}	Restart Current after Disable	V_{ZCD}<V_{DIS}, V_{CC}>V_{CC-OFF}	-80	-120	—	µA
STARTER						
t_{START}	Start Timer Period	—	75	130	300	µs

NEW PRODUCT

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT OVER-VOLTAGE						
I_{OVP}	Dynamic OVP Triggering Current	—	35	40	45	µA
VOVP_TH	Static OVP Threshold	—	2.1	2.25	2.4	V
CURRENT SENSE COMPARATOR						
I_{CS}	Input Bias Current	V_{CS} = 0	—	—	-1	µA
$td_{(H-L)}$	Delay to Output (Note 6)	—		200	350	ns
$V_{CS-clamp}$	Current Sense Clamp	V_{COMP} = upper clamp	1.6	1.7	1.8	V
$V_{CS-offset}$	Current Sense Offset	V_{MULT} = 0	—	30	—	mV
		V_{MULT} = 2.5V	—	5	—	
GATE DRIVER						
V_{OL}	Output Low Dropout Voltage	I_{GDsink} = 200 mA (Note 6)	—	0.9	1.9	V
V_{OH}	Output High Dropout Voltage	$I_{GDsource}$ = 200 mA (Note 6)	—	2.5	3.0	V
		$I_{GDsource}$ = 20 mA		2.0	2.8	V
t_f	Voltage Fall Time (Note 6)	—	—	30	70	ns
t_r	Voltage Rise Time (Note 6)	—	—	60	110	ns
V_{Oclamp}	Output Clamp Voltage	I_{SOURCE} = 5 mA, V_{CC} =20 V	9	11	13	V
Vos	UVLO Saturation	V_{CC} =0 V to V_{CCon}, I_{SINK} = 10 mA	—	—	1.1	V

Notes: 6. These parameters, although guaranteed by design, are not 100% tested in production.
7. The multiplier output is given by: current sense comparator O/P, $V_{CS} = k \times (V_{COMP} - 2.5V) \times V_{MULT}$.

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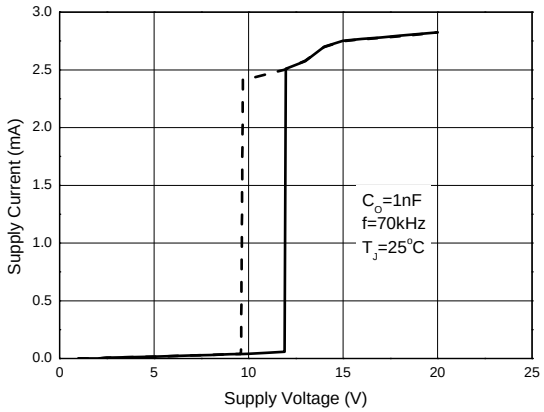
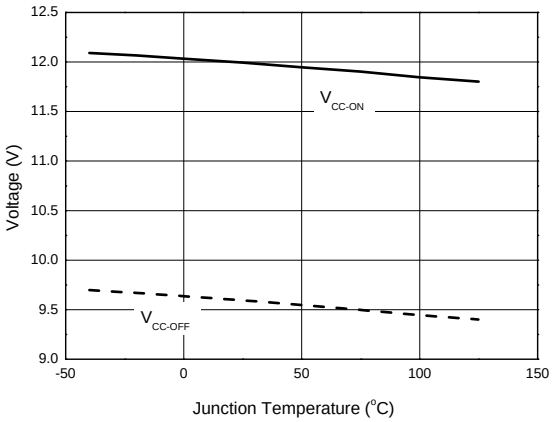
NEW PRODUCT

Performance Characteristics

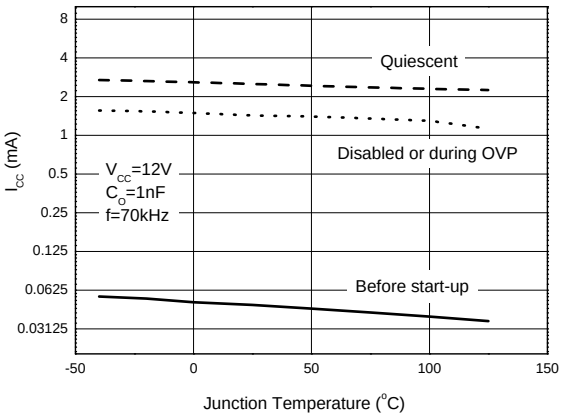
Supply Current vs. Supply Voltage



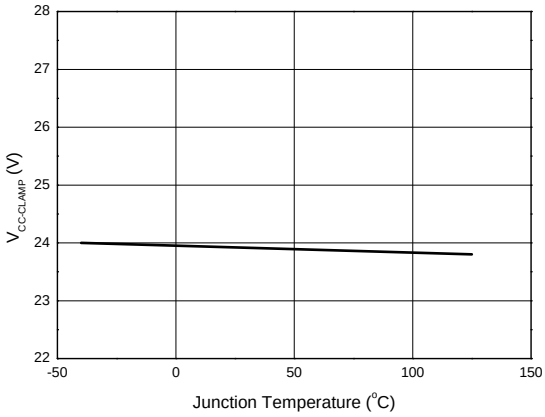
Start-up & UVLO Vs. T_J



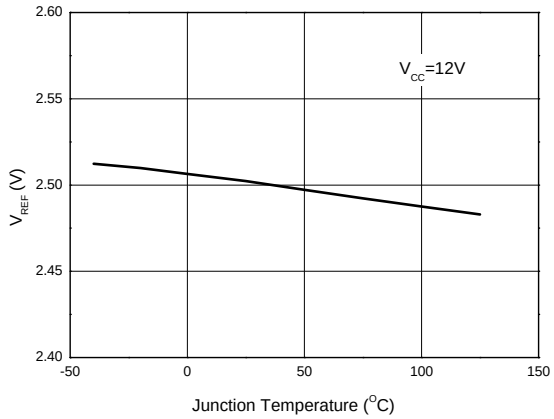
Icc Consumption vs.T_J



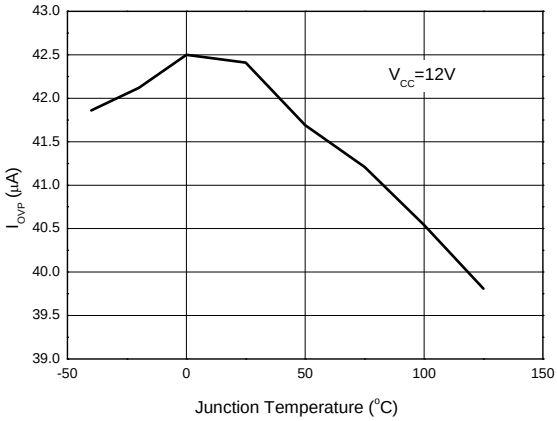
Vcc Zener Voltage Vs. T_J



Feedback Reference Voltage vs. T_J



OVP Current vs. T_J



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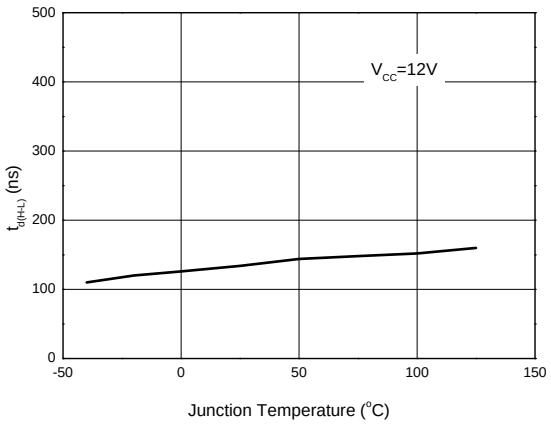
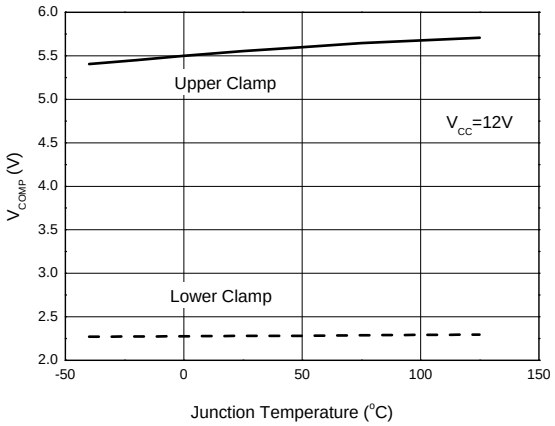
Performance Characteristics (cont.)

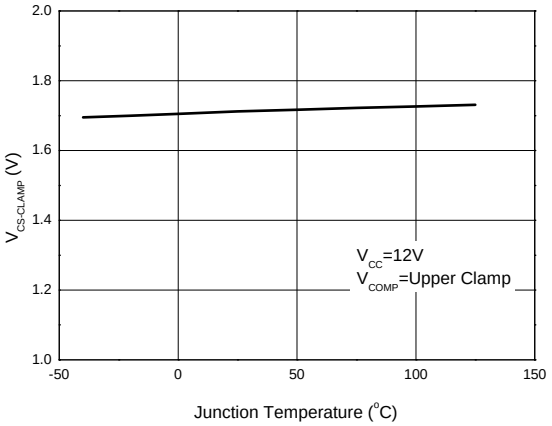
Delay-to-output vs.T_J



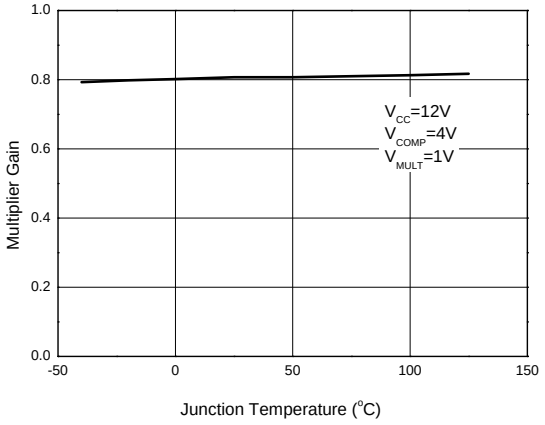
E/A Output Clamp Levels Vs. T_J



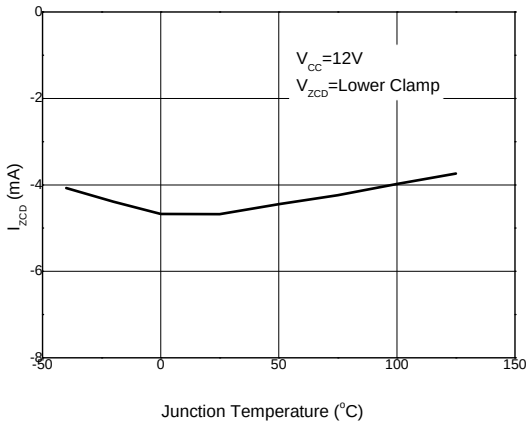
$V_{CS-CLAMP}$ vs.T_J



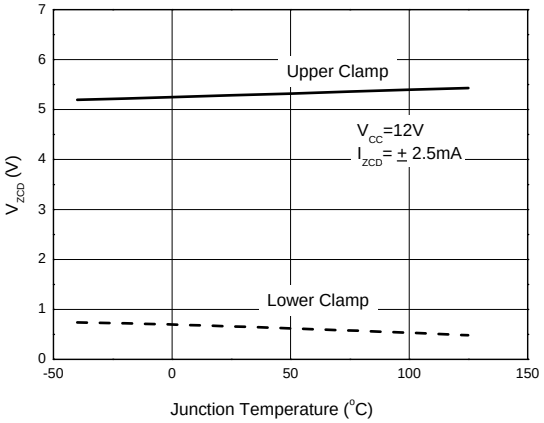
Multiplied Gain Vs. T_J



ZCD Source Capability vs.T_J



ZCD Clamp Levels Vs. T_J



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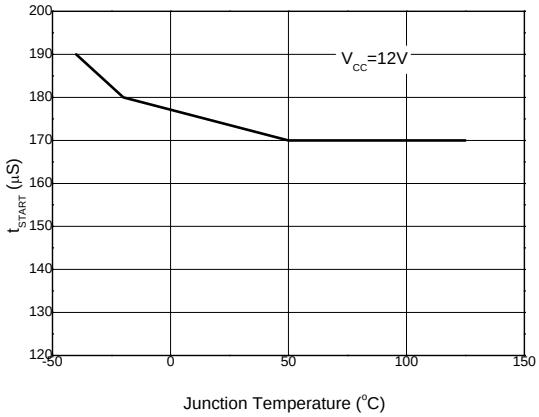
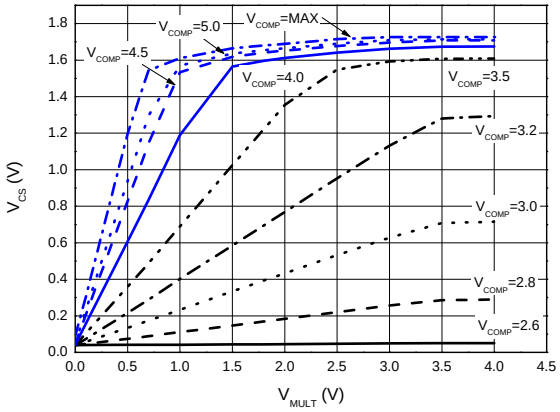
Performance Characteristics (cont.)

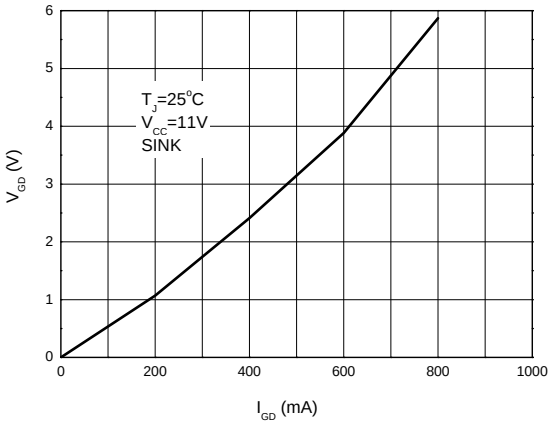
Start-up Timer vs.T_J



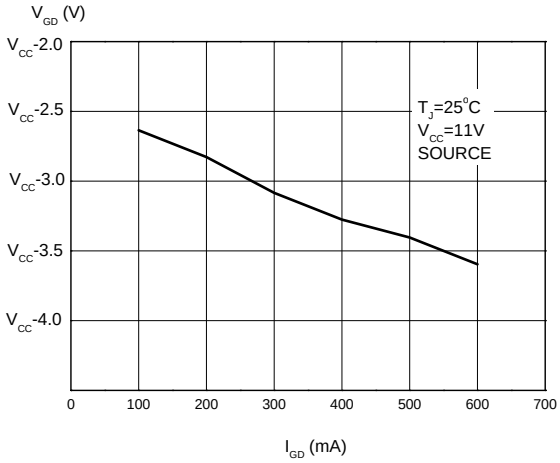
Multiplier Characteristics



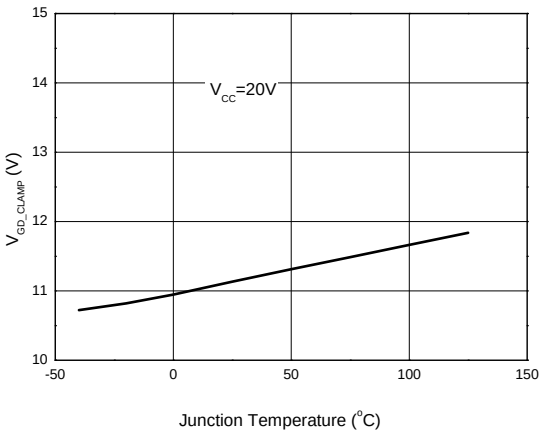
Gate-driver Output Low Saturation



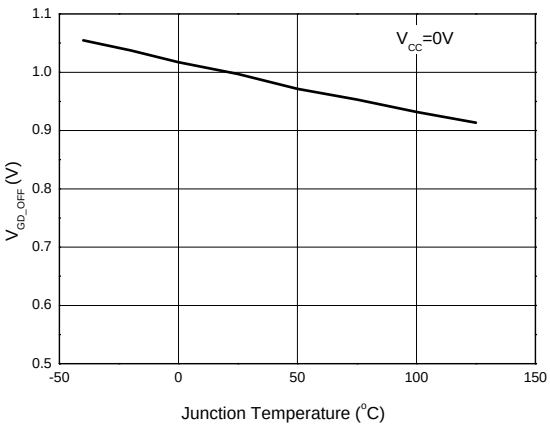
Gate-driver Output High Saturation



Gate-driver Clamp vs. TJ



UVLO Saturation vs. TJ



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Application Information

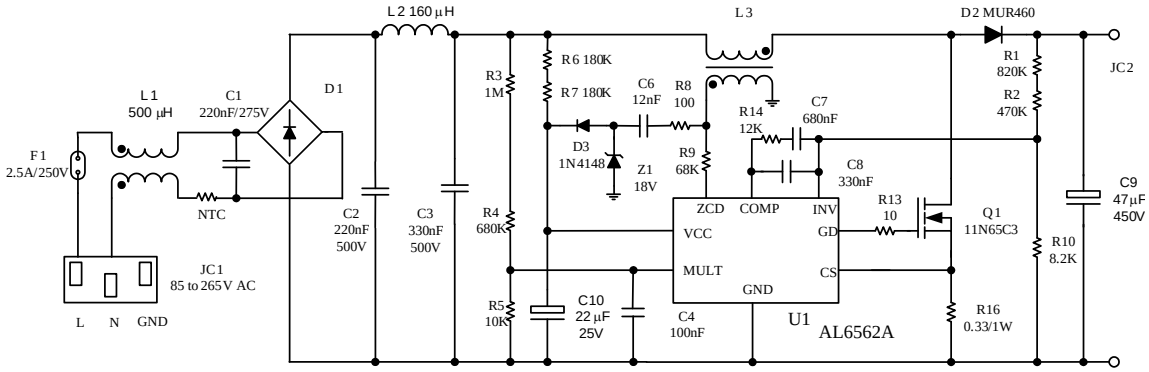


Figure 2 Boost Pre-Regulator PFC

POWER FACTOR CORRECTION

AL6562A functions as a transition mode PFC IC, meaning the MOSFET turns on when inductor current reaches zero, and turns off when the current meets desired input current reference voltage, as shown in Figure 3. A typical current waveform is depicted with envelope as shown, with the input current following that of the input voltage, achieving good power factor.

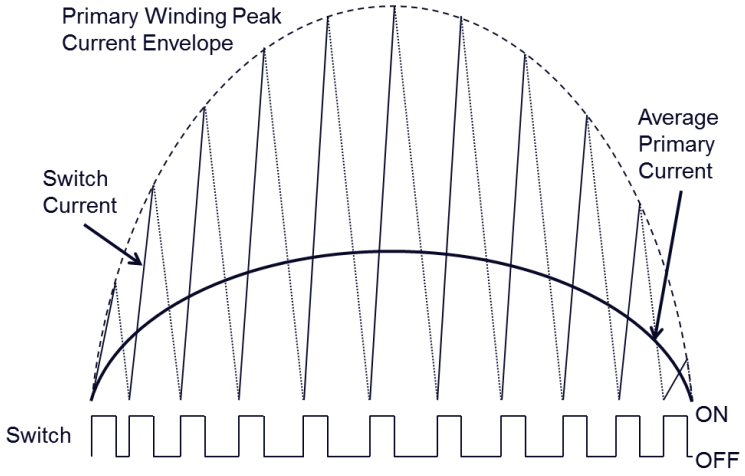


Figure 3 Typical Waveform of Inductor Current with Fixed ON Time

From a mathematical point of view, a PF value can be defined by:

$$PF = \cos(\theta) * k_D = \frac{\cos(\theta)}{\sqrt{1+\sum_2^{\infty}\left(\frac{I_{rms\_n}}{I_{rms\_1}}\right)^2}}$$

Where $\cos(\theta)$ represents displacement factor with θ as the displacement angle between voltage and current fundamentals, and k_D represents distortion respectively.

NEW PRODUCT

Application Information (cont.)

k_D, the distortion can further be defined by:

$$k_D = \frac{I_{rms\_1}}{I_{rms}} = \frac{I_{rms\_1}}{\sqrt{I_{rms\_2}^2 + I_{rms\_3}^2 + \ldots}}$$

Where I_{rms_1} and I_{rms_n} are the RMS (Root Mean Square) value n-th fundamental component of the current respectively. If the current and voltage are in phase, then θ= 0, which will lead to $\cos(\theta) = 1$, and the PF will be simplified as:

$$PF = k_D$$

ZCD (Zero Current Detection)

The ZCD feature detects when the transformer primary current falls to zero, as the voltage across the inductor reverses, to initiate a new cycle that switches on the power MOSFET. The signal for ZCD is obtained by an auxiliary winding on the boost inductor, as shown in Figure 2.

Multiplier

The internal multiplier takes two inputs, one from a portion of the instantaneous rectified line voltage (via pin 3, MULT) and the other from the output of the E/A (via pin 2, COMP), to feed the PWM comparator to determine the exact instant when the MOSFET is to be switched off. The output of multiplier is a rectified sinusoid, similar to the instantaneous rectified line voltage, multiplied by the scaling factor determined by output of the Error Amplifier. The MULT output is then fed into the PWM comparator and is compared to the current sense voltage V_{CS}, to switch the Power MOSFET off. The formula governing all parameters is given by:

Multiplier Output:

$$V_{CS} = k \times (V_{COMP} - 2.5V) \times V_{MULT}$$

Where: k is the multiplier gain. V_{MULT} is set by external resistors R1 and R2.

OVP (Output Overvoltage Protection)

The output voltage can be kept constant by the operation of the PFC circuit close to its nominal value, as shown by Figure 2, which is set by the ratio of the two external resistors R3 and R4. Neglecting ripple current, current flowing through R3, I_{R3}, will equal the current through R4, I_{R4}. As the non-inverting input of the error amplifier is biased inside the AL6562A at 2.5V, the current through R4 is:

$$I_{R4} = \frac{2.5}{R_4} = I_{R3} = \frac{V_O - 2.5}{R_3} \quad (1)$$

If any abrupt change of output voltage, $\Delta V_O > 0$ occurs due to a load drop, the voltage at pin INV will be kept at 2.5V by the local feedback of the EA. The network connected between INV and COMP introduces a time constant to achieve high PF. The current through R4 will remain equal to 2.5/R4, but I_{R3} will become:

$$I'_{R3} = \frac{V_O + \Delta V_O - 2.5}{R_3} \quad (2)$$

The difference current $\Delta I_{R3} = I'_{R3} - I_{R3} = \Delta V_O / R3$ will flow through the compensation network and enter the error amplifier output via pin COMP. The AL6562A monitors the current flowing into the error amplifier output pin. When the detected current is higher than 40μA, the dynamic OVP is triggered. The IC will be disabled and the driver signal will be stopped.

The output ΔVo that is able to trigger the Dynamic OVP function is then:

$$\Delta V_O = 40uA \times R3 \quad (3)$$

NEW PRODUCT

Application Information (cont.)

On the other hand, when the loading of PFC pre-regulator becomes low, the output voltage tends to stay steadily above the nominal value, which is not the case when OVP is triggered by abrupt voltage increase. If this occurs, the E/A will saturate low, the external power transistor is switched OFF, and the IC is put in idle state (static OVP). Normal operation is resumed as the error amplifier goes back into its linear region. As a result, the device will work in burst-mode, with a repetition rate that can be very low. When either OVP is activated, the quiescent consumption of the IC is reduced to minimum by the discharge of the capacitor and increases the hold-up capability of the IC supply.

THD (Total Harmonics Distortion)

The AL6562A reduces the THD by reducing conduction dead-angle occurring to the AC input current near the zero-crossings of the line voltage.

The important reason for this distortion to take place is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low, which is the case near line-voltage zero-crossing. This effect is magnified by the high-frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop.

To overcome this issue, the circuit section designed in the AL6562A forces the PFC regulator to process more energy near the line voltage zero-crossings, as compared to that commanded by the control loop. This results in both minimizing the time interval when energy transfer is lacking, and fully discharging the high-frequency filter capacitor after the bridge.

In essence, the circuit artificially increases the ON-Time of the Power Switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves towards the peak of the sinusoidal waveform.

Therefore, to maximize the benefit from the THD improvement circuit, the high-frequency filter capacitor after the bridge rectifier should be minimized and kept to satisfy the EMI filtering requirements.

Non-Latched IC Disable (Enable)

Pin 1, INV, inverting input to the error amplifier, doubles its function as a not-latched IC disable: a voltage below 0.3V shuts down the IC and reduces its consumption at a lower value. In order to restart the system, a voltage exceeding 0.48V must be applied. The main usage of this function is a remote ON/OFF control interface that can be driven by a PWM controller for power management purposes. However it also offers a certain degree of additional safety since it will make IC shutdown in case the lower resistor of the output divider is shorted to ground or if the upper resistor is missing or fails open.

NEW PRODUCT

Application Information (Cont.)

Single Stage LED Driver with PFC

One of the major applications of AL6562A is to provide a single stage power module with high PF for LED lighting. The following circuit, Figure 4, shows a simplified fly-back AC-DC converter with both CC and CV feedback from output side, to prevent overload and also provide an over-voltage protection facility.

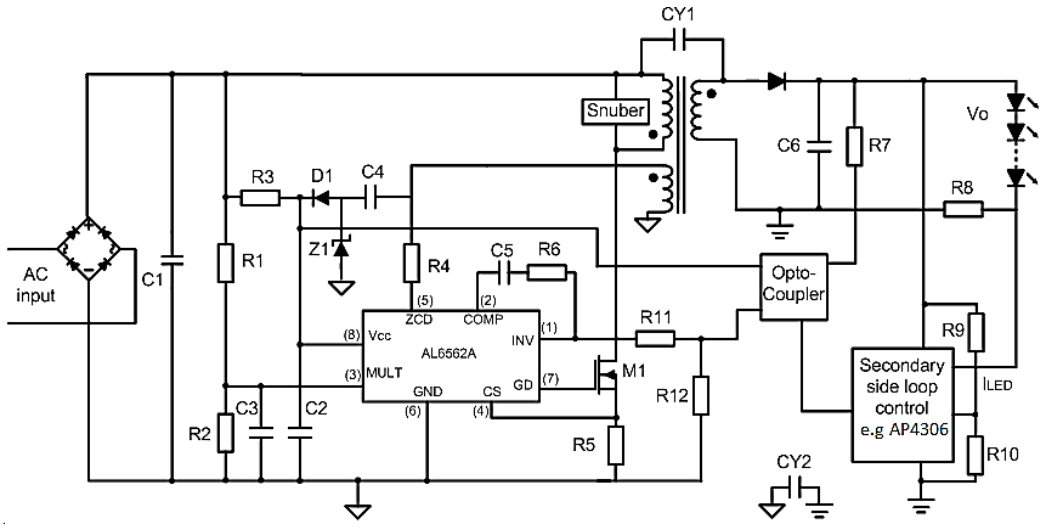


Figure 4 Single Stage PFC Isolated LED lighting

With its high performance, the AL6562A offers the following advantages that make this solution an appropriate method against the traditional PWM controller, where a good PF value is required:

- The input capacitance can be reduced to replace a bulky and expensive high-voltage electrolytic capacitor (as required by regular offline SMPS) by a small-size, cheaper film capacitor.
- Transition mode ensures low turn-on losses in MOSFET and higher efficiency can be achieved.
- Lower parts count means lower material cost, as well as lower assembly cost for limited space.

NEW PRODUCT

Application Information (Cont.)

PFC Pre-Regulator

Another major application of AL6562A is to implement a wide-range mains input PFC pre-regulator, which acts as the input stage for the cascaded DC-DC converter and can deliver above 350W in general.

The AL6562A can easily be implemented as PFC pre-regulator basing on fixed ON time mechanism due to its simplicity.
In fixed ON time mode, AL6562A is also working in transition mode where the inductor current will be turned on when zero crossing is detected.

By using boost-switching technique, the AL6562A shapes the input current by drawing a quasi-sinusoidal current in-phase with the line voltage. A simplified circuit, shown in Figure 5, explains the operation as follows:

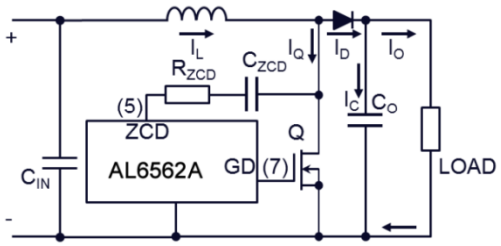


Figure 5 ZCD Pin Synchronization without Auxiliary Winding

The AC mains voltage is rectified by a diode bridge and delivered to the boost converter which boosts the rectified input voltage to a higher regulated DC bus V_O.

The error amplifier compares a portion of the output voltage with an internal reference and generates a signal error proportional to the difference between them. The bandwidth of the internal error amplifier is set to be narrow within 20Hz; the output would be a DC value over a given half-cycle. Output of E/A fed into multiplier, multiplied by a portion of the rectified mains voltage, will generate a scaled rectified sinusoid whose peak amplitude depends on the rectified mains peak voltage as well as the value of error signal.

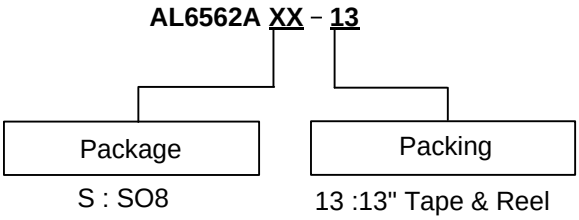
The output of the multiplier is fed into the non-inverting pin of the internal PWM comparator. As the output from the multiplier, a sinusoidal reference for PWM, equals the voltage on the current sense pin CS(4), the MOSFET will be turned off. As a consequence, the peak inductor current will follow the envelope of a rectified sinusoid. After the MOSFET is turned off, the boost inductor discharges its stored energy to the load until zero current is detected and then the MOSFET will be turned on again.

In the case where there is no auxiliary winding on the boost inductor, a solution can be implemented by sconnecting the ZCD pin to the drain of the power MOSFET through an R-C network: in this way the high-frequency edges experienced by the drain will be transferred to the ZCD pin, hence arming and triggering the ZCD comparator.

The resistance value must be properly chosen to limit the current sourced/sunk by the ZCD pin. In typical applications with output voltages around 400V, recommended values for these components are 22pF (or 33pF) for C_{ZCD} and 330K for R_{ZCD}. With these values proper operation is ensured even with a few volts difference between the regulated output voltage and the peak input voltage.

NEW PRODUCT

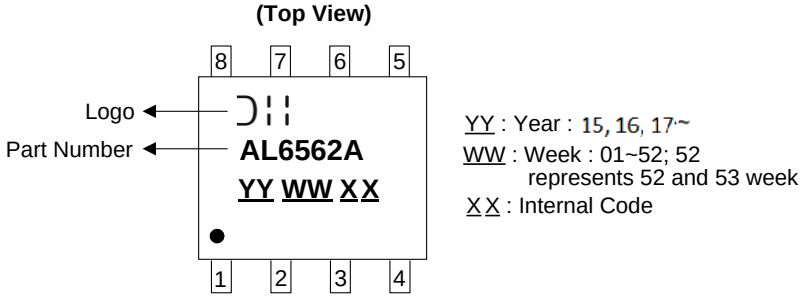
Ordering Information



Part Number	Package	Package code	13" Tape and Reel	
			Quantity	Part Number Suffix
AL6562AS-13	SO-8	S	2,500/Tape & Reel	-13

Marking Information

(1) SO-8



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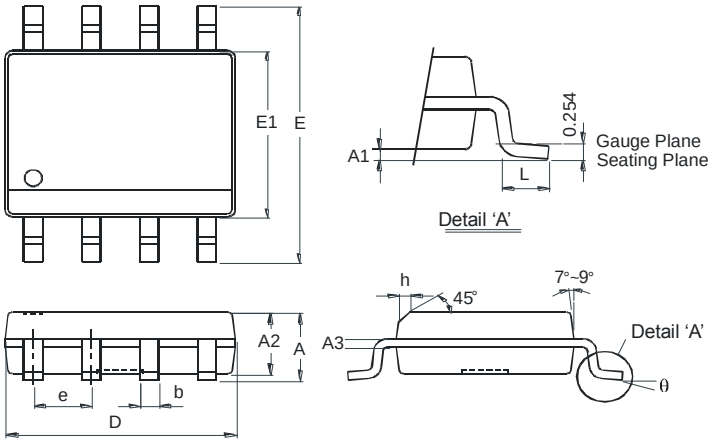
Package Outline Dimensions (All Dimensions in mm.)

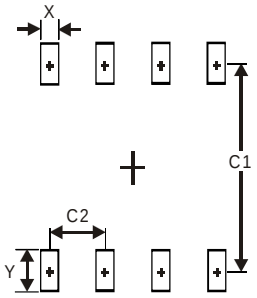
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.



SO-8		
Dim	**Min**	**Max**
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

NEW PRODUCT

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