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REVISION HISTORY

4/12—Rev. B: Initial Version

GENERAL DESCRIPTION

The ADV7844 is a high quality, single-chip, 4:1 multiplexed HDMI receiver and graphics digitizer with an integrated multiformat video decoder.

The ADV7844 incorporates a quad input HDMI-compatible receiver that supports all HDTV formats up to 1080p and display resolutions up to UXGA (1600 × 1200 at 60 Hz).

The ADV7844 incorporates Xpressview™ fast switching on all input HDMI ports. Using the Analog Devices, Inc., hardware-based HDCP engine that minimizes software overhead, Xpressview™ technology allows fast switching between any HDMI input ports in less than 1 second.

The ADV7844 supports all mandatory HDMI 3D TV formats in addition to all HDTV formats up to 1080p 36-bit Deep Color.

The ADV7844 also integrates an HDMI CEC controller that supports the capability discovery and control (CDC) feature.

The ADV7844 offers a flexible audio output port for the audio data decoded from the HDMI stream. HDMI audio formats, including super audio CD (SACD) via DSD and HBR are supported. The ADV7844 also features the audio return channel (ARC) feature. ARC simplifies cabling by combining upstream audio capability in a conventional HDMI cable.

Each HDMI port has dedicated 5 V detect and hot plug assert pins. The HDMI receiver also includes an integrated equalizer that ensures robust operation of the interface with cable lengths up to 30 meters. The HDMI receiver has advanced audio functionality, such as a mute controller, that prevents audible extraneous noise in the audio output.

The multiformat 3D comb filter decoder supports the conversion of PAL, NTSC, and SECAM standards in the form of a composite or an S-Video input signal into a digital ITU-R BT.656 format. SCART and overlay functionality are enabled by the ability of the ADV7844 to process CVBS and standard definition RGB signals simultaneously.

The ADV7844 contains one main component processor (CP), which processes YPbPr and RGB component formats, including RGB graphics. The CP also processes the video signals from the HDMI receiver. The ADV7844 can operate in quad HDMI and analog input mode, thus allowing for fast switching between the ADCs and HDMI.

The ADV7844 supports the decoding of a component RGB/YPbPr video signal into a digital YCbCr or RGB pixel output stream. The support for component video includes 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, and 1250i standards, as well as many other SMPTE and HD standards.

The ADV7844 supports graphics digitization. The ADV7844 is capable of digitizing RGB graphics signals from VGA to UXGA rates and converting them into a digital RGB or YCbCr pixel output stream. Internal EDID is available for one graphic port.

Fabricated in an advanced CMOS process, the ADV7844 is provided in a 19 mm × 19 mm, 425-ball, CSP BGA, surface-mount, RoHS-compliant package, and is specified over the 0°C to 70°C temperature range.

DETAILED FUNCTIONAL BLOCK DIAGRAM

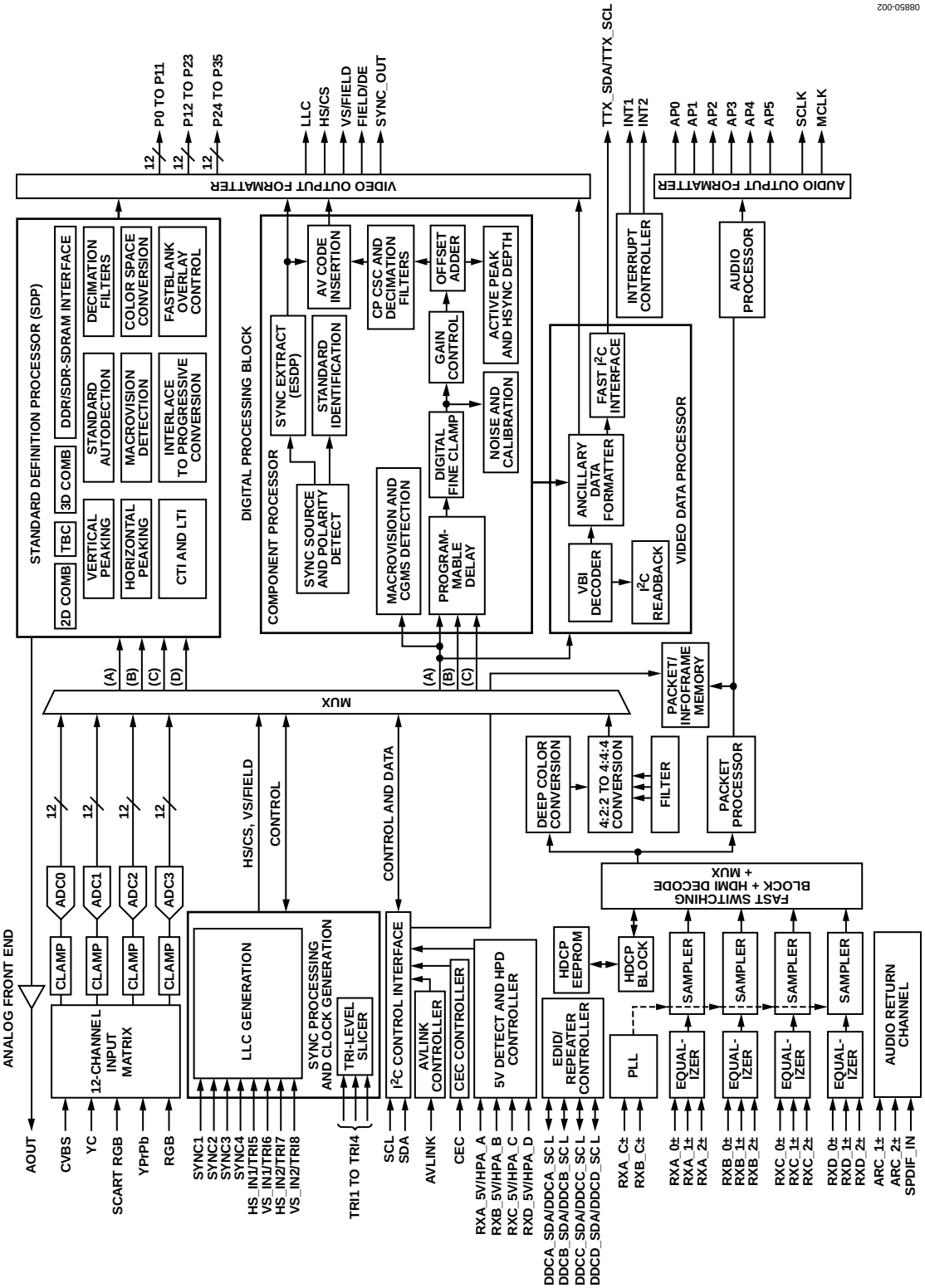


Figure 2. Detailed Functional Block Diagram

SPECIFICATIONS

AVDD = 1.8 V ± 5%, CVDD = 1.8 V ± 5%, DVDD = 1.8 V ± 5%, PVDD = 1.8 V ± 5%, DVDDIO = 3.3 V ± 5%, TVDD = 3.3 V ± 5%, VDD_SDRAM = 3.2 V to 3.4 V (SDR), VDD_SDRAM = 2.35 V to 2.65 V (DDR). T_{MIN} to T_{MAX} = 0°C to 70°C, unless otherwise noted.

ELECTRICAL CHARACTERISTICS

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE						
Resolution (Each ADC)	N				12	Bits
Integral Nonlinearity	INL	27 MHz (at a 12-bit level)		−3.0 to +8.0		LSB
		54 MHz (at a 12-bit level)		−3.0 to +8.0		LSB
		74.25 MHz (at a 12-bit level)		−4.0 to +7.0		LSB
		108 MHz (at a 11-bit level)		−3.5 to +8.0		LSB
		170 MHz (at a 9-bit level)		−0.7 to +1.5		LSB
Differential Nonlinearity	DNL	27 MHz (at a 12-bit level)		−0.7 to +0.8		LSB
		54 MHz (at a 12-bit level)		−0.7 to +0.8		LSB
		75 MHz (at a 12-bit level)		−0.7 to +0.8		LSB
		108 MHz (at a 11-bit level)		−0.7 to +0.8		LSB
		170 MHz (at a 9-bit level)		−0.6 to +0.5		LSB
DIGITAL INPUTS						
Input High Voltage	V_{IH}	XTALN and XTALP pins	1.2			V
Input Low Voltage	V_{IL}	XTALN and XTALP pins			0.4	V
	V_{IH}	Other digital inputs	2			V
	V_{IL}	Other digital inputs			0.8	V
Input Current	I_{IN}	Reset pin			±60	µA
		EP_MISO pin			±60	µA
		SPDIF_IN pin			±60	µA
		TEST4 pin			±60	µA
		TEST6 pin			±60	µA
		Other digital inputs			±10	µA
Input Capacitance	C_{IN}				10	pF
DIGITAL INPUTS (5 V TOLERANT) [1]						
Input High Voltage	V_{IH}		2.6			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}		−82		+82	µA
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}		2.4			V
Output Low Voltage	V_{OL}				0.4	V
High Impedance Leakage Current	I_{LEAK}			10		µA
Output Capacitance	C_{OUT}				20	pF

[1] The following pins are 5 V tolerant: HS_IN1/TRI5, HS_IN2/TRI7, VS_IN1/TRI6, VS_IN2/TRI8, RXA_5V, RXB_5V, RXC_5V, RXD_5V, DDCA_SCL, DDCA_SDA, DDCB_SCL, DDCB_SDA, DDCC_SCL, DDCC_SDA, DDCD_SCL, and DDCD_SDA.

POWER SPECIFICATIONS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS						
Digital Core Power Supply	VDD	1.75	1.8	1.85	V	
Digital I/O Power Supply	DVDDIO	3.14	3.3	3.46	V	
SDRAM Power Supply	VDD_SDRAM					
		3.2	3.3	3.4	V	SDR memory
		2.35	2.5	2.65	V	DDR memory
PLL Power Supply	PVDD	1.71	1.8	1.89	V	
Analog Power Supply	AVDD	1.71	1.8	1.89	V	
Terminator Power Supply	TVDD	3.14	3.3	3.46	V	
Comparator Power Supply	CVDD	1.71	1.8	1.89	V	
CURRENT CONSUMPTION[1, 2, 3]						
Digital Core Supply Current	I_{VDD}		155	220	mA	Analog 1080p sampling at 148 MHz
			149	205	mA	RGB graphics sampling at 162 MHz
			365	445	mA	RGB graphics sampling at 162 MHz in simultaneous mode with all background ports enabled
			148	210	mA	HDMI 1080p: 12-bit Deep Color
			298	385	mA	HDMI 1080p: 12-bit Deep Color with all background ports enabled
			440	475	mA	SD core 576i processing in simultaneous mode with all background ports enabled
			480	525	mA	SCART processing in simultaneous mode with all background ports enabled
Digital I/O Supply Current	I_{DVDDIO}		55	120	mA	Analog 1080p sampling at 148 MHz
			40	122	mA	RGB graphics sampling at 162 MHz
			37	120	mA	RGB graphics sampling at 162 MHz in simultaneous mode with all background ports enabled
			15	175	mA	HDMI 1080p: 12-bit Deep Color
			14	175	mA	HDMI 1080p: 12-bit Deep Color with all background ports enabled
			9	11	mA	SD core 576i processing in simultaneous mode with all background ports enabled
			9	10	mA	SCART processing in simultaneous mode with all background ports enabled
PLL Supply Current	I_{PVDD}		27	30	mA	Analog 1080p sampling at 148 MHz
			25	29	mA	RGB graphics sampling at 162 MHz
			24	28	mA	RGB graphics sampling at 162 MHz in simultaneous mode with all background ports enabled
			34	37	mA	HDMI 1080p: 12-bit Deep Color
			35	38	mA	HDMI 1080p: 12-bit Deep Color with all background ports enabled
			33	36	mA	SD core 576i processing in simultaneous mode with all background ports enabled
			33	38	mA	SCART processing in simultaneous mode with all background ports enabled

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Analog Supply Current	I_{AVDD}		210	235	mA	Analog 1080p sampling at 148 MHz
			215	240	mA	RGB graphics sampling at 162 MHz
			214	235	mA	RGB graphics sampling at 162 MHz in simultaneous mode with all background ports enabled
			0	0.1	mA	HDMI 1080p: 12-bit Deep Color
			0	0.1	mA	HDMI 1080p: 12-bit Deep Color with all background ports enabled
			80	90	mA	SD core 576i processing in simultaneous mode with all background ports enabled
			260	285	mA	SCART processing in simultaneous mode with all background ports enabled
Terminator Supply Current[4]	I_{TVDD}		85	95	mA	One port connected
			260	280	mA	Four ports connected
Comparator Supply Current	I_{CVDD}		105	120	mA	HDMI 1080p: 12-bit Deep Color
			420	440	mA	HDMI 1080p: 12-bit Deep Color in simultaneous mode with all background ports enabled
Memory Interface Supply Current	I_{VDD_SDRAM}		28	35	mA	CVBS input sampling at 54 MHz
Power-Down Currents[5]	I_{DVDDIO}			0.1	mA	
	I_{VDD_SDRAM}			2.6	mA	
	I_{VDD}			10	mA	
	I_{AVDD}			0.1	mA	
	I_{CVDD}			0.5	mA	
	I_{TVDD}			2.2	mA	
	I_{PVDD}			1.7	mA	
Power-Up Time	t_{PWRUP}		25		ms	

[1] All maximum current values are guaranteed by characterization to assist in power supply design.
[2] Typical current consumption values are recorded with nominal voltage supply levels, SMPTE bar video pattern, and at room temperature.
[3] Maximum current consumption values are recorded with maximum rated voltage supply levels, MoireX video pattern, and at maximum rated temperature.
[4] Termination power supply includes TVDD current consumed off chip.
[5] Power-down mode entered by setting Bit POWER_DOWN high.

ANALOG SPECIFICATIONS

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLAMP CIRCUITRY [1]					
Input Impedance	Clamps switched off		10		MΩ
Analog (AIN1 – AIN12)					
ADC Midscale (CML)			0.91		V
ADC Full-Scale Level			CML + 0.55		V
ADC Zero-Scale Level			CML – 0.55		V
ADC Dynamic Range			1.1		V
Clamp Level (When Locked)	Component input, Y signal		CML – 0.12		V
	Component input, Pr signal		CML		V
	Component input, Pb signal		CML		V
	PC RGB input (R, G, B signals)		CML – 0.12		V
	CVBS input		CML – 0.205		V
	SCART RGB input (R, G, B signals)		CML – 0.205		V
	S-Video input (Y Signal)		CML – 0.205		V
	S-Video input (C Signal)		CML		V
Large Clamp Source Current	SDP only		0.3		mA
Large Clamp Sink Current	SDP only		0.4		mA
Fine Clamp Source Current	SDP only		9		µA
Fine Clamp Sink Current	SDP only		8		µA

[1] Specified for external clamp capacitor of 100 nF.

VIDEO SPECIFICATIONS

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS						
Differential Phase	DP	CVBS input (modulated five-step)		0.6		Degrees
Differential Gain	DG	CVBS input (modulated five-step)		0.8		%
Luma Nonlinearity	LNL	CVBS input (modulated five-step)		0.9		%
NOISE SPECIFICATIONS		Measured at 27 MHz LLC				
SNR Unweighted		Luma ramp		63		dB
SNR Unweighted		Luma flat field		64		dB
Analog Front-End Crosstalk				60		dB
LOCK TIME SPECIFICATIONS (SDP)						
Horizontal Lock Range				±5		%
Vertical Lock Range			40		70	Hz
Subcarrier Lock Range	f_{SC}			±0.8		kHz
Color Lock-In Time				60		Lines
Sync Depth Range[1]			20		200	%
Color Burst Range			1		200	%
Vertical Lock Time				300		ms
Horizontal Lock Time				100		Lines
CHROMA SPECIFICATIONS (SDP)						
Chroma Amplitude Error				0.9		%
Chroma Phase Error				0.3		Degrees
Chroma Luma Intermodulation				0.3		%

TIMING CHARACTERISTICS

Data and I²C Timing Characteristics

Table 5.

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK AND CRYSTAL						
Crystal Frequency, XTAL				28.63636		MHz
Crystal Frequency Stability					±50	ppm
Horizontal Sync Input Frequency			10		110	kHz
LLC Frequency Range			12.825		170	MHz
I²C PORTS						
SCL Frequency					400	kHz
SCL Minimum Pulse Width High	t_1		600			ns
SCL Minimum Pulse Width Low	t_2		1.3			µs
Start Condition Hold Time	t_3		600			ns
Start Condition Setup Time	t_4		600			ns
SDA Setup Time	t_5		100			ns
SCL and SDA Rise Time	t_6				1000	ns
SCL and SDA Fall Time	t_7				300	ns
Stop Condition Setup Time	t_8		0.6			µs
TTX I²C PORTS						
SCL Frequency					3.4	MHz
SCL Minimum Pulse Width High	t_1		60			ns
SCL Minimum Pulse Width Low	t_2		160			ns
Start Condition Hold Time	t_3		160			ns
Start Condition Setup Time	t_4		160			ns
SDA Setup Time	t_5		10			ns
SCL and SDA Rise Time	t_6		10		80	ns
SCL and SDA Fall Time	t_7		10		80	ns
Stop Condition Setup Time	t_8		160			ns
RESET FEATURE						
Reset Pulse Width			5			ms
CLOCK OUTPUTS						
LLC Mark-Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
DATA AND CONTROL OUTPUTS[2]						
Data Output Transition Time SDR (SDP)	t_{11}	End of valid data to negative clock edge		2.9	4.6	ns
Data Output Transition Time SDR (SDP)	t_{12}	Negative clock edge to start of valid data		0.2	0.6	ns
Data Output Transition Time SDR (CP)	t_{13}	End of valid data to negative clock edge		1.5	2.2	ns
Data Output Transition Time SDR (CP)	t_{14}	Negative clock edge to start of valid data		0.1	0.3	ns
I²S PORT, MASTER MODE						
SCLK Mark-Space Ratio	t_{15}:t_{16}		45:55		55:45	% duty cycle
LRCLK Data Transition Time	t_{17}	End of valid data to negative SCLK edge			10	ns
LRCLK Data Transition Time	t_{18}	Negative SCLK edge to start of valid data			10	ns
I2Sx Data Transition Time	t_{19}	End of valid data to negative SCLK edge			5	ns
I2Sx Data Transition Time	t_{20}	Negative SCLK edge to start of valid data			5	ns

[1] Guaranteed by characterization.
[2] With the DLL block on output clock bypassed.

TIMING DIAGRAMS

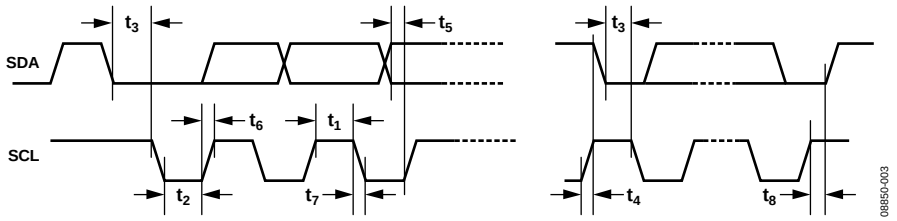


Figure 3. I²C Timing

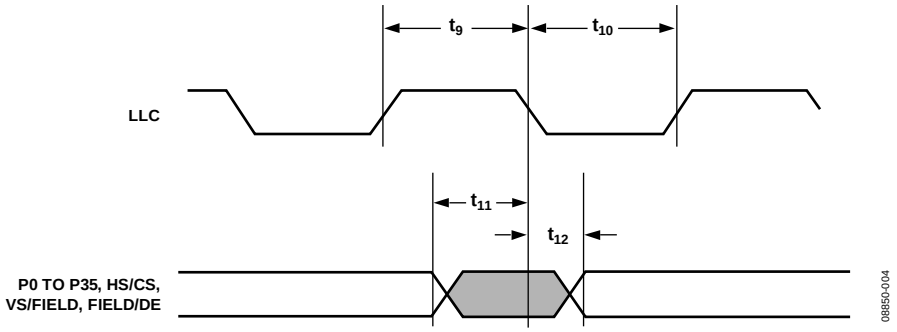


Figure 4. Pixel Port and Control SDR Output Timing (SDP)

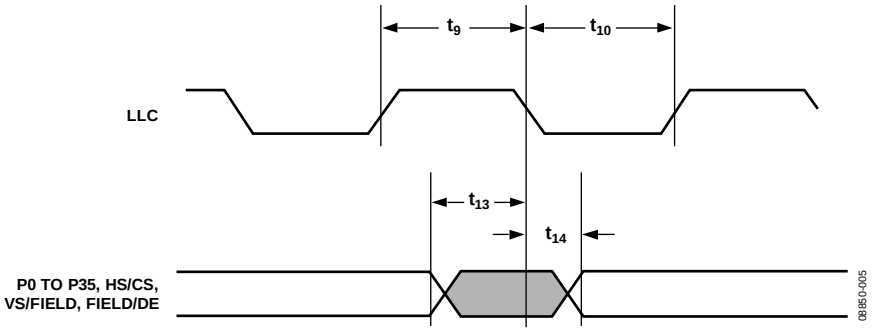


Figure 5. Pixel Port and Control SDR Output Timing (CP)

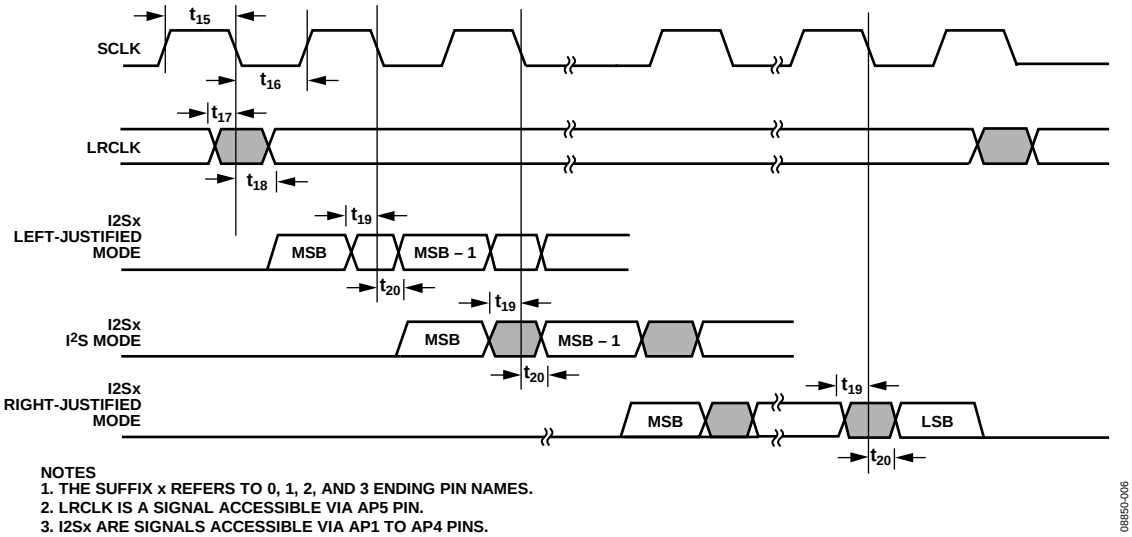


Figure 6. I²S Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVDD to GND	2.2 V
VDD to GND	2.2 V
PVDD to GND	2.2 V
DVDDIO to GND	4.0 V
VDD_SDRAM to GND	4.0 V
CVDD to GND	2.2 V
TVDD to GND	4.0 V
AVDD to PVDD	−0.3 V to +0.3 V
AVDD to VDD	−0.3 V to +0.3 V
TVDD to CVDD	−0.3 V to +2.2 V
DVDDIO to VDD_SDRAM	−0.3 V to +3.3 V
VDD_SDRAM to AVDD	−0.3 V to +2 V
VDD_SDRAM to VDD	−0.3 V to +2 V
Digital Inputs Voltage to GND	−0.3 V to DVDDIO + 0.3 V
Digital Outputs Voltage to GND	−0.3 V to DVDDIO + 0.3 V
5 V Tolerant Digital Inputs to GND[1]	5.5 V
Analog Inputs to GND	−0.3 V to AVDD + 0.3 V
XTALN and XTALP to GND	−0.3 V to PVDD + 0.3 V
Maximum Junction Temperature ($T_{J\ MAX}$)	125°C
Storage Temperature Range	−65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

[1] The following inputs are 3.3 V inputs but are 5 V tolerant: HS_IN1/TRI5, HS_IN2/TRI7, VS_IN1/TRI6, VS_IN2/TRI8, DDCA_SCL, DDCA_SDA, DDCB_SCL, DDCB_SDA, DDCC_SCL, DDCC_SDA, DDCD_SCL, and DDCD_SDA.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL PERFORMANCE

To reduce power consumption when using the ADV7844, the user is advised to turn off unused sections of the part.

Due to PCB metal variation, and therefore variation in PCB heat conductivity, the value of θ_{JA} may differ for various PCBs.

The most efficient measurement solution is obtained using the package surface temperature to estimate the die temperature because this eliminates the variance associated with the θ_{JA} value.

The maximum junction temperature ($T_{J\ MAX}$) of 125°C must not be exceeded. The following equation calculates the junction temperature using the measured package surface temperature and applies only when no heat sink is used on the device under test (DUT):

$$T_J = T_S + (\Psi_{JT} \times W_{TOTAL})$$

where:
T_S is the package surface temperature (°C).
Ψ_{JT} = 0.7°C/W for the 425-ball CSP_BGA.

$$W_{TOTAL} = (PVDD \times I_{PVDD}) + (0.4 \times TVDD \times I_{TVDD}) + (CVDD \times I_{CVDD}) + (AVDD \times I_{AVDD}) + (VDD \times I_{VDD}) + (A \times DVDDIO \times I_{DVDDIO}) + (VDD\_SDRAM \times I_{VDD\_SDRAM})$$

where 0.4 reflects the 40% of TVDD power that is dissipated on the part itself.
A = 0.5 when the output pixel clock is >74 MHz.
A = 0.75 when the output pixel clock is ≤74 MHz.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

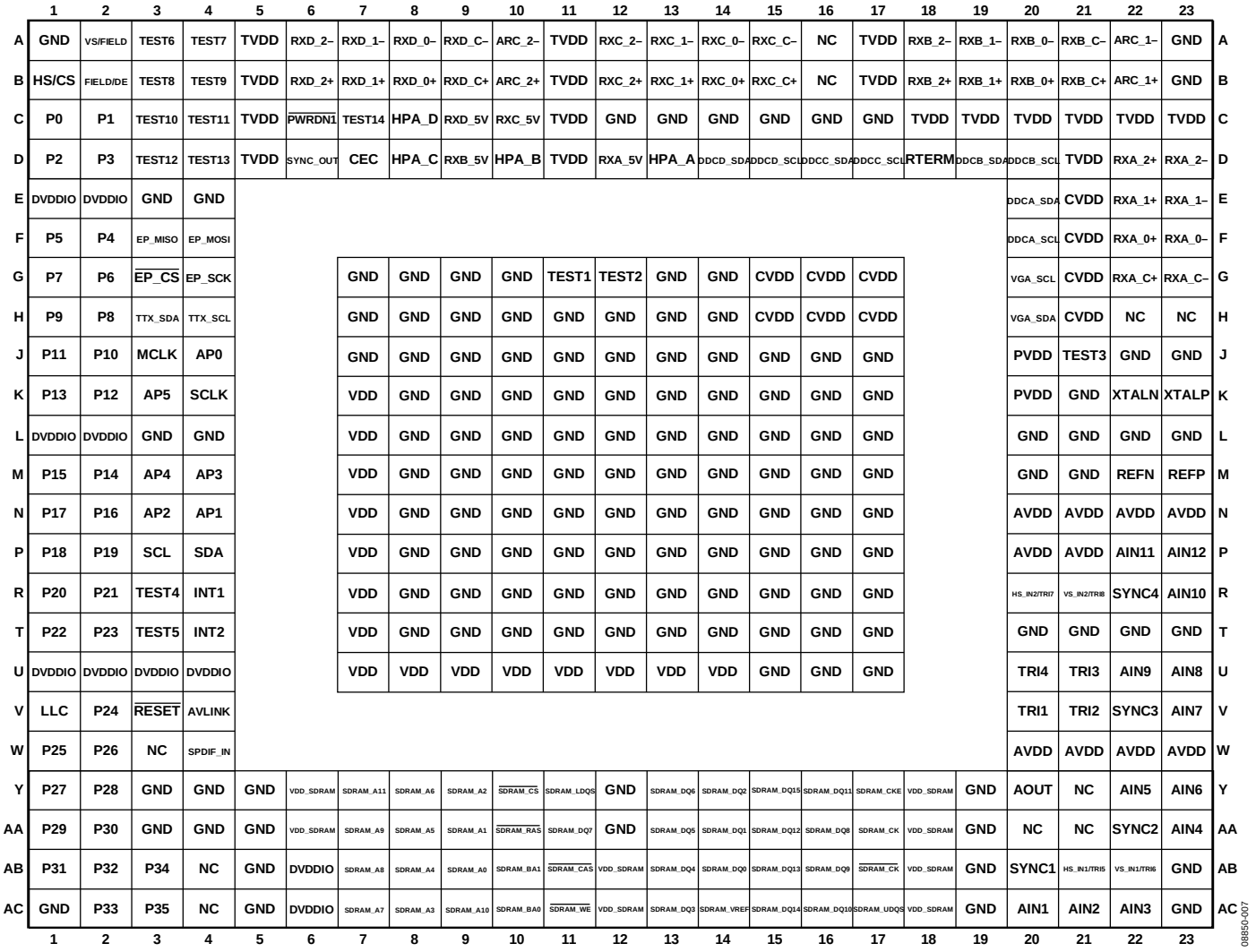


Figure 7. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
A1	GND	Ground	Ground.
A2	VS/FIELD	Digital video output	Vertical Synchronization Output Signal (VS). Field Synchronization Output Signal in All Interlaced Video Modes (FIELD). VS or FIELD can be configured for this pin.
A3	TEST6	Test pin	Float this pin.
A4	TEST7	Test pin	Float this pin.
A5	TVDD	Power	Terminator Supply Voltage (3.3 V).
A6	RXD_2−	HDMI input	Digital Input Channel 2 Complement of Port D in the HDMI Interface.
A7	RXD_1−	HDMI input	Digital Input Channel 1 Complement of Port D in the HDMI Interface.
A8	RXD_0−	HDMI input	Digital Input Channel 0 Complement of Port D in the HDMI Interface.
A9	RXD_C−	HDMI input	Digital Input Clock Complement of Port D in the HDMI Interface.
A10	ARC_2−	HDMI input/output	Audio Return Channel (ARC) Complement in ARC Interface 2.
A11	TVDD	Power	Terminator Supply Voltage (3.3 V).
A12	RXC_2−	HDMI input	Digital Input Channel 2 Complement of Port C in the HDMI Interface.
A13	RXC_1−	HDMI input	Digital Input Channel 1 Complement of Port C in the HDMI Interface.
A14	RXC_0−	HDMI input	Digital Input Channel 0 Complement of Port C in the HDMI Interface.
A15	RXC_C−	HDMI input	Digital Input Clock Complement of Port C in the HDMI Interface.
A16	NC	No connect	No Connect.
A17	TVDD	Power	Terminator Supply Voltage (3.3 V).
A18	RXB_2−	HDMI input	Digital Input Channel 2 Complement of Port B in the HDMI Interface.
A19	RXB_1−	HDMI input	Digital Input Channel 1 Complement of Port B in the HDMI Interface.
A20	RXB_0−	HDMI input	Digital Input Channel 0 Complement of Port B in the HDMI Interface.
A21	RXB_C−	HDMI input	Digital Input Clock Complement of Port B in the HDMI Interface.
A22	ARC_1−	HDMI input/output	Audio Return Channel (ARC) Complement in ARC Interface 1.
A23	GND	Ground	Ground.
B1	HS/CS	Digital video output	Horizontal Synchronization Output Signal (HS). Composite Synchronization Signal (CS). CS is a single signal containing both horizontal and vertical synchronization pulses. HS or CS can be configured for this pin.
B2	FIELD/DE	Miscellaneous digital	Field Synchronization Output Signal in All Interlaced Video Modes (FIELD). Data Enable (DE). DE is a signal that indicates active pixel data. DE or FIELD can be configured for this pin.
B3	TEST8	Test pin	Float this pin.
B4	TEST9	Test pin	Float this pin.
B5	TVDD	Power	Terminator Supply Voltage (3.3 V).
B6	RXD_2+	HDMI input	Digital Input Channel 2 True of Port D in the HDMI Interface.
B7	RXD_1+	HDMI input	Digital Input Channel 1 True of Port D in the HDMI Interface.
B8	RXD_0+	HDMI input	Digital Input Channel 0 True of Port D in the HDMI Interface.
B9	RXD_C+	HDMI input	Digital Input Clock True of Port D in the HDMI Interface.
B10	ARC_2+	HDMI input/output	Audio Return Channel (ARC) True in ARC Interface 2.
B11	TVDD	Power	Terminator Supply Voltage (3.3 V).
B12	RXC_2+	HDMI input	Digital Input Channel 2 True Of Port C in the HDMI Interface.
B13	RXC_1+	HDMI input	Digital Input Channel 1 True Of Port C in the HDMI Interface.
B14	RXC_0+	HDMI input	Digital Input Channel 0 True Of Port C in the HDMI Interface.
B15	RXC_C+	HDMI input	Digital Input Clock True Of Port C in the HDMI Interface.
B16	NC	No Connect	No Connect.
B17	TVDD	Power	Terminator Supply Voltage (3.3 V).
B18	RXB_2+	HDMI input	Digital Input Channel 2 True of Port B in the HDMI Interface.
B19	RXB_1+	HDMI input	Digital Input Channel 1 True of Port B in the HDMI Interface.
B20	RXB_0+	HDMI input	Digital Input Channel 0 True of Port B in the HDMI Interface.
B21	RXB_C+	HDMI input	Digital Input Clock True of Port B in the HDMI Interface.
B22	ARC_1+	HDMI input/output	Audio Return Channel (ARC) True in ARC Interface 1.
B23	GND	Ground	Ground.

Pin No.	Mnemonic	Type	Description
C1	P0	Digital video output	Video Pixel Output Port.
C2	P1	Digital video output	Video Pixel Output Port.
C3	TEST10	Test pin	Float this pin.
C4	TEST11	Test pin	Float this pin.
C5	TVDD	Power	Terminator Supply Voltage (3.3 V).
C6	$\overline{\text{PWRDN1}}$	Miscellaneous digital	Controls the Power-Up of the ADV7844. Should be connected to a digital 3.3 V I/O supply to power up the ADV7844.
C7	TEST14	Test pin	Tie this pin to ground via a 4.7 kΩ resistor.
C8	HPA_D	Miscellaneous digital	Hot Plug Assert Signal Output for HDMI Port D.
C9	RXD_5V	HDMI input	5 V Detect Pin for Port D in the HDMI Interface.
C10	RXC_5V	HDMI input	5 V Detect Pin for Port C in the HDMI Interface.
C11	TVDD	Power	Terminator Supply Voltage (3.3 V).
C12	GND	Ground	Ground.
C13	GND	Ground	Ground.
C14	GND	Ground	Ground.
C15	GND	Ground	Ground.
C16	GND	Ground	Ground.
C17	GND	Ground	Ground.
C18	TVDD	Power	Terminator Supply Voltage (3.3 V).
C19	TVDD	Power	Terminator Supply Voltage (3.3 V).
C20	TVDD	Power	Terminator Supply Voltage (3.3 V).
C21	TVDD	Power	Terminator Supply Voltage (3.3 V).
C22	TVDD	Power	Terminator Supply Voltage (3.3 V).
C23	TVDD	Power	Terminator Supply Voltage (3.3 V).
D1	P2	Digital video output	Video Pixel Output Port.
D2	P3	Digital video output	Video Pixel Output Port.
D3	TEST12	Test pin	Float this pin.
D4	TEST13	Test pin	Float this pin.
D5	TVDD	Power	Terminator Supply Voltage (3.3 V).
D6	SYNC_OUT	Miscellaneous digital	Sliced synchronization output.
D7	CEC	Digital input/output	Consumer Electronic Control Channel.
D8	HPA_C	Miscellaneous digital	Hot Plug Assert Signal Output for HDMI Port C.
D9	RXB_5V	HDMI input	5 V Detect Pin for Port B in the HDMI Interface.
D10	HPA_B	Miscellaneous digital	Hot Plug Assert Signal Output for HDMI Port B.
D11	TVDD	Power	Terminator Supply Voltage (3.3 V).
D12	RXA_5V	HDMI input	5 V Detect Pin for Port A in the HDMI Interface.
D13	HPA_A	Miscellaneous digital	Hot Plug Assert Signal Output for HDMI Port A.
D14	DDCD_SDA	Digital input/output	HDCP Slave Serial Data Port D. DDCD_SDA is a 3.3 V input/output that is 5 V tolerant.
D15	DDCD_SCL	Digital input	HDCP Slave Serial Clock Port D. DDCD_SCL is a 3.3 V input that is 5 V tolerant.
D16	DDCC_SDA	Digital input/output	HDCP Slave Serial Data Port C. DDCC_SDA is a 3.3 V input/output that is 5 V tolerant.
D17	DDCC_SCL	Digital input	HDCP Slave Serial Clock Port C. DDCC_SCL is a 3.3 V input that is 5 V tolerant.
D18	RTERM	Miscellaneous analog	Sets Internal Termination Resistance. A 500 Ω resistor between this pin and GND should be used.
D19	DDCB_SDA	Digital input/output	HDCP Slave Serial Data Port B. DDCB_SDA is a 3.3 V input/output that is 5 V tolerant.
D20	DDCB_SCL	Digital input	HDCP Slave Serial Clock Port B. DDCB_SCL is a 3.3 V input that is 5 V tolerant.
D21	TVDD	Power	Terminator Supply Voltage (3.3 V).
D22	RXA_2+	HDMI input	Digital Input Channel 2 True of Port A in the HDMI Interface.
D23	RXA_2−	HDMI input	Digital Input Channel 2 Complement of Port A in the HDMI Interface.
E1	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
E2	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
E3	GND	Ground	Ground.
E4	GND	Ground	Ground.
E20	DDCA_SDA	Digital input/output	HDCP Slave Serial Data Port A. DDCA_SDA is a 3.3 V input/output that is 5 V tolerant.
E21	CVDD	Power	Comparator Supply Voltage (1.8 V).

Pin No.	Mnemonic	Type	Description
E22	RXA_1+	HDMI input	Digital Input Channel 1 True of Port A in the HDMI Interface.
E23	RXA_1−	HDMI input	Digital Input Channel 1 Complement of Port A in the HDMI Interface.
F1	P5	Digital video output	Video Pixel Output Port.
F2	P4	Digital video output	Video Pixel Output Port.
F3	EP_MISO	Digital output	SPI Master In/Slave Out for External EDID Interface.
F4	EP_MOSI	Digital input	SPI Master Out/Slave In for External EDID Interface.
F20	DDCA_SCL	Digital input	HDCP Slave Serial Clock Port A. DDCA_SCL is a 3.3 V input that is 5 V tolerant.
F21	CVDD	Power	Comparator Supply Voltage (1.8 V).
F22	RXA_0+	HDMI input	Digital Input Channel 0 True of Port A in the HDMI Interface.
F23	RXA_0−	HDMI input	Digital Input Channel 0 Complement of Port A in the HDMI Interface.
G1	P7	Digital video output	Video Pixel Output Port.
G2	P6	Digital video output	Video Pixel Output Port.
G3	$\overline{\text{EP\_CS}}$	Digital output	SPI Chip Select for External EDID Interface.
G4	EP_SCK	Digital output	SPI Clock for External EDID Interface.
G7	GND	Ground	Ground.
G8	GND	Ground	Ground.
G9	GND	Ground	Ground.
G10	GND	Ground	Ground.
G11	TEST1	Test	Do Not Connect.
G12	TEST2	Test	Do Not Connect.
G13	GND	Ground	Ground.
G14	GND	Ground	Ground.
G15	CVDD	Power	Comparator Supply Voltage (1.8 V).
G16	CVDD	Power	Comparator Supply Voltage (1.8 V).
G17	CVDD	Power	Comparator Supply Voltage (1.8 V).
G20	VGA_SCL	Miscellaneous digital	DDC Port Serial Clock Input for VGA.
G21	CVDD	Power	Comparator Supply Voltage (1.8 V).
G22	RXA_C+	HDMI input	Digital Input Clock True of Port A in the HDMI Interface.
G23	RXA_C−	HDMI input	Digital Input Clock Complement of Port A in the HDMI Interface.
H1	P9	Digital video output	Video Pixel Output Port.
H2	P8	Digital video output	Video Pixel Output Port.
H3	TTX_SDA	Miscellaneous digital	I^2C Port Serial Data Input/Output. SDA is the data line for the teletext port.
H4	TTX_SCL	Miscellaneous digital	I^2C Port Serial Clock Input. SCL is the clock line for the teletext port.
H7	GND	Ground	Ground.
H8	GND	Ground	Ground.
H9	GND	Ground	Ground.
H10	GND	Ground	Ground.
H11	GND	Ground	Ground.
H12	GND	Ground	Ground.
H13	GND	Ground	Ground.
H14	GND	Ground	Ground.
H15	CVDD	Power	Comparator Supply Voltage (1.8 V).
H16	CVDD	Power	Comparator Supply Voltage (1.8 V).
H17	CVDD	Power	Comparator Supply Voltage (1.8 V).
H20	VGA_SDA	Miscellaneous digital	DDC Port Serial Data Input/Output for VGA.
H21	CVDD	Power	Comparator Supply Voltage (1.8 V).
H22	NC	No Connect	No Connect.
H23	NC	No Connect	No Connect.
J1	P11	Digital video output	Video Pixel Output Port.
J2	P10	Digital video output	Video Pixel Output Port.
J3	MCLK	Miscellaneous	Audio Master Clock Output.
J4	AP0	Miscellaneous	Audio Output.
J7	GND	Ground	Ground.

Pin No.	Mnemonic	Type	Description
J8	GND	Ground	Ground.
J9	GND	Ground	Ground.
J10	GND	Ground	Ground.
J11	GND	Ground	Ground.
J12	GND	Ground	Ground.
J13	GND	Ground	Ground.
J14	GND	Ground	Ground.
J15	GND	Ground	Ground.
J16	GND	Ground	Ground.
J17	GND	Ground	Ground.
J20	PVDD	Power	PLL Supply Voltage (1.8 V).
J21	TEST3	Test	Do Not Connect.
J22	GND	Ground	Ground.
J23	GND	Ground	Ground.
K1	P13	Digital video output	Video Pixel Output Port.
K2	P12	Digital video output	Video Pixel Output Port.
K3	AP5	Miscellaneous	Audio Output.
K4	SCLK	Miscellaneous digital	Audio Serial Clock Output.
K7	VDD	Power	Digital Core Supply Voltage (1.8 V).
K8	GND	Ground	Ground.
K9	GND	Ground	Ground.
K10	GND	Ground	Ground.
K11	GND	Ground	Ground.
K12	GND	Ground	Ground.
K13	GND	Ground	Ground.
K14	GND	Ground	Ground.
K15	GND	Ground	Ground.
K16	GND	Ground	Ground.
K17	GND	Ground	Ground.
K20	PVDD	Power	PLL Supply Voltage (1.8 V).
K21	GND	Ground	Ground.
K22	XTALN	Miscellaneous analog	Input Pin for 28.63636 MHz Crystal.
K23	XTALP	Miscellaneous analog	Input pin for 28.63636 MHz Crystal or an external 1.8 V, 28.63636 MHz Clock Oscillator Source to Clock the ADV7844.
L1	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
L2	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
L3	GND	Ground	Ground.
L4	GND	Ground	Ground.
L7	VDD	Power	Digital Core Supply Voltage (1.8 V).
L8	GND	Ground	Ground.
L9	GND	Ground	Ground.
L10	GND	Ground	Ground.
L11	GND	Ground	Ground.
L12	GND	Ground	Ground.
L13	GND	Ground	Ground.
L14	GND	Ground	Ground.
L15	GND	Ground	Ground.
L16	GND	Ground	Ground.
L17	GND	Ground	Ground.
L20	GND	Ground	Ground.
L21	GND	Ground	Ground.
L22	GND	Ground	Ground.
L23	GND	Ground	Ground.

Pin No.	Mnemonic	Type	Description
M1	P15	Digital video output	Video Pixel Output Port.
M2	P14	Digital video output	Video Pixel Output Port.
M3	AP4	Miscellaneous	Audio Output.
M4	AP3	Miscellaneous	Audio Output.
M7	VDD	Power	Digital Core Supply Voltage (1.8 V).
M8	GND	Ground	Ground.
M9	GND	Ground	Ground.
M10	GND	Ground	Ground.
M11	GND	Ground	Ground.
M12	GND	Ground	Ground.
M13	GND	Ground	Ground.
M14	GND	Ground	Ground.
M15	GND	Ground	Ground.
M16	GND	Ground	Ground.
M17	GND	Ground	Ground.
M20	GND	Ground	Ground.
M21	GND	Ground	Ground.
M22	REFN	Miscellaneous analog	Internal Voltage Reference Output.
M23	REFP	Miscellaneous analog	Internal Voltage Reference Output.
N1	P17	Digital video output	Video Pixel Output Port.
N2	P16	Digital video output	Video Pixel Output Port.
N3	AP2	Miscellaneous	Audio Output.
N4	AP1	Miscellaneous	Audio Output.
N7	VDD	Power	Digital Core Supply Voltage (1.8 V).
N8	GND	Ground	Ground.
N9	GND	Ground	Ground.
N10	GND	Ground	Ground.
N11	GND	Ground	Ground.
N12	GND	Ground	Ground.
N13	GND	Ground	Ground.
N14	GND	Ground	Ground.
N15	GND	Ground	Ground.
N16	GND	Ground	Ground.
N17	GND	Ground	Ground.
N20	AVDD	Power	Analog Supply Voltage (1.8 V).
N21	AVDD	Power	Analog Supply Voltage (1.8 V).
N22	AVDD	Power	Analog Supply Voltage (1.8 V).
N23	AVDD	Power	Analog Supply Voltage (1.8 V).
P1	P18	Digital video output	Video Pixel Output Port.
P2	P19	Digital video output	Video Pixel Output Port.
P3	SCL	Miscellaneous digital	I^2C Port Serial Clock Input. SCL is the clock line for the control port.
P4	SDA	Miscellaneous digital	I^2C Port Serial Data Input/Output. SDA is the data line for the control port.
P7	VDD	Power	Digital Core Supply Voltage (1.8 V).
P8	GND	Ground	Ground.
P9	GND	Ground	Ground.
P10	GND	Ground	Ground.
P11	GND	Ground	Ground.
P12	GND	Ground	Ground.
P13	GND	Ground	Ground.
P14	GND	Ground	Ground.
P15	GND	Ground	Ground.
P16	GND	Ground	Ground.
P17	GND	Ground	Ground.

Pin No.	Mnemonic	Type	Description
P20	AVDD	Power	Analog Supply Voltage (1.8 V).
P21	AVDD	Power	Analog Supply Voltage (1.8 V).
P22	AIN11	Analog video input	Analog Video Input Channel.
P23	AIN12	Analog video input	Analog Video Input Channel.
R1	P20	Digital video output	Video Pixel Output Port.
R2	P21	Digital video output	Video Pixel Output Port.
R3	TEST4	Test	This pin should be tied to ground.
R4	INT1	Miscellaneous digital	Interrupt. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user control.
R7	VDD	Power	Digital Core Supply Voltage (1.8 V).
R8	GND	Ground	Ground.
R9	GND	Ground	Ground.
R10	GND	Ground	Ground.
R11	GND	Ground	Ground.
R12	GND	Ground	Ground.
R13	GND	Ground	Ground.
R14	GND	Ground	Ground.
R15	GND	Ground	Ground.
R16	GND	Ground	Ground.
R17	GND	Ground	Ground.
R20	HS_IN2/TRI7	Miscellaneous analog	HS on Graphics Port 2 (HS_IN2). The HS input signal is used for 5-wire timing mode. Trilevel/Bilevel Input on the SCART or D-Terminal Connector (TRI7). (Selection available via the I^2C.)
R21	VS_IN2/TRI8	Miscellaneous analog	VS on Graphics Port 2 (VS_IN2). The VS input signal is used for 5-wire timing mode. Trilevel/Bilevel Input on the SCART or D-Terminal Connector (TRI8). (Selection available via the I^2C.)
R22	SYNC4	Miscellaneous analog	This is a synchronization on green or luma input (SOG/SOY) used in embedded synchronization mode. User configurable.
R23	AIN10	Analog video input	Analog Video Input Channel.
T1	P22	Digital video output	Video Pixel Output Port.
T2	P23	Digital video output	Video Pixel Output Port.
T3	TEST5	Test	Do Not Connect.
T4	INT2	Miscellaneous digital	Interrupt. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user control.
T7	VDD	Power	Digital Core Supply Voltage (1.8 V).
T8	GND	Ground	Ground.
T9	GND	Ground	Ground.
T10	GND	Ground	Ground.
T11	GND	Ground	Ground.
T12	GND	Ground	Ground.
T13	GND	Ground	Ground.
T14	GND	Ground	Ground.
T15	GND	Ground	Ground.
T16	GND	Ground	Ground.
T17	GND	Ground	Ground.
T20	GND	Ground	Ground.
T21	GND	Ground	Ground.
T22	GND	Ground	Ground.
T23	GND	Ground	Ground.
U1	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
U2	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
U3	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
U4	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
U7	VDD	Power	Digital Core Supply Voltage (1.8 V).

Pin No.	Mnemonic	Type	Description
U8	VDD	Power	Digital Core Supply Voltage (1.8 V).
U9	VDD	Power	Digital Core Supply Voltage (1.8 V).
U10	VDD	Power	Digital Core Supply Voltage (1.8 V).
U11	VDD	Power	Digital Core Supply Voltage (1.8 V).
U12	VDD	Power	Digital Core Supply Voltage (1.8 V).
U13	VDD	Power	Digital Core Supply Voltage (1.8 V).
U14	VDD	Power	Digital Core Supply Voltage (1.8 V).
U15	GND	Ground	Ground.
U16	GND	Ground	Ground.
U17	GND	Ground	Ground.
U20	TRI4	Miscellaneous analog	Trilevel or Bilevel Input on the SCART or D-Type Connector. (Selection available via the I^2C.)
U21	TRI3	Miscellaneous analog	Trilevel or Bilevel Input on the SCART or D-Type Connector. (Selection available via the I^2C.)
U22	AIN9	Analog video input	Analog Video Input Channel.
U23	AIN8	Analog video input	Analog Video Input Channel.
V1	LLC	Digital video output	Line-Locked Output Clock for the Pixel Data.
V2	P24	Digital video output	Video Pixel Output Port.
V3	$\overline{\text{RESET}}$	Miscellaneous digital	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7844 circuitry.
V4	AVLINK	Digital input/output	Digital SCART Control Channel.
V20	TRI1	Miscellaneous analog	Trilevel or Bilevel Input on the SCART or D-Type Connector. (Selection available via the I^2C.)
V21	TRI2	Miscellaneous analog	Trilevel or Bilevel Input on the SCART or D-Type Connector. (Selection available via the I^2C.)
V22	SYNC3	Miscellaneous analog	This is a synchronization on green or luma input (SOG/SOY) used in embedded synchronization mode. User configurable.
V23	AIN7	Analog video input	Analog Video Input Channel.
W1	P25	Digital video output	Video Pixel Output Port.
W2	P26	Digital video output	Video Pixel Output Port.
W3	NC	No connect	No Connect.
W4	SPDIF_IN	Miscellaneous digital	S/PDIF Stream Input.
W20	AVDD	Power	Analog Supply Voltage (1.8 V).
W21	AVDD	Power	Analog Supply Voltage (1.8 V).
W22	AVDD	Power	Analog Supply Voltage (1.8 V).
W23	AVDD	Power	Analog Supply Voltage (1.8 V).
Y1	P27	Digital video output	Video Pixel Output Port.
Y2	P28	Digital video output	Video Pixel Output Port.
Y3	GND	Ground	Ground.
Y4	GND	Ground	Ground.
Y5	GND	Ground	Ground.
Y6	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
Y7	SDRAM_A11	SDRAM interface	Address Output. Interface to external RAM address lines.
Y8	SDRAM_A6	SDRAM interface	Address Output. Interface to external RAM address lines.
Y9	SDRAM_A2	SDRAM interface	Address Output. Interface to external RAM address lines.
Y10	$\overline{\text{SDRAM\_CS}}$	SDRAM interface	Chip Select. $\overline{\text{SDRAM\_CS}}$ enables and disables the command decoder on the RAM. One of four command signals to the external SDRAM.
Y11	SDRAM_LDQS	SDRAM interface	Lower Data Strobe Pin. Data strobe pins are used for the RAM interface. This is an input when reading data from external memory and output when writing data to external memory. It is edge-aligned when reading from external memory and centered with data when reading to external memory. SDRAM_ LDQS corresponds to the data on SDRAM_DQ7 to SDRAM_DQ0.
Y12	GND	Ground	Ground.
Y13	SDRAM_DQ6	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
Y14	SDRAM_DQ2	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.

Pin No.	Mnemonic	Type	Description
Y15	SDRAM_DQ15	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
Y16	SDRAM_DQ11	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
Y17	SDRAM_CKE	SDRAM interface	Clock Enable. This pin acts as an enable to the clock signals of the external RAM.
Y18	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
Y19	GND	Ground	Ground.
Y20	AOUT	Analog monitor output	Analog Monitor Output.
Y21	NC	No connect	No Connect.
Y22	AIN5	Analog video input	Analog Video Input Channel.
Y23	AIN6	Analog video input	Analog Video Input Channel.
AA1	P29	Digital video output	Video Pixel Output Port.
AA2	P30	Digital video output	Video Pixel Output Port.
AA3	GND	Ground	Ground.
AA4	GND	Ground	Ground.
AA5	GND	Ground	Ground.
AA6	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
AA7	SDRAM_A9	SDRAM interface	Address Output. Interface to external RAM address lines.
AA8	SDRAM_A5	SDRAM interface	Address Output. Interface to external RAM address lines.
AA9	SDRAM_A1	SDRAM interface	Address Output. Interface to external RAM address lines.
AA10	$\overline{\text{SDRAM\_RAS}}$	SDRAM interface	Row Address Select Command Signal. One of four command signals to the external SDRAM.
AA11	SDRAM_DQ7	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AA12	GND	Ground	Ground.
AA13	SDRAM_DQ5	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AA14	SDRAM_DQ1	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AA15	SDRAM_DQ12	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AA16	SDRAM_DQ8	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AA17	SDRAM_CK	SDRAM interface	Differential Clock Output. All address and control output signals to the RAM should be sampled on the positive edge of SDRAM_CK and on the negative edge of $\overline{\text{SDRAM\_CK}}$.
AA18	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
AA19	GND	Ground	Ground.
AA20	NC	No connect	No Connect.
AA21	NC	No connect	No Connect.
AA22	SYNC2	Miscellaneous analog	This is a synchronization on green or luma input (SOG/SOY) used in embedded synchronization mode. User configurable.
AA23	AIN4	Analog video input	Analog Video Input Channel.
AB1	P31	Digital video output	Video Pixel Output Port.
AB2	P32	Digital video output	Video Pixel Output Port.
AB3	P34	Digital video output	Video Pixel Output Port.
AB4	NC	No connect	No Connect.
AB5	GND	Ground	Ground.
AB6	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
AB7	SDRAM_A8	SDRAM interface	Address Output. Interface to external RAM address lines.
AB8	SDRAM_A4	SDRAM interface	Address Output. Interface to external RAM address lines.
AB9	SDRAM_A0	SDRAM interface	Address Output. Interface to external RAM address lines.
AB10	SDRAM_BA1	SDRAM interface	Bank Address Output. Interface to external RAM bank address lines.
AB11	$\overline{\text{SDRAM\_CAS}}$	SDRAM interface	Column Address Select Command Signal. One of four command signals to the external SDRAM.
AB12	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
AB13	SDRAM_DQ4	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AB14	SDRAM_DQ0	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AB15	SDRAM_DQ13	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AB16	SDRAM_DQ9	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.

Pin No.	Mnemonic	Type	Description
AB17	SDRAM_CK	SDRAM interface	Differential Clock Output. All address and control output signals to the RAM should be sampled on the positive edge of SDRAM_CK and on the negative edge of SDRAM_CK.
AB18	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
AB19	GND	Ground	Ground.
AB20	SYNC1	Miscellaneous analog	This is a synchronization on green or luma input (SOG/SOY) used in embedded synchronization mode. User configurable.
AB21	HS_IN1/TRI5	Miscellaneous analog	HS on Graphics Port 1 (HS_IN1). The HS input signal is used for 5-wire timing mode. Trilevel/Bilevel Input on the SCART or D-Terminal Connector (TRI5). (Selection available via the I²C.)
AB22	VS_IN1/TRI6	Miscellaneous analog	VS on Graphics Port 1 (VS_IN2). The VS input signal is used for 5-wire timing mode. Trilevel/Bilevel Input on the SCART or D-Terminal Connector (TRI6). (Selection available via the I²C.)
AB23	GND	Ground	Ground.
AC1	GND	Ground	Ground.
AC2	P33	Digital video output	Video Pixel Output Port.
AC3	P35	Digital video output	Video Pixel Output Port.
AC4	NC	No connect	No Connect.
AC5	GND	Ground	Ground.
AC6	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
AC7	SDRAM_A7	SDRAM interface	Address Output. Interface to external RAM address lines.
AC8	SDRAM_A3	SDRAM interface	Address Output. Interface to external RAM address lines.
AC9	SDRAM_A10	SDRAM interface	Address Output. Interface to external RAM address lines.
AC10	SDRAM_BA0	SDRAM interface	Bank Address Output. Interface to external RAM bank address lines.
AC11	SDRAM_WE	SDRAM interface	Write Enable Output Command Signal. One of four command signals to the external SDRAM.
AC12	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
AC13	SDRAM_DQ3	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AC14	SDRAM_VREF	SDRAM interface	1.25 V Reference for DDR SDRAM Interface or 1.65 V for SDR.
AC15	SDRAM_DQ14	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AC16	SDRAM_DQ10	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AC17	SDRAM_UDQS	SDRAM interface	Upper Data Strobe Pin. Data strobe pins are used for the RAM interface. This is an input when reading data from external memory and an output when writing data to external memory. It is edge-aligned with data when reading from external memory and centered with data when writing to external memory. SDRAM_UDQS corresponds to the data on SDRAM_DQ15 to SDRAM_DQ8.
AC18	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
AC19	GND	Ground	Ground.
AC20	AIN1	Analog video input	Analog Video Input Channel.
AC21	AIN2	Analog video input	Analog Video Input Channel.
AC22	AIN3	Analog video input	Analog Video Input Channel.
AC23	GND	Ground	Ground.

POWER SUPPLY SEQUENCING

POWER-UP SEQUENCE

The recommended power-up sequence of the ADV7844 is as follows:

1. 3.3 V supplies
2. 2.5 V supply (applies only if using DDR memory)
3. 1.8 V supplies

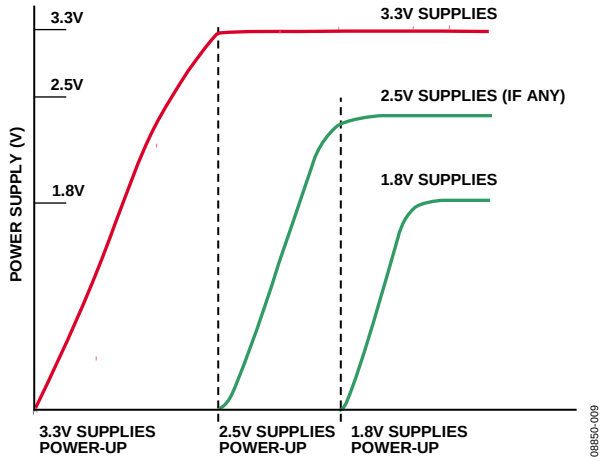


Figure 8. Recommended Power-Up Sequence

Notes

Reset should be held low while the supplies are being powered up.

- 3.3 V supplies should be powered up first.
- 2.5 V supply should be powered after the 3.3 V supplies are established but before the 1.8 V supplies.
- 1.8 V supplies should be powered up last.

The ADV7844 can alternatively be powered up by asserting all supplies simultaneously.

In this case, care must be taken to ensure that a lower rated supply does not go above a higher rated supply level, as the supplies are being established.

POWER-DOWN SEQUENCE

The ADV7844 supplies can be deasserted simultaneously as long as a higher rated supply does not go below a lower rated supply.

FUNCTIONAL OVERVIEW

HDMI RECEIVER

The ADV7844 front end incorporates a 4:1 multiplexed HDMI receiver with Xpressview fast switching technology and support for HDMI features including ARC and 3D TV. Building on the feature set of Analog Devices existing HDMI devices, the ADV7844 also offers support for all HD TV formats up to 12-bit, 1080p Deep Color and all display resolutions up to UXGA (1600 × 1200 at 60 Hz). Xpressview fast switching technology, using Analog Devices hardware-based HDCP engine that minimizes software overhead, allows switching between any two input ports in less than 1 second.

With the inclusion of HDCP 1.4, the ADV7844 can receive encrypted video content. The HDMI interface of the ADV7844 allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewal of that authentication during transmission, as specified by the HDCP 1.4 protocol. Repeater support is also offered by the ADV7844.

The ADV7844 supports the audio return channel feature. There is a dedicated S/PDIF input on which audio can be received for retransmission on the HDMI input. A wide range of 3D video formats is supported, including frame packing 1080p 24 Hz, 720p 50 Hz, and 720p 60 Hz.

The HDMI receiver incorporates active equalization of the HDMI data signals. This equalization compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at longer lengths and higher frequencies. It is capable of equalizing for cable lengths up to 30 meters to achieve robust receiver performance at even the highest HDMI data rates.

The HDMI receiver offers advanced audio functionality. It supports multichannel I²S audio for up to eight channels. It also supports a 6-DSD channel interface with each channel carrying an oversampled 1-bit representation of the audio signal as delivered on SACD. The ADV7844 can also receive HBR audio packet streams and outputs them through the HBR interface in an S/PDIF format conforming to the IEC60958 standard.

The receiver contains an audio mute controller that can detect a variety of conditions that may result in audible extraneous noise in the audio output. On detection of these conditions, the audio signal can be ramped to mute to prevent audio clicks or pops.

HDMI receiver features include:

- 4:1 multiplexed HDMI receiver
- HDMI, ARC, and 3D format support, DVI 1.0
- 225 MHz HDMI receiver
- Integrated equalizer
- High-bandwidth Digital Content Protection (HDCP 1.4) on background ports
- Internal HDCP keys
- 36-/30-bit Deep Color support
- PCM, HBR, and DSD audio packet support
- Repeater support
- Internal E-EDID RAM
- Hot plug assert output pin for each HDMI port
- CEC controller

ANALOG FRONT END

The ADV7844 analog front end comprises four 170 MHz, 12-bit ADCs that digitize the analog video signal before applying it to the standard definition processor (SDP) or component processor (CP). The analog front end uses differential channels to each ADC to ensure high performance in a mixed-signal application.

The front end also includes a 12-channel input mux that enables multiple video signals to be applied to the ADV7844 without the requirement of an external mux.

Current and voltage clamp control loops ensure that any dc offsets are removed from the video signal. The clamps are positioned in front of each ADC to ensure that the video signal remains within the range of the converter.

The ADCs are configured to run up to 8× oversampling mode when decoding composite or S-Video inputs. For component 525i, 625i, 525p, and 625p sources, 4× oversampling is performed. All other video standards are 1× oversampled. Oversampling the video signals reduces the cost and complexity of external antialiasing filters with the benefit of an increased signal-to-noise ratio (SNR).

Optional internal antialiasing filters with programmable bandwidth are positioned in front of each ADC. These filters can be used to band limit video signals, removing spurious, out-of-band noise.

The ADV7844 can support the simultaneous processing of CVBS and RGB standard definition signals to enable SCART compatibility and overlay functionality. A combination of CVBS and RGB inputs can be mixed with the output under the control of I²C registers.

Analog front-end features include:

- Four 170 MHz, NSV, 12-bit ADCs that enable true 12-bit video decoding
- 12-channel analog input mux that enables multiple source connections without the requirement of an external mux
- Four current and voltage clamp control loops that ensure any dc offsets are removed from the video signal
- SCART functionality and SD RGB overlay on CVBS controlled by fast blank input
- SCART source switching detection through the TRI1 to TRI8 inputs
- Four programmable antialiasing filters

STANDARD DEFINITION PROCESSOR

The SDP is capable of decoding a large selection of baseband video signals in composite and S-Video formats. The video standards supported by the SDP include PAL, PAL 60, PAL M, PAL N, PAL NC, NTSC M/J, NTSC 4.43, and SECAM. The ADV7844 can automatically detect the video standard and process it accordingly.

The SDP has a 3D temporal comb filter and a five-line adaptive 2D comb filter that gives superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to the video standard and signal quality with no user intervention required. The SDP has an IF filter block that compensates for attenuation in the high frequency chroma spectrum due to a tuner SAW filter. The SDP has specific luminance and chrominance parameter controls for brightness, contrast, saturation, and hue.

The ADV7844 implements a patented Adaptive Digital Line Length Tracking (ADLLT™) algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV7844 to track and decode poor quality video sources (such as VCRs) and noisy sources (such as tuner outputs, VCR players, and camcorders). Frame TBC ensures stable clock synchronization between the decoder and the downstream devices.

The SDP also contains both a luma transient improvement (LTI) block and a chroma transient improvement (CTI) block. These increase the edge rate on the luma and chroma transitions, resulting in a sharper video image.

The SDP has a Macrovision® detection circuit that allows Type I, Type II, and Type III Macrovision protection levels. The decoder is also fully robust to all Macrovision signal inputs.

SDP features include:

- Advanced adaptive 3D comb (using either external DDR or SDR SDRAM memory)
- Adaptive 2D five-line comb filters for NTSC and PAL that give superior chrominance and luminance separation for composite video
- Full automatic detection and autoswitching of all worldwide standards (PAL, NTSC, and SECAM)
- Automatic gain control with white peak mode that ensures the video is always processed without loss of the video processing range
- Proprietary architecture for locking to weak, noisy, and unstable sources from VCRs and tuners
- IF filter block that compensates for high frequency luma attenuation due to tuner SAW filter
- LTI and CTI
- Vertical and horizontal programmable luma peaking filters
- 8× oversampling (108 MHz) for CVBS, and S-Video modes
- Line-locked clock (LLC) output
- Free-run output mode that provides stable timing when no video input is present or video lock is lost
- Internal color bar test pattern
- Advanced TBC with frame synchronization, which ensures nominal clock and data for nonstandard input
- Interlace-to-progressive conversion for 525i and 625i formats, enabling direct drive of HDMI Tx devices
- Color controls that include hue, brightness, saturation, and contrast

COMPONENT PROCESSOR

The CP section of the ADV7844 is capable of decoding and digitizing a wide range of component video formats in any color space. Component video standards supported by the CP are 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, 1250i, VGA up to UXGA at 60 Hz, and many other standards.

The any-to-any, 3 × 3 CSC matrix is placed between the analog front end and the CP section. This enables YPbPr to RGB and RGB to YCbCr conversions. Many other standards of color space can be implemented using the color space converter.

The CP section contains circuitry to enable the detection of Macrovision encoded YPbPr signals for 525i, 625i, 525p, and 625p. It is designed to be fully robust when decoding these types of signals.

VBI extraction of CGMS data is performed by the CP section of the ADV7844 for interlaced, progressive, and high definition scanning rates. The data extracted can be read back over the I^2C interface.

CP features include:

- 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, and many other HDTV formats are supported
- Supports 720p 24 Hz/25 Hz formats
- Manual adjustments including gain (contrast), offset (brightness), hue, and saturation
- Support for analog component YPbPr and RGB video formats with embedded synchronization, composite synchronization or separate HS and VS
- Any-to-any, 3 × 3 CSC matrix that supports YCbCr-to-RGB and RGB-to- YCbCr, fully programmable or preprogrammable configurations
- Synchronization source polarity detector (SSPD) that determines the source and polarity of the synchronization signals that accompany the input video
- Macrovision copy protection detection on component formats (525i, 625i, 525p, and 625p)
- Free-run output mode that provides stable timing when no video input is present or video lock is lost
- Arbitrary pixel sampling support for nonstandard video sources
- 170 MHz conversion rate, which supports RGB input resolutions up to 1600 × 1200 at 60 Hz
- Automatic or manual clamp-and-gain controls for graphics modes
- Contrast, brightness, hue, and saturation controls

- 32-phase ADC DLL that allows optimum pixel clock sampling
- Automatic detection of synchronization source and polarity by SSPD block
- Standard identification enabled by STDI block
- RGB that can be color space converted to YCbCr and decimated to a 4:2:2 format for video-centric back-end IC interfacing
- Data enable (DE) output signal supplied for direct connection to HDMI/DVI Tx IC

OTHER FEATURES

The ADV7844 has HS, VS, FIELD, and DE output signals with programmable position, polarity, and width, and two I^2C host port interfaces (control and VBI).

The ADV7844 has two programmable interrupt request output pins, INT1 and INT2. It also features a number of low power modes and a full power-down mode.

The ADV7844 is provided in a 19 mm × 19 mm, RoHS-compliant CSP_BGA package, and is specified over the 0°C to +70°C temperature range.

For more detailed product information about the ADV7844, contact your local Analog Devices sales office.

EXTERNAL MEMORY REQUIREMENTS

The ADV7844 uses external SD RAM for 3D comb and frame synchronizer. The ADV7844 supports either SDR or DDR SD RAM.

SINGLE DATA RATE (SDR)

The ADV7844 can use SDR external memory to provide 3D comb or frame synchronizer operation nonconcurrently.

There is a 64 Mb SDR SDRAM minimum memory requirement. The required memory architecture is four banks of 1 Mb × 16 (4M16) with a speed grade of 133 MHz at CAS latency (CL) 3. Using 22 Ω series termination resistors is recommended for this configuration.

Recommended SDR memory that is compatible with the ADV7844 includes Winbond W9864G6PH-7.

DOUBLE DATA RATE (DDR)

The ADV7844 can use DDR external memory to simultaneously provide 3D comb and frame synchronizer operation.

There is a 128 Mb DDR SDRAM minimum memory requirement. The required memory architecture is four banks of 2 Mb × 16 (8M16) with a speed grade of 133 MHz at CL 2.5. Using 22 Ω series termination resistors is recommended for this configuration

Recommended DDR memory that is compatible with the ADV7844 includes the K4H561638J-LCB3 from Samsung, the MT46V16M16P-6T from Micron Technology, Inc., and the H5DU1262GTR-E3C from Hynix, Inc.

PIXEL INPUT/OUTPUT FORMATTING

The output section of the ADV7844 is highly flexible. The pixel output bus can support up to 36-bit 4:4:4. The pixel data supports both single and double data rates modes. In SDR mode, a 16-/20-/24-bit 4:2:2 or 24-/30-/36-bit 4:4:4 output is possible. In DDR mode, the pixel output port can be configured in 8-/10-/12-bit 4:2:2 modes or 24-/30-/36-bit 4:4:4 modes. Bus rotation and bus inversion are also supported. All output modes are controlled via I^2C controls.

PIXEL DATA OUTPUT MODES FEATURES

The output pixel port features include the following:

- 8-/10-/12-bit ITU-R BT.656 4:2:2 with embedded time codes and/or HS, VS, and FIELD output signals
- SDR 16-/20-/24-/30-/36 bit with embedded time codes and/or HS and VS/FIELD pin timing
- DDR 8-/10-/12-bit 4:2:2 with embedded time codes and/or HS, VS, and FIELD output signals
- DDR 24-/30-/36 bit 4:4:4 with embedded time codes and/or HS, VS, and FIELD output signals

Note that DDR modes are supported up to 54 MHz by characterization.

REGISTER MAP ARCHITECTURE

The registers of the ADV7844 are controlled via a 2-wire serial (I^2C-compatible) interface. The ADV7844 has 12 maps. The IO map has a static I^2C address. All other map addresses must be programmed; this ensures no addressing clashes on the system. Figure 9 shows the register map architecture.

Table 8.

Register Map Name	Default Address	Programmable Address	Location at Which Address Can Be Programmed
IO Map	0x40	Not programmable	Not applicable
CP Map	0x00	Programmable	IO map, Register 0xFD
SDP Map	0x00	Programmable	IO map, Register 0xF1
SDP_IO Map	0x00	Programmable	IO map, Register 0xF2
VDP Map	0x00	Programmable	IO map, Register 0xFE
AVLINK Map	0x00	Programmable	IO map, Register 0xF3
CEC Map	0x00	Programmable	IO map, Register 0xF4
HDMI Map	0x00	Programmable	IO map, Register 0xFB
EDID Map	0x00	Programmable	IO map, Register 0xFA
Repeater Map	0x00	Programmable	IO map, Register 0xF9
AFE, DPLL Map	0x00	Programmable	IO map, Register 0xF8
InfoFrame Map	0x00	Programmable	IO map, Register 0xF5

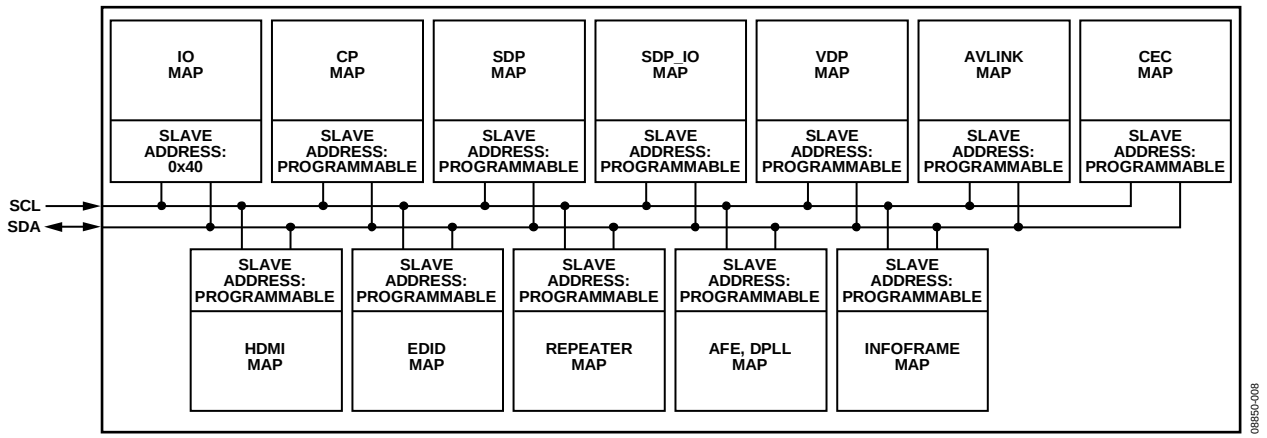
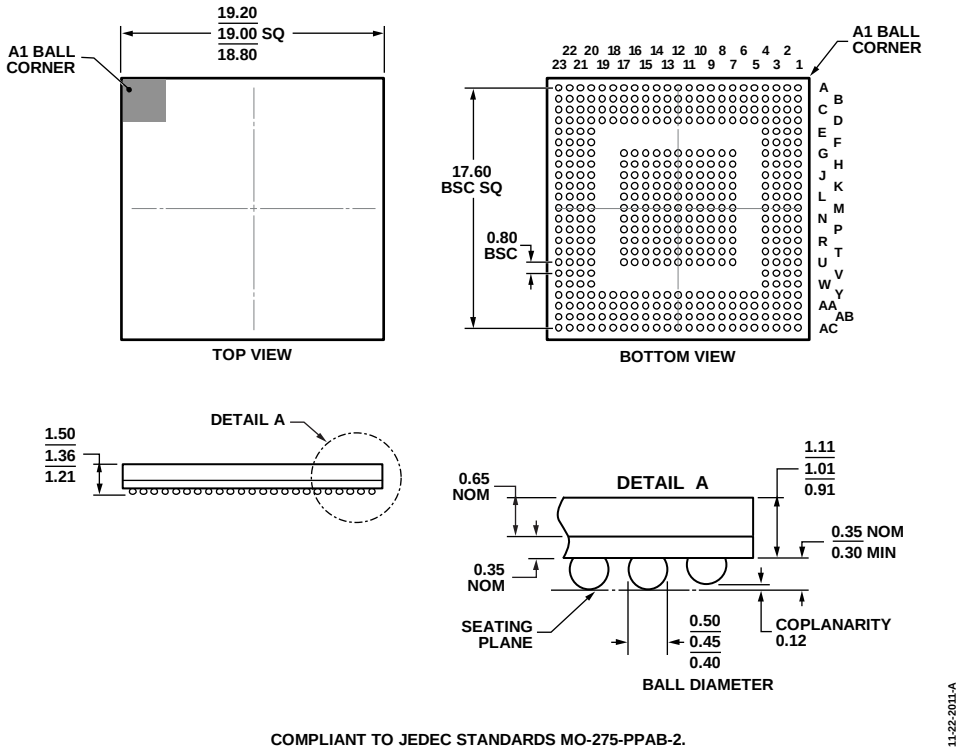


Figure 9. Register Map Architecture

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-275-PPAB-2.

Figure 10. 425-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-425-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Notes	Temperature Range	Package Description	Package Option
ADV7844KBCZ-5	[2, 3]	0°C to +70°C	425-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-425-1
EVAL-ADV7844EB1Z	[3, 4, 5]	0°C to +70°C	Front-End Evaluation Board	

[1] Z = RoHS-Compliant Part.
[2] Speed grade: 5 = 170 MHz.
[3] This part is programmed with internal HDCP keys. Customers must have HDCP adopter status (consult Digital Content Protection, LLC, for licensing requirements) to purchase any components with internal HDCP keys.
[4] An ATV motherboard is also required to process the ADV7844 digital outputs and achieve video output. An ATV video output board is optional to evaluate performance through an HDMI transmitter and video encoder.
[5] Front-end board for the ATV video evaluation platform, fitted with ADV7844KBCZ-5 decoder.

NOTES

NOTES

I²C refers to a communications protocol originally developed by Phillips Semiconductors (now NXP Semiconductors).
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