ADA4859-3* Product Page Quick Links

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- ADA4859-3 Evaluation Board

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- AN-417: Fast Rail-to-Rail Operational Amplifiers Ease Design Constraints in Low Voltage High Speed Systems
- AN-581: Biasing and Decoupling Op Amps in Single Supply Applications

Data Sheet

- ADA4859-3: Single-Supply, Fixed G=2, High Speed, Video Amplifier with Charge Pump Data Sheet

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- UG-140: Universal Evaluation Board for Triple, High Speed Op Amps with Charge Pump Offered in 16-Lead, 4 mm × 4 mm LFCSP Packages

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- MT-032: Ideal Voltage Feedback (VFB) Op Amp
- MT-033: Voltage Feedback Op Amp Gain and Bandwidth
- MT-047: Op Amp Noise
- MT-048: Op Amp Noise Relationships: 1/f Noise, RMS Noise, and Equivalent Noise Bandwidth
- MT-049: Op Amp Total Output Noise Calculations for Single-Pole System
- MT-050: Op Amp Total Output Noise Calculations for Second-Order System
- MT-052: Op Amp Noise Figure: Don't Be Misled
- MT-053: Op Amp Distortion: HD, THD, THD + N, IMD, SFDR, MTPR
- MT-056: High Speed Voltage Feedback Op Amps
- MT-058: Effects of Feedback Capacitance on VFB and CFB Op Amps
- MT-059: Compensating for the Effects of Input Capacitance on VFB and CFB Op Amps Used in Current-to-Voltage Converters
- MT-060: Choosing Between Voltage Feedback and Current Feedback Op Amps

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- PCN-PDN Information
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Discussions

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REVISION HISTORY

11/12—Rev. 0 to Rev. A

Changes to Power-Down Section ... 14

11/08—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = 5 V, G = 2, R_F = 550 Ω, R_L = 150 Ω, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.1 V p-p		265		MHz
	V_{OUT} = 2 V p-p		195		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 2 V p-p, C_L = 6 pF		60		MHz
Slew Rate	V_{OUT} = 2 V step		740		V/µs
Settling Time to 0.1%	V_{OUT} = 2 V step		20		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion (HD2/HD3)	f_C = 1 MHz, V_O = 2 V p-p		−84/−93		dBc
	f_C = 5 MHz, V_O = 2 V p-p		−70/−83		dBc
Crosstalk	f = 5 MHz		−80		dBc
Total Output Noise	f = 1 MHz		17		nV/√Hz
Input Current Noise	f = 1 MHz		2		pA/√Hz
Differential Gain Error			0.01		%
Differential Phase Error			0.02		Degrees
DC PERFORMANCE					
Output Offset Voltage		−25	+9	+25	mV
+Input Bias Current		−2	+0.7	+2	µA
Closed-Loop Gain		1.9	2	2.1	V/V
INPUT CHARACTERISTICS					
Input Resistance	+IN		15		MΩ
Input Capacitance	+IN		1.5		pF
Input Common-Mode Voltage Range		−1.8		+3.8	V
OUTPUT CHARACTERISTICS					
Output Voltage Swing		−1.4 to +3.6	−1.7 to +3.8		V
Output Overdrive Recovery Time	Rise/fall, f = 5 MHz		15		ns
Maximum Linear Output Current @ V_O = 1 V_{PEAK}	f_C = 1 MHz, HD2 ≤ −50 dBc		19		mA
POWER-DOWN					
Input Voltage	Enabled		1.9		V
	Powered down		2		V
Bias Current		−0.1		+0.1	µA
Turn-On Time			0.5		µs
Turn-Off Time			2		µs
POWER SUPPLY					
Operating Range		3		5.5	V
Total Quiescent Current					
Amplifier		15	17	21	mA
Charge Pump			21		mA
Total Quiescent Current When Powered Down					
Amplifier		0.15	0.25	0.3	mA
Charge Pump			4		mA
Positive Power Supply Rejection Ratio	Referred to output		−55	−50	dB
Negative Power Supply Rejection Ratio	Referred to output		−51	−47	dB
Charge Pump Output Voltage		−3.2	−3	−2.5	V
Charge Pump Sink Current				150	mA

T_A = 25°C, V_S = 3.3 V, G = 2, R_F = 550 Ω, R_L = 150 Ω, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.1 V p-p		260		MHz
	V_{OUT} = 2 V p-p		165		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 2 V p-p, C_L = 6 pF		65		MHz
Slew Rate	V_{OUT} = 2 V step, R_L = 150 Ω		530		V/µs
Settling Time to 0.1%	V_{OUT} = 2 V step		20		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 1 MHz, V_O = 2 V p-p		−84/−86		dBc
	f_C = 5 MHz, V_O = 2 V p-p		−73/−77		dBc
Crosstalk	f = 5 MHz		−80		dBc
Total Output Noise	f = 1 MHz		17		nV/√Hz
Input Current Noise	f = 1 MHz		2		pA/√Hz
Differential Gain Error			0.02		%
Differential Phase Error			0.03		Degrees
DC PERFORMANCE					
Output Offset Voltage		−25	+9	+25	mV
+Input Bias Current		−2	+0.7	+2	µA
Closed-Loop Gain		1.9	2	2.1	V/V
INPUT CHARACTERISTICS					
Input Resistance	+IN		15		MΩ
Input Capacitance	+IN		1.5		pF
Input Common-Mode Voltage Range		−0.9		+2.2	V
OUTPUT CHARACTERISTICS					
Output Voltage Swing		−0.7 to +2.1	−1 to +2.3		V
Output Overdrive Recovery Time	Rise/fall, f = 5 MHz		15		ns
Maximum Linear Output Current @ V_O = 1 V_{PEAK}	f_C = 1 MHz, HD2 ≤ −50 dBc		18		mA
POWER-DOWN					
Input Voltage	Enabled		1.25		V
	Powered down		1.35		V
Bias Current		−0.1		+0.1	µA
Turn-On Time			0.5		µs
Turn-Off Time			2		µs
POWER SUPPLY					
Operating Range		3		5.5	V
Total Quiescent Current					
Amplifier		14	17	20	mA
Charge Pump			19		mA
Total Quiescent Current When Powered Down					
Amplifier		0.15	0.25	0.3	mA
Charge Pump			2		mA
Positive Power Supply Rejection Ratio	Referred to output		−54	−50	dB
Negative Power Supply Rejection Ratio	Referred to output		−50	−47	dB
Charge Pump Output Voltage		−2.1	−2	−1.8	V
Charge Pump Sink Current				45	mA

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Internal Power Dissipation[1]	
16-Lead LFCSP	See Figure 2
Input Voltage (Common-Mode)	($-V_S$ – 0.2 V) to ($+V_S$ – 1.8 V)
Differential Input Voltage	$\pm V_S$
Output Short-Circuit Duration	Observe power derating curves
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +105°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] Specification is for device in free air.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the ADA4859-3 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

To ensure proper operation, it is necessary to observe the maximum power derating curves in Figure 2.

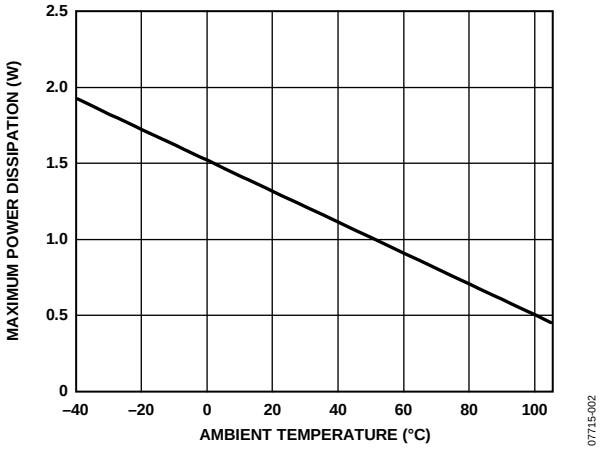

Figure 2. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

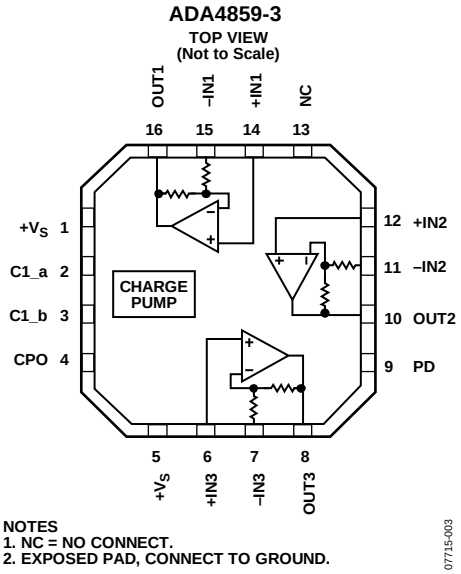

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$+V_S$	Positive Supply for Charge Pump.
2	C1_a	Charge Pump Capacitor Side a.
3	C1_b	Charge Pump Capacitor Side b.
4	CPO	Charge Pump Output.
5	$+V_S$	Positive Supply.
6	+IN3	Noninverting Input 3.
7	–IN3	Inverting Input 3.
8	OUT3	Output 3.
9	PD	Power Down.
10	OUT2	Output 2.
11	–IN2	Inverting Input 2.
12	+IN2	Noninverting Input 2.
13	NC	No Connect.
14	+IN1	Noninverting Input 1.
15	–IN1	Inverting Input 1.
16	OUT1	Output 1.
17 (EPAD)	Exposed Pad (EPAD)	The exposed pad must be connected to the ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, G = 2, R_F = 550 Ω, R_L = 150 Ω, large signal V_{OUT} = 2 V p-p, small signal V_{OUT} = 0.1 V p-p, and T = 25°C, unless otherwise noted.

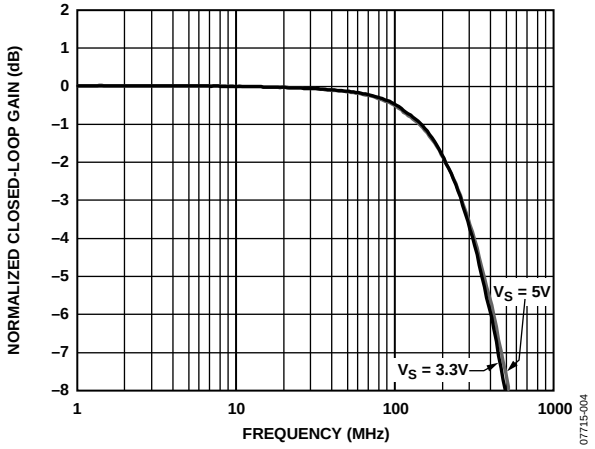

Figure 4. Small Signal Frequency Response vs. Supply Voltage

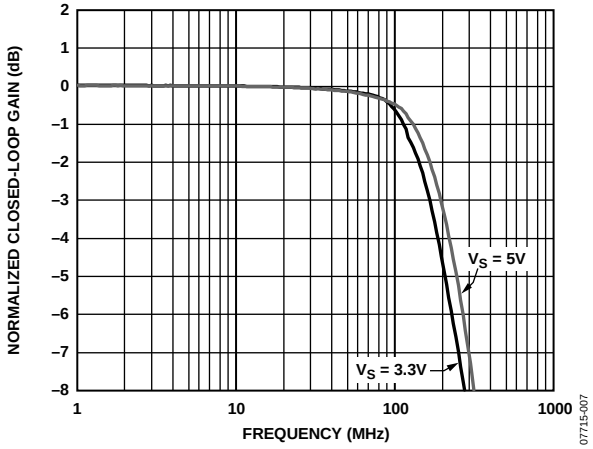

Figure 7. Large Signal Frequency Response vs. Supply Voltage

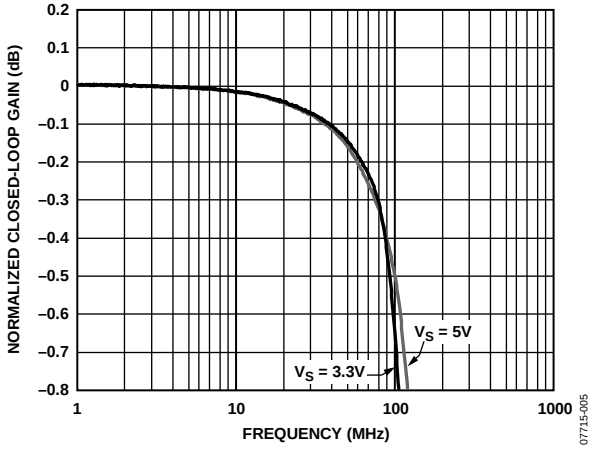

Figure 5. Large Signal 0.1 dB Flatness vs. Supply Voltage

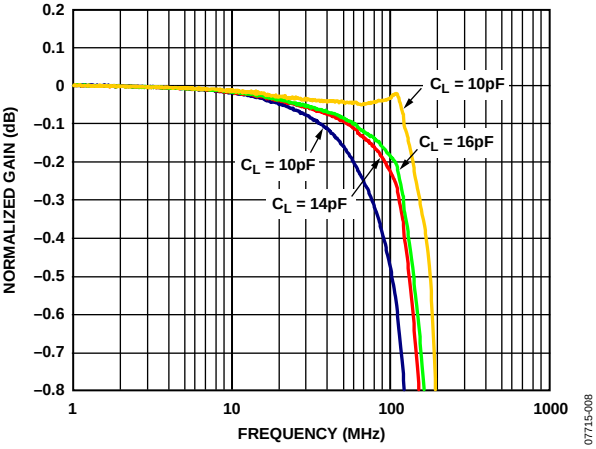

Figure 8. Large Signal 0.1 dB Flatness vs. Capacitive Load

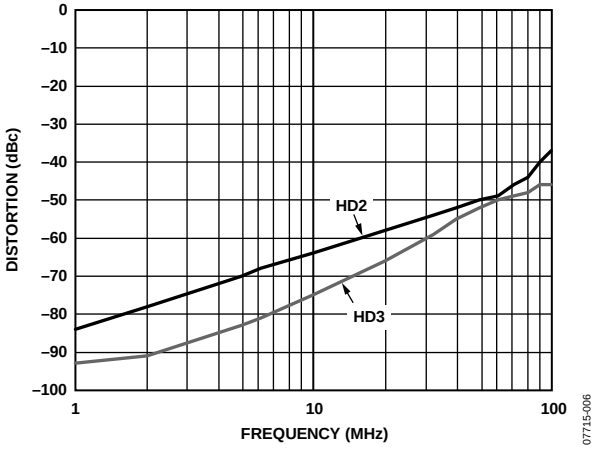

Figure 6. Harmonic Distortion vs. Frequency

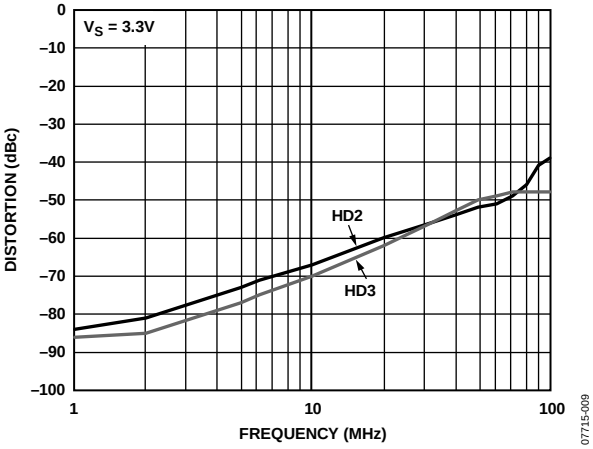

Figure 9. Harmonic Distortion vs. Frequency

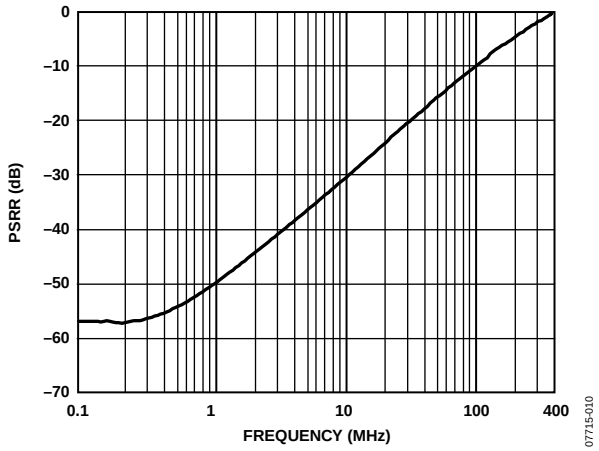

Figure 10. Power Supply Rejection Ratio (PSRR) vs. Frequency

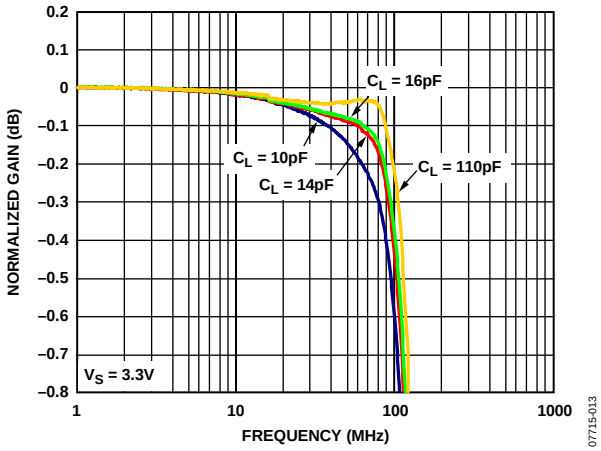

Figure 13. Large Signal 0.1 dB Flatness vs. Capacitive Load

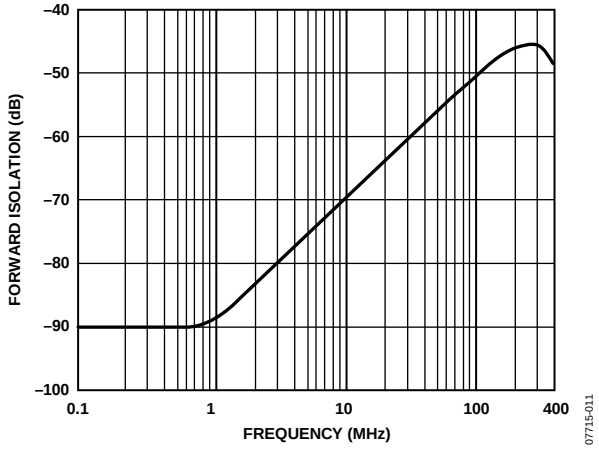

Figure 11. Forward Isolation vs. Frequency

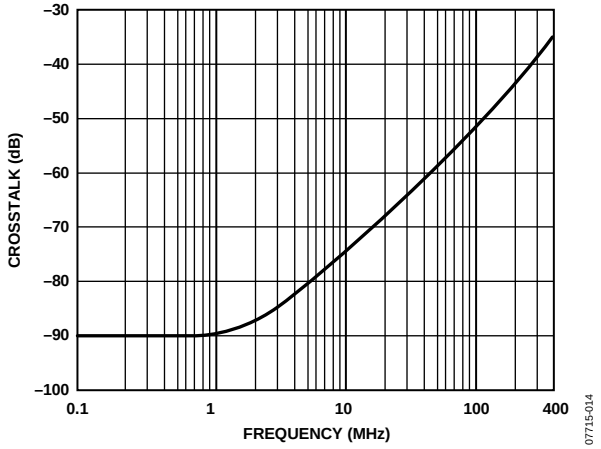

Figure 14. Crosstalk vs. Frequency

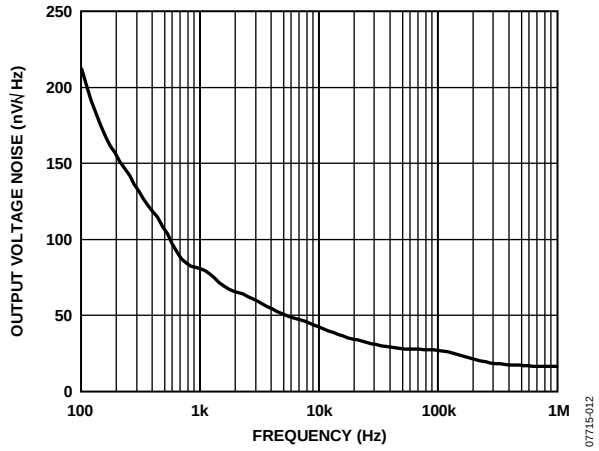

Figure 12. Total Output Voltage Noise vs. Frequency

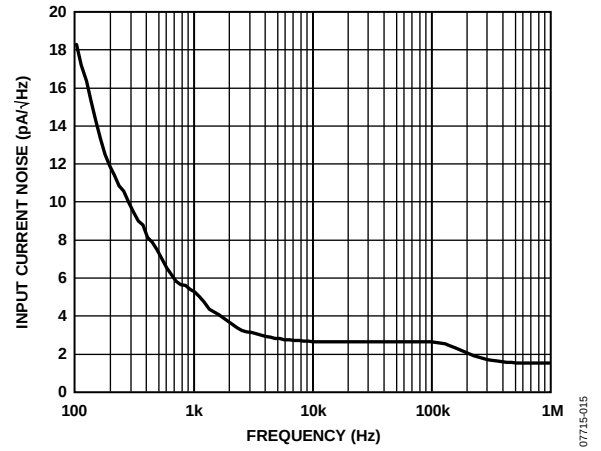

Figure 15. Noninverting Input Current Noise vs. Frequency

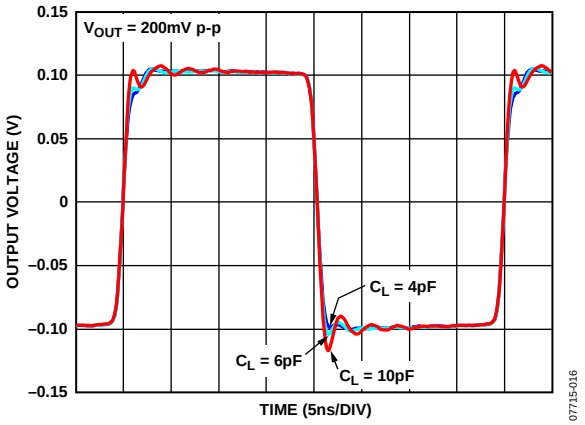

Figure 16. Small Signal Transient Response vs. Capacitive Load

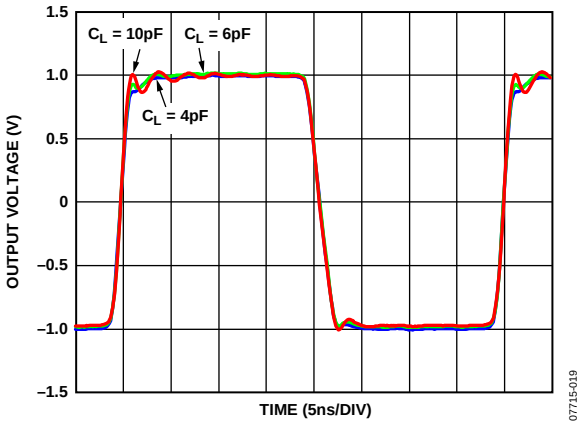

Figure 19. Large Signal Transient Response vs. Capacitive Load

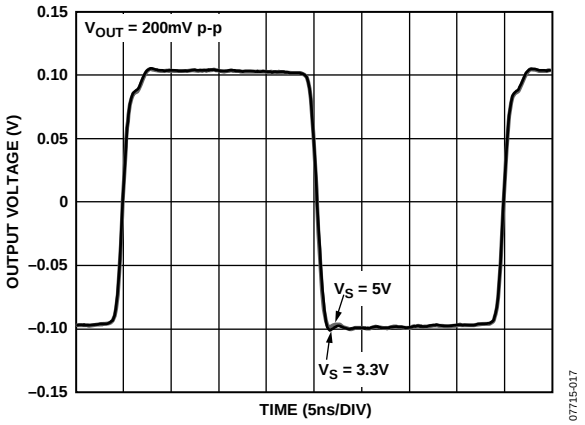

Figure 17. Small Signal Transient Response vs. Supply Voltage, C_L = 4 pF

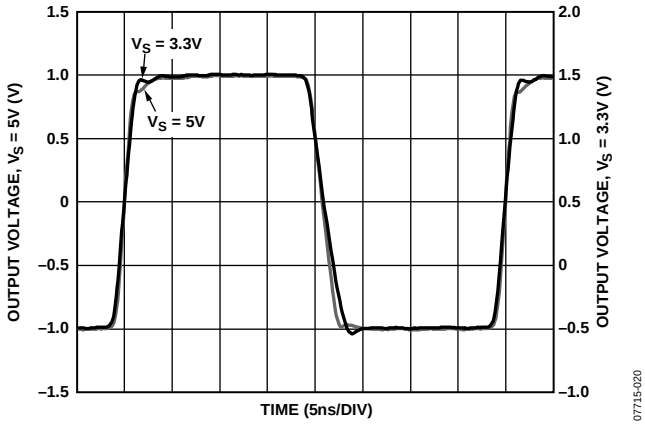

Figure 20. Large Signal Transient Response vs. Supply Voltage, C_L = 4 pF

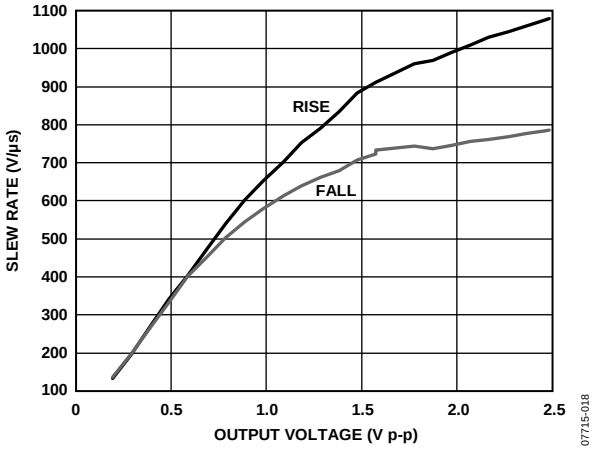

Figure 18. Slew Rate vs. Output Voltage

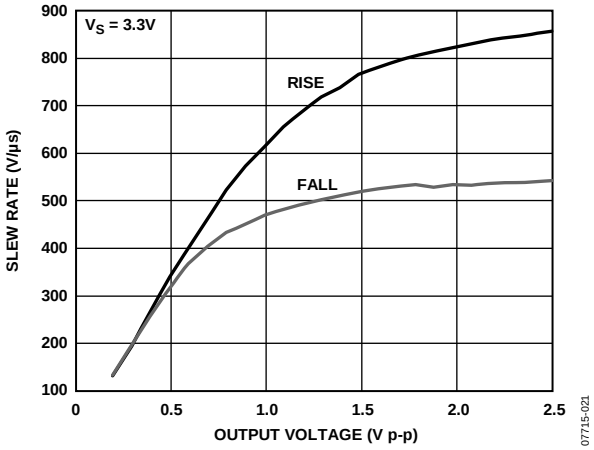

Figure 21. Slew Rate vs. Output Voltage

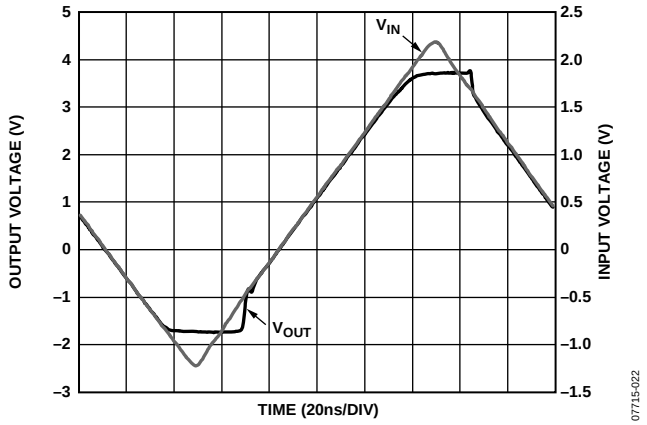

Figure 22. Output Overdrive Recovery

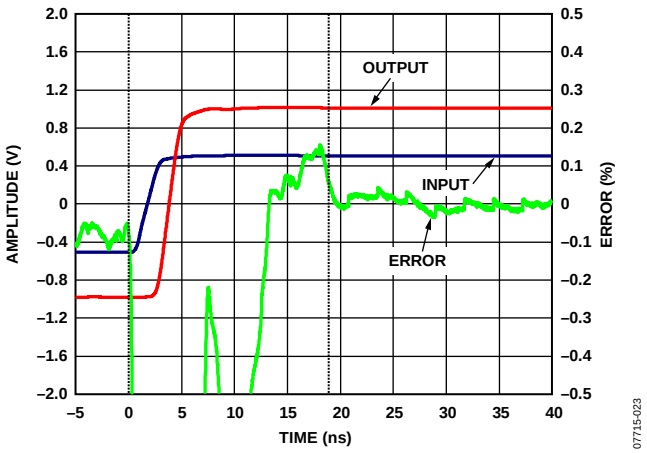

Figure 23. Settling Time (Rise)

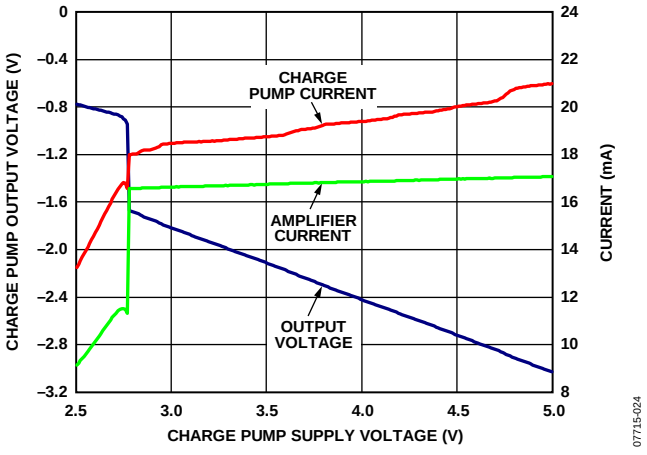

Figure 24. Charge Pump Voltage and Current vs. Supply Voltage

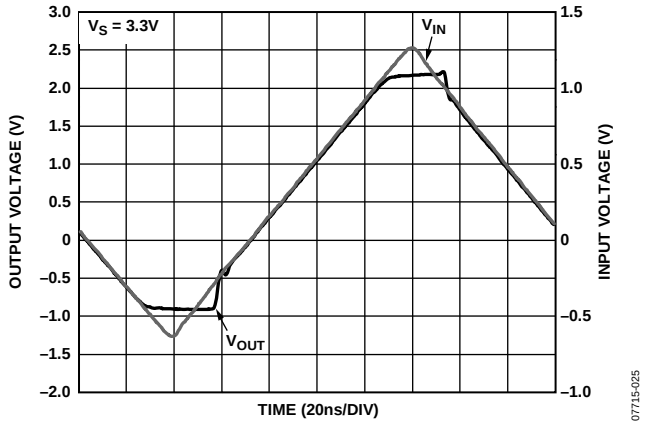

Figure 25. Output Overdrive Recovery

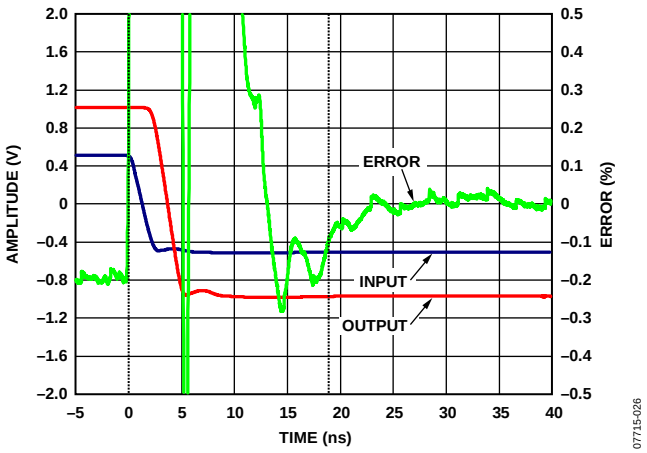

Figure 26. Settling Time, (Fall)

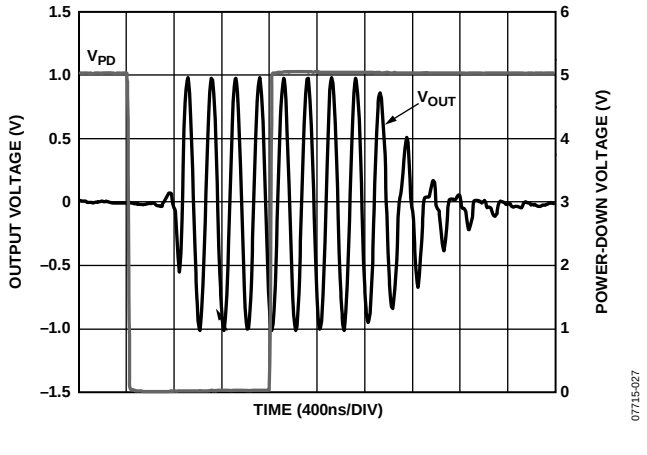

Figure 27. Enable/Power-Down Time

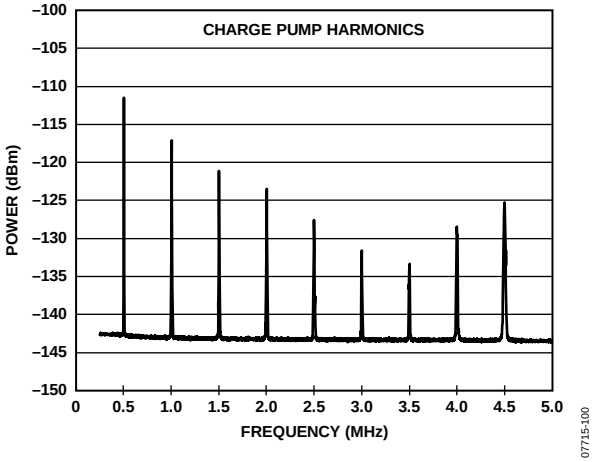

Figure 28. Output Spectrum vs. Frequency

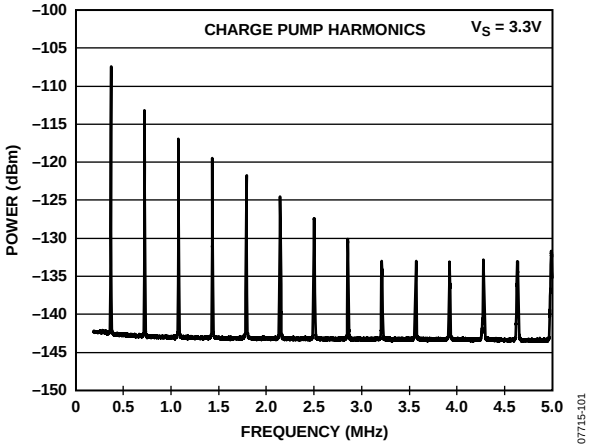

Figure 29. Output Spectrum vs. Frequency

THEORY OF OPERATION

OVERVIEW

The ADA4859-3 is a fixed gain of two, current feedback amplifier designed for exceptional performance as a triple video amplifier. Its specifications make it especially suitable for SD and HD video applications. The ADA4859-3 provides HD video output on a single supply as low as 3.0 V while only consuming 13 mA per amplifier. It also features a power-down pin (PD) that reduces the quiescent current to 4 mA when activated.

The ADA4859-3 can be used in applications that require both ac- and dc-coupled inputs and outputs. The output stage on the ADA4859-3 is capable of driving 2 V p-p video signals into two doubly terminated video loads (150 Ω each) on a single 5 V supply. The input range of the ADA4859-3 includes ground, whereas the output range is limited by the output headroom set by the voltage drop across two diodes from each rail, which occurs 1.2 V from the positive and negative supply rails.

CHARGE PUMP OPERATION

The on-board charge pump creates a negative supply for the amplifier. It provides different negative voltages depending on the power supply voltage. For a +5 V supply, the negative supply generated is equal to −3 V with 150 mA of output supply current, and for a +3.3 V supply, the negative supply is equal to −2 V with 45 mA of output supply current.

Figure 30 shows the charging cycle when the supply voltage, $+V_S$, charges C1 through Φ_1 to ground. During this cycle, C1 quickly charges to reach the $+V_S$ voltage. The discharge cycle then begins with switching Φ_1 off and switching Φ_2 on, as shown in Figure 31. When C1 = C2, the charge in C1 is divided between the two capacitors and slowly increases the voltage in C2 until it reaches a predetermined voltage (−3 V for the +5 V supply and −2 V for the +3.3 V supply). The typical charge pump charging and discharging frequency is 550 kHz with a 150 Ω load and no input signal. This frequency changes with the load current, and it can get much slower if the amplifier is powered down and no external current is used.

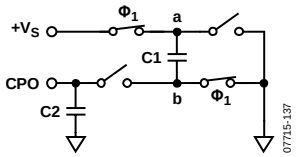

Figure 30. Charging Cycle

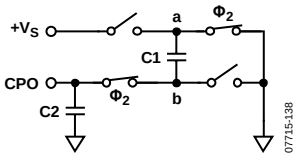

Figure 31. Discharging Cycle

The ADA4859-3 specifications make it especially suitable for SD and HD video applications. It also allows dc-coupled video signal with its black level set to 0 V and its sync tip down to −300 mV for YPbPr video.

The charge pump is always on, even when the power-down pin (PD) is enabled and the amplifier is off. However, it would be in an idle state if the negative current were not used. Each amplifier needs −6.3 mA of current, which totals −19 mA for all three amplifiers. This means additional negative current may be available by the charge pump for external use. Pin 4 (CPO) is the charge pump output, which provides access to the negative supply generated by the charge pump. Placing a 1 µF charge capacitor at the CPO pin is essential to hold the charge and regulate the ripple.

If the negative supply is used to power another device in the system, it is only possible for the 5 V supply operation. In the 3.3 V supply operation, the charge pump output current is very limited. The capacitor at the CPO pin, which regulates the ripple of the negative voltage, can be used as a coupling capacitor for the external device. However, the charge pump current should be limited to a maximum of 50 mA for external use. When powering down the ADA4859-3, the charge pump is not affected and its output voltage and current remain available for external use.

APPLICATIONS INFORMATION

USING THE ADA4859-3 IN GAINS EQUAL TO +1, −1

The ADA4859-3 was designed to offer outstanding video performance, simplify applications, and minimize board area.

The ADA4859-3 is a triple amplifier with on-chip feedback and gain set resistors. The gain is fixed internally at G = +2. The inclusion of the on-chip resistors not only simplifies the design of the application but also eliminates six surface-mount resistors, saving valuable board space and lowering assembly costs. Although the ADA4859-3 has a fixed gain of G = +2, it can be used in other gain configurations, such as G = −1 and G = +1.

Unity-Gain Operation

Option 1

There are two options for obtaining unity gain (G = +1). The first is shown in Figure 32. In this configuration, the −IN input pin is tied to the output. (Feedback is provided through the two internal 550 Ω resistors in parallel), and the input is applied to the noninverting input. The noise gain for this configuration is 1.

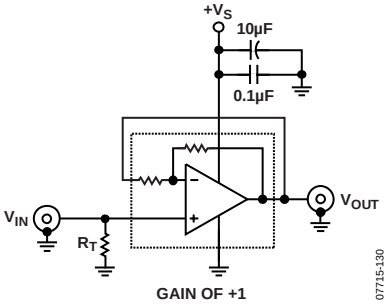

Figure 32. Unity Gain of Option 1

Option 2

Another option exists for running the ADA4859-3 as a unity-gain amplifier. In this configuration, the noise gain is +2, see Figure 33. The frequency response and transient response for this configuration closely match the gain of +2 plots because the noise gains are equal. This method does have twice the noise gain of Option 1; however, in applications that do not require low noise, Option 2 offers less peaking and ringing. By tying the inputs together, the net gain of the amplifier becomes +1. Equation 1 shows the transfer characteristic for the schematic shown in Figure 33.

$$V_{OUT} = V_{IN}\left(\frac{-R_F}{R_G}\right) + V_{IN}\left(\frac{R_F + R_G}{R_G}\right) \quad (1)$$

which simplifies to $V_{OUT} = V_{IN}$.

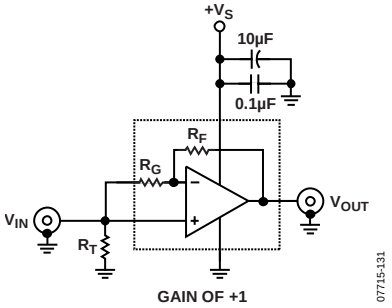

Figure 33. Unity Gain of Option 2

Inverting Unity-Gain Operation

In this configuration, the noninverting input is tied to ground and the input signal is applied to the inverting input. The noise gain for this configuration is +2, see Figure 34.

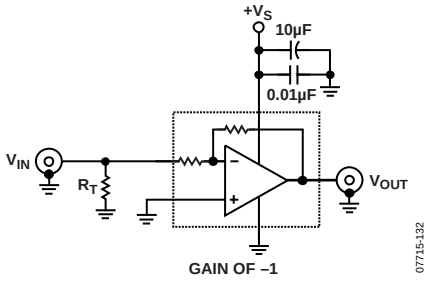

Figure 34. Inverting Configuration (G = −1)

Figure 35 shows the small signal frequency response for both gain of +1 (Option 1 and Option 2) and gain of −1 configurations. It is clear that the G = +1 Option 2 has better flatness and no peaking compared to Option 1.

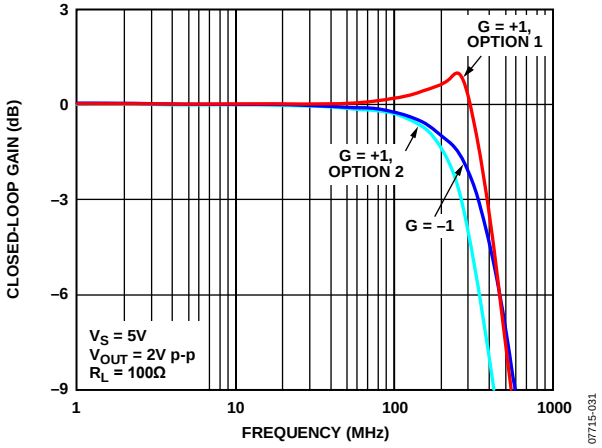

Figure 35. Large Signal, G = +1 and G = −1

VIDEO LINE DRIVER

The ADA4859-3 was designed to excel in video driver applications. Figure 36 shows a typical schematic for a video driver operating on bipolar supplies.

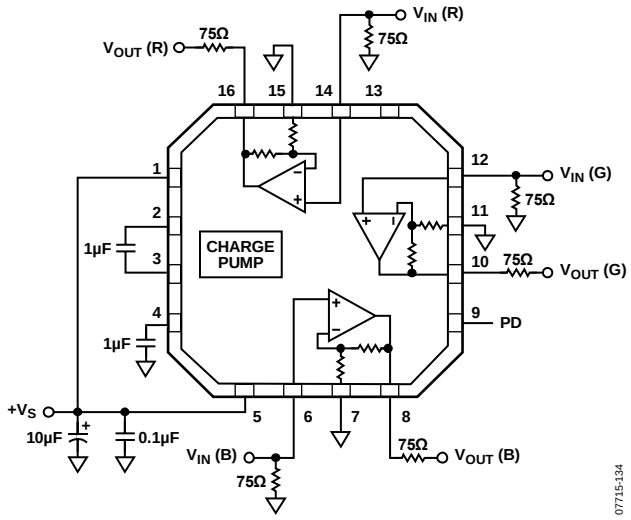

Figure 36. Video Driver Schematic

In applications that require multiple video loads be driven simultaneously, the ADA4859-3 can deliver. Figure 37 shows the ADA4859-3 configured with two video loads, and Figure 38 shows the large signal performance for multiple video loads.

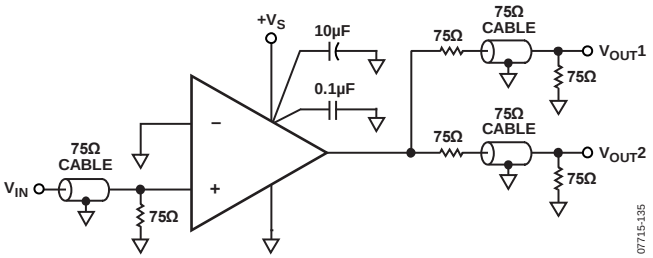

Figure 37. Video Driver Schematic for Two Video Loads

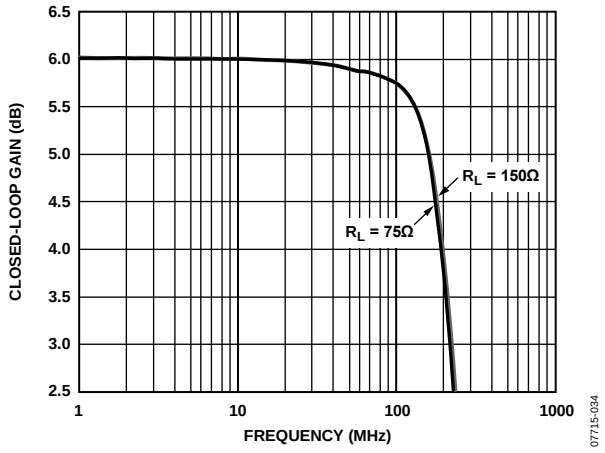

Figure 38. Large Signal Frequency Response for Various Loads

POWER-DOWN

The ADA4859-3 is equipped with a PD (power-down) pin for all three amplifiers. This allows the user the ability to reduce the quiescent supply current when an amplifier is not active. The power-down threshold levels are derived from ground level. The amplifiers are powered down when the voltage applied to the PD pin is greater than a certain voltage from ground. In a 5 V supply application, the voltage is greater than 2 V, and in a 3.3 V supply application, the voltage is greater than 1.5 V. The amplifier is enabled whenever the PD pin is connected to ground. If the PD pin is not used, it is best to connect it to ground. Note that the power-down feature does not control the charge pump output voltage and current.

Table 5. Power-Down Voltage Control

PD Pin	5 V	3.3 V
Not Active	<1.5 V	<1 V
Active	>2 V	>1.5 V

LAYOUT CONSIDERATIONS

As is the case with all high speed applications, careful attention to printed circuit board (PCB) layout details prevents associated board parasitics from becoming problematic. Proper RF design technique is mandatory. The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance return path. Removing the ground plane on all layers from the area near the input and output pins reduces stray capacitance. Locate termination resistors and loads as close as possible to their respective inputs and outputs. Keep input and output traces as far apart as possible to minimize coupling (crosstalk) through the board. Adherence to microstrip or stripline design techniques for long signal traces (greater than about 1 inch) is recommended.

POWER SUPPLY BYPASSING

Careful attention must be paid to bypassing the power supply pins of the ADA4859-3. Use high quality capacitors with low equivalent series resistance (ESR), such as multilayer ceramic capacitors (MLCCs), to minimize supply voltage ripple and power dissipation. A large, usually tantalum, 10 µF to 47 µF capacitor located in proximity to the ADA4859-3 is required to provide good decoupling for lower frequency signals. In addition, locate 0.1 µF MLCC decoupling capacitors as close to each of the power supply pins as is physically possible, no more than 1/8-inch away. The ground returns should terminate immediately into the ground plane. Locating the bypass capacitor return close to the load return minimizes ground loops and improves performance.

OUTLINE DIMENSIONS

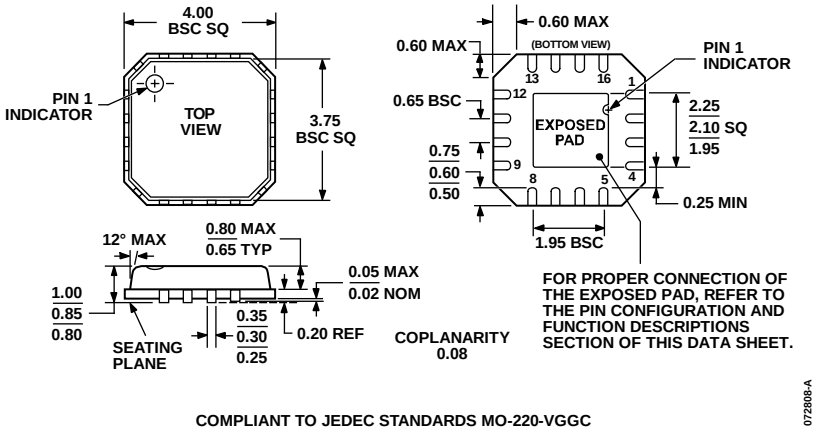

Figure 39.16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad (CP-16-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADA4859-3ACPZ-R2	–40°C to +105°C	16-Lead LFCSP_VQ	CP-16-4	250
ADA4859-3ACPZ-R7	–40°C to +105°C	16-Lead LFCSP_VQ	CP-16-4	1,500
ADA4859-3ACPZ-RL	–40°C to +105°C	16-Lead LFCSP_VQ	CP-16-4	5,000
ADA4859-3ACP-EBZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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