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Updated Outline Dimensions ... 13
Changes to Ordering Guide ... 13

3/2010—Rev. F to Rev. G
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1/2010—Rev. E to Rev. F
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8/2007—Rev. D to Rev. E
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2/2006—Rev. C to Rev. D
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3/2004—Rev. B to Rev. C
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10/2001—Rev. 0 to Rev. A
Edit to 16-Lead CSP and 5-Lead SC70 Pin Configuration ... 1
Edit to Ordering Guide ... 3

7/2001—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

4.5 V ≤ V_S ≤ 16 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			2	10	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +85°C		5		µV/°C
Input Bias Current	I_B			80	600	nA
		−40°C ≤ T_A ≤ +85°C			800	nA
Input Offset Current	I_{OS}			1	80	nA
		−40°C ≤ T_A ≤ +85°C			130	nA
Input Voltage Range		Common-mode input	−0.5		V_S + 0.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to V_S, −40°C ≤ T_A ≤ +85°C	54	95		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.5 V to (V_S − 0.5 V)	3	10		V/mV
Input Impedance	Z_{IN}			400		kΩ
Input Capacitance	C_{IN}			1		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 100 µA		V_S − 0.005		V
		V_S = 16 V, I_L = 5 mA	15.85	15.95		V
		−40°C ≤ T_A ≤ +85°C	15.75			V
		V_S = 4.5 V, I_L = 5 mA	4.2	4.38		V
		−40°C ≤ T_A ≤ +85°C	4.1			V
Output Voltage Low	V_{OL}	I_L = 100 µA		5		mV
		V_S = 16 V, I_L = 5 mA		42	150	mV
		−40°C ≤ T_A ≤ +85°C			250	mV
		V_S = 4.5 V, I_L = 5 mA		95	300	mV
		−40°C ≤ T_A ≤ +85°C			400	mV
Continuous Output Current	I_{OUT}			35		mA
Peak Output Current	I_{PK}	V_S = 16 V		250		mA
POWER SUPPLY						
Supply Voltage	V_S		4.5		16	V
Power Supply Rejection Ratio	PSRR	V_S = 4 V to 17 V, −40°C ≤ T_A ≤ +85°C	70	90		dB
Supply Current/Amplifier	I_{SY}	V_O = V_S/2, no load		700	850	µA
		−40°C ≤ T_A ≤ +85°C			1	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 200 pF	4	6		V/µs
Gain Bandwidth Product	GBP	R_L = 10 kΩ, C_L = 10 pF		5		MHz
Phase Margin	$Ø_m$	R_L = 10 kΩ, C_L = 10 pF		65		Degrees
Channel Separation				75		dB
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		26		nV/√Hz
	e_n	f = 10 kHz		25		nV/√Hz
Current Noise Density	i_n	f = 10 kHz		0.8		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (V_S)	18 V
Input Voltage	−0.5 V to V_S + 0.5 V
Differential Input Voltage	V_S
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

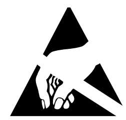
θ_{JA} is specified for worst-case conditions, that is, for a device soldered onto a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead SC70 (KS-5)	376	126	°C/W
8-Lead MSOP (RM-8)	210	45	°C/W
14-Lead TSSOP (RU-14)	180	35	°C/W
16-Lead LFCSP (CP-16-23)	38[1]	30[1]	°C/W

[1] DAP is soldered down to the printed circuit board (PCB).

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

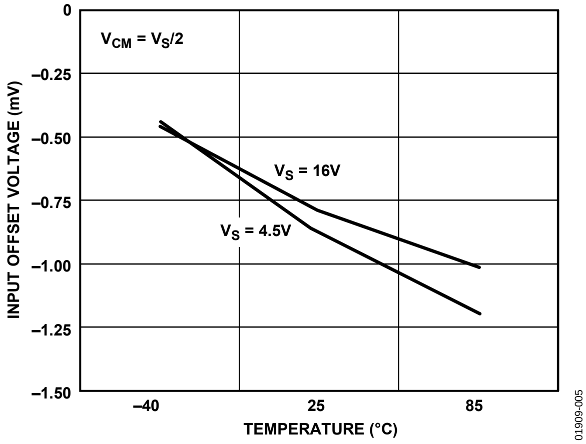


Figure 5. Input Offset Voltage vs. Temperature

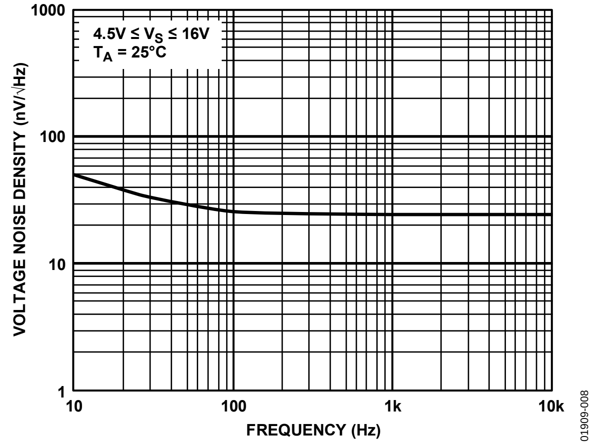


Figure 8. Voltage Noise Density vs. Frequency

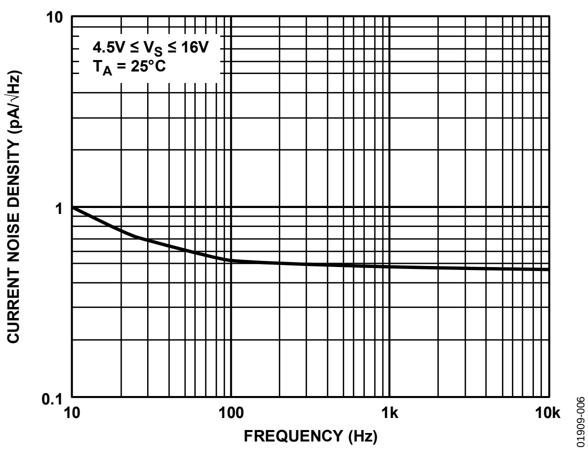


Figure 6. Current Noise

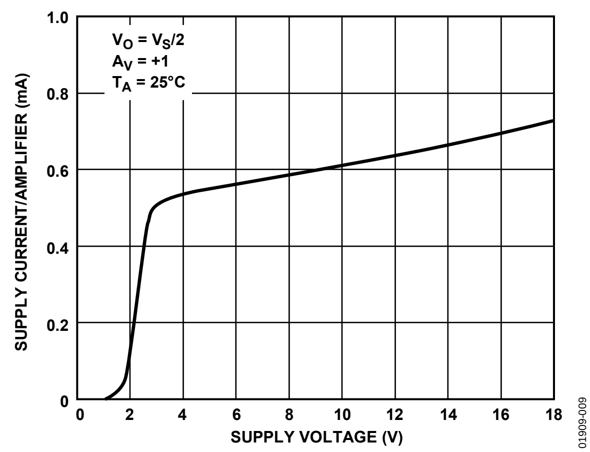


Figure 9. Supply Current/Amplifier vs. Supply Voltage

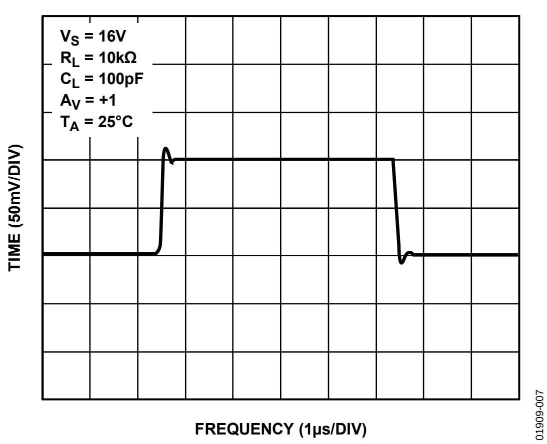


Figure 7. Small Signal Transient Response

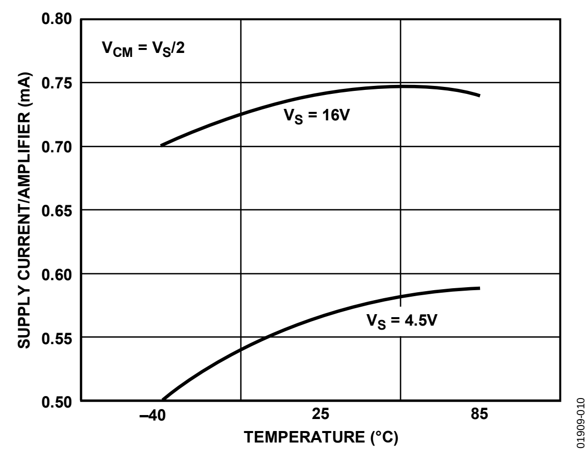


Figure 10. Supply Current/Amplifier vs. Temperature

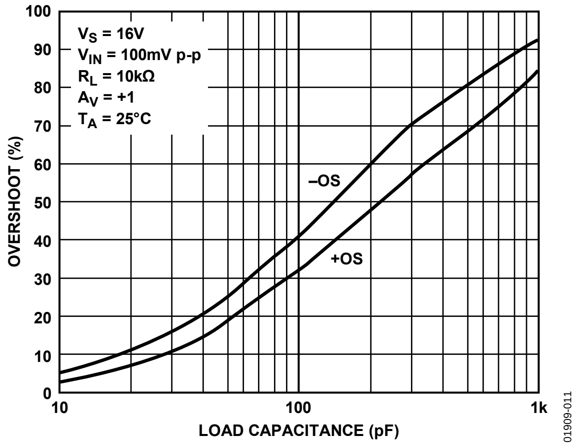


Figure 11. Small Signal Overshoot vs. Load Capacitance

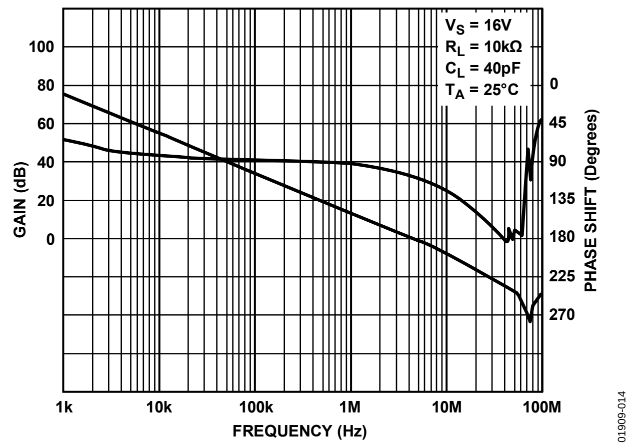


Figure 14. Open-Loop Gain and Phase Shift vs. Frequency

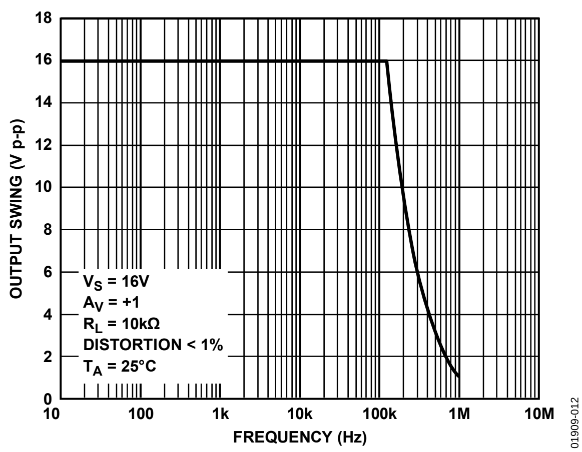


Figure 12. Closed-Loop Output Swing vs. Frequency

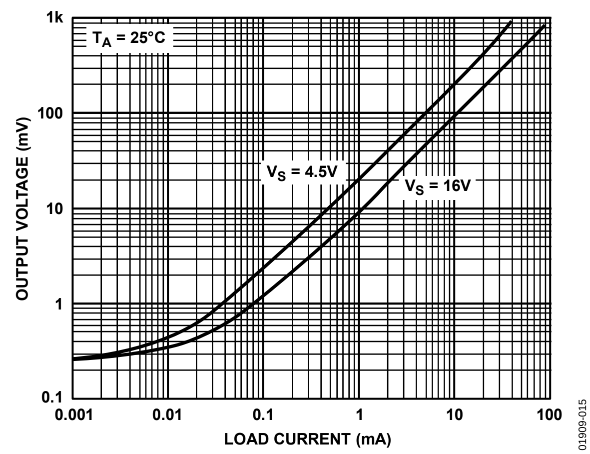


Figure 15. Output Voltage to Supply Rail vs. Load Current

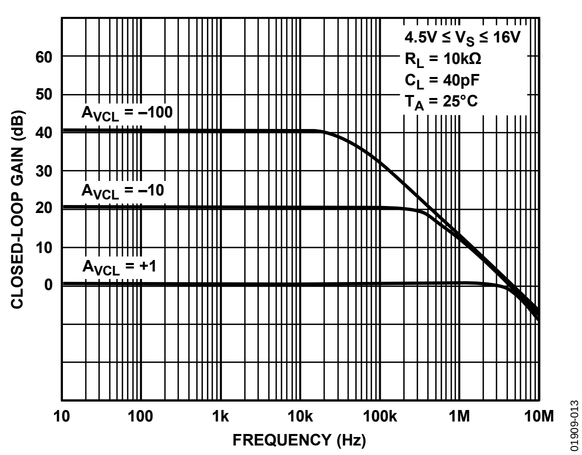


Figure 13. Closed-Loop Gain vs. Frequency

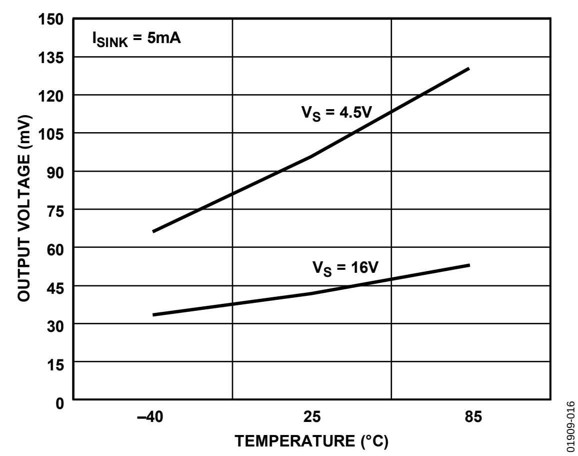


Figure 16. Output Voltage Swing to Rail vs. Temperature

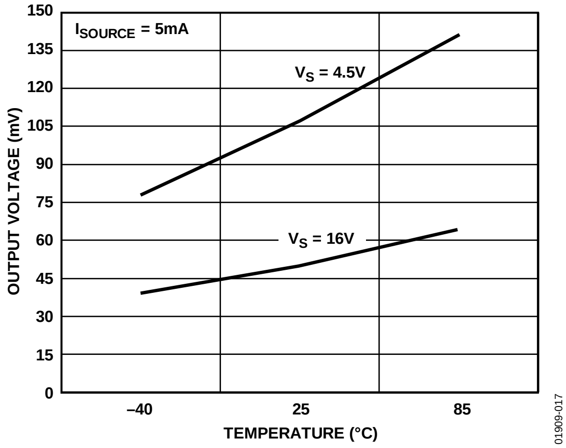


Figure 17. Output Voltage Swing to Rail vs. Temperature

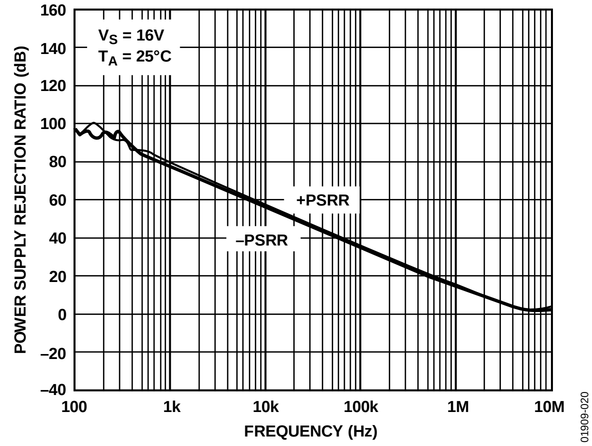


Figure 20. Power Supply Rejection Ratio vs. Frequency

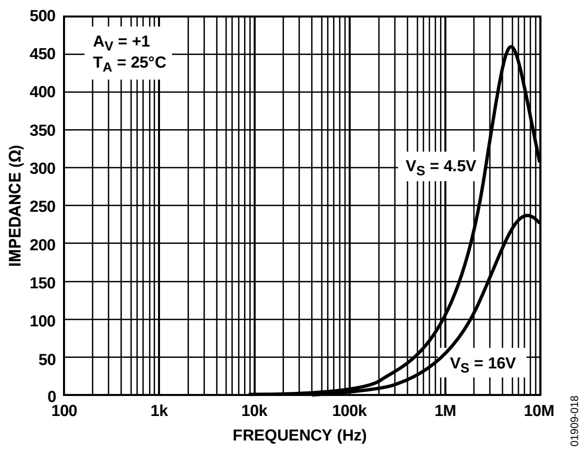


Figure 18. Closed-Loop Output Impedance vs. Frequency

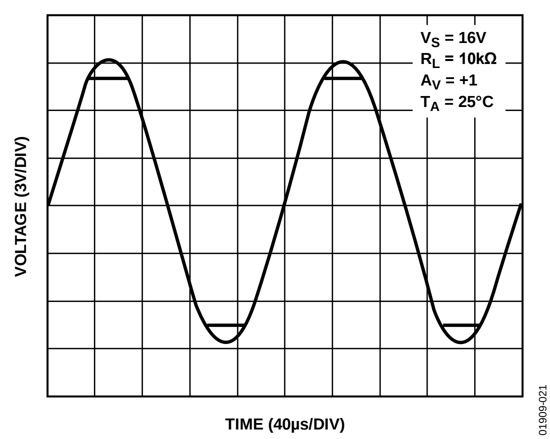


Figure 21. No Phase Reversal

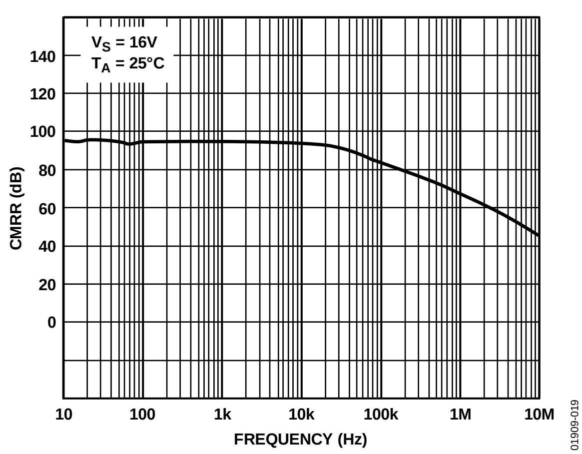


Figure 19. Common-Mode Rejection Ratio (CMRR) vs. Frequency

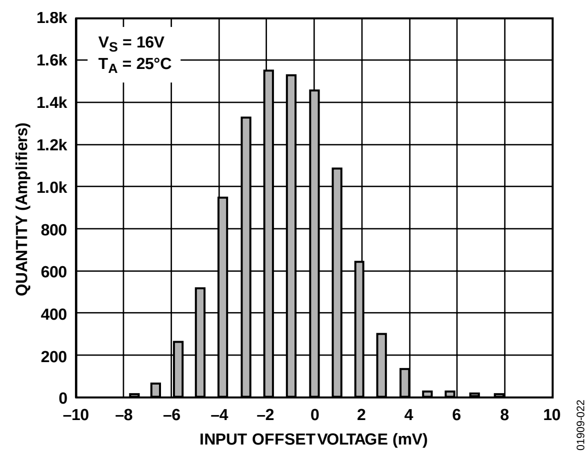


Figure 22. Input Offset Voltage Distribution

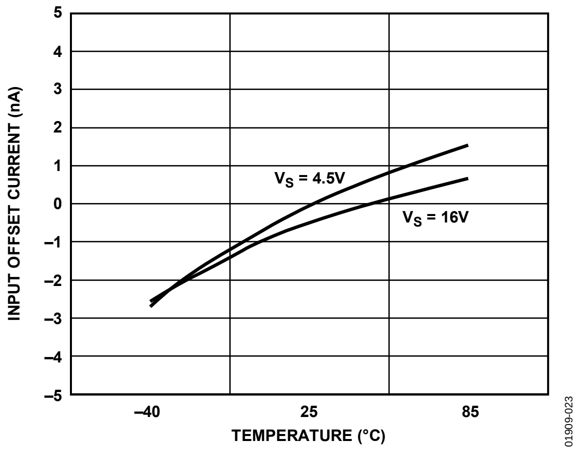


Figure 23. Input Offset Current vs. Temperature

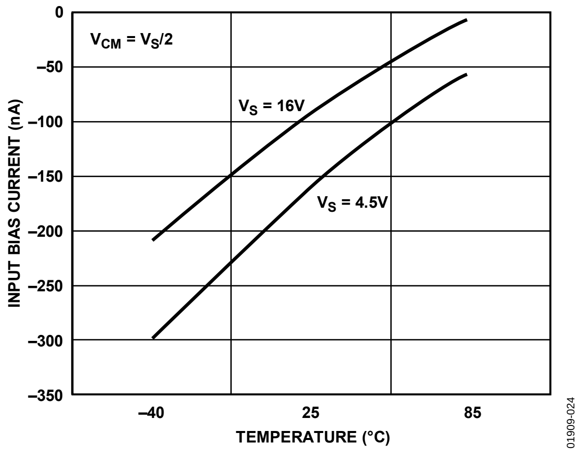


Figure 24. Input Bias Current vs. Temperature

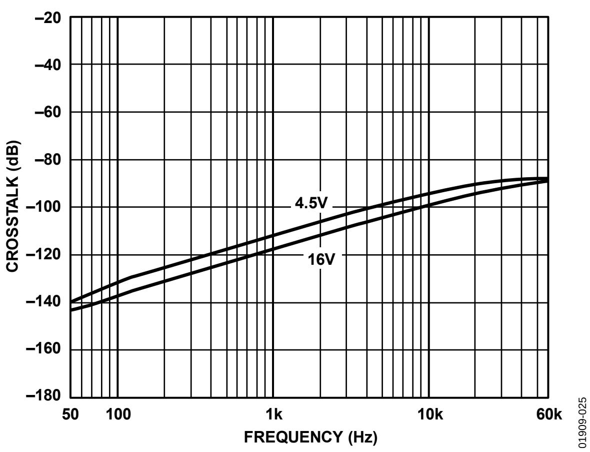


Figure 25. Channel A vs. Channel B Crosstalk

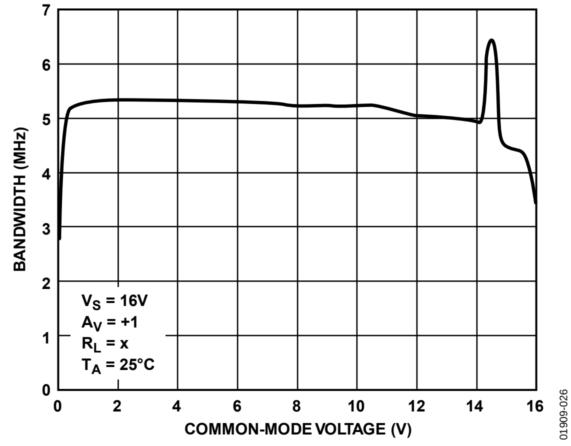


Figure 26. Frequency vs. Common-Mode Voltage (V_S = 16 V)

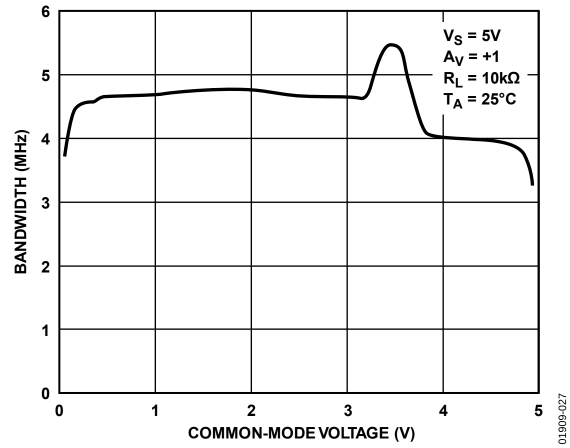


Figure 27. Frequency vs. Common-Mode Voltage (V_S = 5 V)

THEORY OF OPERATION

The AD8565/AD8566/AD8567 are designed to drive large capacitive loads in LCD applications. They have high output current drive and rail-to-rail input/output operation and are powered from a single 16 V supply. They are also intended for other applications where low distortion and high output current drive are needed.

Figure 28 shows a simplified equivalent circuit for the AD8565/AD8566/AD8567. The rail-to-rail bipolar input stage is composed of two PNP differential pairs, Q4 to Q5 and Q10 to Q11, operating in series with diode protection networks, D1 to D2. Diode network D1 to D2 serves as protection against large transients for Q4 to Q5 to accommodate rail-to-rail input swing. D5 to D6 protect Q10 to Q11 against Zenering. In normal operation, Q10 to Q11 are off, and their input stage is buffered from the operational amplifier inputs by Q6 to D3 and Q8 to D4.

Operation of the input stage is best understood as a function of applied common-mode voltage: when the inputs of the AD8565/AD8566/AD8567 are biased midway between the supplies, the differential signal path gain is controlled by resistive loads Q4 to Q5 (via R9, R10). As the input common-mode level is reduced toward the negative supply (V_{NEG} or GND), the input transistor current sources, I1 and I2, are forced into saturation, thereby forcing the Q6 to D3 and Q8 to D4 networks into cutoff. However, Q4 to Q5 remain active, providing input stage gain.

Inversely, when common-mode input voltage is increased toward the positive supply, Q4 to Q5 are driven into cutoff, Q3 is driven into saturation, and Q4 becomes active, providing bias to the Q10 to Q11 differential pair. The point at which the Q10 to Q11 differential pair becomes active is approximately equal to (V_{POS} − 1 V).

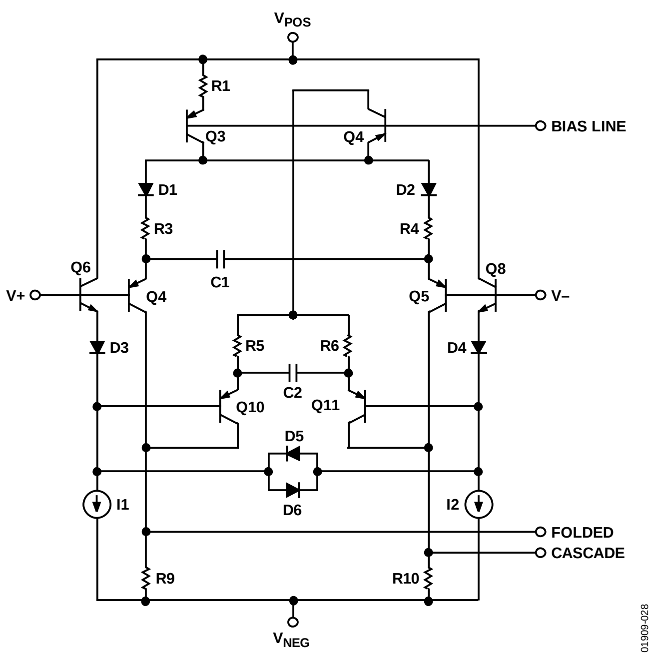


Figure 28. AD8565/AD8566/AD8567 Equivalent Input Circuit

The benefit of this type of input stage is low bias current. The input bias current is the sum of base currents of Q4 to Q5 and Q6 to Q8 over the range from (V_{NEG} + 1 V) to (V_{POS} − 1 V). Outside this range, the input bias current is dominated by the sum of base currents of Q10 to Q11 for input signals close to V_{NEG} and of Q6 to Q8 (Q10 to Q11) for signals close to V_{POS}. From this type of design, the input bias current of the AD8565/AD8566/AD8567 not only exhibits different amplitude but also exhibits different polarities. Figure 29 provides the characteristics of the input bias current vs. the common-mode voltage. It is important to keep in mind that the source impedances driving the inputs are balanced for optimum dc and ac performance.

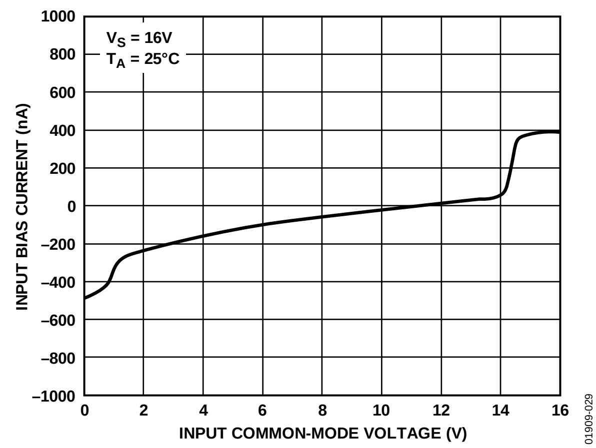


Figure 29. AD8565/AD8566/AD8567 Input Bias Current vs. Common-Mode Voltage

To achieve rail-to-rail output performance, the AD8565/AD8566/AD8567 design uses a complementary common-source (or gmRL) output. This configuration allows output voltages to approach the power supply rails, particularly if the output transistors are allowed to enter the triode region on extremes of signal swing, which are limited by V_{GS}, the transistor sizes, and output load current. In addition, this type of output stage exhibits voltage gain in an open-loop gain configuration. The amount of gain depends on the total load resistance at the output of the AD8565/AD8566/AD8567.

INPUT OVERVOLTAGE PROTECTION

As with any semiconductor device, whenever the input exceeds either supply voltages, attention needs to be paid to the input overvoltage characteristics. As an overvoltage occurs, the amplifier could be damaged, depending on the voltage level and the magnitude of the fault current. When the input voltage exceeds either supply by more than 0.6 V, internal positive-negative (pn) junctions allow current to flow from the input to the supplies.

This input current is not inherently damaging to the device as long as it is limited to 5 mA or less. If a condition exists using the AD8565/AD8566/AD8567 where the input exceeds the supply more than 0.6 V, an external series resistor must be added. The size of the resistor can be calculated by using the maximum over-voltage divided by 5 mA. This resistance must be placed in series with either input exposed to an overvoltage.

OUTPUT PHASE REVERSAL

The AD8565/AD8566/AD8567 are immune to phase reversal. Although device output does not change phase, large currents due to input overvoltage could damage the device. In applications where the possibility of an input voltage exceeding the supply voltage exists, overvoltage protection must be used as described in the Input Overvoltage Protection section.

POWER DISSIPATION

The maximum allowable internal junction temperature of 150°C limits the maximum power dissipation of AD8565/AD8566/AD8567 devices. As the ambient temperature increases, the maximum power dissipated by AD8565/AD8566/AD8567 devices must decrease linearly to maintain maximum junction temperature. If this maximum junction temperature is exceeded momentarily, the device still operates properly once the junction temperature is reduced below 150°C. If the maximum junction temperature is exceeded for an extended period, overheating could lead to permanent damage of the device.

The maximum safe junction temperature, T_{JMAX}, is 150°C. Using the following formula, the maximum power that an AD8565/AD8566/AD8567 device can safely dissipate as a function of temperature can be obtained:

$$P_{DISS} = T_{JMAX} - T_A/\theta_{JA}$$

where:
P_{DISS} is the AD8565/AD8566/AD8567 power dissipation.
T_{JMAX} is the AD8565/AD8566/AD8567 maximum allowable junction temperature (150°C).
T_A is the ambient temperature of the circuit.
θ_{JA} is the AD8565/AD8566/AD8567 package thermal resistance, junction-to-ambient.

The power dissipated by the device can be calculated as

$$P_{DISS} = (V_S - V_{OUT}) \times I_{LOAD}$$

where:
V_S is the supply voltage.
V_{OUT} is the output voltage.
I_{LOAD} is the output load current.

Figure 30 shows the maximum power dissipation vs. temperature. To achieve proper operation, use the previous equation to calculate P_{DISS} for a specific package at any given temperature or use Figure 30.

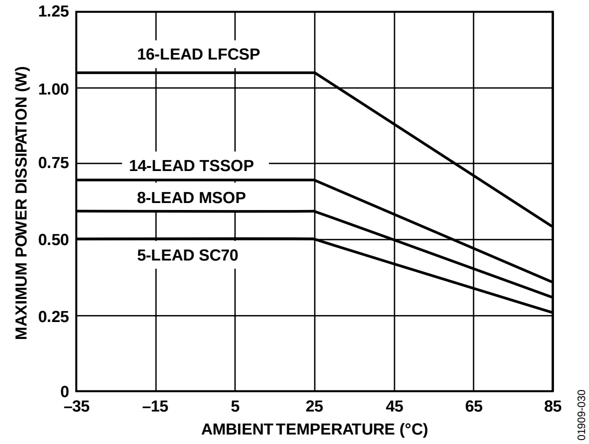


Figure 30. Maximum Power Dissipation vs. Temperature for 5-Lead SC70, 8-Lead MSOP, 14-Lead TSSOP, and 16-Lead LFCSP Packages

THERMAL PAD—AD8567

The AD8567 LFCSP comes with a thermal pad that is attached to the substrate. This substrate is connected to the most positive supply, that is, Pin 3 in the LFCSP package and Pin 4 in the TSSOP package. To be electrically safe, the thermal pad must be soldered to an area on the board that is electrically isolated or connected to V_{DD}. Attaching the thermal pad to ground adversely affects the performance of the part.

Soldering down this thermal pad dramatically improves the heat dissipation of the package. It is necessary to attach vias that connect the soldered thermal pad to another layer on the board. This provides an avenue to dissipate the heat away from the part. Without vias, the heat is isolated directly under the part.

TOTAL HARMONIC DISTORTION + NOISE (THD + N)

The AD8565/AD8566/AD8567 feature low total harmonic distortion. Figure 31 shows THD + N vs. frequency. The THD + N over the entire supply range is below 0.008%. When the device is powered from a 16 V supply, the THD + N stays below 0.003%. Figure 31 shows the AD8566 in a unity noninverting configuration.

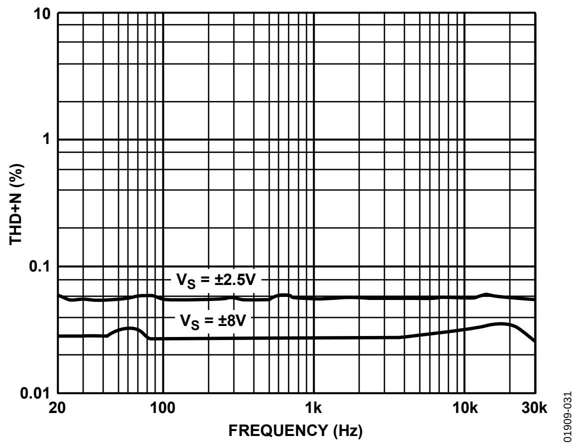


Figure 31. THD + N vs. Frequency

SHORT-CIRCUIT OUTPUT CONDITIONS

The AD8565/AD8566/AD8567 do not have internal short-circuit protection circuitry. As a precautionary measure, it is recommended not to short the output directly to the positive power supply or to ground.

It is not recommended to operate the AD8565/AD8566/AD8567 with more than 35 mA of continuous output current. The output current can be limited by placing a series resistor at the output of the amplifier whose value can be derived using

$$R_X \geq \frac{V_S}{35\text{ mA}}$$

For a 5 V single-supply operation, R_X must have a minimum value of 143 Ω.

LCD PANEL APPLICATIONS

The AD8565/AD8566/AD8567 amplifier is designed for LCD panel applications or applications where large capacitive load drive is required. It can instantaneously source/sink greater than 250 mA of current. At unity gain, it can drive 1 µF without compensation. This makes the AD8565/AD8566/AD8567 ideal for LCD V_{COM} driver applications.

To evaluate the performance of the AD8565/AD8566/AD8567, a test circuit was developed to simulate the V_{COM} driver application for an LCD panel. Figure 32 shows the test circuit. Series capacitors and resistors connected to the output of the op amp represent the load of the LCD panel. The 300 Ω and 3 kΩ feedback resistors are used to improve settling time. This test circuit simulates the worst-case scenario for a V_{COM}. It drives a represented load that is connected to a signal switched symmetrically around V_{COM}.

Figure 33 shows a scope photo of the instantaneous output peak current capability of the AD8565/AD8566/AD8567.

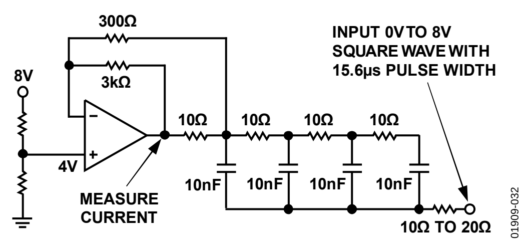


Figure 32. V_{COM} Test Circuit with Supply Voltage at 16 V

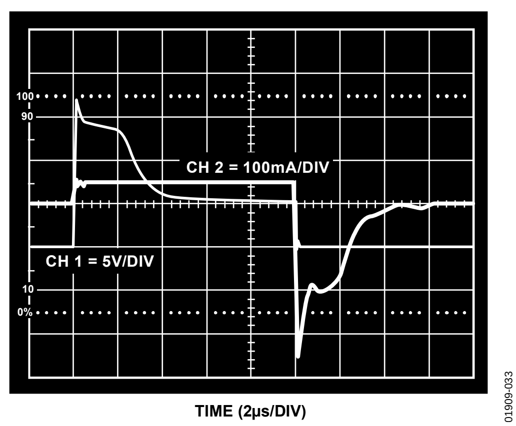


Figure 33. Scope Photo of the V_{COM} Instantaneous Peak Current

OUTLINE DIMENSIONS

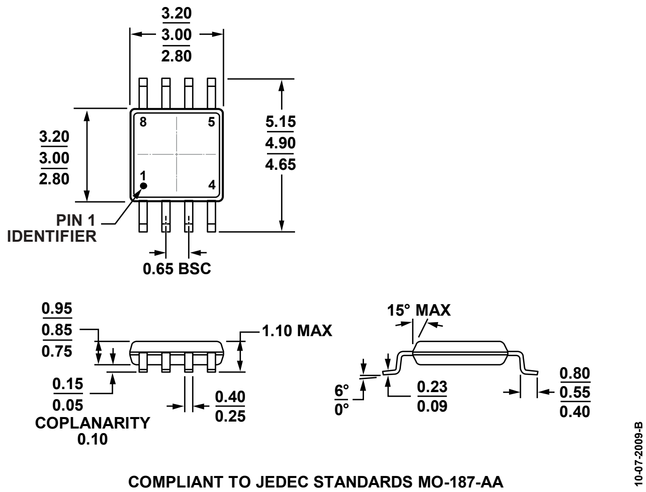


Figure 34. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

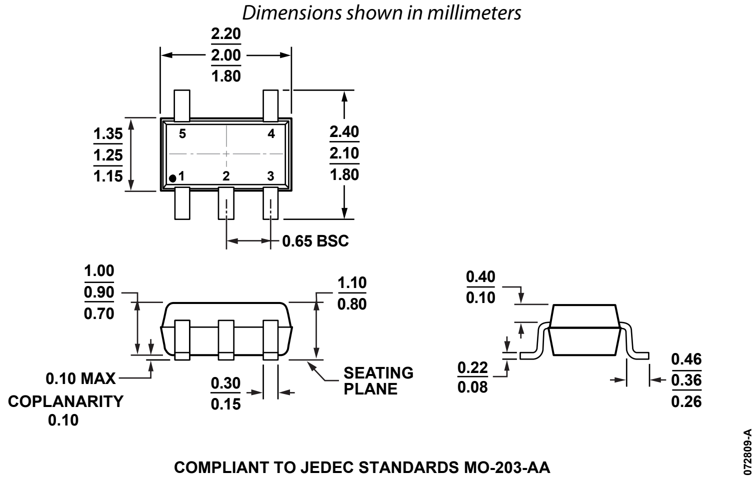


Figure 35. 5-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-5)
Dimensions shown in millimeters

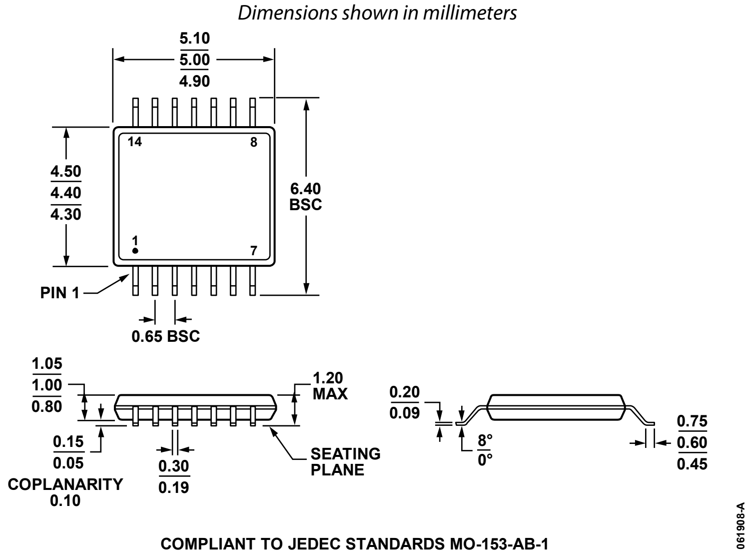


Figure 36. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

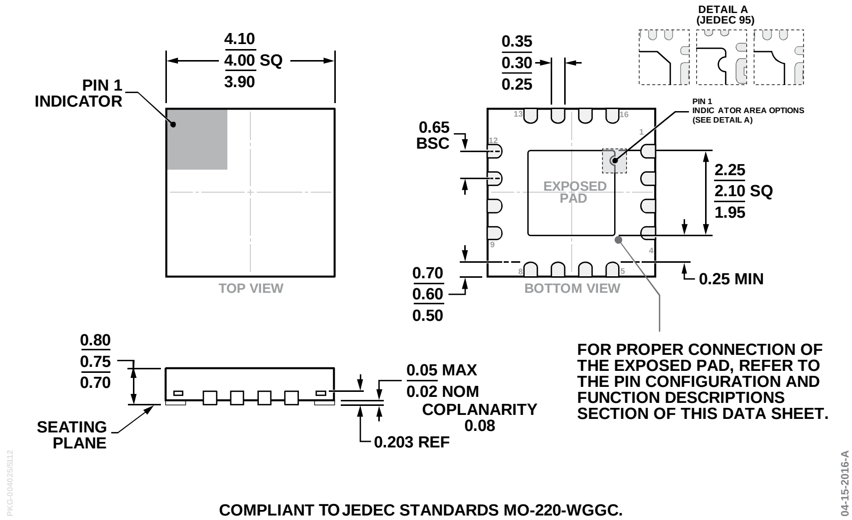


Figure 37. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-23)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Absolute Maximum (V)	Temperature Range	Package Description	Package Option	Branding
AD8565AKSZ-REEL7	18	−40°C to +85°C	5-Lead SC70	KS-5	A0N
AD8566ARMZ-R2	18	−40°C to +85°C	8-Lead MSOP	RM-8	ATA#
AD8566ARMZ-REEL	18	−40°C to +85°C	8-Lead MSOP	RM-8	ATA#
AD8566WARMZ-REEL	18	−40°C to +85°C	8-Lead MSOP	RM-8	LG3
AD8567ARUZ	18	−40°C to +85°C	14-Lead TSSOP	RU-14	
AD8567ARUZ-REEL	18	−40°C to +85°C	14-Lead TSSOP	RU-14	
AD8567ACPZ-R2	18	−40°C to +85°C	16-Lead LFCSP	CP-16-23	
AD8567ACPZ-REEL	18	−40°C to +85°C	16-Lead LFCSP	CP-16-23	
AD8567ACPZ-REEL7	18	−40°C to +85°C	16-Lead LFCSP	CP-16-23	

[1] Z = RoHS Compliant Part, # denotes RoHs compliant product, may be top or bottom marked.
[2] Qualified for automotive applications.

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