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REVISION HISTORY

9/15—Rev. G to Rev. H

Changed NC to DNC ... Throughout
Changes to Figure 1 ... 1
Changes to Figure 6 and Table 4 ... 9

5/13—Rev. F to Rev. G

Changes to General Description Section ... 1
Deleted Evaluation Board for the AD5544 Section and Figure 30 to Figure 35; Renumbered Sequentially ... 22
Updated Outline Dimensions ... 21
Changes to Ordering Guide ... 22

1/12—Rev. E to Rev. F

Changes to Figure 1 ... 1
Added Figure 18; Renumbered Sequentially ... 11
Changes to Evaluation Board Schematics Section ... 22

6/11—Rev. D to Rev. E

Added 32-Lead LFCSP ... Throughout
Changes to Table 1, Supply Characteristics Parameters ... 3
Changes to Table 2, Supply Characteristics Parameters ... 5
Added Figure 6, Renumbered Subsequent Figures, Changes to Table 4 ... 7
Changed Applications Section to Applications Information Section, Added Reference Selection and Amplifier Selection Sections ... 19
Added Evaluation Board for the AD5544 Section ... 21
Updated Outline Dimensions ... 17
Changes to Ordering Guide ... 18

9/09—Rev. C to Rev. D

Changes to Features Section ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 4
Changes to Figure 12 ... 9
Changes to Figure 19 ... 10
Changes to Table 8 and Table 9 ... 13
Changes to Ordering Guide ... 16

8/09—Rev. B to Rev. C

Change to Table 1 ... 3
Change to Table 2 ... 4

8/09—Rev. A to Rev. B

Changes to Features Section ... 1
Changes to Figure 2 ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 4
Moved Timing Diagram ... 5
Added Figure 4; Renumbered Sequentially ... 5
Change to Table 3 ... 6
Changes to Table 4 ... 7
Changes to Typical Performance Characteristics Section ... 8
Changes to Figure 19 ... 10
Moved Table 5, Table 6, and Table 7 ... 12
Moved Truth Tables Section ... 13
Deleted Figure 27; Renumbered Sequentially ... 14
Updated Outline Dimensions ... 16
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12/04—Rev. 0 to Rev. A

Updated Format..... Universal
Change to Electrical Characteristics Tables.....4
Change to Pin Description Table 10
Addition of Power Supply Sequence Section.....19
Addition of Layout and Power Supply Bypassing Section.....19
Addition of Grounding Section 19
Addition of Figure 32.....19

4/00—Revision 0: Initial Version

SPECIFICATIONS

AD5544 ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V, $I_{OUT}x$ = virtual GND, $A_{GND}x$ = 0 V, $V_{REF}A = V_{REF}B = V_{REF}C = V_{REF}D$ = 10 V, T_A = full operating temperature range of −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Condition/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE[1]						
Resolution	N	1 LSB = $V_{REF}x/2^{16}$ = 153 µV when V_{REF} = 10 V			16	Bits
Relative Accuracy	INL	AD5544BRSZ			±1	LSB
		AD5544ARSZ			±2	LSB
		AD5544BCPZ			±1	LSB
		AD5544ACPZ-1			±4	LSB
Differential Nonlinearity	DNL	AD5544BRSZ			±1	LSB
		AD5544ARSZ			±1.5	LSB
		AD5544BCPZ			±1	LSB
		AD5544ACPZ-1			±1	LSB
Output Leakage Current	$I_{OUT}x$	Data = 0x0000, T_A = 25°C			10	nA
		Data = 0x0000, T_A = 85°C			20	nA
Full-Scale Gain Error	G_{FSE}	Data = 0xFFFF		±0.75	±3	mV
Full-Scale Tempco[2]	TCV_{FS}			1		ppm/°C
Feedback Resistor	$R_{FB}x$	V_{DD} = 5 V	4	6	8	kΩ
REFERENCE INPUT						
$V_{REF}x$ Range	$V_{REF}x$		−15		+15	V
Input Resistance	$R_{REF}x$		4	6	8	kΩ
Input Resistance Match	$R_{REF}x$	Channel-to-channel		0.35		%
Input Capacitance[2]	$C_{REF}x$			5		pF
ANALOG OUTPUT						
Output Current	$I_{OUT}x$	Data = 0xFFFF	1.25		2.5	mA
Output Capacitance[2]	$C_{OUT}x$	Code dependent		35		pF
LOGIC INPUT AND OUTPUT						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				1	µA
Input Capacitance[2]	C_{IL}				10	pF
Logic Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Logic Output High Voltage	V_{OH}	I_{OH} = 100 µA	4			V
INTERFACE TIMING[2, 3]						
Clock Width High	t_{CH}		25			ns
Clock Width Low	t_{CL}		25			ns
$\overline{CS}$ to Clock Setup	t_{CSS}		0			ns
Clock to $\overline{CS}$ Hold	t_{CSH}		25			ns
Clock to SDO Propagation Delay	t_{PD}		2		20	ns
Load DAC Pulse Width	t_{LDAC}		25			ns
Data Setup	t_{DS}		20			ns
Data Hold	t_{DH}		20			ns
Load Setup	t_{LDS}		5			ns
Load Hold	t_{LDH}		25			ns
SUPPLY CHARACTERISTICS						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Positive Supply Current	I_{DD}	Logic inputs = 0 V			5	µA
Negative Supply Current	I_{SS}	Logic inputs = 0 V, V_{SS} = −5 V		0.001	9	µA

Parameter	Symbol	Test Condition/Comments	Min	Typ	Max	Unit
Power Dissipation	P_{DISS}	Logic inputs = 0 V			1.25	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%			0.006	%/%
AC CHARACTERISTICS[4]						
Output Voltage Settling Time	t_S	To ±0.1% of full scale, data = 0x0000 to 0xFFFF to 0x0000		0.9		µs
Reference Multiplying Bandwidth (BW)	BW − 3 dB	$V_{REF}x$ = 5 V p-p, data = 0xFFFF, C_{FB} = 2.0 pF,		12		MHz
DAC Glitch Impulse	Q	$V_{REF}x$ = 8 V, data = 0x0000 to 0x8000 to 0x0000		−1		nV-sec
Feedthrough Error	$V_{OUT}x/V_{REF}x$	Data = 0x0000, $V_{REF}x$ = 100 mV rms, f = 100 kHz		−65		dB
Crosstalk Error	$V_{OUT}A/V_{REF}B$	Data = 0x0000, $V_{REF}B$ = 100 mV rms, adjacent channel, f = 100 kHz		−90		dB
Digital Feedthrough	Q	$\overline{CS}$ = 1, f_{CLK} = 1 MHz		0.6		nV-sec
Total Harmonic Distortion	THD	$V_{REF}x$ = 5 V p-p, data = 0xFFFF, f = 1 kHz		−98		dB
Output Spot Noise Voltage	e_N	f = 1 kHz, BW = 1 Hz		7		nV/√Hz

[1] All static performance tests (except $I_{OUT}x$) are performed in a closed-loop system using an external precision OP177 I-to-V converter amplifier. The AD5544 R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C.
[2] These parameters are guaranteed by design and not subject to production testing.
[3] All input control signals are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.
[4] All ac characteristic tests are performed in a closed-loop system using an AD8038 I-to-V converter amplifier.

AD5554 ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V, $I_{OUT}x$ = virtual GND, $A_{GND}x$ = 0 V, $V_{REF}A = V_{REF}B = V_{REF}C = V_{REF}D$ = 10 V, T_A = full operating temperature range of −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Condition/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE[1]						
Resolution	N	1 LSB = $V_{REF}x/2^{14}$ = 610 µV when $V_{REF}x$ = 10 V			14	Bits
Relative Accuracy	INL				±0.5	LSB
Differential Nonlinearity	DNL				±1	LSB
Output Leakage Current	$I_{OUT}x$	Data = 0x0000, T_A = 25°C			10	nA
		Data = 0x0000, T_A = 85°C			20	nA
Full-Scale Gain Error	G_{FSE}	Data = 0x3FFF		±2	±10	mV
Full-Scale Tempco[2]	TCV_{FS}			1		ppm/°C
Feedback Resistor	$R_{FB}x$	V_{DD} = 5 V	4	6	8	kΩ
REFERENCE INPUT						
$V_{REF}x$ Range	$V_{REF}x$		−15		+15	V
Input Resistance	$R_{REF}x$		4	6	8	kΩ
Input Resistance Match	$R_{REF}x$	Channel-to-channel		1		%
Input Capacitance[2]	$C_{REF}x$			5		pF
ANALOG OUTPUT						
Output Current	$I_{OUT}x$	Data = 0x3FFF	1.25		2.5	mA
Output Capacitance[2]	$C_{OUT}x$	Code dependent		80		pF
LOGIC INPUT AND OUTPUT						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				1	µA
Input Capacitance[2]	C_{IL}				10	pF
Logic Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Logic Output High Voltage	V_{OH}	I_{OH} = 100 µA	4			V
INTERFACE TIMING[2, 3]						
Clock Width High	t_{CH}		25			ns
Clock Width Low	t_{CL}		25			ns
$\overline{CS}$ to Clock Setup	t_{CSS}		0			ns

Parameter	Symbol	Test Condition/Comments	Min	Typ	Max	Unit
Clock to $\overline{CS}$ Hold	t_{CSH}		25			ns
Clock to SDO Propagation Delay	t_{PD}		2		20	ns
Load DAC Pulse Width	t_{LDAC}		25			ns
Data Setup	t_{DS}		20			ns
Data Hold	t_{DH}		20			ns
Load Setup	t_{LDS}		5			ns
Load Hold	t_{LDH}		25			ns
SUPPLY CHARACTERISTICS						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Positive Supply Current	I_{DD}	Logic inputs = 0 V			5	µA
Negative Supply Current	I_{SS}	Logic inputs = 0 V, V_{SS} = −5 V		0.001	9	µA
Power Dissipation	P_{DISS}	Logic inputs = 0 V			1.25	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%			0.006	%/%
AC CHARACTERISTICS[4]						
Output Voltage Settling Time	t_S	To ±0.1% of full scale, data = 0x0000 to 0x3FFF to 0x0000		0.9		µs
Reference Multiplying Bandwidth (BW)	BW − 3 dB	$V_{REF}x$ = 5 V p-p, data = 0xFFFF, C_{FB} = 2.0 pF		12		MHz
DAC Glitch Impulse	Q	$V_{REF}x$ = 8 V, data = 0x0000 to 0x2000 to 0x0000		−1		nV-sec
Feedthrough Error	$V_{OUT}x/V_{REF}x$	Data = 0x0000, $V_{REF}x$ = 100 mV rms, f = 100 kHz		−65		dB
Crosstalk Error	$V_{OUT}A/V_{REF}B$	Data = 0x0000, $V_{REF}B$ = 100 mV rms, adjacent channel, f = 100 kHz		−90		dB
Digital Feedthrough	Q	$\overline{CS}$ = 1, f_{CLK} = 1 MHz		0.6		nV-sec
Total Harmonic Distortion	THD	$V_{REF}x$ = 5 V p-p, data = 0x3FFF, f = 1 kHz		−98		dB
Output Spot Noise Voltage	e_N	f = 1 kHz, BW = 1 Hz		7		nV/√Hz

[1] All static performance tests (except I_{OUT}) are performed in a closed-loop system using an external precision OP177 I-to-V converter amplifier. The AD5554 R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C.
[2] These parameters are guaranteed by design and not subject to production testing.
[3] All input control signals are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.
[4] All ac characteristic tests are performed in a closed-loop system using an AD8038 I-to-V converter amplifier,.

TIMING DIAGRAMS

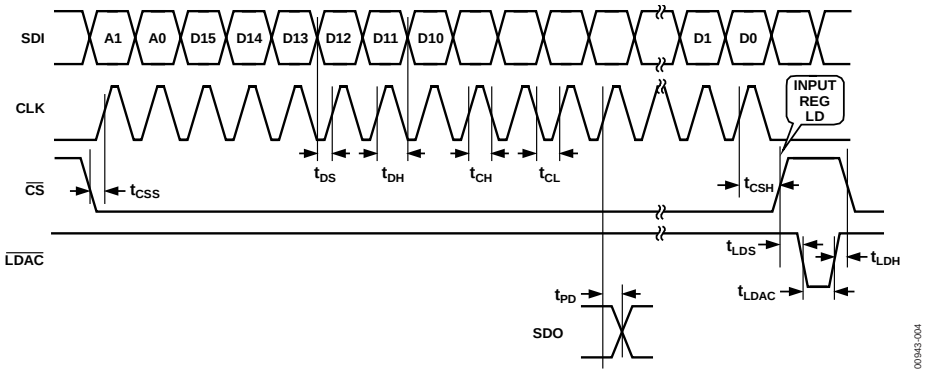


Figure 3. AD5544 Timing Diagram

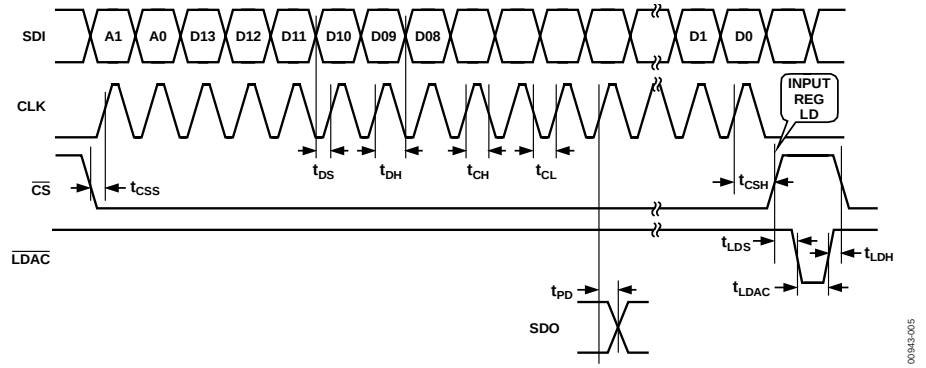


Figure 4. AD5554 Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

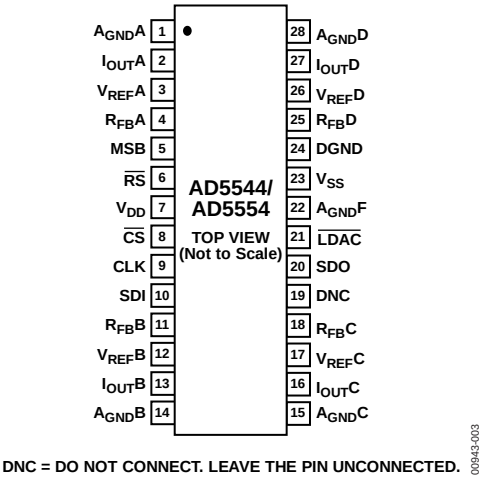
Parameter	Rating
V_{DD} to GND	−0.3 V, +8 V
V_{SS} to GND	+0.3 V, −7 V
$V_{REF}x$ to GND	−18 V, +18 V
Logic Input and Output to GND	−0.3 V, +8 V
$V(I_{OUT}x)$ to GND	−0.3 V, V_{DD} + 0.3 V
$A_{GND}x$ to DGND	−0.3 V, +0.3 V
Input Current to Any Pin Except Supplies	±50 mA
Package Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
Thermal Resistance	θ_{JA}
28-Lead SSOP	100°C/W
32-Lead LFCSP	32.5°C/W
Maximum Junction Temperature (T_J Max)	150°C
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Vapor Phase, 60 Sec	215°C
Infrared, 15 Sec	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

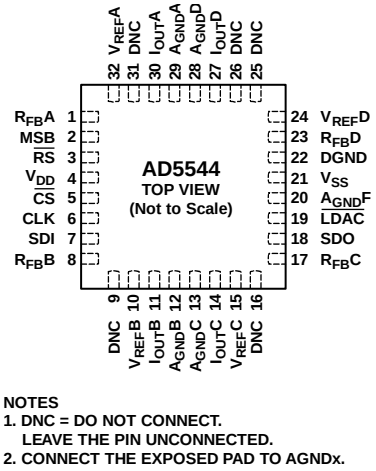
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



DNC = DO NOT CONNECT. LEAVE THE PIN UNCONNECTED.

Figure 5. TSSOP Pin Configuration



NOTES
1. DNC = DO NOT CONNECT.
   LEAVE THE PIN UNCONNECTED.
2. CONNECT THE EXPOSED PAD TO AGNDx.

Figure 6. LFCSP Pin Configuration

Table 4. Pin Function Descriptions

TSSOP Pin No.	LFCSP Pin No.	Mnemonic	Description
1	29	$A_{GND}A$	DAC A Analog Ground.
2	30	$I_{OUT}A$	DAC A Current Output.
3	32	$V_{REF}A$	DAC A Reference Voltage Input Terminal. Establishes DAC A full-scale output voltage. This pin can be tied to the V_{DD} pin.
4	1	$R_{FB}A$	DAC A Feedback Resistor Connection. Establish the voltage output for DAC A by connecting this pin to an external amplifier output.
5	2	MSB	MSB Bit. Set this pin during a reset pulse ($\overline{RS}$) or at system power-on if tied to ground or V_{DD}.
6	3	$\overline{RS}$	Reset Pin, Active Low Input. Input registers and DAC registers are set to all 0s or half-scale code (0x8000 for the AD5544 and 0x2000 for the AD5554), determined by the voltage on the MSB pin. Register data = 0x0000 when MSB = 0.
7	4	V_{DD}	Positive Power Supply Input. Specified range of operation: 5 V ± 10%.
8	5	$\overline{CS}$	Chip Select, Active Low Input. Disables shift register loading when high. Transfers serial register data to the input register when $\overline{CS}$/$\overline{LDAC}$ returns high. Does not affect $\overline{LDAC}$ operation.
9	6	CLK	Clock Input. Positive edge clocks data into the shift register.
10	7	SDI	Serial Data Input. Input data loads directly into the shift register.
11	8	$R_{FB}B$	DAC B Feedback Resistor Connection. Establish the voltage output for DAC B by connecting this pin to an external amplifier output.
12	10	$V_{REF}B$	DAC B Reference Voltage Input Terminal. Establishes DAC B full-scale output voltage. This pin can be tied to the V_{DD} pin.
13	11	$I_{OUT}B$	DAC B Current Output.
14	12	$A_{GND}B$	DAC B Analog Ground.
15	13	$A_{GND}C$	DAC C Analog Ground.
16	14	$I_{OUT}C$	DAC C Current Output.
17	15	$V_{REF}C$	DAC C Reference Voltage Input Terminal. Establishes DAC C full-scale output voltage. This pin can be tied to the V_{DD} pin.
18	17	$R_{FB}C$	DAC C Feedback Resistor Connection. Establish the voltage output for DAC C by connecting this pin to an external amplifier output.
19	9, 16, 25, 26, 31	DNC	Do Not Connect. Leave these pins unconnected.
20	18	SDO	Serial Data Output. Input data loads directly into the shift register. Data appears at SDO at 19 clock pulses for the AD5544 and 17 clock pulses for the AD5554 after input at the SDI pin.
21	19	$\overline{LDAC}$	Load DAC Register Strobe, Level Sensitive Active Low. Transfers all input register data to DAC registers. Asynchronous active low input. See Table 8 and Table 9 for operation.

TSSOP Pin No.	LFCSP Pin No.	Mnemonic	Description
22	20	$A_{GND}F$	High Current Analog Force Ground.
23	21	V_{SS}	Negative Bias Power Supply Input. Specified range of operation: −5.5 V to +0.3 V.
24	22	DGND	Digital Ground Pin.
25	23	$R_{FB}D$	DAC D Feedback Resistor Connection. Establish the voltage output for DAC D by connecting this pin to an external amplifier output.
26	24	$V_{REF}D$	DAC D Reference Voltage Input Terminal. Establishes DAC D full-scale output voltage. This pin can be tied to the V_{DD} pin.
27	27	$I_{OUT}D$	DAC D Current Output.
28	28	$A_{GND}D$	DAC D Analog Ground.
N/A[1]		EPAD	Connect the exposed pad to AGNDx.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

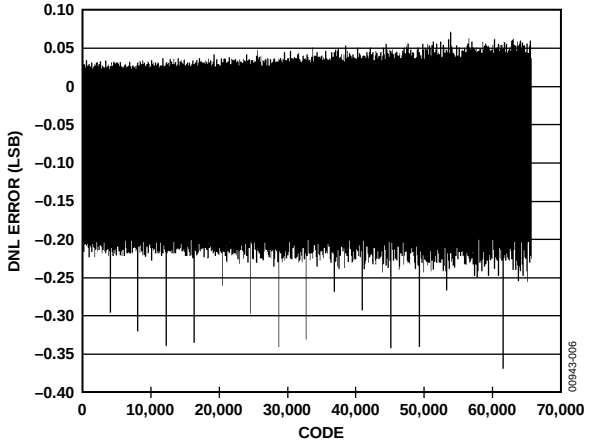


Figure 7. AD5544 DNL vs. Code, T_A = 25°C

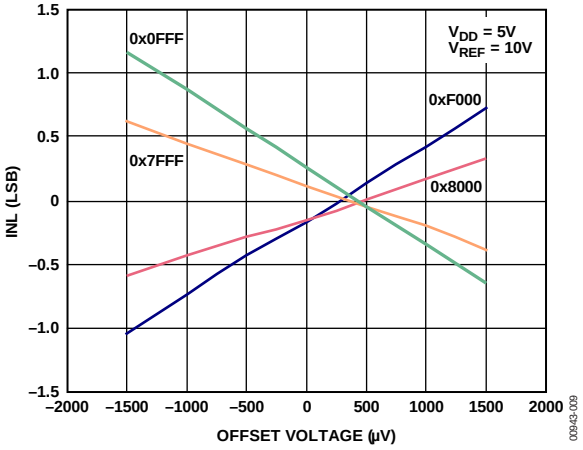


Figure 10. AD5544 Integral Nonlinearity Error vs. Op Amp Offset

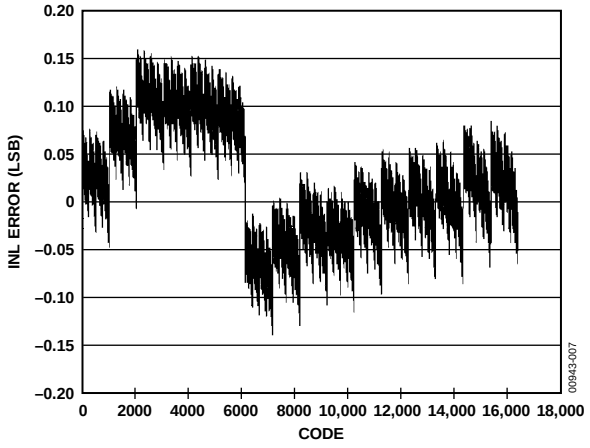


Figure 8. AD5554 INL vs. Code, T_A = 25°C

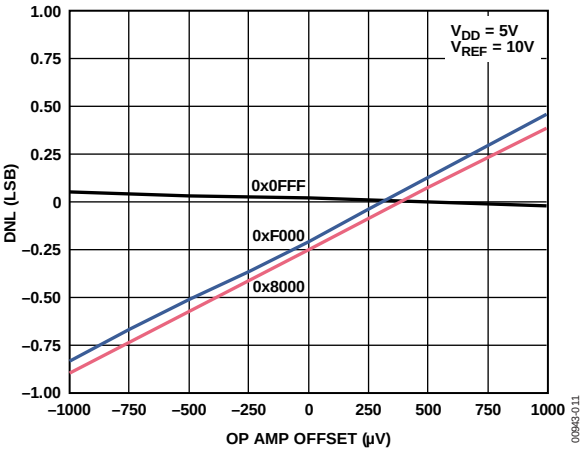


Figure 11. AD5544 Differential Nonlinearity Error vs. Op Amp Offset

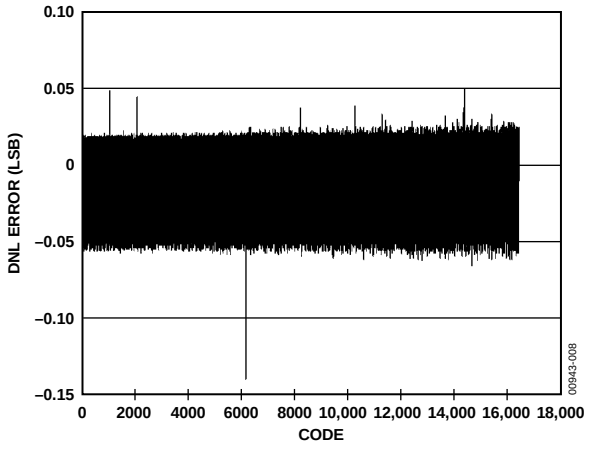


Figure 9. AD5554 DNL vs. Code, T_A = 25°C

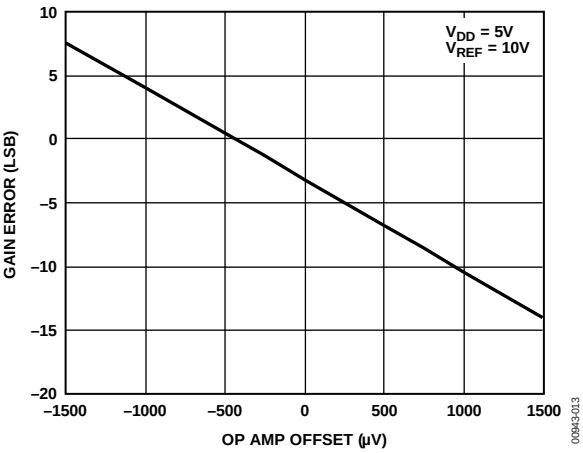


Figure 12. AD5544 Gain Error vs. Op Amp Offset

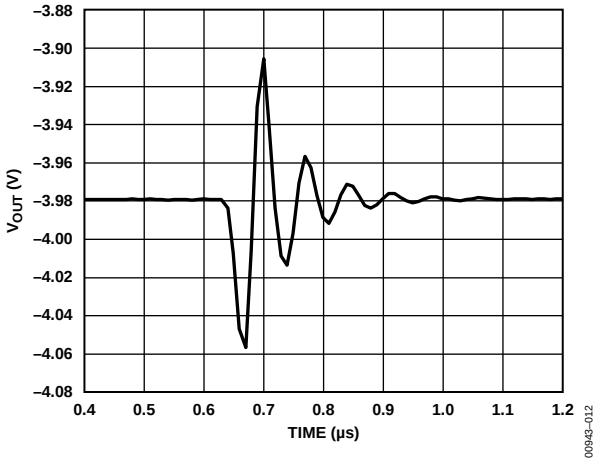


Figure 13. AD5544 Midscale Transition

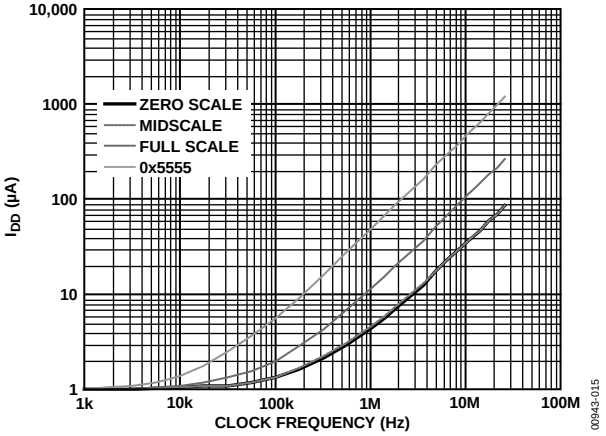


Figure 16. AD5544 Power Supply Current vs. Clock Frequency

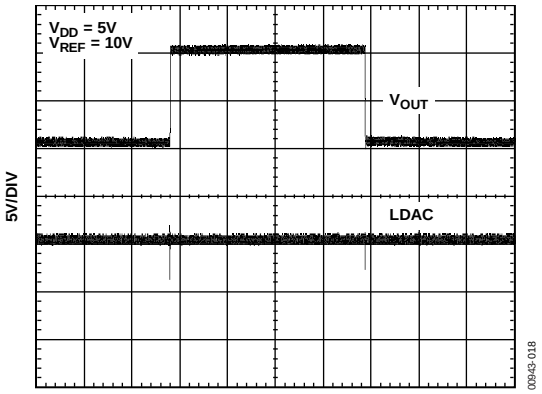


Figure 14. AD5544 Large Signal Settling Time

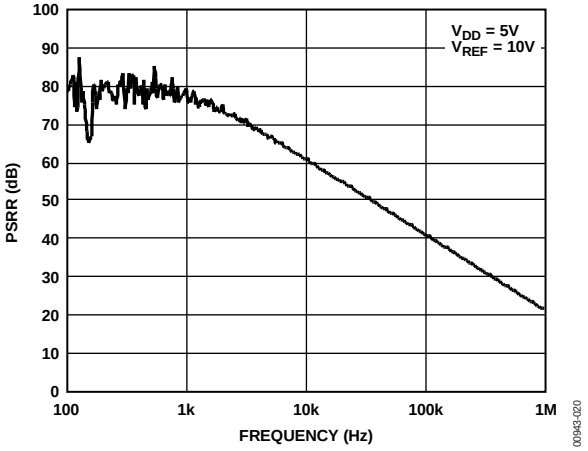


Figure 17. AD5544/AD5554 Power Supply Rejection vs. Frequency

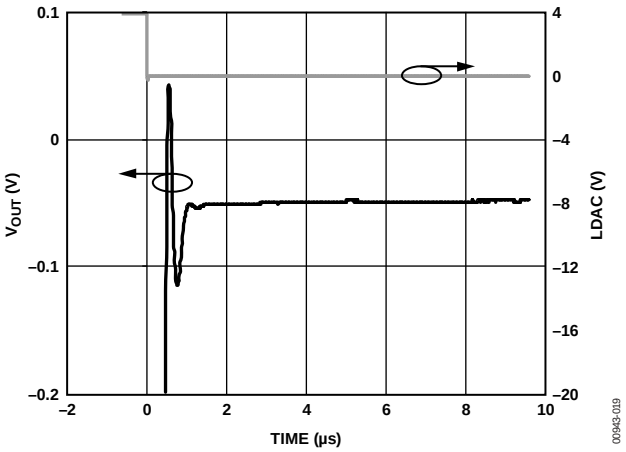


Figure 15. AD5544 Small Signal Settling Time

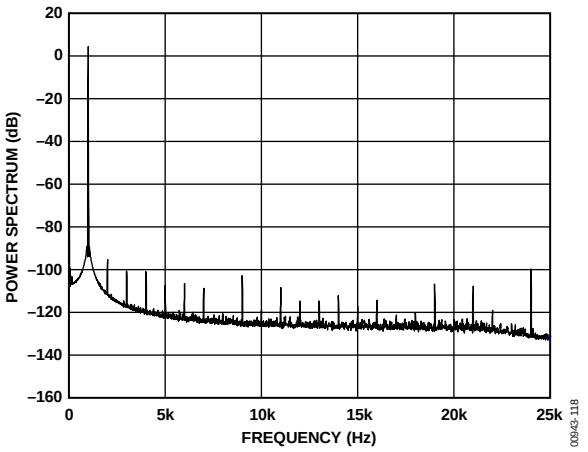


Figure 18. AD5544/AD5554 Analog THD

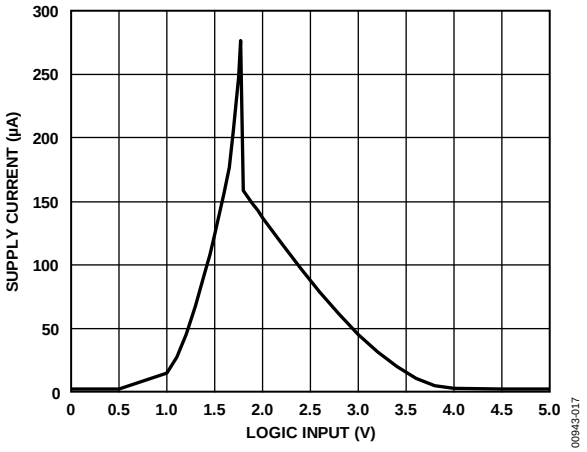


Figure 19. AD5544/AD5554 Power Supply Current vs. Logic Input Voltage

THEORY OF OPERATION

The AD5544 and the AD5554 contain four 16-bit and 14-bit, current output DACs, respectively. Each DAC has its own independent multiplying reference input. Both the AD5544 and the AD5554 use a 3-wire, SPI-compatible serial data interface, with a configurable asynchronous $\overline{RS}$ pin for half-scale (MSB = 1) or zero-scale (MSB = 0) preset. In addition, an $\overline{LDAC}$ strobe enables 4-channel, simultaneous updates for hardware synchronized output voltage changes.

DIGITAL-TO-ANALOG CONVERTER (DAC)

Each part contains four current-steering R-R ladder DACs. Figure 20 shows a typical equivalent DAC. Each DAC contains a matching feedback resistor for use with an external I-to-V converter amplifier. The $R_{FB}x$ pin connects to the output of the external amplifier. The $I_{OUT}x$ terminal connects to the inverting input of the external amplifier. The $A_{GND}x$ pin should be Kelvin-connected to the load point, requiring full 16-bit accuracy. These DACs are designed to operate with both negative and positive reference voltage.

The V_{DD} power pin is used only by the logic to drive the DAC switches on and off. Note that a matching switch is used in series with the internal 5 kΩ feedback resistor. If users attempt to measure the value of R_{FB}, power must be applied to V_{DD} to achieve continuity. An additional V_{SS} bias pin is used to guard the substrate during high temperature applications, minimizing zero-scale leakage currents that double every 10°C. The DAC output voltage is determined by V_{REF} and the digital data (D) in the following equations:

$$V_{OUT} = -V_{REF} \times \frac{D}{65{,}536} \quad \text{(for the AD5544)} \tag{1}$$

$$V_{OUT} = -V_{REF} \times \frac{D}{16{,}384} \quad \text{(for the AD5554)} \tag{2}$$

Note that the output polarity is opposite the V_{REF} polarity for dc reference voltages.

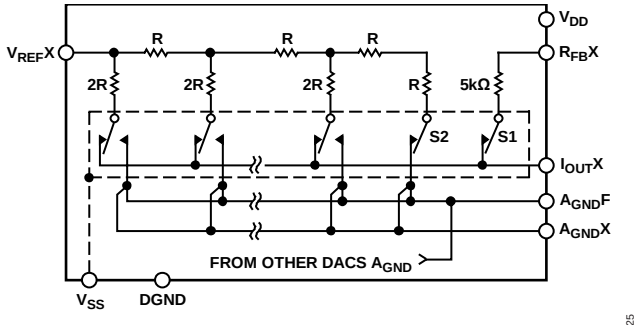


Figure 20. Typical Equivalent DAC Channel

These DACs are also designed to accommodate ac reference input signals. Both the AD5544 and the AD5554 accommodate input reference voltages in the range of −15 V to +15 V. The reference voltage inputs exhibit a constant nominal input resistance of 5 kΩ ± 30%. On the other hand, the $I_{OUT}A$, $I_{OUT}B$, $I_{OUT}C$, and $I_{OUT}D$ DAC outputs are code dependent and produce various output resistances and capacitances. The choice of external amplifier should take into account the variation in impedance generated by the AD5544/AD5554 on the inverting input node of the amplifier. The feedback resistance, in parallel with the DAC ladder resistance, dominates output voltage noise. For multiplying mode applications, an external feedback compensation capacitor, C_{FB}, may be needed to provide a critically damped output response for step changes in reference input voltages. Figure 21 shows the gain vs. frequency performance at various attenuation settings using a 23 pF external feedback capacitor connected across the $I_{OUT}x$ and $R_{FB}x$ terminals for the AD5544 and the AD5554, respectively. To maintain good analog performance, power supply bypassing of 0.01 µF, in parallel with 1 µF, is recommended. Under these conditions, a clean power supply with low ripple voltage capability should be used. Switching power supplies is usually not suitable for this application due to the higher ripple voltage and PSS frequency-dependent characteristics. It is best to derive the supply of the AD5544/AD5554 from system analog supply voltages. Do not use the digital supply (see Figure 22).

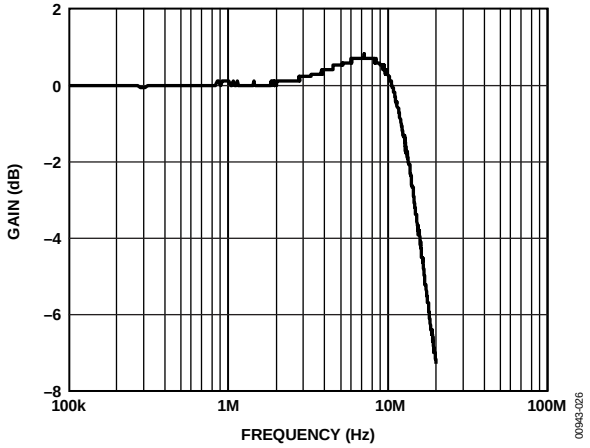


Figure 21. AD5554 Reference Multiplying Bandwidth vs. Code

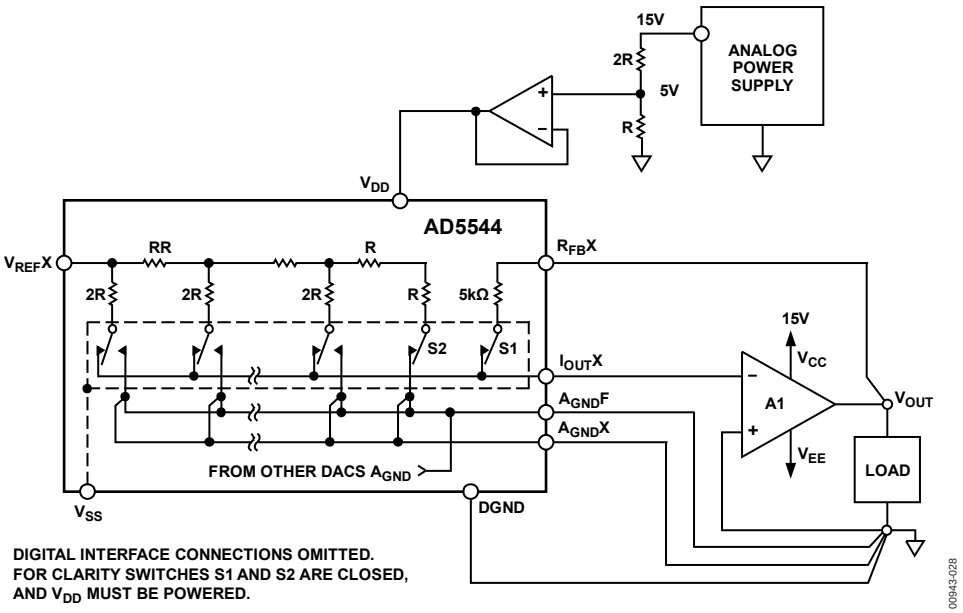


Figure 22. Recommended Kelvin-Sensed Hookup

SERIAL DATA INTERFACE

The AD5544/AD5554 use a 3-wire ($\overline{CS}$, SDI, CLK), SPI-compatible serial data interface. Serial data of the AD5544/AD5554 is clocked into the serial input register in an 18-bit and 16-bit data-word format, respectively. The MSB bits are loaded first. Table 5 defines the 18 data-word bits for the AD5544, and Table 6 defines the 16 data-word bits for the AD5554. Data is placed on the SDI pin and clocked into the register on the positive clock edge of CLK, subject to the data setup and data hold time requirements specified in the interface timing specifications (see Table 1 and Table 2).

Data can be clocked in only while the $\overline{CS}$ chip select pin is active low. For the AD5544, only the last 18 bits clocked into the serial register are interrogated when the $\overline{CS}$ pin returns to the logic high state; extra data bits are ignored. For the AD5554, only the last 16 bits clocked into the serial register are interrogated when the $\overline{CS}$ pin returns to the logic high state. Because most microcontrollers output serial data in 8-bit bytes, three right justified data bytes can be written to the AD5544. Keeping the $\overline{CS}$ line low between the first, second, and third byte transfers results in a successful serial register update.

Similarly, two right justified data bytes can be written to the AD5554. Keeping the $\overline{CS}$ line low between the first and second byte transfer results in a successful serial register update.

When the data is properly aligned in the shift register, the positive edge of the $\overline{CS}$ initiates the transfer of new data to the target DAC register, determined by the decoding of Address Bit A1 and Address Bit A0. For the AD5544, Table 5, Table 7, Table 8, and Figure 3 define the characteristics of the software serial interface.

For the AD5554, Table 6, Table 7, Table 9, and Figure 4 define the characteristics of the software serial interface. Figure 23 and Figure 24 show the equivalent logic interface for the key digital control pins for the AD5544. The AD5554 has a similar configuration, except that it has 14 data bits. Two additional pins, $\overline{RS}$ and MSB, provide hardware control over the preset function and DAC register loading. If these functions are not needed, the $\overline{RS}$ pin can be tied to logic high. The asynchronous input $\overline{RS}$ pin forces all input and the DAC registers to either the zero-code state (MSB = 0) or the half-scale state (MSB = 1).

Table 5. AD5544 Serial Input Register Data Format (Data Is Loaded in the MSB-First Format)[1]

MSB																	LSB
B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

[1] Only the last 18 bits of data clocked into the serial register (address + data) are inspected when the positive edge of the $\overline{CS}$ line returns to logic high. At this point, an internally generated load strobe transfers the serial register data contents (Bit D15 to Bit D0) to the decoded DAC input register address determined by Bit A1 and Bit A0. Any extra bits clocked into the AD5544 shift register are ignored; only the last 18 bits clocked in are used. If double-buffered data is not needed, the $\overline{LDAC}$ pin can be tied logic low to disable the DAC registers.

Table 6. AD5554 Serial Input Register Data Format (Data Is Loaded in the MSB-First Format)[1]

MSB															LSB
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

[1] Only the last 16 bits of data clocked into the serial register (address + data) are inspected when the positive edge of the $\overline{CS}$ line returns to logic high. At this point, an internally generated load strobe transfers the serial register data contents (Bit D13 to Bit D0) to the decoded DAC input register address determined by Bit A1 and Bit A0. Any extra bits clocked into the AD5554 shift register are ignored; only the last 16 bits clocked in are used. If double-buffered data is not needed, the $\overline{LDAC}$ pin can be tied logic low to disable the DAC registers.

Table 7. Address Decode

A1	A0	DAC Decoded
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

TRUTH TABLES

Table 8. AD5544[1] Control Logic Truth Table

$\overline{CS}$	CLK	$\overline{LDAC}$	$\overline{RS}$	MSB[2]	Serial Shift Register Function[3]	Input Register Function	DAC Register
High	X	High	High	X	No effect	Latched	Latched
Low	Low	High	High	X	No effect	Latched	Latched
Low	↑ +[3]	High	High	X	Shift register data advanced one bit	Latched	Latched
Low	High	High	High	X	No effect	Latched	Latched
↑ +[3]	Low	High	High	X	No effect	Selected DAC updated with current shift register contents[4]	Latched
High	X	Low	High	X	No effect	Latched	Transparent
High	X	High	High	X	No effect	Latched	Latched
High	X	↑ +[3]	High	X	No effect	Latched	Latched
High	X	High	Low	0	No effect	Latched data = 0x0000	Latched data = 0x0000
High	X	High	Low	High	No effect	Latched data = 0x8000	Latched data = 0x8000

[1] For the AD5544, data appears at the SDO pin 19 clock pulses after input at the SDI pin.
[2] X means don't care.
[3] ↑ + is a positive logic transition.
[4] At power-on, both the input register and the DAC register are loaded with all 0s.

Table 9. AD5554[1] Control Logic Truth Table

$\overline{CS}$	CLK	$\overline{LDAC}$	$\overline{RS}$	MSB[2]	Serial Shift Register Function[3]	Input Register Function[3]	DAC Register
High	X	High	High	X	No effect	Latched	Latched
Low	L	High	High	X	No effect	Latched	Latched
Low	↑ +[3]	High	High	X	Shift register data advanced one bit	Latched	Latched
Low	High	High	High	X	No effect	Latched	Latched
↑ +[3]	Low	High	High	X	No effect	Selected DAC updated with current shift register contents[4]	Latched
High	X	Low	High	X	No effect	Latched	Transparent
High	X	High	High	X	No effect	Latched	Latched
High	X	↑ +[3]	High	X	No effect	Latched	Latched
High	X	High	Low	0	No effect	Latched data = 0x0000	Latched data = 0x0000
High	X	High	Low	High	No effect	Latched data = 0x2000	Latched data = 0x2000

[1] For the AD5554, data appears at the SDO pin 17 clock pulses after input at the SDI pin.
[2] X means don't care.
[3] ↑ + is a positive logic transition.
[4] At power-on, both the input register and the DAC register are loaded with all 0s.

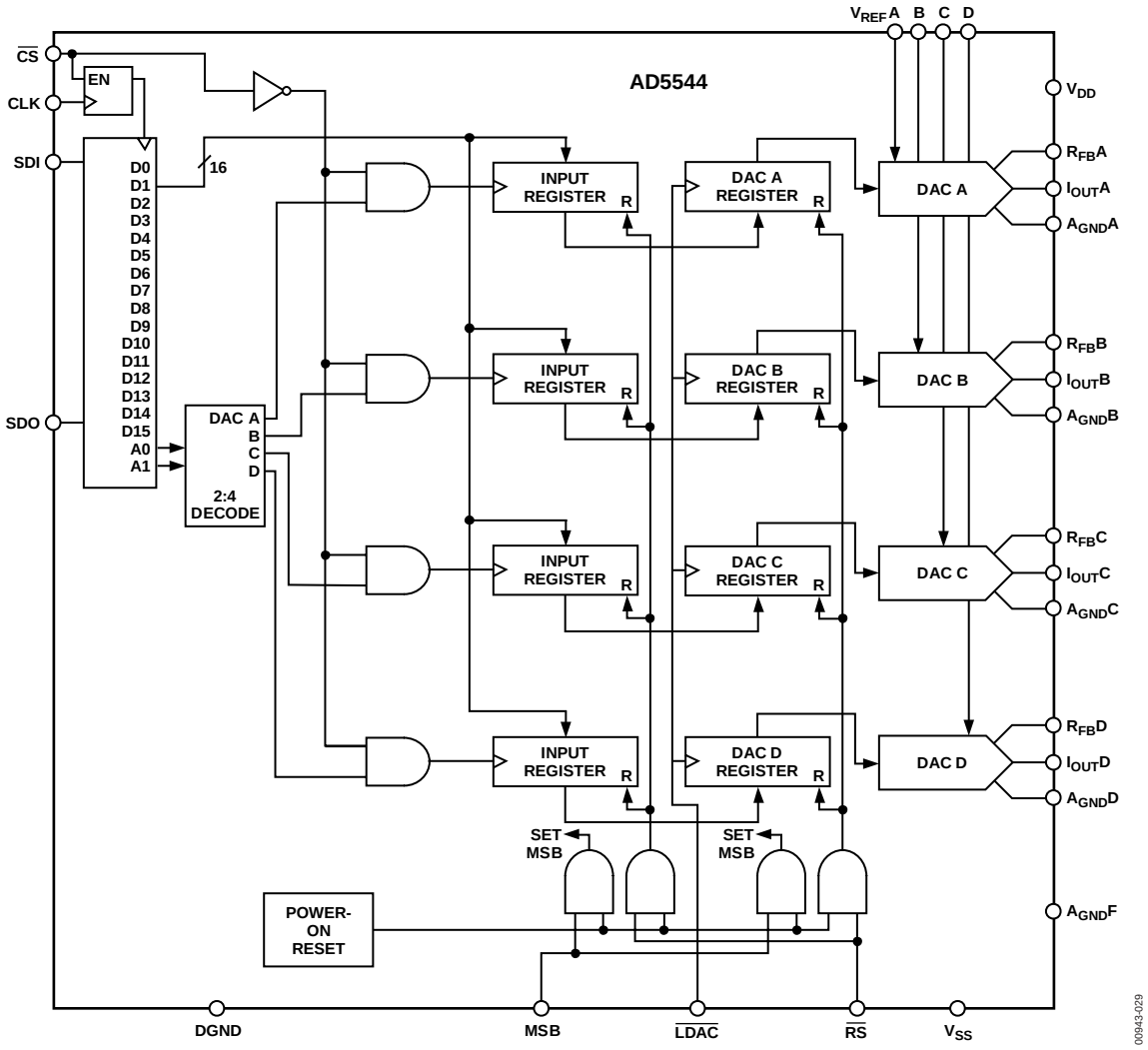


Figure 23. System Level Digital Interfacing

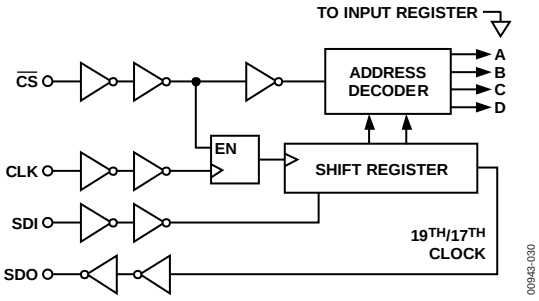


Figure 24. AD5544/AD5554 Equivalent Logic Interface

POWER-ON RESET

When the V_{DD} power supply is turned on, an internal reset strobe forces all the input and DAC registers to the zero-code state or half-scale state, depending on the MSB pin voltage. The V_{DD} power supply should have a smooth positive ramp without drooping to have consistent results, especially in the region of V_{DD} = 1.5 V to 2.3 V. The V_{SS} supply has no effect on the power-on reset performance. The DAC register data stays at a zero-scale or half-scale setting until a valid serial register data load takes place.

ESD PROTECTION CIRCUITS

All logic input pins contain back-biased ESD protection Zener diodes that are connected to ground (DGND) and V_{DD}, as shown in Figure 25.

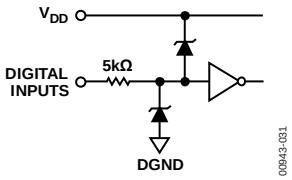


Figure 25. Equivalent ESD Production Circuits

POWER SUPPLY SEQUENCE

As standard practice, it is recommended that V_{DD}, V_{SS}, and ground be powered up prior to any reference. The ideal power-up sequence is as follows: A_{GND}x, DGND, V_{DD}, V_{SS}, V_{REF}x, and the digital inputs. A noncompliance power-up sequence may elevate the reference current, but the devices resume normal operation once V_{DD} and V_{SS} are powered up.

LAYOUT AND POWER SUPPLY BYPASSING

It is good practice to employ a compact, minimum lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 µF to 0.1 µF disc or chip ceramic capacitors. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at V_{DD} to minimize any transient disturbance and filter any low frequency ripple (see Figure 26). Users should not apply switching regulators for V_{DD} due to the power supply rejection ratio (PSRR) degradation over frequency.

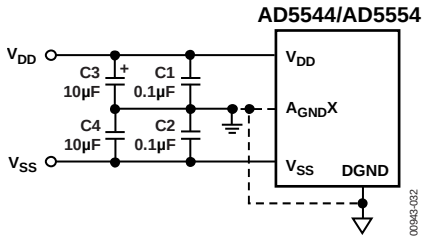


Figure 26. Power Supply Bypassing and Grounding Connection

GROUNDING

The DGND and $A_{GND}x$ pins of the AD5544/AD5554 serve as digital and analog ground references. To minimize the digital ground bounce, the DGND terminal should be joined remotely at a single point to the analog ground plane (see Figure 26).

APPLICATIONS INFORMATION

The AD5544/AD5554 are, inherently, two-quadrant multiplying DACs. That is, they can be easily set up for unipolar output operation. The full-scale output polarity is the inverse of the reference input voltage.

In some applications, it may be necessary to generate the full four-quadrant multiplying capability or a bipolar output swing. This is easily accomplished using an additional external amplifier (A2) configured as a summing amplifier (see Figure 27).

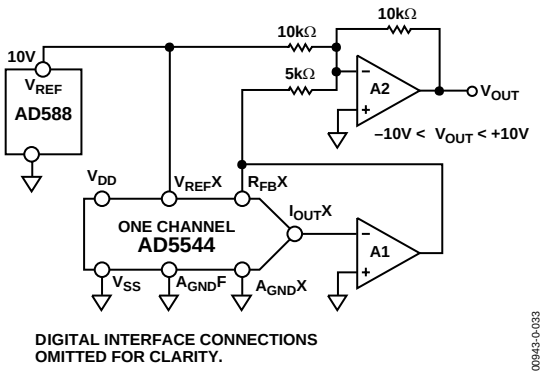


Figure 27. Four-Quadrant Multiplying Application Circuit

In this circuit, the first and second amplifiers (A1 and A2) provide a total gain of 2, which increases the output voltage span to 20 V. Biasing the external amplifier with a 10 V offset from the reference voltage results in a full four-quadrant multiplying circuit. The transfer equation of this circuit shows that both negative and positive output voltages are created as the input data (D) is incremented from code zero (V_{OUT} = −10 V) to midscale (V_{OUT} = 0 V) to full scale (V_{OUT} = 10 V).

$$V_{OUT}\left(\frac{D}{32{,}768}-1\right)\times -V_{REF} \text{ (for the AD5544)} \quad (3)$$

$$V_{OUT}\left(\frac{D}{8192}-1\right)\times -V_{REF} \text{ (for the AD5554)} \quad (4)$$

REFERENCE SELECTION

When selecting a reference for use with the AD55xx series of current output DACs, pay attention to the output voltage, temperature coefficient specification of the reference. Choosing a precision reference with a low output temperature coefficient minimizes error sources. Table 10 lists some of the references available from Analog Devices, Inc., that are suitable for use with this range of current output DACs.

AMPLIFIER SELECTION

The primary requirement for the current-steering mode is an amplifier with low input bias currents and low input offset voltage. Because of the code-dependent output resistance of the DAC, the input offset voltage of an op amp is multiplied by the variable gain of the circuit. A change in this noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed upon the desired change in output between the two codes and gives rise to a differential linearity error, which, if large enough, can cause the DAC to be nonmonotonic.

The input bias current of an op amp also generates an offset at the voltage output because of the bias current flowing in the feedback resistor, R_{FB}.

Common-mode rejection of the op amp is important in voltage-switching circuits because it produces a code-dependent error at the voltage output of the circuit.

Provided that the DAC switches are driven from true wideband, low impedance sources (V_{IN} and AGND), they settle quickly. Consequently, the slew rate and settling time of a voltage-switching DAC circuit is determined largely by the output op amp. To obtain minimum settling time in this configuration, minimize capacitance at the V_{REF} node (the voltage output node in this application) of the DAC. This is done by using low input capacitance buffer amplifiers and careful board design.

Analog Devices offers a wide range of amplifiers for both precision dc and ac applications, as listed in Table 11 and Table 12.

Table 10. Suitable Analog Devices Precision References

Part No.	Output Voltage (V)	Initial Tolerance (%)	Maximum Temperature Drift (ppm/°C)	I_{SS} (mA)	Output Noise (µV p-p)	Package(s)
ADR01	10	0.05	3	1	20	8-lead SOIC
ADR01	10	0.05	9	1	20	5-lead TSOT, 5-lead SC70
ADR02	5.0	0.06	3	1	10	8-lead SOIC
ADR02	5.0	0.06	9	1	10	5-lead TSOT, 5-lead SC70
ADR03	2.5	0.1	3	1	6	8-lead SOIC
ADR03	2.5	0.1	9	1	6	5-lead TSOT, 5-lead SC70
ADR06	3.0	0.1	3	1	10	8-lead SOIC
ADR06	3.0	0.1	9	1	10	5-lead TSOT, 5-lead SC70
ADR420	2.048	0.05	3	0.5	1.75	8-lead SOIC, 8-lead MSOP
ADR421	2.50	0.04	3	0.5	1.75	8-lead SOIC, 8-lead MSOP
ADR423	3.00	0.04	3	0.5	2	8-lead SOIC, 8-lead MSOP
ADR425	5.00	0.04	3	0.5	3.4	8-lead SOIC, 8-lead MSOP
ADR431	2.500	0.04	3	0.8	3.5	8-lead SOIC, 8-lead MSOP
ADR435	5.000	0.04	3	0.8	8	8-lead SOIC, 8-lead MSOP
ADR391	2.5	0.16	9	0.12	5	5-lead TSOT
ADR395	5.0	0.10	9	0.12	8	5-lead TSOT

Table 11. Suitable Analog Devices Precision Op Amps

Part No.	Supply Voltage (V)	V_{OS} Maximum (µV)	I_B Maximum (nA)	0.1 Hz to 10 Hz Noise (µV p-p)	Supply Current (µA)	Package(s)
OP97	±2 to ±20	25	0.1	0.5	600	8-lead SOIC, 8-lead PDIP
OP1177	±2.5 to ±15	60	2	0.4	500	8-lead MSOP, 8-lead SOIC
AD8675	±5 to ±18	75	2	0.1	2300	8-lead MSOP, 8-lead SOIC
AD8671	±5 to ±15	75	12	0.077	3000	8-lead MSOP, 8-lead SOIC
ADA4004-1	±5 to ±15	125	90	0.1	2000	8-lead SOIC, 5-lead SOT-23
AD8603	1.8 to 5	50	0.001	2.3	40	5-lead TSOT
AD8607	1.8 to 5	50	0.001	2.3	40	8-lead MSOP, 8-lead SOIC
AD8605	2.7 to 5	65	0.001	2.3	1000	5-lead WLCSP, 5-lead SOT-23
AD8615	2.7 to 5	65	0.001	2.4	2000	5-lead TSOT
AD8616	2.7 to 5	65	0.001	2.4	2000	8-lead MSOP, 8-lead SOIC

Table 12. Suitable Analog Devices High Speed Op Amps

Part No.	Supply Voltage (V)	BW at ACL (MHz)	Slew Rate (V/µs)	V_{OS} (Max) (µV)	I_B (Max) (nA)	Package(s)
AD8065	5 to 24	145	180	1500	0.006	8-lead SOIC, 5-lead SOT-23
AD8066	5 to 24	145	180	1500	0.006	8-lead SOIC, 8-lead MSOP
AD8021	5 to 24	490	120	1000	10,500	8-lead SOIC, 8-lead MSOP
AD8038	3 to 12	350	425	3000	750	8-lead SOIC, 5-lead SC70
ADA4899-1	5 to 12	600	310	35	100	8-lead LFCSP, 8-lead SOIC
AD8057	3 to 12	325	1000	5000	500	5-lead SOT-23, 8-lead SOIC
AD8058	3 to 12	325	850	5000	500	8-lead SOIC, 8-lead MSOP
AD8061	2.7 to 8	320	650	6000	350	5-lead SOT-23, 8-lead SOIC
AD8062	2.7 to 8	320	650	6000	350	8-lead SOIC, 8-lead MSOP
AD9631	±3 to ±6	320	1300	10,000	7000	8-lead SOIC, 8-lead PDIP

OUTLINE DIMENSIONS

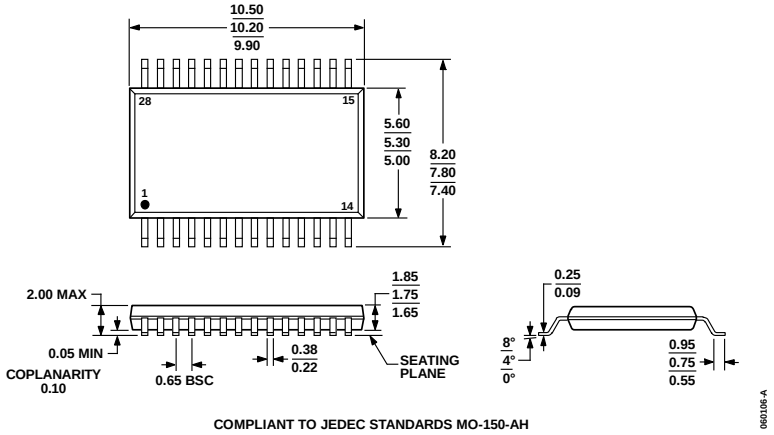


Figure 28. 28-Lead Shrink Small Outline Package [SSOP]
(RS-28)
Dimensions shown in millimeters

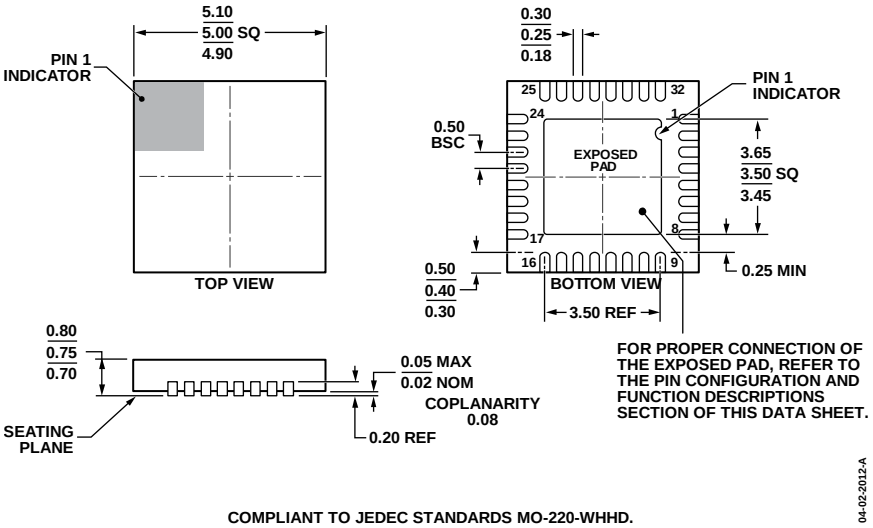


Figure 29. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-11)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	RES Bit	INL LSB	DNL LSB	Temperature Range	Package Description	Package Option
AD5544ARS	16	±2	±1.5	−40°C to +125°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
AD5544ARSZ	16	±2	±1.5	−40°C to +125°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
AD5544ARSZ-REEL7	16	±2	±1.5	−40°C to +125°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
AD5544BRSZ	16	±1	±1	−40°C to +125°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
AD5544BRSZ-REEL7	16	±1	±1	−40°C to +125°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
AD5544ACPZ-1-R2	16	±4	±1	−40°C to +125°C	32-Lead LFCSP_WQ	CP-32-11
AD5544ACPZ-1-RL7	16	±4	±1	−40°C to +125°C	32-Lead LFCSP_WQ	CP-32-11
AD5544BCPZ-R2	16	±1	±1	−40°C to +125°C	32-Lead LFCSP_WQ	CP-32-11
AD5544BCPZ-RL7	16	±1	±1	−40°C to +125°C	32-Lead LFCSP_WQ	CP-32-11
AD5554BRSZ	14	±0.5	±1	−40°C to +125°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
EV-AD5544/45SDZ					Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).