**Data Sheet** 

# **AD524**

# **TABLE OF CONTENTS**

Features	1
Functional Block Diagram	1
General Description	1
Product Highlights	1
Revision History	2
Specifications	3
Absolute Maximum Ratings	8
Connection Diagrams	8
ESD Caution	8
Typical Performance Characteristics	9
Test Circuits	14
Theory of Operation	15
Input Protection	15

	Input Offset and Output Offset	. 1:
	Gain	. 16
	Input Bias Currents	. 17
	Common-Mode Rejection	. 17
	Grounding	. 18
	Sense Terminal	. 18
	Reference Terminal	. 18
	Programmable Gain	. 20
	Auto-Zero Circuits	. 20
	Error Budget Analysis	. 2
	References	. 23
О	outline Dimensions	. 24
	Ordering Guide	21

# **REVISION HISTORY**

# 1/2018—Rev. F to Rev. G

Changes to General Description	1
Change to Output Offset Voltage vs. Temperature Parameter,	
Unit Column, Table 1	3
Added References Section	23
Updated Outline Dimensions	24
Changes to Ordering Guide	25

### 11/2007—Rev. E to Rev. F

11/200/—Rev. E to Rev. F	
Updated Format	Universa
Changes to General Description	1
Changes to Figure 1	1
Changes to Figure 3 and Figure 4 Captions	8
Changes to Error Budget Analysis Section	21
Changes to Ordering Guide	25

4/1999—Rev. D to Rev. E

# **SPECIFICATIONS**

At  $V_{\text{S}}$  =  $\pm 15$  V,  $R_{\text{L}}$  = 2  $k\Omega$  and  $T_{\text{A}}$  = +25°C, unless otherwise noted.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at the final electrical test. Results from those tests are used to calculate outgoing quality levels.

Table 1.

		AD524	A		AD52	4B	T
Parameter	Min	Тур	Max	Min	Тур	Max	Unit
GAIN							
Gain Equation (External Resistor Gain Programming)		$\frac{1000}{R_{\rm G}} + 1$	± 20%	$\left[\frac{4}{}\right]$	$\frac{0,000}{R_{G}} + 1$	± 20%	
Gain Range (Pin Programmable)		1 to 100	00		1 to 10	000	
Gain Error <sup>1</sup>							
G = 1			±0.05			±0.03	%
G = 10			±0.25			±0.15	%
G = 100			±0.5			±0.35	%
G = 1000			±2.0			±1.0	%
Nonlinearity							
G = 1			±0.01			±0.005	%
G = 10, G = 100			±0.01			±0.005	%
G = 1000			±0.01			±0.01	%
Gain vs. Temperature							
G = 1			5			5	ppm/°C
G = 10			15			10	ppm/°C
G = 100			35			25	ppm/°C
G = 1000			100			50	ppm/°C
VOLTAGE OFFSET (May be Nulled)							
Input Offset Voltage			250			100	μV
vs. Temperature			2			0.75	μV/°C
Output Offset Voltage			5			3	mV
vs. Temperature			100			50	μV/°C
Offset Referred to the Input vs. Supply							
G = 1	70			75			dB
G = 10	85			95			dB
G = 100	95			105			dB
G = 1000	100			110			dB
INPUT CURRENT							
Input Bias Current			±50			±25	nA
vs. Temperature		±100			±100		pA/°C
Input Offset Current			±35			±15	nA
vs. Temperature		±100			±100		pA/°C

	AD524A	AD524B	
Parameter	Min Typ Max	Min Typ Max	Unit
INPUT			
Input Impedance			
Differential Resistance	10 <sup>9</sup>	10 <sup>9</sup>	Ω
Differential Capacitance	10	10	рF
Common-Mode Resistance	10 <sup>9</sup>	10 <sup>9</sup>	Ω
Common-Mode Capacitance	10	10	pF
Input Voltage Range			
Maximum Differential Input Linear (V <sub>DL</sub> ) <sup>2</sup>	±10	±10	V
Maximum Common-Mode Linear (V <sub>CM</sub> ) <sup>2</sup>	(G )		V
	$12 V - \left(\frac{G}{2} \times V_{D}\right)$	$12 \text{ V} - \left(\frac{\text{G}}{2} \times \text{V}_{\text{D}}\right)$	
Common-Mode Rejection DC to 60 Hz with 1 k $\Omega$ Source Imbalance			V
G = 1	70	75	dB
G = 10	90	95	dB
G = 100	100	105	dB
G = 1000	110	115	dB
OUTPUT RATING			
$V_{OUT}$ , $R_L = 2 k\Omega$	±10	±10	V
DYNAMIC RESPONSE			
Small Signal – 3 dB			
G = 1	1	1	MHz
G = 10	400	400	kHz
G = 100	150	150	kHz
G = 1000	25	25	kHz
Slew Rate	5.0	5.0	V/µs
Settling Time to 0.01%, 20 V Step			
G = 1 to 100	15	15	μs
G = 1000	75	75	μs
NOISE			
Voltage Noise, 1 kHz			
RTI	7	7	nV/√Hz
RTO	90	90	nV√Hz
RTI, 0.1 Hz to 10 Hz			
G = 1	15	15	μV p-p
G = 10	2	2	μV p-p
G = 100, 1000	0.3	0.3	μV p-p
Current Noise			
0.1 Hz to 10 Hz	60	60	рА р-р
SENSE INPUT			
R <sub>IN</sub>	20	20	kΩ ± 20%
I <sub>IN</sub>	15	15	μΑ
Voltage Range	±10	±10	V
Gain to Output	1	1	%
REFERENCE INPUT			
R <sub>IN</sub>	40	40	kΩ ± 20%
I <sub>IN</sub>	15	15	μΑ
Voltage Range	±10	±10	V
Gain to Output	1	1	%

		AD524	4A		AD52	4B	
Parameter	Min	Тур	Max	Min	Тур	Max	Unit
TEMPERATURE RANGE							
Specified Performance	-25		+85	-25		+85	°C
Storage	-65		+150	-65		+150	°C
POWER SUPPLY							
Power Supply Range	±6	±15	±18	±6	±15	±18	V
Quiescent Current		3.5	5.0		3.5	5.0	mA

 $<sup>^{\</sup>mbox{\tiny 1}}$  Does not include effects of external resistor,  $R_{\mbox{\tiny G}}.$ 

Example: G = 10,  $V_D = 0.50$ .

At  $V_S$  = ±15 V,  $R_L$  = 2 k $\Omega$  and  $T_A$  = +25°C, unless otherwise noted.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at the final electrical test. Results from those tests are used to calculate outgoing quality levels.

Table 2.

	Α	D524C	А	D524S	
Parameter	Min Ty	р Мах	Min Ty	ур Мах	Unit
GAIN					
Gain Equation (External Resistor Gain Programming)	40,00	n 7	[40.00	n 7	
	$\left[\frac{40,000}{R_G}\right]$	$\frac{6}{1} + 1 \pm 20\%$	$\frac{40,00}{R_G}$	$\begin{bmatrix} 0 \\ +1 \end{bmatrix} \pm 20\%$	
Gain Range (Pin Programmable)	1 1	to 1000	1 1	to 1000	
Gain Error <sup>1</sup>					
G = 1		±0.02		±0.05	%
G = 10		±0.1		±0.25	%
G = 100		±0.25		±0.5	%
G = 1000		±0.5		±2.0	%
Nonlinearity					
G = 1		±0.003		±0.01	%
G = 10, G = 100		±0.003		±0.01	%
G = 1000		±0.01		±0.01	%
Gain vs. Temperature					
G = 1		5		5	ppm/°C
G = 10		10		10	ppm/°C
G = 100		25		25	ppm/°C
G = 1000		50		50	ppm/°C
/OLTAGE OFFSET (May be Nulled)					
Input Offset Voltage		50		100	μV
vs. Temperature		0.5		2.0	μV/°C
Output Offset Voltage		2.0		3.0	mV
vs. Temperature		25		50	μV
Offset Referred to the Input vs. Supply					
G = 1	80		75		dB
G = 10	100		95		dB
G = 100	110		105		dB
G = 1000	115		110		dB

 $<sup>^{2}</sup>$  V<sub>OL</sub> is the maximum differential input voltage at G = 1 for specified nonlinearity.

 $V_{\text{DL}}$  at the maximum = 10 V/G.

 $V_D$  = actual differential input voltage.

 $V_{CM} = 12 \text{ V} - (10/2 \times 0.50 \text{ V}) = 9.5 \text{ V}.$ 

	AD524C	:	AD524	S	
Parameter	Min Typ		Min Typ	Max	Unit
INPUT CURRENT					
Input Bias Current		±15		±50	nA
vs. Temperature	±100		±100		pA/°C
Input Offset Current		±10		±35	nA
vs. Temperature	±100		±100		pA/°C
INPUT					
Input Impedance					
Differential Resistance	10 <sup>9</sup>		10 <sup>9</sup>		Ω
Differential Capacitance	10		10		pF
Common-Mode Resistance	10 <sup>9</sup>		10 <sup>9</sup>		Ω
Common-Mode Capacitance	10		10		pF
Input Voltage Range					'
Maximum Differential Input Linear (V <sub>DL</sub> ) <sup>2</sup>	±10	<u> </u>	±10		V
Maximum Common-Mode Linear (V <sub>CM</sub> ) <sup>2</sup>	(6		,	)	V
	$12 \text{ V} - \left(\frac{\text{G}}{2} \times \right)$	V <sub>D</sub>	$12 \text{ V} - \left(\frac{\text{G}}{2}\right)$	$\times$ $V_D$	
	(2	)	( 2	)	
Common-Mode Rejection DC to 60 Hz with 1 kΩ Source Imbalance					V
G = 1	80		70		dB
G = 10	100		90		dB
G = 100	110		100		dB
G = 1000	120	1	110		dB
OUTPUT RATING					
$V_{OUT}$ , $R_L = 2 k\Omega$	±10		±10		V
DYNAMIC RESPONSE					
Small Signal – 3 dB					
G = 1	1		1		MHz
G = 10	400		400		kHz
G = 100	150		150		kHz
G = 1000	25		25		kHz
Slew Rate	5.0		5.0		V/µs
Settling Time to 0.01%, 20 V Step					
G = 1  to  100	15		15		μs
G = 1000	75		75		μs
NOISE					
Voltage Noise, 1 kHz					
RTI	7		7		nV/√Hz
RTO	90		90		nV√Hz
RTI, 0.1 Hz to 10 Hz					
G = 1	15		15		μV р-р
G = 10	2		2		μV p-p
G = 100, 1000	0.3		0.3		μV р-р
Current Noise					
0.1 Hz to 10 Hz	60		60		рА р-р
SENSE INPUT					
R <sub>IN</sub>	20		20		$k\Omega \pm 20\%$
I <sub>IN</sub>	15		15		μΑ
Voltage Range	±10	<u> </u>	±10		٧
Gain to Output	1		1		%

		AD524C			AD524		
Parameter	Min	Тур	Max	Min	Тур	Max	Unit
REFERENCE INPUT							
R <sub>IN</sub>		40			40		$k\Omega \pm 20\%$
I <sub>IN</sub>		15			15		μΑ
Voltage Range	10			10			V
Gain to Output		1			1		%
TEMPERATURE RANGE							
Specified Performance	-25		+85	-55		+85	°C
Storage	-65		+150	-65		+150	°C
POWER SUPPLY							
Power Supply Range	±6	±15	±18	±6	±15	±18	V
Quiescent Current		3.5	5.0		3.5	5.0	mA

 $<sup>^1</sup>$  Does not include effects of external resistor R<sub>G</sub>.  $^2$  V<sub>OL</sub> is the maximum differential input voltage at G = 1 for specified nonlinearity. V<sub>DL</sub> at the maximum = 10 V/G. V<sub>D</sub> = actual differential input voltage. Example: G = 10, V<sub>D</sub> = 0.50. V<sub>CM</sub> = 12 V - (10/2  $\times$  0.50 V) = 9.5 V.

# **ABSOLUTE MAXIMUM RATINGS**

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation	450 mW
Input Voltage <sup>1</sup>	
(Either Input Simultaneously) $ V_{IN}  +  V_S $	<36 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
(R)	−65°C to +125°C
(D, E)	−65°C to +150°C
Operating Temperature Range	
AD524A/AD524B/AD524C	−25°C to +85°C
AD524S	−55°C to +125°C
Lead Temperature (Soldering, 60 sec)	+300°C

 $<sup>^1</sup>$  Maximum input voltage specification refers to maximum voltage to which either input terminal may be raised with or without device power applied. For example, with  $\pm 18$  volt supplies maximum,  $V_{\text{IN}}$  is  $\pm 18$  V; with zero supply voltage maximum,  $V_{\text{IN}}$  is  $\pm 36$  V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

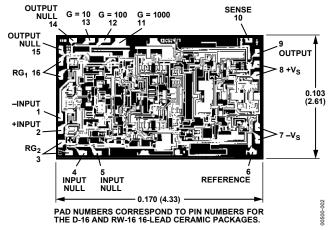


Figure 2. Metallization Photograph Contact factory for latest dimensions; Dimensions shown in inches and (mm)

### **CONNECTION DIAGRAMS**

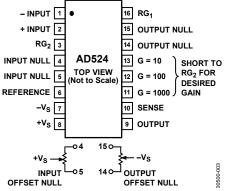
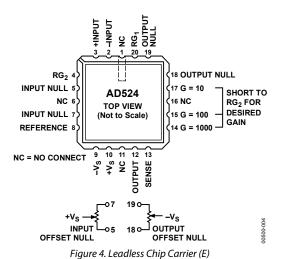


Figure 3. Ceramic (D) and SOIC (RW-16 and D-16) Packages



**ESD CAUTION** 



**ESD** (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

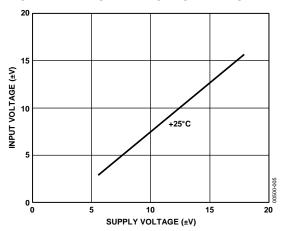


Figure 5. Input Voltage Range vs. Supply Voltage, G = 1

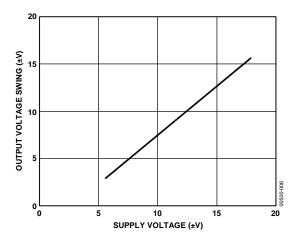


Figure 6. Output Voltage Swing vs. Supply Voltage

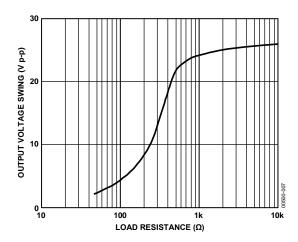


Figure 7. Output Voltage Swing vs. Load Resistance

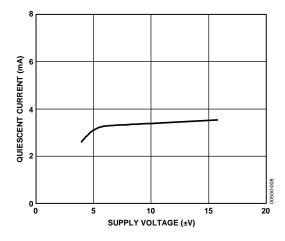


Figure 8. Quiescent Current vs. Supply Voltage

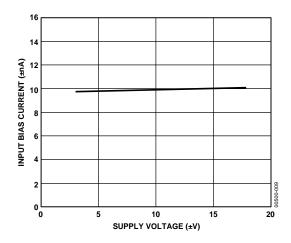


Figure 9. Input Bias Current vs. Supply Voltage

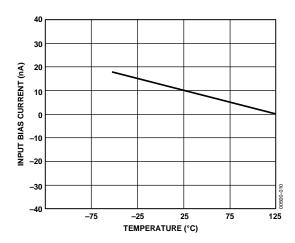


Figure 10. Input Bias Current vs. Temperature

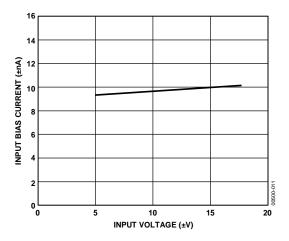


Figure 11. Input Bias Current vs. Input Voltage

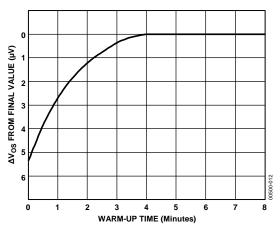


Figure 12. Offset Voltage, RTI, Turn-On Drift

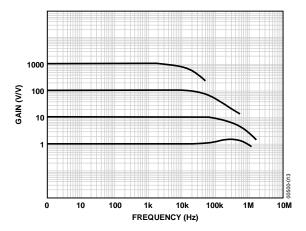


Figure 13. Gain vs. Frequency

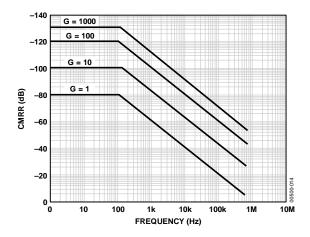


Figure 14. CMRR vs. Frequency, RTI, Zero to 1000 Source Imbalance

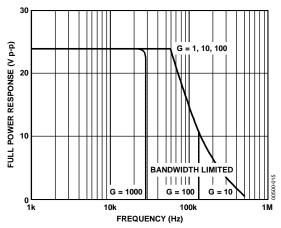


Figure 15. Large Signal Frequency Response

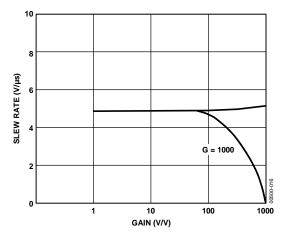


Figure 16. Slew Rate vs. Gain

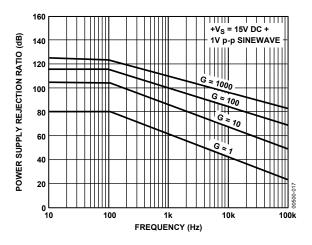


Figure 17. Positive PSRR vs. Frequency

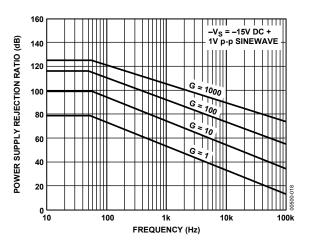


Figure 18. Negative PSRR vs. Frequency

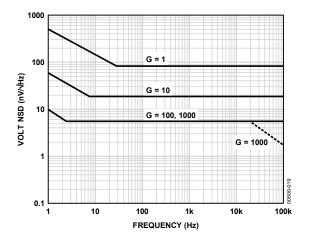


Figure 19. RTI Noise Spectral Density vs. Gain

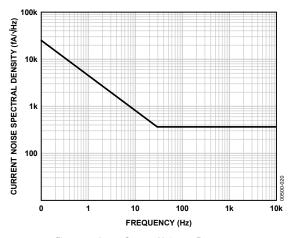


Figure 20. Input Current Noise vs. Frequency

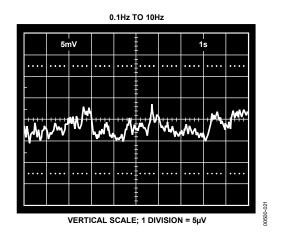


Figure 21. Low Frequency Noise, G = 1 (System Gain = 1000)

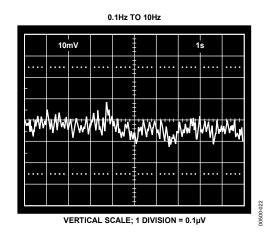


Figure 22. Low Frequency Noise, G = 1000 (System Gain = 100,000)

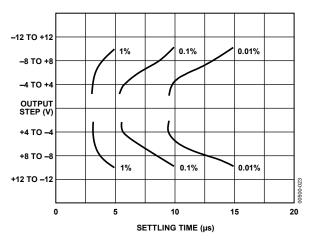


Figure 23. Settling Time, Gain = 1

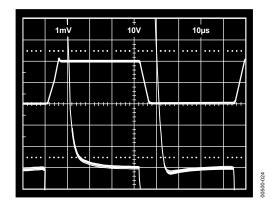


Figure 24. Large Signal Pulse Response and Settling Time, Gain =1

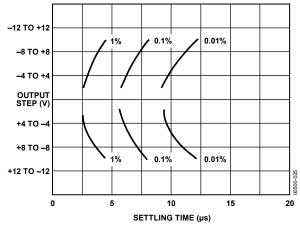


Figure 25. Settling Time, Gain = 10

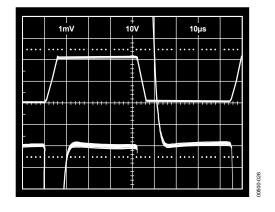


Figure 26. Large Signal Pulse Response and Settling Time, Gain = 10

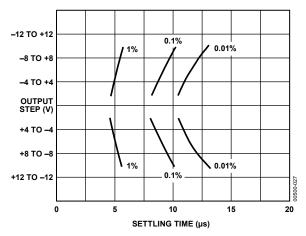


Figure 27. Settling Time, Gain = 100

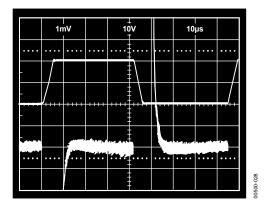


Figure 28. Large Signal Pulse Response and Settling Time, Gain = 100

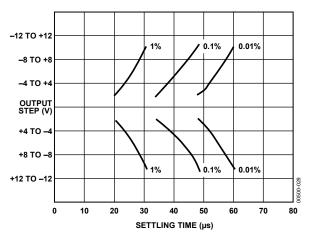


Figure 29. Settling Time, Gain = 1000

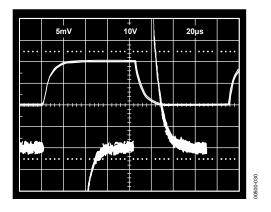


Figure 30. Large Signal Pulse Response and Settling Time, Gain = 1000

# **TEST CIRCUITS**

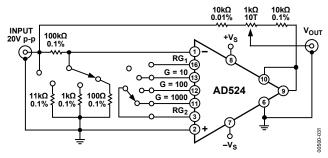


Figure 31. Settling Time Test Circuit

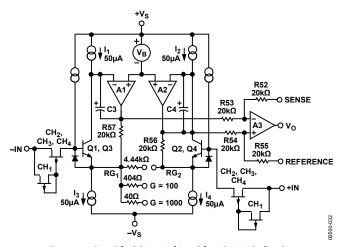


Figure 32. Simplified Circuit of Amplifier; Gain is Defined as  $((R56 + R57)/(R_G)) + 1$ ; For a Gain of 1,  $R_G$  is an Open Circuit

# THEORY OF OPERATION

The AD524 is a monolithic instrumentation amplifier based on the classic 3-op amp circuit. The advantage of monolithic construction is the closely matched components that enhance the performance of the input preamplifier. The preamplifier section develops the programmed gain by the use of feedback concepts. The programmed gain is developed by varying the value of  $R_{\rm G}$  (smaller values increase the gain) while the feedback forces the collector currents (Q1, Q2, Q3, and Q4) to be constant, which impresses the input voltage across  $R_{\rm G}$ .

As  $R_G$  is reduced to increase the programmed gain, the transconductance of the input preamplifier increases to the transconductance of the input transistors. This has three important advantages. First, this approach allows the circuit to achieve a very high open-loop gain of  $3 \times 10^8$  at a programmed gain of 1000, thus reducing gain-related errors to a negligible 30 ppm. Second, the gain bandwidth product, which is determined by C3 or C4 and the input transconductance, reaches 25 MHz. Third, the input voltage noise reduces to a value determined by the collector current of the input transistors for an RTI noise of  $7 \text{ nV}/\sqrt{\text{Hz}}$  at G = 1000.

#### **INPUT PROTECTION**

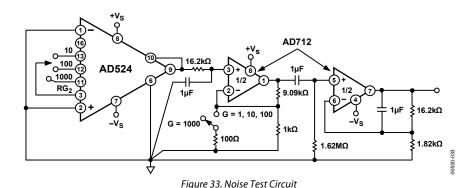
As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overloads, that is, voltage levels in excess of the full scale for the selected gain range. At low gains (10 or less), the gain resistor acts as a current limiting element in series with the inputs. At high gains, the lower value of  $R_{\rm G}$  does not adequately protect the inputs

from excessive currents. Standard practice is to place series limiting resistors in each input, but to limit input current to below 5 mA with a full differential overload (36 V) requires over  $7k\Omega$  of resistance, which adds  $10~\text{nV}\sqrt{\text{Hz}}$  of noise. To provide both input protection and low noise, a special series protection FET is used.

A unique FET design was used to provide a bidirectional current limit, thereby protecting against both positive and negative overloads. Under nonoverload conditions, three channels (CH<sub>2</sub>, CH<sub>3</sub>, CH<sub>4</sub>) act as a resistance ( $\approx$ 1 k $\Omega$ ) in series with the input as before. During an overload in the positive direction, a fourth channel, CH<sub>1</sub>, acts as a small resistance ( $\approx$ 3 k $\Omega$ ) in series with the gate, which draws only the leakage current, and the FET limits I<sub>DSS</sub>. When the FET enhances under a negative overload, the gate current must go through the small FET formed by CH<sub>1</sub> and when this FET goes into saturation, the gate current is limited and the main FET goes into controlled enhancement. The bidirectional limiting holds the maximum input current to 3 mA over the 36 V range.

#### INPUT OFFSET AND OUTPUT OFFSET

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations causes errors. Intelligent systems can often correct this factor with an auto-zero cycle, but there are many small-signal high-gain applications that do not have this capability.



Rev. G | Page 15 of 25

Voltage offset and drift comprise two components each; input and output offset and offset drift. Input offset is the component of offset that is directly proportional to gain, that is, input offset as measured at the output at G=100 is 100 times greater than at G=1. Output offset is independent of gain. At low gains, output offset drift is dominant, at high gains, input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G=1 (where input effects are insignificant), whereas input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input related numbers are referred to the input (RTI) that is the effect on the output is G times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

By separating these errors, one can evaluate the total error independent of the gain setting used. In a given gain configuration, both errors can be combined to give a total error referred to the input (RTI) or output (RTO) by the following formulas:

Total error RTI = input error + (output error/gain)

 $Total\ error\ RTO = (gain \times input\ error) + output\ error$ 

As an illustration, a typical AD524 might have a +250  $\mu V$  output offset and a -50  $\mu V$  input offset. In a unity gain configuration, the total output offset would be 200  $\mu V$  or the sum of the two. At a gain of 100, the output offset would be -4.75 mV or: +250  $\mu V$  + 100(-50  $\mu V)$  = -4.75 mV.

The AD524 provides for both input and output offset adjustment. This simplifies very high precision applications and minimizes offset voltage changes in switched gain applications. In such applications, the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G=1.

#### **GAIN**

The AD524 has internal high accuracy pretrimmed resistors for pin programmable gains of 1, 10, 100, and 1000. One of the preset gains can be selected by pin strapping the appropriate gain terminal and  $RG_2$  together (for G = 1,  $RG_2$  is not connected).

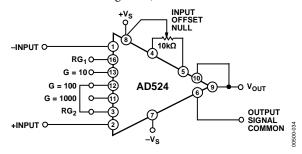


Figure 34. Operating Connections for G = 100

The AD524 can be configured for gains other than those that are internally preset; there are two methods to do this. The first method uses just an external resistor connected between Pin 3 and Pin 16 (see Figure 35), which programs the gain according to the following formula:

$$R_G = \frac{40 \text{ k}\Omega}{G = -1}$$

For best results,  $R_G$  should be a precision resistor with a low temperature coefficient. An external  $R_G$  affects both gain accuracy and gain drift due to the mismatch between it and the internal thin-film resistors. Gain accuracy is determined by the tolerance of the external  $R_G$  and the absolute accuracy of the internal resistors ( $\pm 20\%$ ). Gain drift is determined by the mismatch of the temperature coefficient of  $R_G$  and the temperature coefficient of the internal resistors ( $\pm 50$  ppm/°C typical).

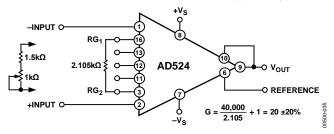


Figure 35. Operating Connections for G = 20

The second method uses the internal resistors in parallel with an external resistor (see Figure 36). This technique minimizes the gain adjustment range and reduces the effects of temperature coefficient sensitivity.

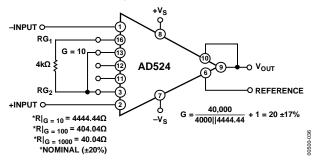


Figure 36. Operating Connections for G = 20, Low Gain Temperature Coefficient Technique

The AD524 can also be configured to provide gain in the output stage. Figure 37 shows an H pad attenuator connected to the reference and sense lines of the AD524. R1, R2, and R3 should be made as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 precisely sets the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

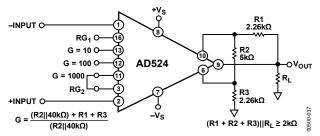


Figure 37. Gain of 2000

**Table 4. Output Gain Resistor Values** 

Output Gain	R2	R1, R3	Nominal Gain
2	5 kΩ	2.26 kΩ	2.02
5	1.05 kΩ	2.05 kΩ	5.01
10	1 kΩ	4.42 kΩ	10.1

#### **INPUT BIAS CURRENTS**

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. Bias currents are an additional source of input error and must be considered in a total error budget. The bias currents, when multiplied by the source resistance, appear as an offset voltage. What is of concern in calculating bias current errors is the change in bias current with respect to signal voltage and temperature. Input offset current is the difference between the two input bias currents. The effect of offset current is an input offset voltage whose magnitude is the offset current times the source impedance imbalance.

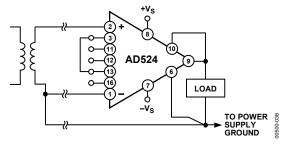


Figure 38. Indirect Ground Returns for Bias Currents—Transformer Coupled

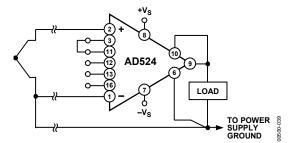


Figure 39. Indirect Ground Returns for Bias Currents—Thermocouple

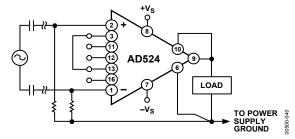


Figure 40. Indirect Ground Returns for Bias Currents-AC-Coupled

Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying floating input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground.

### **COMMON-MODE REJECTION**

Common-mode rejection is a measure of the change in output voltage when both inputs are changed equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. Common-mode rejection ratio (CMRR) is a ratio expression whereas common-mode rejection (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80 dB.

In an instrumentation amplifier, ac common-mode rejection is only as good as the differential phase shift. Degradation of ac common-mode rejection is caused by unequal drops across differing track resistances and a differential phase shift due to varied stray capacitances or cable capacitances. In many applications, shielded cables are used to minimize noise. This technique can create common-mode rejection errors unless the shield is properly driven. Figure 41 and Figure 42 show active data guards that are configured to improve ac common-mode rejection by bootstrapping the capacitances of the input cabling, thus minimizing differential phase shift.

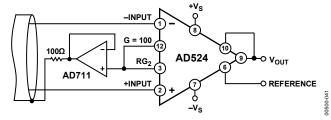


Figure 41. Shield Driver,  $G \ge 100$ 

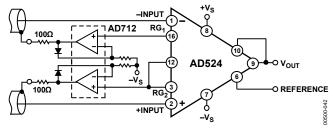


Figure 42. Differential Shield Driver

#### **GROUNDING**

Many data acquisition components have two or more ground pins that are not connected together within the device. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, because current flows through the ground wires and etch stripes of the circuit cards, and because these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the data acquisition components. Separate ground returns should be provided to minimize the current flow in the path from the sensitive points to the system ground point. In this way, supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Because the output voltage is developed with respect to the potential on the reference terminal, an instrumentation amplifier can solve many grounding problems.

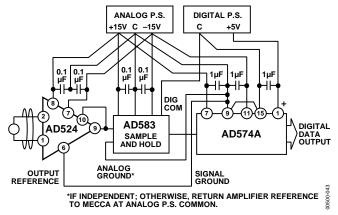


Figure 43. Basic Grounding Practice

### **SENSE TERMINAL**

The sense terminal is the feedback point for the instrument amplifier's output amplifier. Normally, it is connected to the instrument amplifier output. If heavy load currents are to be drawn through long leads, voltage drops due to current flowing through lead resistance can cause errors. The sense terminal can be wired to the instrument amplifier at the load, thus putting the IxR drops inside the loop and virtually eliminating this error source.

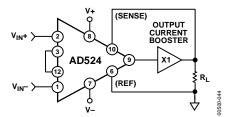


Figure 44. AD524 Instrumentation Amplifier with Output Current Booster

Typically, IC instrumentation amplifiers are rated for a full  $\pm 10$  volt output swing into 2 k $\Omega.$  In some applications, however, the need exists to drive more current into heavier loads. Figure 44 shows how a high current booster may be connected inside the loop of an instrumentation amplifier to provide the required current boost without significantly degrading overall performance. Nonlinearities and offset and gain inaccuracies of the buffer are minimized by the loop gain of the AD524 output amplifier. Offset drift of the buffer is similarly reduced.

#### REFERENCE TERMINAL

The reference terminal can be used to offset the output by up to  $\pm 10$  V. This is useful when the load is floating or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered that the total output swing is  $\pm 10$  V to be shared between signal and reference offset.

When the AD524 is of the 3-amplifier configuration it is necessary that nearly zero impedance be presented to the reference terminal.

Any significant resistance from the reference terminal to ground increases the gain of the noninverting signal path, thereby upsetting the common-mode rejection of the AD524.

In the AD524, a reference source resistance unbalances the CMR trim by the ratio of 20 k $\Omega/R_{REF}.$  For example, if the reference source impedance is 1  $\Omega$ , CMR is reduced to 86 dB (20 k $\Omega/1$   $\Omega$  = 86 dB). An operational amplifier can be used to provide that low impedance reference point, as shown in Figure 45. The input offset voltage characteristics of that amplifier adds directly to the output offset voltage performance of the instrumentation amplifier.

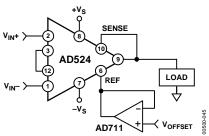


Figure 45. Use of Reference Terminal to Provide Output Offset

An instrumentation amplifier can be turned into a voltageto-current converter by taking advantage of the sense and reference terminals, as shown in Figure 46.

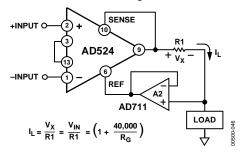


Figure 46. Voltage-to-Current Converter

By establishing a reference at the low side of a current setting resistor, an output current may be defined as a function of input voltage, gain, and the value of that resistor. Because only a small current is demanded at the input of the buffer amplifier (A2)

the forced current,  $I_L$ , largely flows through the load. Offset and drift specifications of A2 must be added to the output offset and drift specifications of the AD524.

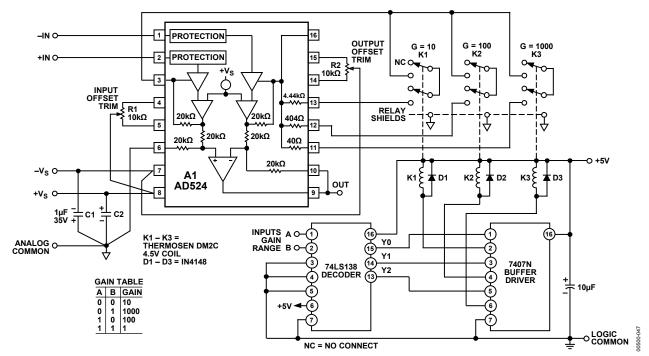


Figure 47. Three-Decade Gain Programmable Amplifier

#### **PROGRAMMABLE GAIN**

Figure 47 shows the AD524 being used as a software programmable gain amplifier. Gain switching can be accomplished with mechanical switches such as DIP switches or reed relays. It should be noted that the on resistance of the switch in series with the internal gain resistor becomes part of the gain equation and has an effect on gain accuracy.

The AD524 can also be connected for gain in the output stage. Figure 48 shows an AD711 used as an active attenuator in the output amplifier's feedback loop. The active attenuation presents very low impedance to the feedback resistors, therefore minimizing the common-mode rejection ratio degradation.

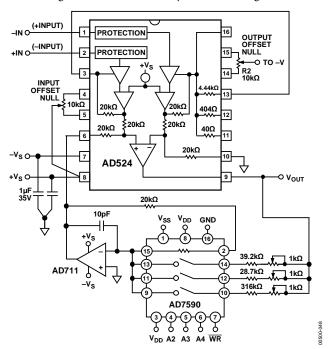


Figure 48. Programmable Output Gain

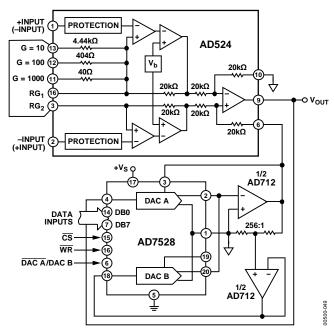


Figure 49. Programmable Output Gain Using a DAC

Another method for developing the switching scheme is to use a DAC. The AD7528 dual DAC, which acts essentially as a pair of switched resistive attenuators having high analog linearity and symmetrical bipolar transmission, is ideal in this application. The multiplying DAC's advantage is that it can handle inputs of either polarity or zero without affecting the programmed gain. The circuit shown uses an AD7528 to set the gain (DAC A) and to perform a fine adjustment (DAC B).

#### **AUTO-ZERO CIRCUITS**

In many applications, it is necessary to provide very accurate data in high gain configurations. At room temperature, the offset effects can be nulled by the use of offset trim potentiometers. Over the operating temperature range, however, offset nulling becomes a problem. The circuit of Figure 50 shows a CMOS DAC operating in bipolar mode and connected to the reference terminal to provide software controllable offset adjustments.

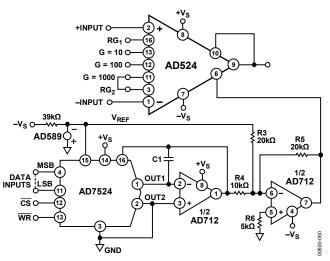
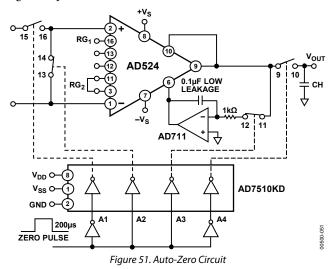


Figure 50. Software Controllable Offset

In many applications, complex software algorithms for autozero applications are not available. For those applications, Figure 51 provides a hardware solution.



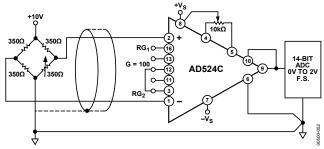


Figure 52. Typical Bridge Application

#### **ERROR BUDGET ANALYSIS**

To illustrate how instrumentation amplifier specifications are applied, review a typical case where an AD524 is required to amplify the output of an unbalanced transducer. Figure 52 shows a differential transducer, unbalanced by 100  $\Omega$ , supplying a 0 mV to 20 mV signal to an AD524C. The output of the  $I_A$  feeds a 14-bit ADC with a 0 V to 2 V input voltage range. The operating temperature range is  $-25^{\circ}$ C to  $+85^{\circ}$ C. Therefore, the largest change in temperature,  $\Delta$ T, within the operating range is from ambient to  $+85^{\circ}$ C ( $85^{\circ}$ C  $-25^{\circ}$ C =  $60^{\circ}$ C).

In many applications, differential linearity and resolution are of prime importance in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (45 ppm = 0.004%) are significant. Furthermore, if a system has an intelligent processor monitoring the analog-to-digital output, the addition of an autogain/auto-zero cycle removes all reducible errors and may eliminate the requirement for initial calibration. This also reduces errors to 0.004%.

**Table 5. Error Budget Analysis** 

			Effect on Absolute	Effect on Absolute	Effect
Error Source	AD524C Specifications	Calculation	Accuracy at T <sub>A</sub> = 25°C	Accuracy at T <sub>A</sub> = 85°C	on Resolution
Gain Error	±0.25%	±0.25% = 2500 ppm	2500 ppm	2500 ppm	-
Gain Instability	25 ppm	(25 ppm/°C)(60°C) = 1500 ppm	_	1500 ppm	_
Gain Nonlinearity	±0.003%	±0.003% = 30 ppm	_	_	30 ppm
Input Offset Voltage	±50 μV, RTI	$\pm 50 \mu\text{V}/20 \text{mV} = \pm 2500 \text{ppm}$	2500 ppm	2500 ppm	_
Input Offset Voltage Drift	±0.5 μV/°C -	$(\pm 0.5 \mu\text{V/°C})(60^{\circ}\text{C}) = 30 \mu\text{V}$ 30 $\mu\text{V}/20 \text{mV} = 1500 \text{ppm}$	-	1500 ppm	-
Output Offset Voltage <sup>1</sup>	±2.0 mV	±2.0 mV/20 mV = 1000 ppm	1000 ppm	1000 ppm	_
Output Offset Voltage Drift <sup>1</sup>	±25 μV/°C	$(\pm 25 \mu V/^{\circ}C)(60^{\circ}C) = 1500 \mu V$ 1500 μV/20 mV = 750 ppm	_	750 ppm	-
Bias Current-Source Imbalance Error	±15 nA	$(\pm 15 \text{ nA})(100 \Omega) = 1.5 \mu\text{V}$ 1.5 μV/20 mV = 75 ppm	75 ppm	75 ppm	-
Bias Current-Source Imbalance Drift	±100 pA/°C	$(\pm 100 \text{ pA/°C})(100 \Omega)(60 ^{\circ}\text{C}) = 0.6 \mu\text{V}$ 0.6 μV/20 mV = 30 ppm	-	30 ppm	-
Offset Current-Source Imbalance Error	±10 nA	$(\pm 10 \text{ nA})(100 \Omega) = 1 \mu\text{V}$ 1 μV/20 mV = 50 ppm	50 ppm	50 ppm	-
Offset Current-Source Imbalance Drift	±100 pA/°C	(100 pA/°C)(100 Ω)(60°C) = 0.6 μV 0.6 μV/20 mV = 30 ppm	-	30 ppm	-
Offset Current-Source Resistance-Error	±10 nA	(10 nA)(175 $\Omega$ ) = 3.5 $\mu$ V 3.5 $\mu$ V/20 mV = 87.5 ppm	87.5 ppm	87.5 ppm	-
Offset Current-Source Resistance-Drift	±100 pA/°C	(100 pA/°C)(175 $\Omega$ )(60°C) = 1 $\mu$ V 1 $\mu$ V/20 mV = 50 ppm	-	50 ppm	-
Common Mode Rejection 5 V DC	115 dB	115 dB = 1.8 ppm $\times$ 5 V = 8.8 $\mu$ V 8.8 $\mu$ V/20 mV = 444 ppm	444 ppm	444 ppm	-
Noise, RTI (0.1 Hz to 10 Hz)	0.3 μV p-p	0.3 μV p-p/20 mV = 15 ppm	_	_	15 ppm
	•	Total Error	6656.5 ppm	10516.5 ppm	45 ppm

<sup>&</sup>lt;sup>1</sup> Output offset voltage and output offset voltage drift are given as RTI figures.

Figure 53 shows a simple application in which the variation of the cold junction voltage of a Type J thermocouple-iron  $\pm$  constantan is compensated for by a voltage developed in series by the temperature sensitive output current of an AD590 semiconductor temperature sensor.

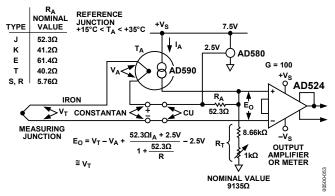


Figure 53. Cold Junction Compensation

The circuit is calibrated by adjusting  $R_T$  for proper output voltage with the measuring junction at a known reference temperature and the circuit near 25°C. If resistors with low temperature coefficients are used, compensation accuracy is to within  $\pm 0.5$ °C, for temperatures between +15°C and +35°C. Other thermocouple types may be accommodated with the standard resistance values shown in Table 5. For other ranges

of ambient temperature, the equation in Figure 53 may be solved for the optimum values of  $R_T$  and  $R_A$ .

The microprocessor controlled data acquisition system shown in Figure 54 includes both auto-zero and autogain capability. By dedicating two of the differential inputs, one to ground and one to the A/D reference, the proper program calibration cycles can eliminate both initial accuracy errors and accuracy errors over temperature. The auto-zero cycle, in this application, converts a number that appears to be ground and then writes that same number (8-bit) to the AD7524, which eliminates the zero error. Because its output has an inverted scale, the autogain cycle converts the A/D reference and compares it with full-scale. A multiplicative correction factor is then computed and applied to subsequent readings.

#### **REFERENCES**

The following reference materials provide additional information that supplements material found in the data sheet.

A Designer's Guide to Instrumentation Amplifiers, 3<sup>RD</sup> Edition, 2006. Analog Devices.

Application Note, AN-306, *Synchronous System Measures*  $\mu\Omega s$ , Analog Devices.

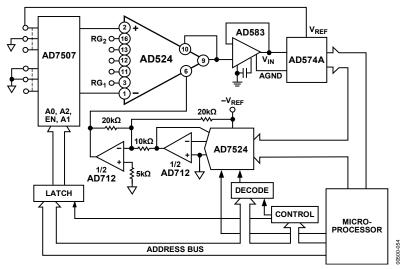
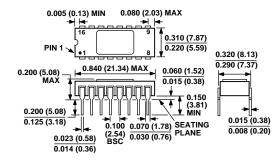


Figure 54. Microprocessor Controlled Data Acquisition System

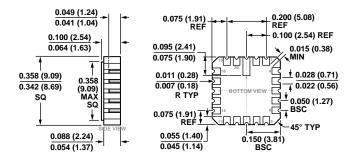
# **OUTLINE DIMENSIONS**



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 55. 16-Lead Side-Brazed Ceramic Dual In-Line [SBDIP] (D-16)

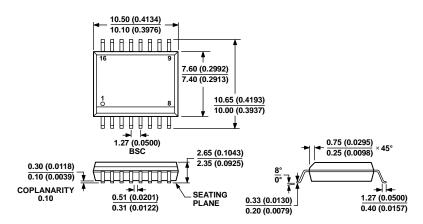
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 56. 20-Terminal Ceramic Leadless Chip Carrier [LCC] (E-20)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 57. 16-Lead Standard Small Outline Package [SOIC\_W] Wide Body (RW-16) Dimensions shown in millimeters and (inches) 32707-

# **ORDERING GUIDE**

Model <sup>1, 2</sup>	Temperature Range	Package Description	Package Option
AD524AD	-40°C to +85°C	16-Lead SBDIP	D-16
AD524ADZ	-40°C to +85°C	16-Lead SBDIP	D-16
AD524AR-16	-40°C to +85°C	16-Lead SOIC_W	RW-16
AD524ARZ-16	-40°C to +85°C	16-Lead SOIC_W	RW-16
AD524ARZ-16-REEL7	-40°C to +85°C	16-Lead SOIC_W, 7"Tape and Reel	RW-16
AD524BD	-40°C to +85°C	16-Lead SBDIP	D-16
AD524BDZ	-40°C to +85°C	16-Lead SBDIP	D-16
AD524BE	-40°C to +85°C	20-Terminal LCC	E-20
AD524CD	-40°C to +85°C	16-Lead SBDIP	D-16
AD524CDZ	-40°C to +85°C	16-Lead SBDIP	D-16
AD524SD	−55°C to +125°C	16-Lead SBDIP	D-16
AD524SD/883B	−55°C to +125°C	16-Lead SBDIP	D-16
5962-8853901EA	−55°C to +125°C	16-Lead SBDIP	D-16
AD524SE/883B	−55°C to +125°C	20-Terminal LCC	E-20
AD524SCHIPS	−55°C to +125°C	Die	

<sup>&</sup>lt;sup>1</sup> Z = RoHS Compliant Part.

<sup>&</sup>lt;sup>2</sup> Refer to the official DESC drawing for tested specifications of the 5962-8853901EA model.