A3901

Dual Full Bridge Low Voltage Motor Driver

SELECTION GUIDE

Part Number	Packing
A3901SEJTR-T	Tape and reel, 1500 pieces/reel

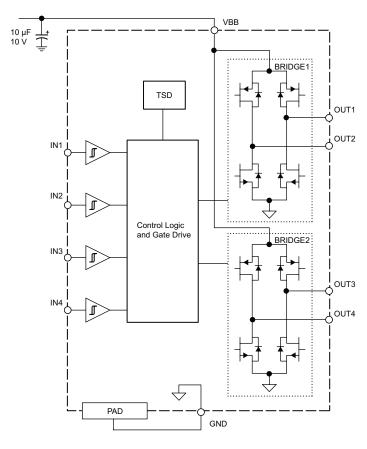
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Load Supply Voltage	V_{BB}		_	-	7	V
Output Current per Channel*	I _{OUT}		_	_	400	mA
Logic Input Voltage Range	V _{IN}		-0.3	-	6	V
Junction Temperature	T_{J}		-	-	150	°C
Storage Temperature Range	$T_{ m stg}$		-55	-	150	°C
Operating Temperature Range	T _A		-20	-	85	°C

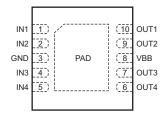
^{*}Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.



FUNCTIONAL BLOCK DIAGRAM



TERMINAL DIAGRAM



Number	Name	Description
1	IN1	Logic input 1
2	IN2	Logic input 2
3	GND	Ground terminal
4	IN3	Logic input 3
5	IN4	Logic input 4
6	OUT4	Bridge2 output to load
7	OUT3	Bridge2 output to load
8	VBB	Load supply terminal
9	OUT2	Bridge1 output to load
10	OUT1	Bridge1 output to load
_	Pad	Exposed pad for thermal dissipation; connect to GND externally



A3901

Dual Full Bridge Low Voltage Motor Driver

ELECTRICAL CHARACTERISTICS at $T_A\!=\!25^{\circ}\text{C},$ and $V_{BB}\!=\!2.5$ to 5.5 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Тур.	Max.	Units
		Source driver, V _{BB} = 3 V, I _{OUT} = 300 mA	1	1.8	2.2	Ω
Output On Resistance	P	Source driver, $V_{BB} = 5 \text{ V}$, $I_{OUT} = 300 \text{ mA}$	1	1.2	1.4	Ω
Output On Resistance	R _{DS(on)}	Sink driver, $V_{BB} = 3 \text{ V}$, $I_{OUT} = 300 \text{ mA}$	0.5	1.2	1.4	Ω
		Sink driver, $V_{BB} = 5 \text{ V}$, $I_{OUT} = 300 \text{ mA}$	0.5	0.8	1.0	Ω
Clamp Diode		I = 300 mA		_	1.5	V
		All outputs PWMed at 20 kHz		0.6	-	mA
Motor Supply Current	I_{BB}	Sleep mode, V _{BB} = 3 V		_	100	nA
		Sleep mode, V _{BB} = 5 V		< 50	500	nA
Logic Input Voltage	V _{IN(1)}		V _{BB} /2	_	-	V
	V _{IN(0)}		_	_	0.5	V
Lagia Input Current	I _{IN(1)}	$V_{IN} = 2.0 \text{ V}$		<100	500	nA
Logic Input Current	I _{IN(0)}	$V_{IN} = 0.5 V$		<-100	-500	nA
Input Voltage Hysteresis	V _{hys}		_	150	-	mV
Propagation Delay	t _{pd(on)}	Input Low to Sink On, Input High to Source On	_	130	_	ns
	t _{pd(off)}	Input High to Sink Off, Input Low to Source Off		50	-	ns
Crossover Delay	t _{COD}		_	80	_	ns
Thermal Shut Down Temperature	T_{J}			150	-	°C
Thermal Shut Down Hysteresis	T_{Jhys}		_	10	_	°C

THERMAL CHARACTERISTICS								
Characteristics	Symbol	Test Conditions	Rating	Unit				
	$R_{ heta JA}$	Measured on 4-layer board based on JEDEC standard	45	°C/W				
Package Thermal Resistance*		Measured on 2-layer board with copper limited to solder pads and 0.88 in ² . of copper on each side	65	°C/W				

^{*}Additional thermal information is available on the Allegro Web site.



MOTOR OPERATION TRUTH TABLE

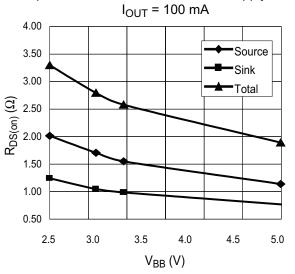
	IN	[x ¹		OUT12	OUT2	OUT3	OUT4	Function		
Stepper Motor										
IN1	IN2	IN3	IN4					Full Stepping	Half-Stepping	
0	0	0	0	OFF	OFF	OFF	OFF	Sleep Mode	Sleep Mode	
1	0	1	0	Н	L	Н	L	Step 1	Step 1	
0	0	1	0	OFF	OFF	Н	L	_	Step 2	
0	1	1	0	L	Н	Н	L	Step 2	Step 3	
0	1	0	0	L	Н	OFF	OFF	_	Step 4	
0	1	0	1	L	Н	L	Н	Step 3	Step 5	
0	0	0	1	OFF	OFF	L	Н	_	Step 6	
1	0	0	1	Н	L	L	Н	Step 4	Step 7	
1	0	0	0	Н	L	OFF	OFF	_	Step 8	
DC Moto	or (Dual)									
IN1 o	r IN3	IN2 o	r IN4							
()	()	OFF	OFF	OFF	OFF	Hi-Z (Sleep Mode)/Coast		
1	1	0		Н	L	Н	L	Forward		
()	1		L	Н	L	Н	Reverse		
1	1		1	L	L	L	L	Brake		
DC Moto	r (Single,	Parallele	d)							
IN1 aı	nd IN3	IN2 aı	nd IN4							
()	()	OFF	OFF	OFF	OFF	Hi-Z (Sleep Mode)/Coast		
	1	()	Н	L	Н	L	For	ward	
()		1	L	Н	L	Н	Rev	erse	
	1		1	L	L	L	L	Brake		
DC Moto	or (Extern									
IN1 o	r IN3	IN2 o	r IN4							
	1	(0	Н	L	Н	L	Forward		
()	0		OFF	OFF	OFF	OFF	Fast Decay		
()		1	L	Н	L	Н	Reverse		
(0	(0	OFF	OFF	OFF	OFF	Fast Decay		
	1		0	Н	L	Н	L	Forward		
	1		1	L	L	L	L	Slow Decay		
	2		1	L	Н	L	Н	Reverse		
(J		1		11		1 1	100	CIBC	



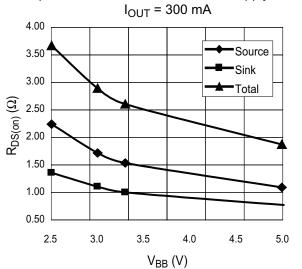
 $[\]begin{array}{l} {}^{1}0=logic\ low,\ V_{INx}{<}\ V_{IN(0)(max)};\ 1=logic\ high,\ V_{INx}{>}\ V_{IN(1)(min)} \\ {}^{2}H=voltage\ high,\ source\ driver\ on;\ L=voltage\ low,\ sink\ driver\ on \end{array}$

CHARACTERISTIC PERFORMANCE

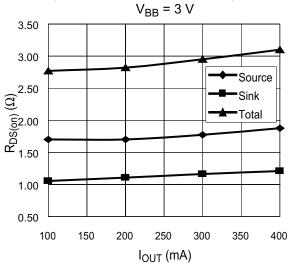
Output On Resistance versus Load Supply Voltage



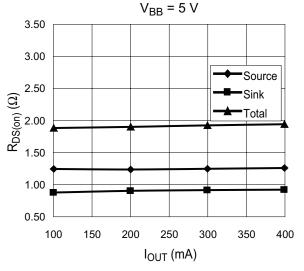
Output On Resistance versus Load Supply Voltage



Output On Resistance versus Output Current



Output On Resistance versus Output Current





FUNCTIONAL DESCRIPTION

Device Operation. The A3901 is a dual full-bridge low voltage motor driver capable of operating one stepper motor or up to two DC motors. MOSFET output stages substantially reduce the voltage drop and the power dissipation of the outputs of the A3901 compared to typical drivers with bipolar transistors.

Internal circuit protection includes thermal shutdown with hysteresis, clamp diodes, and crossover current protection.

The A3901 is designed for portable applications with a power-off (Sleep mode) current of 50 nA typical, and an operating voltage of 2.5 to 5.5 V. The A3901 logic inputs are 3 to 5 V logic compatible.

Output current can be regulated by pulse width modulating (PWM) the inputs. The full-bridge outputs can be paralleled for higher-current applications (see figure 6).

In conditions where the logic supply voltage drops below 2.5 V, both the sink and the source $R_{DS(on)}$ will increase beyond the specified values. In extreme cases, no power will be delivered to the motor(s). However, the device will not be damaged.

In stepping operation, the device can drive in either full- or half-step mode. The stepping mode is set by the signal pattern on the INx terminals, as shown in the stepping timing diagrams.

External PWM. Pulse width modulating the inputs allows the output current to be regulated. Slow decay mode is achieved by holding one input high while PWMing the other input. Holding one input low and PWMing the other input results in fast decay. See the External PWM diagram.

Sleep Mode. Pulling all inputs to 0.5 V or less, sends the A3901 into Sleep mode, during which it draws 50 nA typical.

Thermal Shutdown. The A3901 will disable the outputs if the junction temperature reaches 165°C. When thermal shutdown is entered, after the junction temperature drops 15°C, the outputs will be re-enabled.

Brake Mode. When driving DC motors, the A3901 will go into Brake mode (turn on both sink drivers) when all inputs, INx, are logic 1. There is no protection during braking, so care must be taken to ensure that the peak current during braking does not exceed the absolute maximum current.



APPLICATION INFORMATION

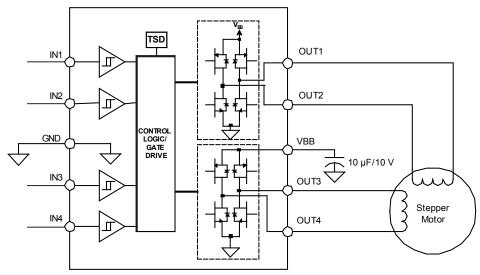


Figure 4a. Typical stepper motor control application

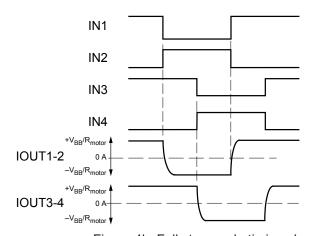


Figure 4b. Full step mode timing chart

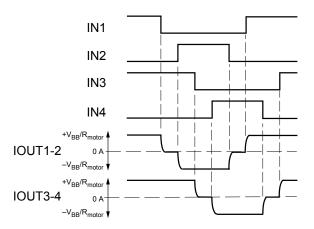


Figure 4c. Half step mode timing chart



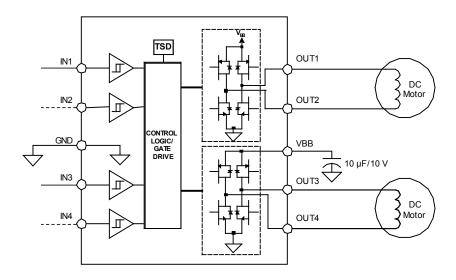


Figure 5. Typical dual DC motor control application. Either IN1 or IN2 can be used to drive OUT1 and OUT2. Either IN3 or IN4 can be used to drive OUT3 and OUT4.

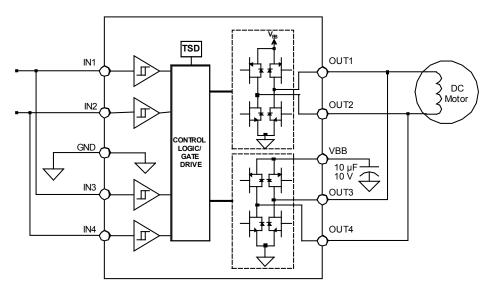


Figure 6. Typical single DC motor control (paralleled outputs)



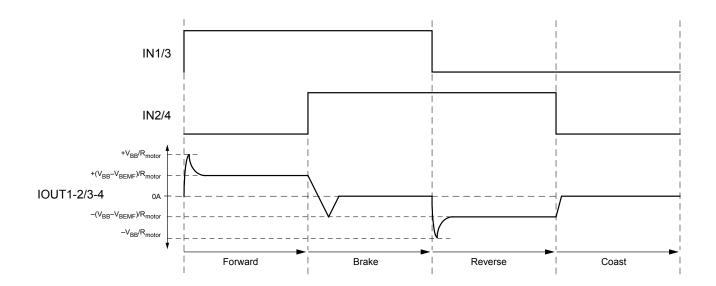


Figure 7. Typical dual DC motor control application

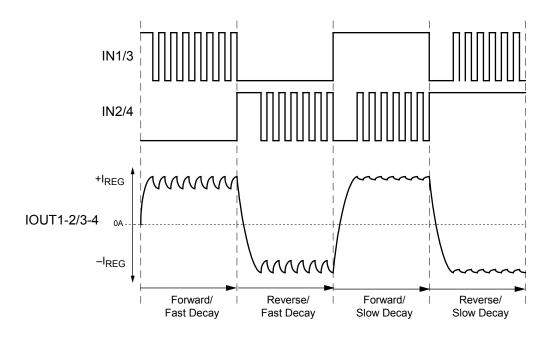
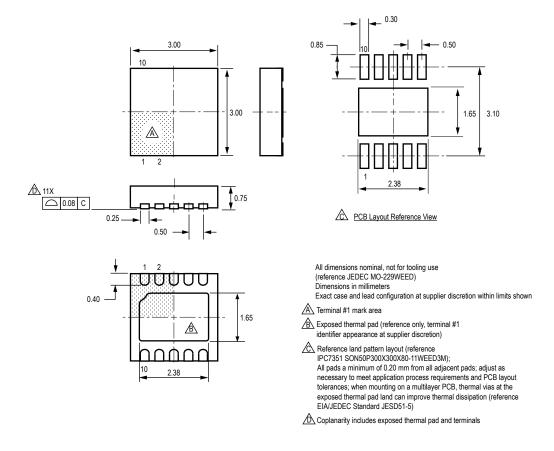


Figure 8. External PWM current control in fast and slow decay modes



Package EJ, 10-contact DFN



A3901

Dual Full Bridge Low Voltage Motor Driver

Revision History

Number	Date	Description			
4	June 19, 2013	Update R _{DS(on)} specifications			
5	February 7, 2014	Updated Electrical Characteristics and disclaimer statement			
6	March 12, 2019	Minor editorial updates			
7	March 18, 2020	Minor editorial updates			

Copyright 2020, Allegro MicroSystems.

Allegro MicroSystems reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in any devices or systems, including but not limited to life support devices or systems, in which a failure of Allegro's product can reasonably be expected to cause bodily harm.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

Copies of this document are considered uncontrolled documents.

For the latest version of this document, visit our website:

www.allegromicro.com

