Description (continued)

These devices include, on a single silicon chip, a Hall-voltage generator, small-signal amplifier, chopper stabilization, a latch, and a MOSFET output. Advanced BiCMOS processing is used to take advantage of low-voltage and low-power requirements, component matching, very low input-offset errors, and small component geometries.

Range 'E' devices are rated for operation over a temperature range of -40°C to 85°C; range 'L' devices are rated for operation over a temperature range of -40°C to 150°C. Two package styles provide a magnetically optimized package for most applications. 'LH' is a miniature low-profile surface-mount package, 'UA' is a three-lead SIP for through-hole mounting. For the A3213, a microleadless DFN/MLP package 'EL' also is available. Each package is available in a lead (Pb) free version (suffix, –T) , with a 100% matte tin plated leadframe.

Product Selection Guide

Part Number	Mounting	Packing[1]	Ambient, T_A (ºC)	DC (%)	$I_{DDAVG(TYP)}$ (µA)
A3213EELLT-T[2]	EL package, MLP/DFN Surface mount	7-in. reel 3000 pieces/reel	–40 to 85	25	460
A3213ELHLT-T	LH package Surface Mount				
A3213EUA-T	UA package SIP through hole	Bulk 500 pieces/bag			
~~A3213LLHLT-T[3]~~	LH package Surface Mount	7-in. reel 3000 pieces/reel	–40 to 150		
~~A3213LUA-T[3]~~	UA package SIP through hole	Bulk 500 pieces/bag			
A3214ELHLT-T	LH package Surface Mount	7-in. reel 3000 pieces/reel	–40 to 85	0.10	11
~~A3214LLHLT-T[3]~~	LH package Surface Mount	7-in. reel 3000 pieces/reel	–40 to 150		
~~A3214LUA-T[3]~~	UA package SIP through hole	Bulk 500 pieces/bag			

[1]Contact Allegro for additional packing options.
[2]Allegro products sold in DFN package types are not intended for automotive applications.
[3]Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change May 2, 2011. Deadline for receipt of LAST TIME BUY orders is October 31, 2011. Recommended substitutes: for the A3213LLHLT-T use the A3213ELHLT-T, for the A3213LUA-T use the A3213EUA-T, for the A3214LLHLT-T use the A3214ELHLT-T, and for the A3214LUA-T use the A3214EUA-T.

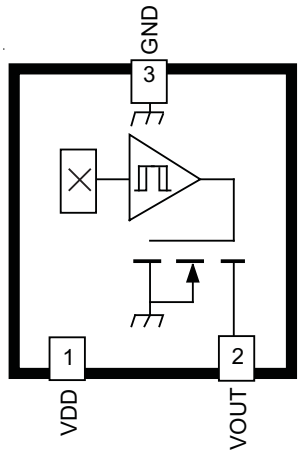
Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{DD}		6	V
Magnetic Flux Density	B		Unlimited	G
Output Off Voltage	V_{OUT}		6	V
Output Current	I_{OUT}		1	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
		Range L	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

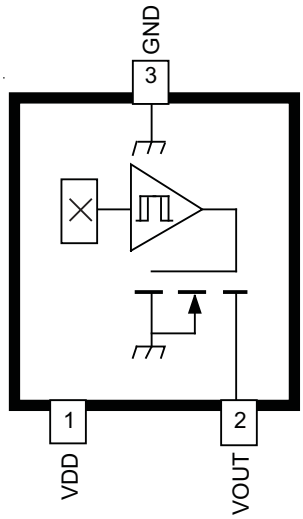
Pin-out Diagrams

Number		Name	Description
EL, LH	UA		
1	1	VDD	Input power supply; tie to GND with bypass capacitor
3	2	GND	Ground
2	3	VOUT	Output signal

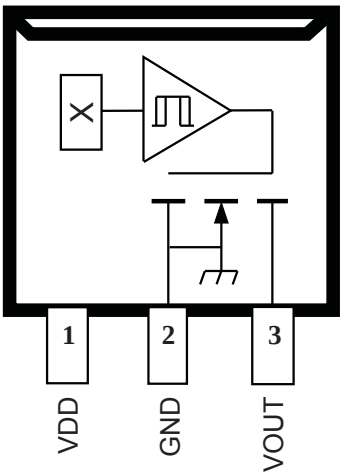
EL Package



LH Package



UA Package



ELECTRICAL CHARACTERISTICS valid over operating voltage and temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Units
Supply Voltage Range	V_{DD}	Operating[1)]	2.4	3.0	5.5	V
Output Leakage Current	I_{OFF}	V_{OUT} = 5.5 V, $B_{RPN} < B < B_{RPS}$	–	<1.0	1.0	µA
Output On Voltage	V_{OUT}	I_{OUT} = 1 mA, V_{DD} = 3.0 V	–	100	300	mV
Awake Time	t_{awake}		–	60	90	µs
Period	t_{period}	A3213	–	240	360	µs
		A3214, T_A = 25°C, V_{DD} = 3 V	–	60	90	ms
Duty Cycle	DC	A3213	–	25	–	%
		A3214	–	0.10	–	%
Chopping Frequency	f_C		–	340	–	kHz
Supply Current	$I_{DD(EN)}$	Chip awake (enabled)	–	–	2.0	mA
	$I_{DD(DIS)}$	Chip asleep (disabled)	–	–	8.0	µA
	$I_{DD(AVG)}$	A3213	–	460	850	µA
		A3214	–	11	22	µA

[1]Typical Data is at T_A = 25°C and V_{DD} = 3.0 V and is for design information only.
[2]Operate and release points will vary with supply voltage. B_{OPx} = operate point (output turns ON); B_{RPx} = release point (output turns OFF).

MAGNETIC CHARACTERISTICS valid over operating voltage and temperature range, unless otherwise noted[1]

Characteristic	Symbol[2]	Test Conditions	Min.	Typ.[3]	Max.	Units[4]
Operate Points	B_{OPS}	South pole to branded side	–	42	70	G
	B_{OPN}	North pole to branded side	–70	–48	–	G
Release Points	B_{RPS}	South pole to branded side	10	32	–	G
	B_{RPN}	North pole to branded side	–	–38	–10	G
Hysteresis	B_{hys}	$\lvert B_{OPx} - B_{RPx} \rvert$	–	10	–	G

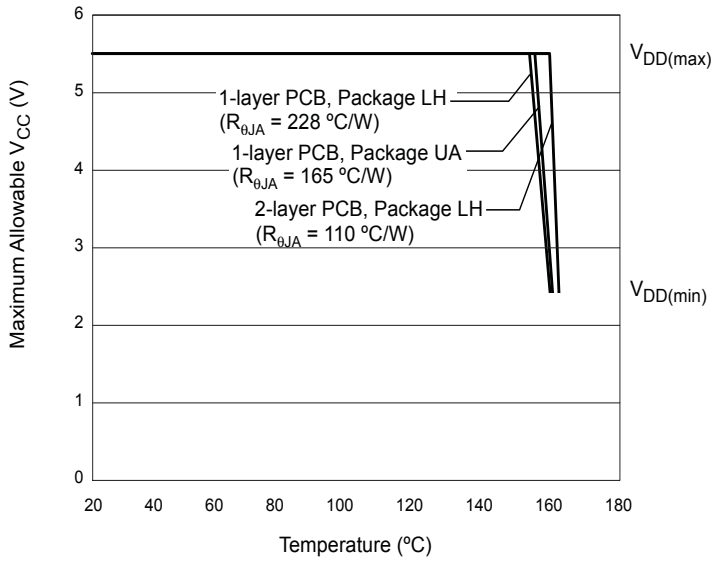
[1]As used here, negative flux densities are defined as less than zero (algebraic convention) and -50 G is less than +10 G.
[2]B_{OPx} = operate point (output turns ON); B_{RPx} = release point (output turns OFF).
[3]Typical Data is at T_A = 25°C and V_{DD} = 3.0 V and is for design information only.
[4]1 gauss (G) is exactly equal to 0.1 millitesla (mT).

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

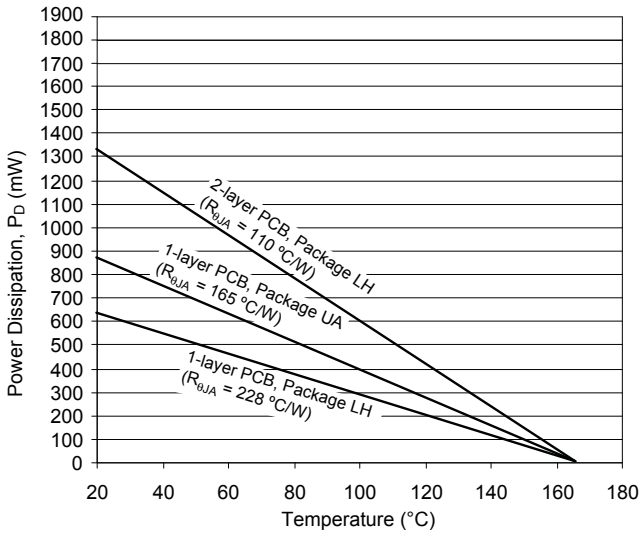
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	°C/W
		Package LH, 2-layer PCB with 0.463 in.² of copper area each side connected by thermal vias	110	°C/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	°C/W

*Additional thermal information available on Allegro website.

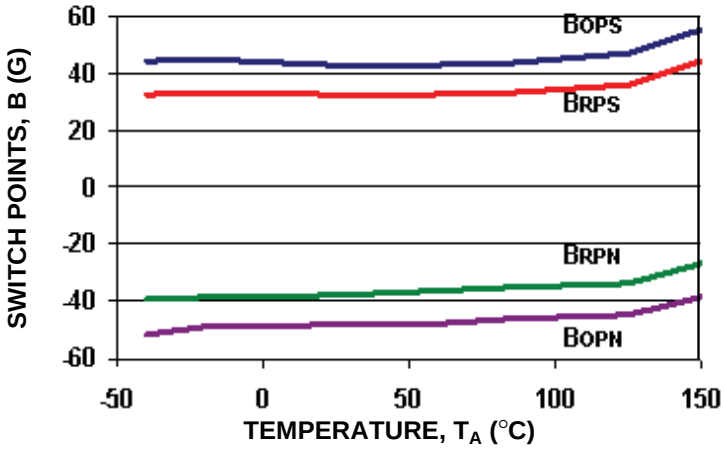
Power Derating Curve

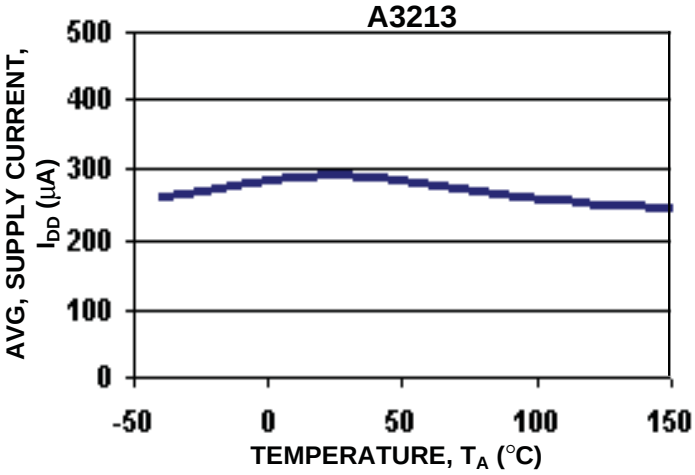


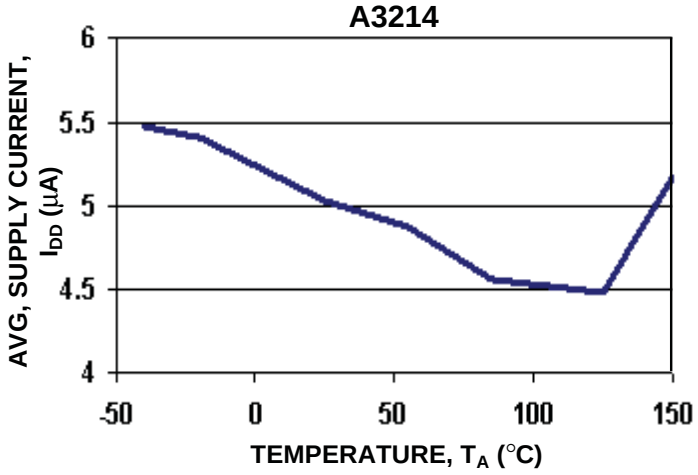
Power Dissipation versus Ambient Temperature

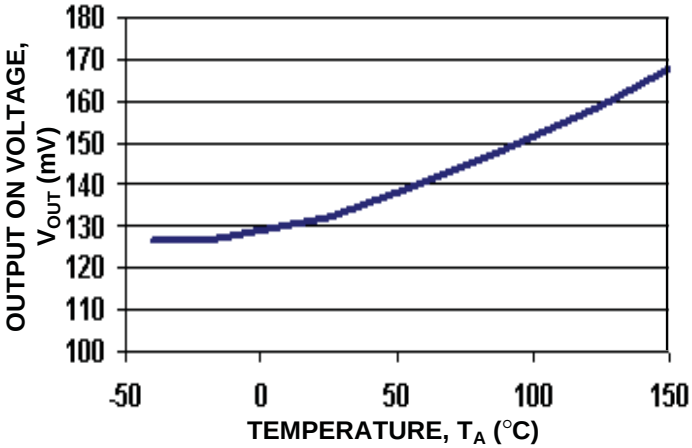


TYPICAL OPERATING CHARACTERISTICS
as a function of temperature (V_{DD} = 3 V)

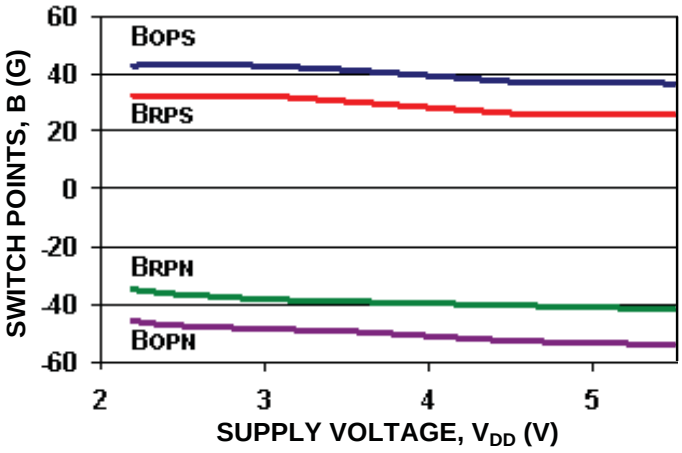




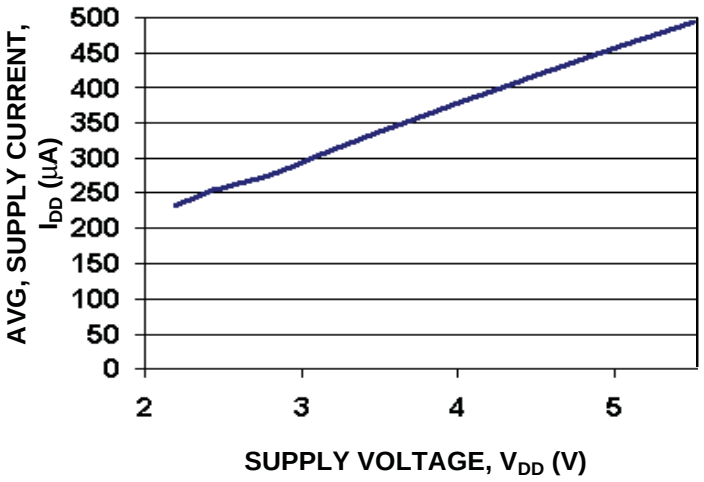




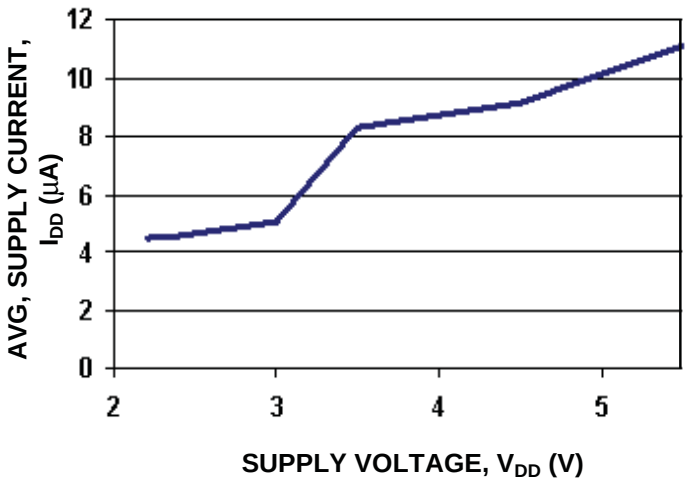
TYPICAL OPERATING CHARACTERISTICS
as a function of supply voltage (T_A = 25°C)



A3213

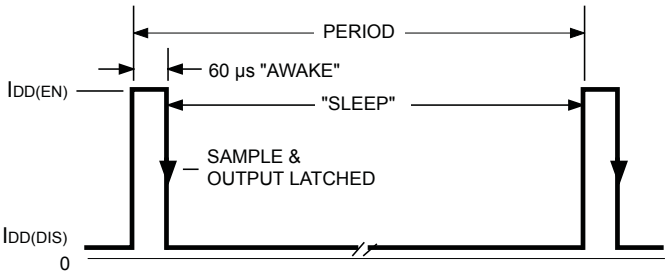


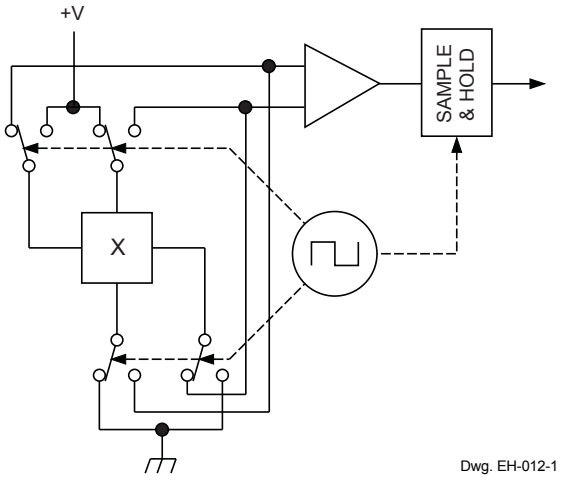
A3214



FUNCTIONAL DESCRIPTION

Low Average Power. Internal timing circuitry activates the IC for 60 µs and deactivates it for the remainder of the period (240 µs for the A3213 and 60 ms for the A3214). A short "awake" time allows for stabilization prior to the sampling and data latching on the falling edge of the timing pulse. The output during the "sleep" time is latched in the last sampled state. The supply current is not affected by the output state.

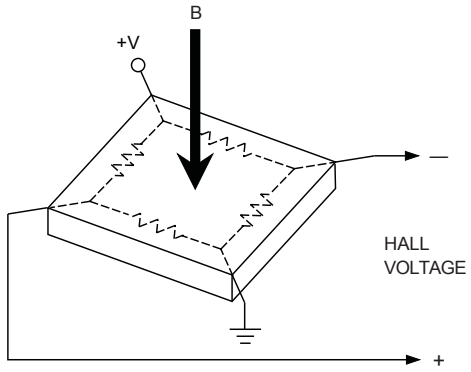




Dwg. EH-012-1

Chopper-Stabilized Technique. The Hall element can be considered as a resistor array similar to a Wheatstone bridge. A large portion of the offset is a result of the mismatching of these resistors. These devices use a proprietary dynamic offset cancellation technique, with an internal high-frequency clock to reduce the residual offset voltage of the Hall element that is normally caused by device overmolding, temperature dependencies, and thermal stress. The chopper-stabilizing technique cancels the mismatching of the resistor circuit by changing the direction of the current flowing through the Hall plate using CMOS switches and Hall voltage measurement taps, while maintaing the Hall-voltage signal that is induced by the external magnetic flux. The signal is then captured by a sample-and-hold circuit and further processed using low-offset bipolar circuitry. This technique produces devices that have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique will also slightly degrade the device output repeatability. A relatively high sampling frequency is used in order that faster signals can be processed.

More detailed descriptions of the circuit operation can be found in Technical Paper STP 97-10, *Monolithic Magnetic Hall Sensing Using Dynamic Quadrature Offset Cancellation* and Technical Paper STP 99-1, *Chopper-Stabilized Amplifiers With A Track-and-Hold Signal Demodulator*.



Dwg. AH-011-2

Operation. The output of this device switches low (turns on) when a magnetic field perpendicular to the Hall element exceeds the operate point B_{OPS} (or is less than B_{OPN}). After turn-on, the output is capable of sinking up to 1 mA and the output voltage is $V_{OUT(ON)}$. When the magnetic field is reduced below the release point B_{RPS} (or increased above B_{RPN}), the device output switches high (turns off). The difference in the magnetic operate and release points is the hysteresis (B_{hys}) of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

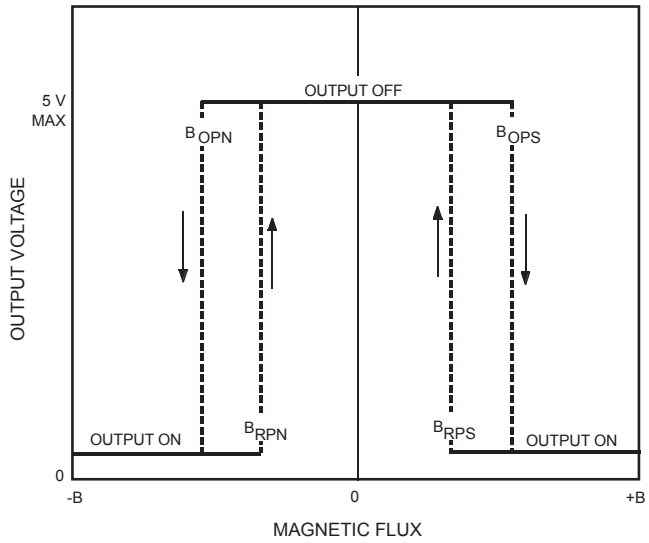
As used here, negative flux densities are defined as less than zero (algebraic convention) and -50 G is less than +10 G.

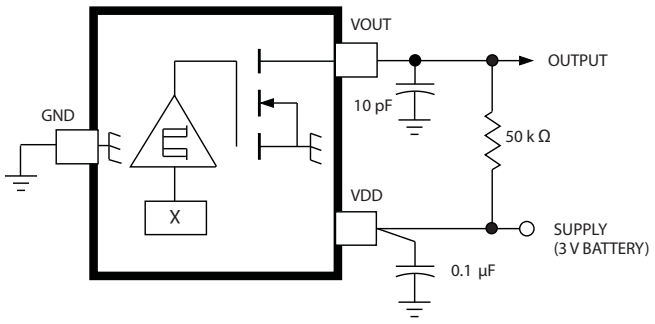
Applications. Allegro's pole-independent sensing technique allows for operation with either a north pole or south pole magnet orientation, enhancing the flexibility of the device in application assembling. The state-of-the-art technology provides the same output polarity for either pole face.

It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall element) between the supply and ground of the device to reduce both external noise and noise generated by the chopper-stabilization technique. This is especially true due to the relatively high impedance of battery supplies.

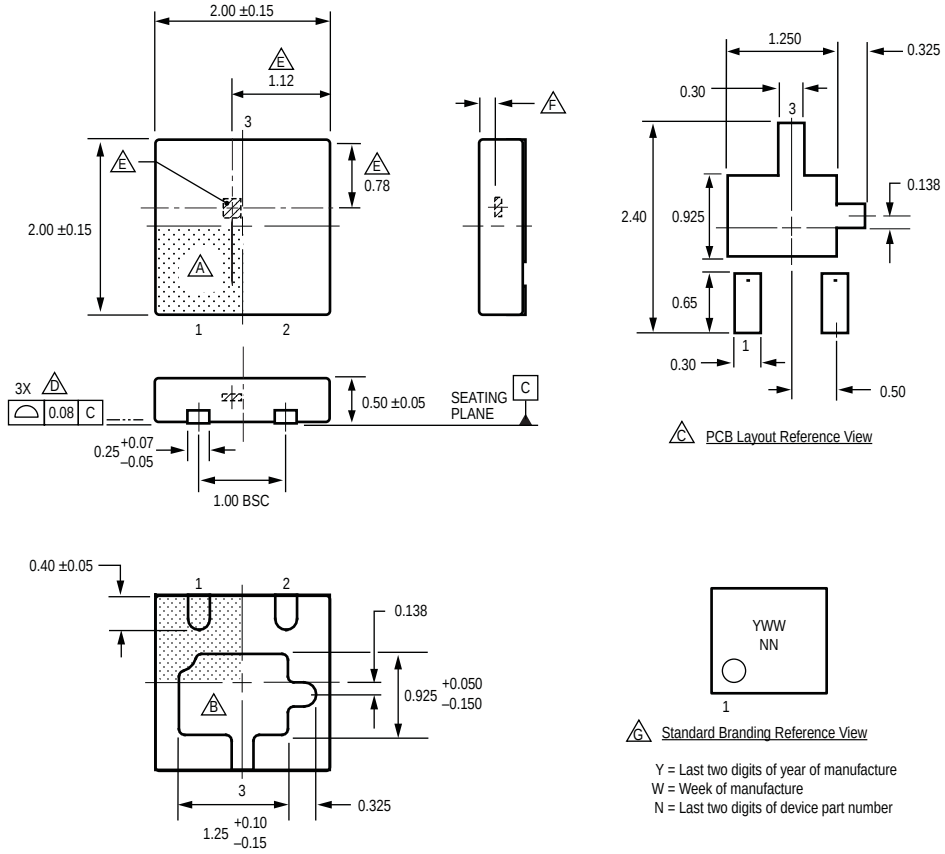
The simplest form of magnet that will operate these devices is a bar magnet with either pole near the branded surface of the device. Many other methods of operation are possible. Extensive applications information on magnets and Hall-effect devices is also available in the *Allegro Electronic Data Book* AMS-702 or *Application Note* 27701, or at

www.allegromicro.com





Package EL, 3-Contact MLP/DFN



For Reference Only, not for tooling use (reference DWG-2865; reference JEDEC MO-229UCCD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

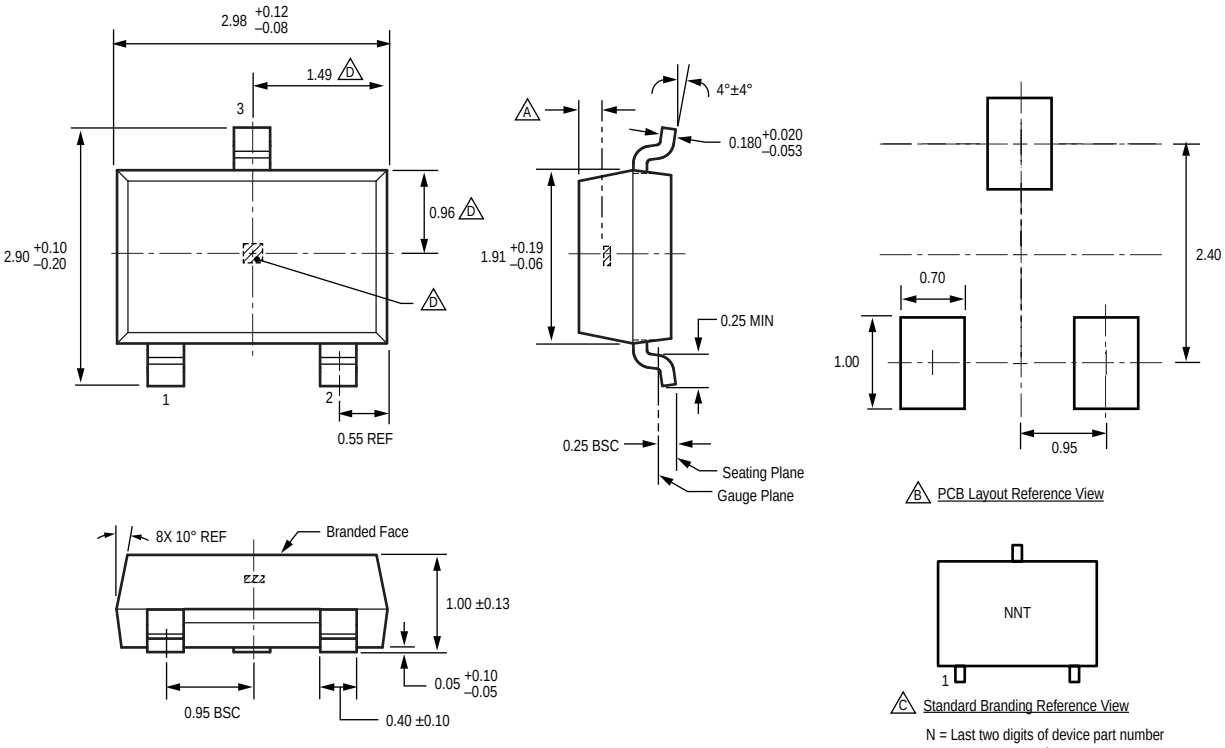
D Coplanarity includes exposed thermal pad and terminals

E Hall Element (not to scale)

F Active Area Depth, 0.18 mm NOM

G Branding scale and appearance at supplier discretion

Package LH, 3-Pin (SOT-23W)



N = Last two digits of device part number
T = Temperature code

For Reference Only; not for tooling use (reference dwg. 802840)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

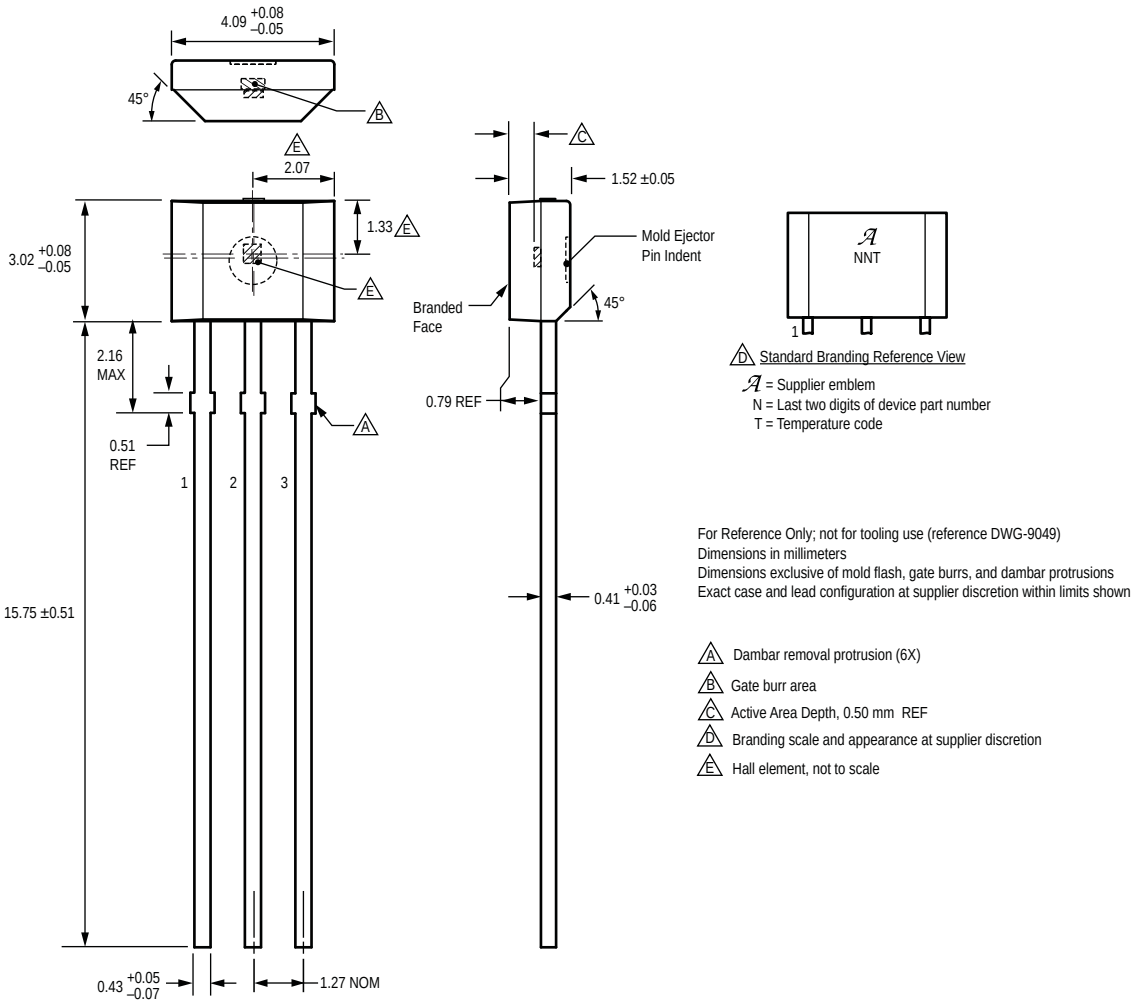
A Active Area Depth, 0.28 mm REF

B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

Package UA, 3-Pin SIP



For Reference Only; not for tooling use (reference DWG-9049)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Dambar removal protrusion (6X)
B Gate burr area
C Active Area Depth, 0.50 mm REF
D Branding scale and appearance at supplier discretion
E Hall element, not to scale

Revision History

Revision	Revision Date	Description of Revision
Rev. U	October 26, 2011	Update product availability

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www.allegromicro.com