1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC + 1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

† **NOTICE:** Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

DC CHARACTERISTICS			VCC = +2.5V to +5.5V Industrial (I): TA = -40°C to +85°C				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D1	VIH1	High-level input voltage	2.0	—	VCC +1	V	VCC ≥ 2.7V
	VIH2		0.7 VCC	—	VCC +1	V	VCC ≥ 2.7V
D2	VIL1	Low-level input voltage	-0.3	—	0.8	V	VCC ≥ 2.7V
	VIL2		-0.3	—	0.2 VCC	V	VCC ≥ 2.7V
D3	VOL1	Low-level output voltage	—	—	0.4	V	IOL = 2.1 mA, VCC = 4.5V
	VOL2		—	—	0.3	V	IOL = 100 µA, VCC = 2.5V
D4	VOH1	High-level output voltage	2.4	—	—	V	IOL = 400 µA, VCC = 4.5V
	VOH2		VCC -0.2	—	—	V	IOL = 100 µA, VCC = 2.5V
D5	ILI	Input leakage current	—	—	±10	µA	VIN = 0.1V to VCC
D6	ILO	Output leakage current	—	—	±10	µA	VOUT = 0.1V to VCC
D7	CIN, COUT	Pin capacitance (all inputs/outputs)	—	—	7	pF	VIN/VOUT = 0V **(Note 1 & 2)** TA = 25°C, FCLK = 1 MHz
D8	ICC write	Operating current	—	—	3	mA	FCLK = 2 MHz, VCC = 5.5V **(Note 2)**
D9	ICC read		—	—	1	mA	FCLK = 2 MHz, VCC = 5.5V
			—	—	500	µA	FCLK = 1 MHz, VCC = 3.0V
			—	100	—	µA	FCLK = 1 MHz, VCC = 2.5V
D10	ICCS	Standby current	—	—	100	µA	CLK = CS = 0V; VCC = 5.5V
			—	—	30	µA	CLK = CS = 0V; VCC = 3.0V
			—	3	—	µA	CLK = CS = 0V; VCC = 2.5V
							ORG, DI = VSS or VCC

Note 1: This parameter is tested at TA = 25°C and FCLK = 1 MHz.

2: This parameter is periodically sampled and not 100% tested.

AC CHARACTERISTICS

AC CHARACTERISTICS			VCC = +2.5V to +5.5V Industrial (I): TA = -40°C to +85°C				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
1	FCLK	Clock frequency	— —	— —	2 1	MHz MHz	VCC ≥ 4.5V VCC < 4.5V
2	TCKH	Clock high time	250	—	—	ns	
3	TCKL	Clock low time	250	—	—	ns	
4	TCSS	Chip select setup time	50	—	—	ns	Relative to CLK
5	TCSH	Chip select hold time	0	—	—	ns	Relative to CLK
6	TCSL	Chip select low time	250	—	—	ns	
7	TDIS	Data input setup time	100	—	—	ns	Relative to CLK
8	TDIH	Data input hold time	100	—	—	ns	Relative to CLK
9	TPD	Data output delay time	—	—	400	ns	CL = 100 pF
10	TCZ	Data output disable time	—	—	100	ns	CL = 100 pf **(Note 2)**
11	TSV	Status valid time	—	—	500	ns	CL = 100 pF
12	TWC	Program cycle time	—	4	10	ms	Erase/Write mode
13	TEC		—	8	15	ms	ERAL mode (VCC=5V ±10%)
14	TWL		—	16	30	ms	WRAL mode (VCC=5V ±10%)
15	—	Endurance	1M	—	1M	cycles	25°C, VCC = 5.0V, Block mode **(Note 3)**

Note 1: This parameter is tested at TA = 25°C and FCLK = 1 MHz.

2: This parameter is periodically sampled and not 100% tested.

3: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at: www.microchip.com.

FIGURE 1-1: SYNCHRONOUS DATA TIMING

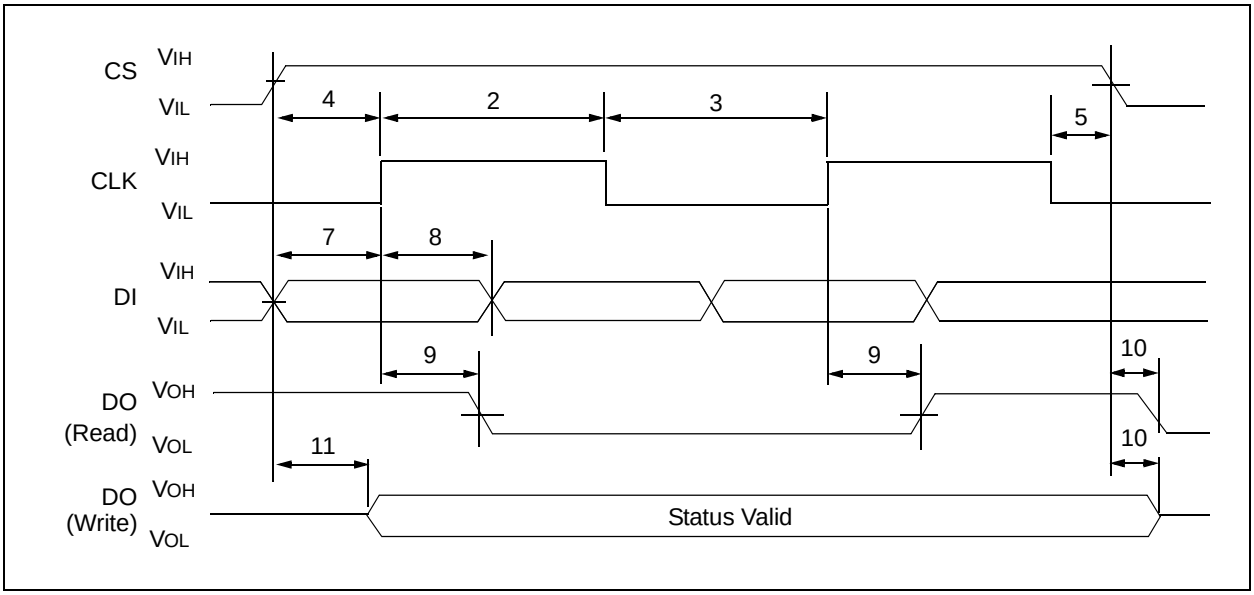


TABLE 1-1: INSTRUCTION SET FOR 93LC46: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A5 A4 A3 A2 A1 A0	—	D15 - D0	25
EWEN	1	00	1 1 XXXX	—	High-Z	9
ERASE	1	11	A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{\text{BSY}}$)	9
ERAL	1	00	1 0 XXXX	—	(RDY/$\overline{\text{BSY}}$)	9
WRITE	1	01	A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25
WRAL	1	00	0 1 XXXX	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25
EWDS	1	00	0 0 XXXX	—	High-Z	9

TABLE 1-2: INSTRUCTION SET FOR 93LC46: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	18
EWEN	1	00	1 1 X X X X X	—	High-Z	10
ERASE	1	11	A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{\text{BSY}}$)	10
ERAL	1	00	1 0 X X X X X	—	(RDY/$\overline{\text{BSY}}$)	10
WRITE	1	01	A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{\text{BSY}}$)	18
WRAL	1	00	0 1 X X X X X	D7 - D0	(RDY/$\overline{\text{BSY}}$)	18
EWDS	1	00	0 0 X X X X X	—	High-Z	10

TABLE 1-3: INSTRUCTION SET FOR 93LC56: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	X A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{\text{BSY}}$)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{\text{BSY}}$)	11
WRITE	1	01	X A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

TABLE 1-4: INSTRUCTION SET FOR 93LC56: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X X	—	High-Z	12
ERASE	1	11	X A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{\text{BSY}}$)	12
ERAL	1	00	1 0 X X X X X X X	—	(RDY/$\overline{\text{BSY}}$)	12
WRITE	1	01	X A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20
WRAL	1	00	0 1 X X X X X X X	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20
EWDS	1	00	0 0 X X X X X X X	—	High-Z	12

TABLE 1-5: INSTRUCTION SET FOR 93LC66: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{\text{BSY}}$)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{\text{BSY}}$)	11
WRITE	1	01	A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/BSY)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

TABLE 1-6: INSTRUCTION SET FOR 93LC66: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X X	—	High-Z	12
ERASE	1	11	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{\text{BSY}}$)	12
ERAL	1	00	1 0 X X X X X X X	—	(RDY/$\overline{\text{BSY}}$)	12
WRITE	1	01	A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20
WRAL	1	00	0 1 X X X X X X X	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20
EWDS	1	00	0 0 X X X X X X X	—	High-Z	12

2.0 FUNCTIONAL DESCRIPTION

When the ORG pin is connected to VCC, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the Ready/Busy status during a programming operation. The Ready/Busy status can be verified during an erase/write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CS.

2.1 Start Condition

The Start bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a Start condition is detected, CS, CLK and DI may change in any combination (except to that of a Start condition), without resulting in any device operation (Read, Write, Erase, EWEN, EWDS, ERAL and WRAL). As soon as CS is high, the device is no longer in the Standby mode.

An instruction following a Start condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become “don't care” bits until a new Start condition is detected.

2.2 Data In/Data Out (DI/DO)

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a “bus conflict” to occur during the “dummy zero” that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

2.3 Data Protection

During power-up, all programming modes of operation are inhibited until VCC has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when VCC has fallen below 1.4V at nominal conditions.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

2.4 Read

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16-bit (x16 organization) or 8-bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

2.5 Erase/Write Enable and Disable (EWEN, EWDS)

The 93LC46/56/66 power up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or VCC is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all erase/write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

2.6 Erase

The ERASE instruction forces all data bits of the specified address to the logical “1” state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the Ready/Busy status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical “0” indicates that programming is still in progress. DO at logical “1” indicates that the register at the specified address has been erased and the device is ready for another instruction.

The erase cycle takes 4 ms per word typical.

2.7 Write

The WRITE instruction is followed by 16 bits (or by 8 bits) of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

The write cycle takes 4 ms per word typical.

2.8 Erase All (ERAL)

The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is ensured at 5V ±10%.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete.

The ERAL cycle takes (8 ms typical).

2.9 Write All (WRAL)

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is ensured at 5V ±10%.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device if CS is brought high after a minimum of 250 ns low (Tcsl).

The WRAL cycle takes 16 ms typical.

FIGURE 2-1: READ TIMING

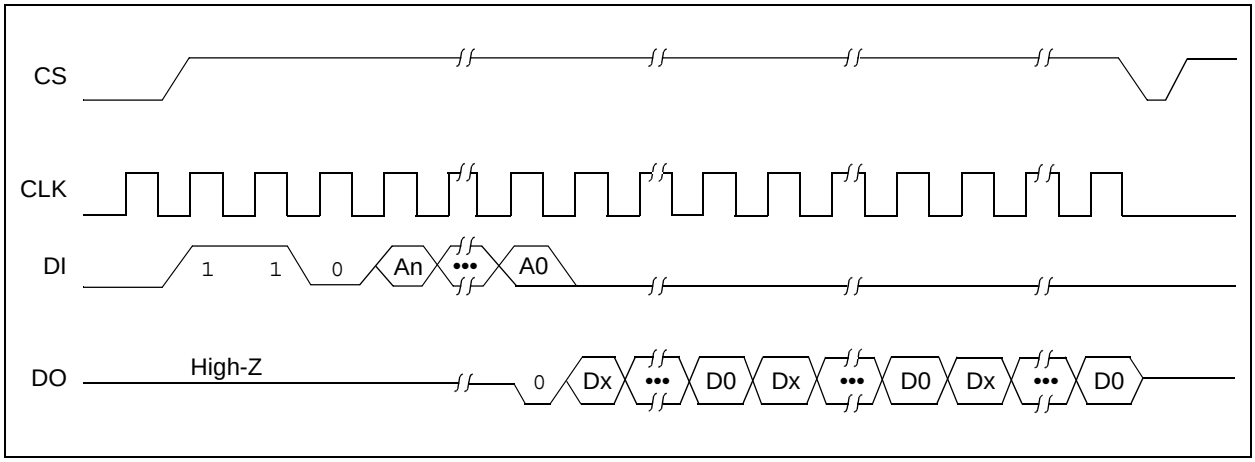


FIGURE 2-2: EWEN TIMING

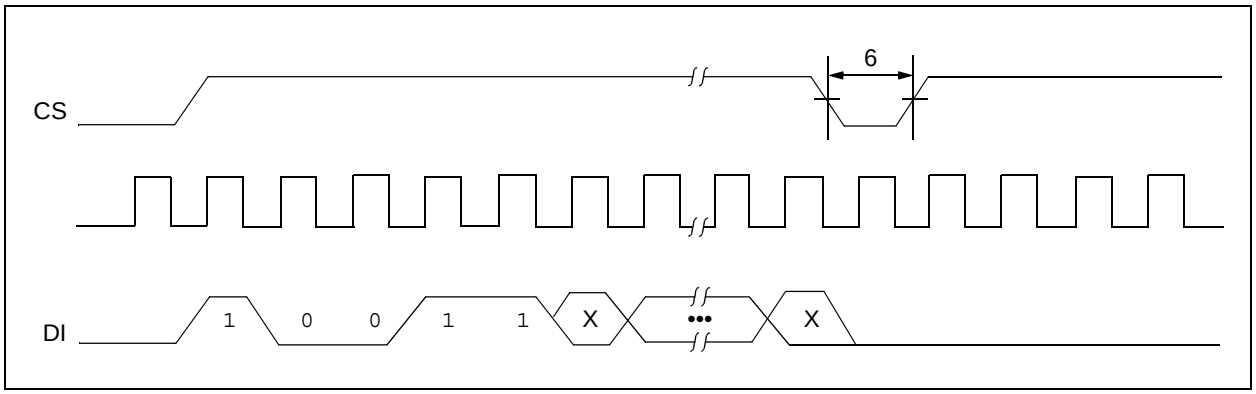


FIGURE 2-3: EWDS TIMING

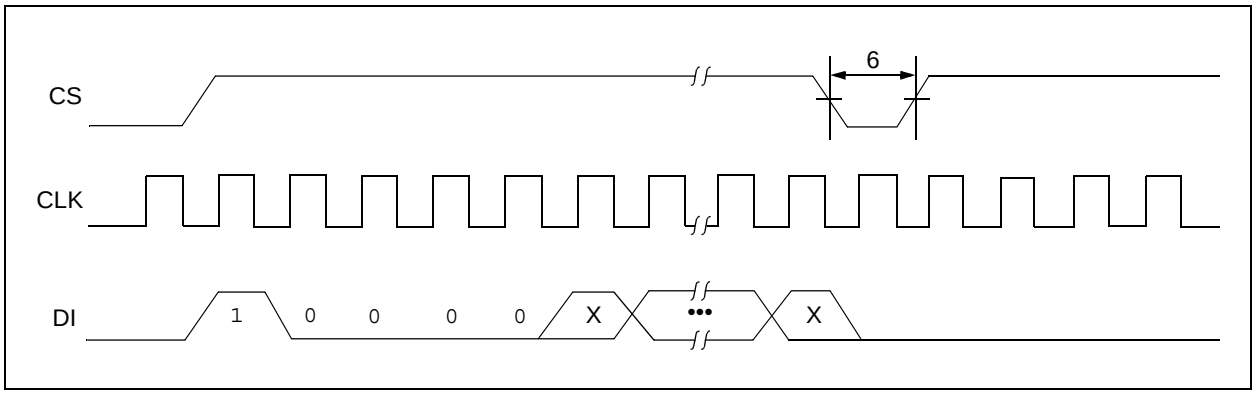


FIGURE 2-4: WRITE TIMING

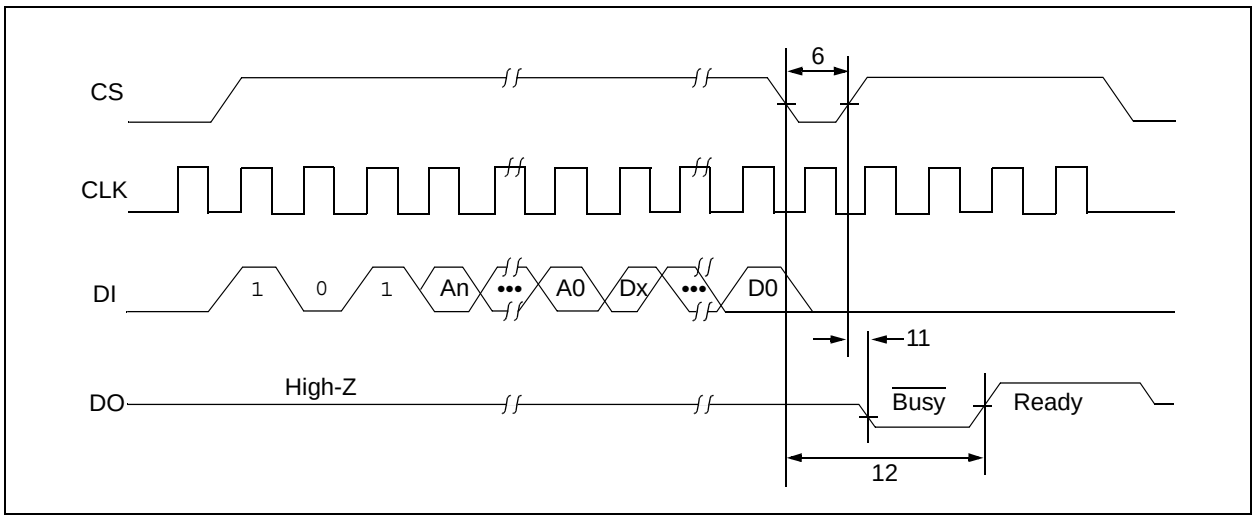


FIGURE 2-5: WRAL TIMING

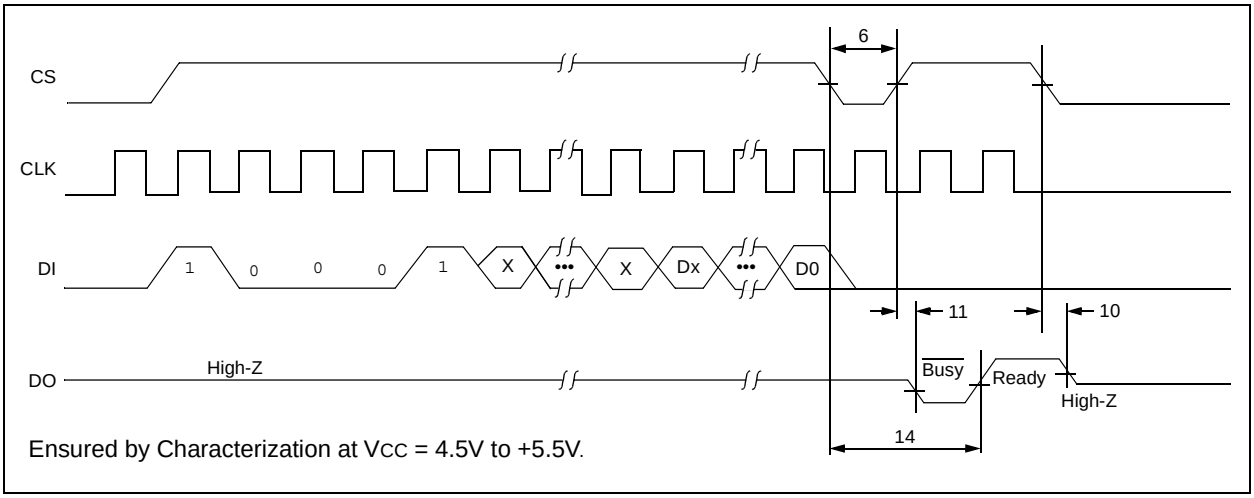


FIGURE 2-6: ERASE TIMING

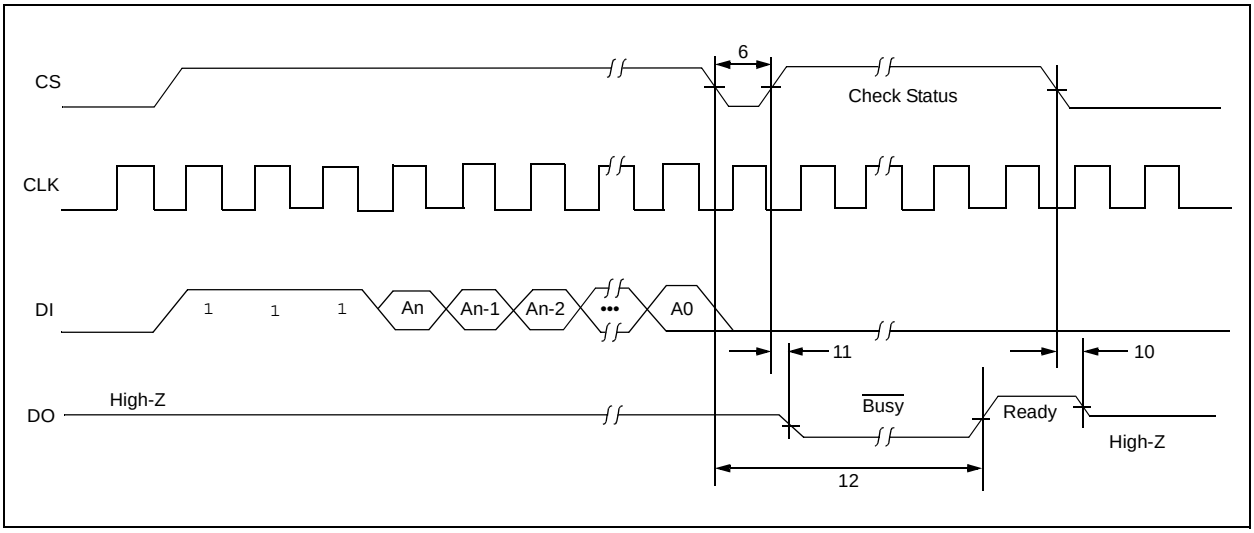
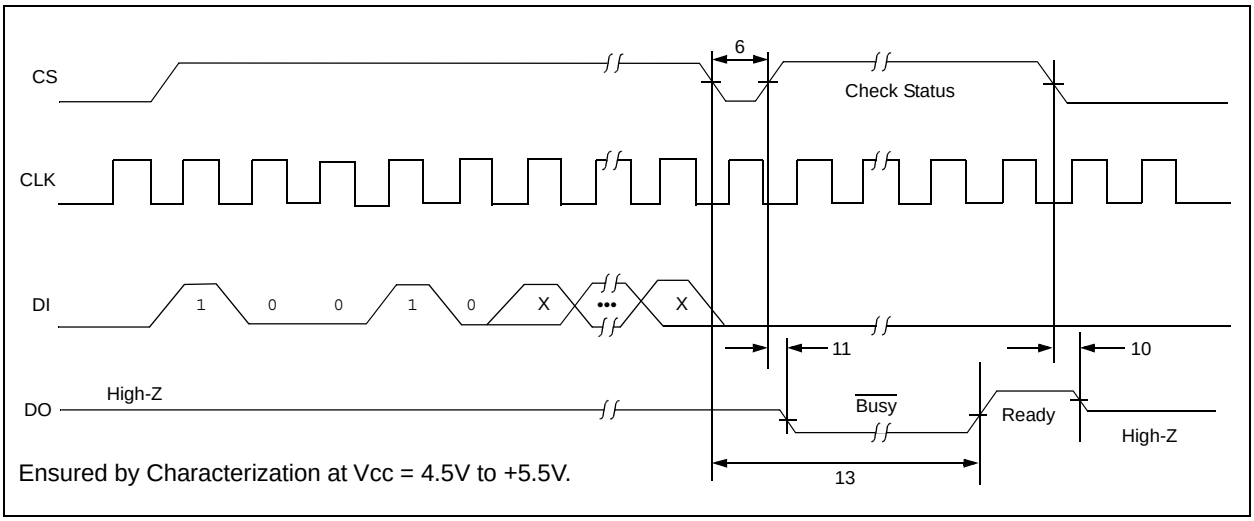


FIGURE 2-7: ERAL TIMING



3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Name	PDIP	SOIC	ROTATED TSSOP	Description
CS	1	1	3	Chip Select
CLK	2	2	4	Serial Data Clock
DI	3	3	5	Serial Data Input
DO	4	4	6	Serial Data Output
VSS	5	5	7	Ground
ORG	6	6	8	Memory Configuration
NU	7	7	1	Not Utilized
Vcc	8	8	2	+1.8V to 5.5V Power Supply

3.1 Chip Select (CS)

A high level selects the device. A low level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought low during a program cycle, the device will go into Standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (TCSL) between consecutive instructions. If CS is low, the internal control logic is held in a Reset status.

Note: CS must go low between consecutive instructions.

3.2 Serial Clock (CLK)

The serial clock is used to synchronize the communication between a master device and the 93LC46/56/66. Opcode, address and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (TCKH) and clock low time (TCKL). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a “don't care” if CS is low (device deselected). If CS is high, but Start condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for Start condition).

CLK cycles are not required during the self-timed write (i.e., auto erase/write) cycle.

After detection of a Start condition the specified number of clock cycles (respectively low-to-high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become “don't care” inputs waiting for a new Start condition to be detected.

3.3 Data In (DI)

Data In is used to clock in a Start bit, opcode, address and data synchronously with the CLK input.

3.4 Data Out (DO)

Data Out is used in the Read mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides Ready/$\overline{\text{Busy}}$ status information during erase and write cycles. Ready/$\overline{\text{Busy}}$ status information is available on the DO pin if CS is brought high after being low for minimum chip select low time (TCSL) and an erase or write operation has been initiated.

The Status signal is not available on DO, if CS is held low or high during the entire write or erase cycle. In all other cases DO is in the High-Z mode. If status is checked after the write/erase cycle, a pull-up resistor on DO is required to read the Ready signal.

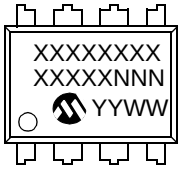
3.5 Organization (ORG)

When ORG is connected to VCC, the (x16) memory organization is selected. When ORG is tied to VSS, the (x8) memory organization is selected. ORG can only be floated for clock speeds of 1 MHz or less for the (x16) memory organization. For clock speeds greater than 1 MHz, ORG must be tied to VCC or VSS.

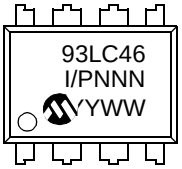
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

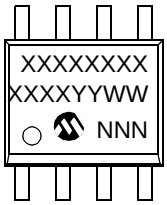
8-Lead PDIP (300 mil)



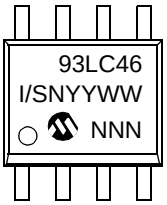
Example:



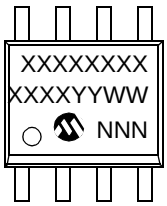
8-Lead SOIC (150 mil)



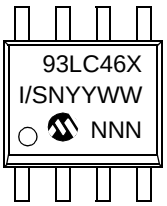
Example:



8-Lead Rotated SOIC (150 mil)



Example:

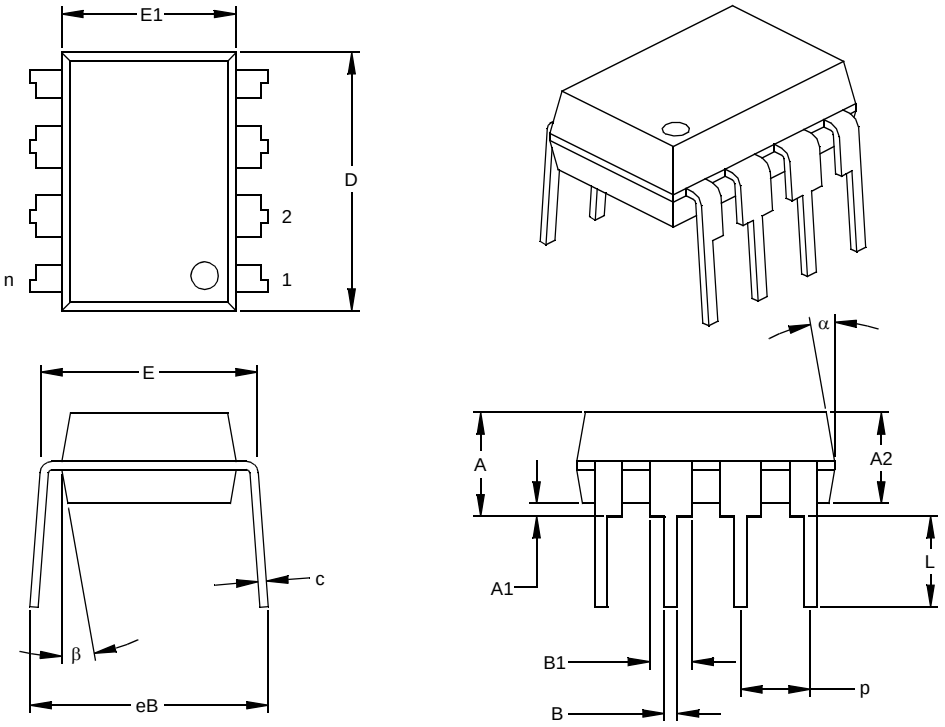


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



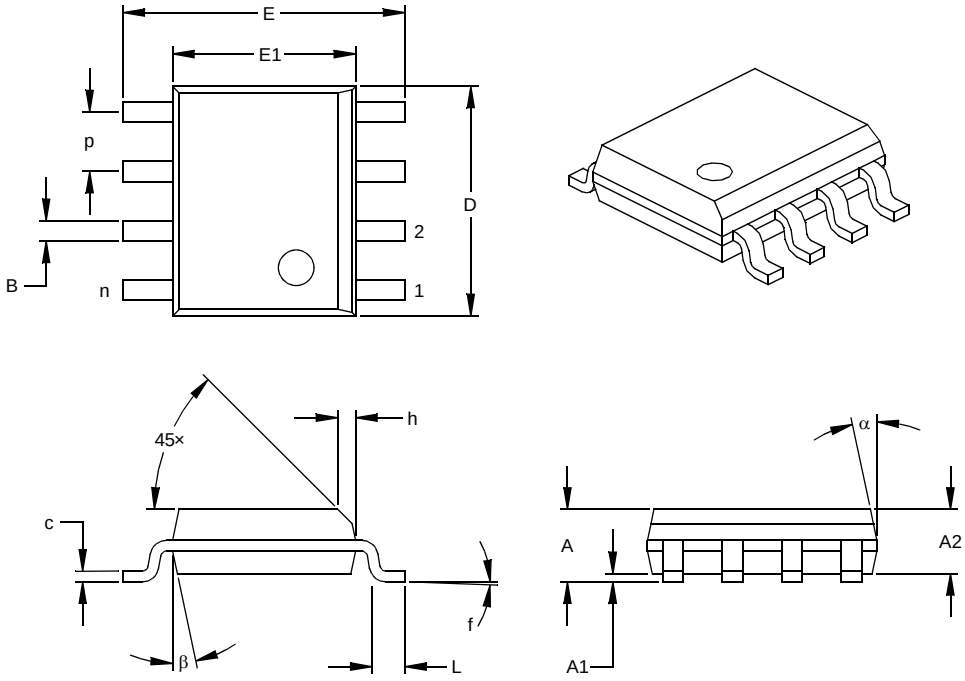
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

APPENDIX A: REVISION HISTORY

Revision B

Added note to page 1 header (Not recommended for new designs).

Updated document format.

Revision C

Added a note to each package outline drawing.

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PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	93LC46:	1K 2.5V Microwire Serial EEPROM
	93LC46X:	1K 2.5V Microwire Serial EEPROM in alternate pinouts (SN package only)
	93LC46T:	1K 2.5V Microwire Serial EEPROM (Tape and Reel)
	93LC46XT:	1K 2.5V Microwire Serial EEPROM (Tape and Reel)
	93LC56:	2K 2.5V Microwire Serial EEPROM
	93LC56X:	2K 2.5V Microwire Serial EEPROM in alternate pinouts (SN package only)
	93LC56T:	2K 2.5V Microwire Serial EEPROM (Tape and Reel)
	93LC56XT:	2K 2.5V Microwire Serial EEPROM (Tape and Reel)
	93LC66:	4K 2.5V Microwire Serial EEPROM
	93LC66X:	4K 2.5V Microwire Serial EEPROM in alternate pinouts (SN package only)
	93LC66T:	4K 2.5V Microwire Serial EEPROM (Tape and Reel)
	93LC66XT:	4K 2.5V Microwire Serial EEPROM (Tape and Reel)
Temperature Range	I	= -40°C to +85°C
Package	P	= Plastic DIP (300 mil body), 8-lead
	SN	= Plastic SOIC (150 mil body), 8-lead

Examples:

a) 93LC46-I/P: 1K, 128x8 or 64x16 Serial EEPROM, PDIP package

b) 93LC46-I/SN: 1K, 128x8 or 64x16 Serial EEPROM, SOIC package

c) 93LC46T-I/SN: 1K, 128x8 or 64x16 Serial EEPROM, SOIC package, tape and reel

d) 93LC46X-I/SN: 1K, 128x8 or 64x16 Serial EEPROM, Rotated SOIC package

e) 93LC56-I/P: 2K, 256x8 or 128x16 Serial EEPROM, PDIP package

f) 93LC56-I/SN: 2K, 256x8 or 128x16 Serial EEPROM, SOIC package

g) 93LC56T-I/SN: 2K, 256x8 or 128x16 Serial EEPROM, SOIC package, tape and reel

h) 93LC56X-I/SN: 2K, 256x8 or 128x16 Serial EEPROM, Rotated SOIC package

i) 93LC66-I/P: 4K, 512x8 or 256x16 Serial EEPROM, PDIP package

j) 93LC66-I/SN: 4K, 512x8 or 256x16 Serial EEPROM, SOIC package

k) 93LC66T-I/SN: 4K, 512x8 or 256x16 Serial EEPROM, SOIC package, tape and reel

l) 93LC66X-I/SN: 4K, 512x8 or 256x16 Serial EEPROM, Rotated SOIC package

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