**FAIRCHILD**

SEMICONDUCTOR ™

# 74LCXZ16245
# Low Voltage 16-Bit Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

## General Description

The LCXZ16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.7V or 3.3V) $V_{CC}$ applications with capability of interfacing to a 5V signal environment. The device is byte controlled. Each byte has separate control inputs which could be shorted together for full 16-bit operation. The T/$\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

When $V_{CC}$ is between 0V and 1.5V, the LCXZ16245 is on the high impedance state during power-up or power-down. This places the outputs in the high impedance (Z) state preventing intermittent low impedance loading or glitching in bus oriented applications.

The LCXZ16245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

## Features

■ 5V tolerant inputs and outputs

■ 2.7V–3.6V $V_{CC}$ specifications provided

■ 4.5 ns $t_{PD}$ max ($V_{CC}$ = 3.3V), 20 μA $I_{CC}$ max

■ Power-down high impedance inputs and outputs

■ Supports live insertion/withdrawal (Note 1)

■ ±24 mA output drive ($V_{CC}$ = 3.0V)

■ Implements patented noise/EMI reduction circuitry

■ Latch-up performance conforms to the requirements of JESD78

■ ESD performance:
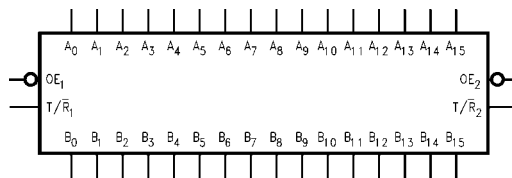   Human body model > 2000V
   Machine model > 200V

**Note 1:** To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to $V_{CC}$ through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| 74LCXZ16245MTD | MTD48 | 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

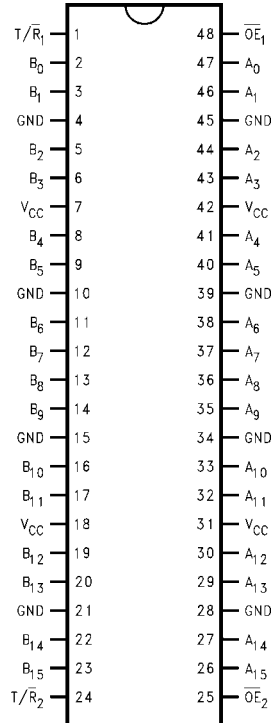Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Logic Symbol

www.fairchildsemi.com

**74LCXZ16245**

## Connection Diagram

**Pin Assignment for SSOP and TSSOP**

| Left | Pin | Pin | Right |
|---|---|---|---|
| $T/\overline{R}_1$ | 1 | 48 | $\overline{OE}_1$ |
| $B_0$ | 2 | 47 | $A_0$ |
| $B_1$ | 3 | 46 | $A_1$ |
| GND | 4 | 45 | GND |
| $B_2$ | 5 | 44 | $A_2$ |
| $B_3$ | 6 | 43 | $A_3$ |
| $V_{CC}$ | 7 | 42 | $V_{CC}$ |
| $B_4$ | 8 | 41 | $A_4$ |
| $B_5$ | 9 | 40 | $A_5$ |
| GND | 10 | 39 | GND |
| $B_6$ | 11 | 38 | $A_6$ |
| $B_7$ | 12 | 37 | $A_7$ |
| $B_8$ | 13 | 36 | $A_8$ |
| $B_9$ | 14 | 35 | $A_9$ |
| GND | 15 | 34 | GND |
| $B_{10}$ | 16 | 33 | $A_{10}$ |
| $B_{11}$ | 17 | 32 | $A_{11}$ |
| $V_{CC}$ | 18 | 31 | $V_{CC}$ |
| $B_{12}$ | 19 | 30 | $A_{12}$ |
| $B_{13}$ | 20 | 29 | $A_{13}$ |
| GND | 21 | 28 | GND |
| $B_{14}$ | 22 | 27 | $A_{14}$ |
| $B_{15}$ | 23 | 26 | $A_{15}$ |
| $T/\overline{R}_2$ | 24 | 25 | $\overline{OE}_2$ |

## Pin Descriptions

| Pin Names | Description |
|---|---|
| $\overline{OE}_n$ | Output Enable Input |
| $T/\overline{R}_n$ | Transmit/Receive Input |
| $A_0$–$A_{15}$ | Side A Inputs or 3-STATE Outputs |
| $B_0$–$B_{15}$ | Side B Inputs or 3-STATE Outputs |
| NC | No Connect |

## Truth Tables

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_1$ | $T/\overline{R}_1$ | |
| L | L | Bus $B_0$–$B_7$ Data to Bus $A_0$–$A_7$ |
| L | H | Bus $A_0$–$A_7$ Data to Bus $B_0$–$B_7$ |
| H | X | HIGH Z State on $A_0$–$A_7$, $B_0$–$B_7$ |

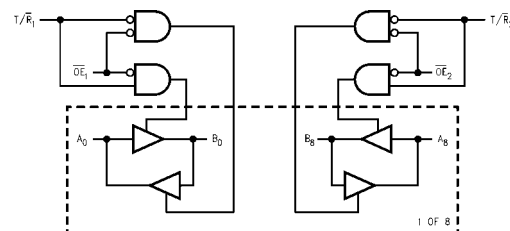| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_2$ | $T/\overline{R}_2$ | |
| L | L | Bus $B_8$–$B_{15}$ Data to Bus $A_8$–$A_{15}$ |
| L | H | Bus $A_8$–$A_{15}$ Data to Bus $B_8$–$B_{15}$ |
| H | X | HIGH Z State on $A_8$–$A_{15}$, $B_8$–$B_{15}$ |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

## Logic Diagram

## Absolute Maximum Ratings(Note 2)

| Symbol | Parameter | Value | Conditions | Units |
|--------|-----------|-------|------------|-------|
| $V_{CC}$ | Supply Voltage | −0.5 to +7.0 | | V |
| $V_I$ | DC Input Voltage | −0.5 to +7.0 | | V |
| $V_O$ | DC Output Voltage | −0.5 to +7.0 | Output in 3-STATE | V |
| | | −0.5 to $V_{CC}$ + 0.5 | Output in HIGH or LOW State (Note 3) | |
| $I_{IK}$ | DC Input Diode Current | −50 | $V_I$ < GND | mA |
| $I_{OK}$ | DC Output Diode Current | −50 | $V_O$ < GND | mA |
| | | +50 | $V_O$ > $V_{CC}$ | |
| $I_O$ | DC Output Source/Sink Current | ±50 | | mA |
| $I_{CC}$ | DC Supply Current per Supply Pin | ±100 | | mA |
| $I_{GND}$ | DC Ground Current per Ground Pin | ±100 | | mA |
| $T_{STG}$ | Storage Temperature | −65 to +150 | | °C |

## Recommended Operating Conditions (Note 4)

| Symbol | Parameter | | Min | Max | Units |
|--------|-----------|--|-----|-----|-------|
| $V_{CC}$ | Supply Voltage | Operating | 2.7 | 3.6 | V |
| $V_I$ | Input Voltage | | 0 | 5.5 | V |
| $V_O$ | Output Voltage | HIGH or LOW State | 0 | $V_{CC}$ | V |
| | | 3-STATE | 0 | 5.5 | |
| $I_{OH}/I_{OL}$ | Output Current | $V_{CC}$ = 3.0V – 3.6V | | ±24 | mA |
| | | $V_{CC}$ = 2.7V – 3.0V | | ±12 | |
| $T_A$ | Free-Air Operating Temperature | | −40 | 85 | °C |
| $\Delta t/\Delta V$ | Input Edge Rate, $V_{IN}$ = 0.8V–2.0V, $V_{CC}$ = 3.0V | | 0 | 10 | ns/V |

**Note 2:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 3:** $I_O$ Absolute Maximum Rating must be observed.

**Note 4:** Unused inputs or I/O's must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = −40°C to +85°C Min | Max | Units |
|--------|-----------|------------|--------------|------|-----|-------|
| $V_{IH}$ | HIGH Level Input Voltage | | 2.7 – 3.6 | 2.0 | | V |
| $V_{IL}$ | LOW Level Input Voltage | | 2.7 – 3.6 | | 0.8 | V |
| $V_{OH}$ | HIGH Level Output Voltage | $I_{OH}$ = −100 μA | 2.7 – 3.6 | $V_{CC}$ − 0.2 | | V |
| | | $I_{OH}$ = −12 mA | 2.7 | 2.2 | | |
| | | $I_{OH}$ = −18 mA | 3.0 | 2.4 | | |
| | | $I_{OH}$ = −24 mA | 3.0 | 2.2 | | |
| $V_{OL}$ | LOW Level Output Voltage | $I_{OL}$ = 100 μA | 2.7 – 3.6 | | 0.2 | V |
| | | $I_{OL}$ = 12 mA | 2.7 | | 0.4 | |
| | | $I_{OL}$ = 16 mA | 3.0 | | 0.4 | |
| | | $I_{OL}$ = 24 mA | 3.0 | | 0.55 | |
| $I_I$ | Input Leakage Current | 0 ≤ $V_I$ ≤ 5.5V | 2.7 – 3.6 | | ±5.0 | μA |
| $I_{OZ}$ | 3-STATE I/O Leakage | 0 ≤ $V_O$ ≤ 5.5V | 2.7 – 3.6 | | ±5.0 | μA |
| | | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | |
| $I_{OFF}$ | Power-Off Leakage Current | $V_I$ or $V_O$ = 5.5V | 0 | | 10 | μA |
| $I_{PU/PD}$ | Power-Up/Power-Down 3-STATE Output Current | $V_O$ = 0.5V to $V_{CC}$, $V_I$ = $V_{CC}$ or GND | 0 - 1.5 | | ±5.0 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_I$ = $V_{CC}$ or GND | 2.7–3.6 | | 225 | μA |
| | | 3.6V ≤ $V_I$, $V_O$ ≤ 5.5V (Note 5) | 2.7–3.6 | | ±225 | |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | $V_{IH}$ = $V_{CC}$ −0.6V | 2.7–3.6 | | 500 | μA |

**Note 5:** Outputs disabled or 3-STATE only.

## AC Electrical Characteristics

| Symbol | Parameter | $T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$ | | | | Units |
|---|---|---|---|---|---|---|
| | | $V_{CC} = 3.3V \pm 0.3V$ | | $V_{CC} = 2.7V$ | | |
| | | $C_L = 50$ pF | | $C_L = 50$ pF | | |
| | | Min | Max | Min | Max | |
| $t_{PHL}$ | Propagation Delay | 1.0 | 4.5 | 1.0 | 5.2 | ns |
| $t_{PLH}$ | $A_n$ to $B_n$ or $B_n$ to $A_n$ | 1.0 | 4.5 | 1.0 | 5.2 | |
| $t_{PZL}$ | Output Enable Time | 1.0 | 6.5 | 1.0 | 7.2 | ns |
| $t_{PZH}$ | | 1.0 | 6.5 | 1.0 | 7.2 | |
| $t_{PLZ}$ | Output Disable Time | 1.0 | 6.4 | 1.0 | 6.9 | ns |
| $t_{PHZ}$ | | 1.0 | 6.4 | 1.0 | 6.9 | |
| $t_{OSHL}$ | Output to Output Skew (Note 6) | | 1.0 | | | ns |
| $t_{OSLH}$ | | | 1.0 | | | |

**Note 6:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) or LOW-to-HIGH ($t_{OSLH}$). Parameter guaranteed by design.

## Dynamic Switching Characteristics

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A = 25°C$ Typical | Units |
|---|---|---|---|---|---|
| $V_{OLP}$ | Quiet Output Dynamic Peak $V_{OL}$ | $C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$ | 3.3 | 0.8 | V |
| $V_{OLV}$ | Quiet Output Dynamic Valley $V_{OL}$ | $C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$ | 3.3 | −0.8 | V |

## Capacitance

| Symbol | Parameter | Conditions | Typical | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = Open, $V_I = 0V$ or $V_{CC}$ | 7 | pF |
| $C_{I/O}$ | Input/Output Capacitance | $V_{CC} = 3.3V$, $V_I = 0V$ or $V_{CC}$ | 8 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | $V_{CC} = 3.3V$, $V_I = 0V$ or $V_{CC}$, f = 10 MHz | 20 | pF |

# AC LOADING and WAVEFORMS Generic for LCX Family



FIGURE 1. AC Test Circuit (C$_L$ includes probe and jig capacitance)

| Test | Switch |
|---|---|
| t$_{PLH}$, t$_{PHL}$ | Open |
| t$_{PZL}$, t$_{PLZ}$ | 6V at V$_{CC}$ = 3.3 ± 0.3V, and 2.7V |
| t$_{PZH}$, t$_{PHZ}$ | GND |



Waveform for Inverting and Non-Inverting Functions



3-STATE Output High Enable and Disable Times for Logic



Propagation Delay. Pulse Width and t$_{rec}$ Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic



t$_{rise}$ and t$_{fall}$

FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, t$_r$ = t$_f$ = 3ns)

| Symbol | V$_{CC}$ | |
|---|---|---|
| | 3.3V ± 0.3V | 2.7V |
| V$_{mi}$ | 1.5V | 1.5V |
| V$_{mo}$ | 1.5V | 1.5V |
| V$_x$ | V$_{OL}$ + 0.3V | V$_{OL}$ + 0.3V |
| V$_y$ | V$_{OH}$ − 0.3V | V$_{OH}$ − 0.3V |

**Schematic Diagram** Generic for LCX Family

input stage

Data

ESD

D2 N+/P−

N1

P1

P2

N2

P4

input stage

Enable

ESD

D4 N+/P−

N3

P3

N4

GTO™

$V_{CC}$

P5

X1

$V_{DD}$

Output

D6
N+/P−

N5
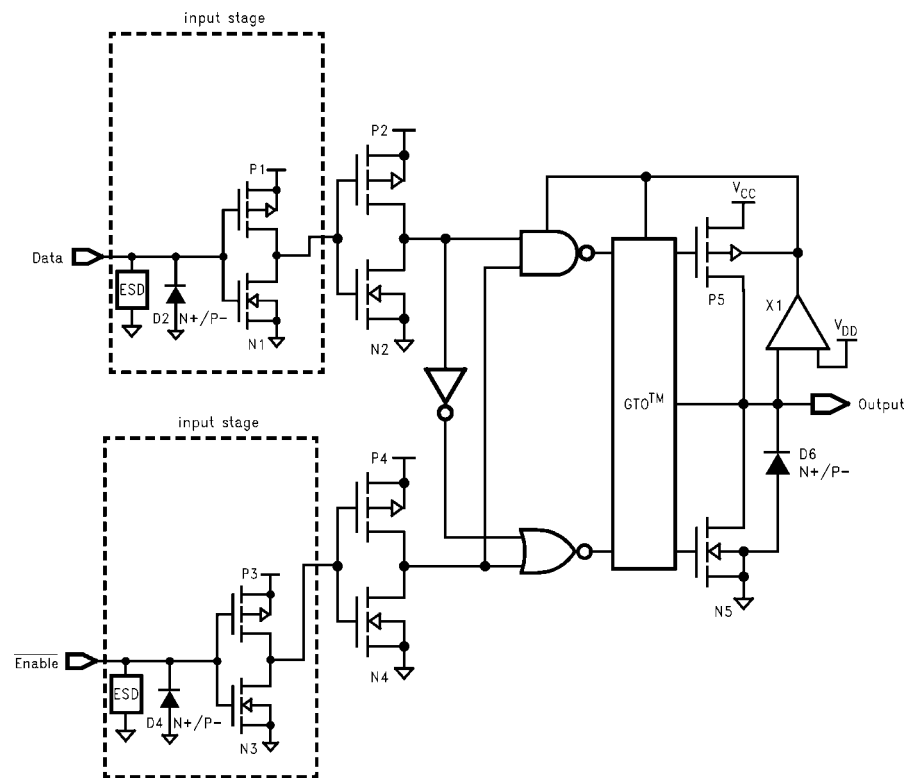
## Physical Dimensions inches (millimeters) unless otherwise noted
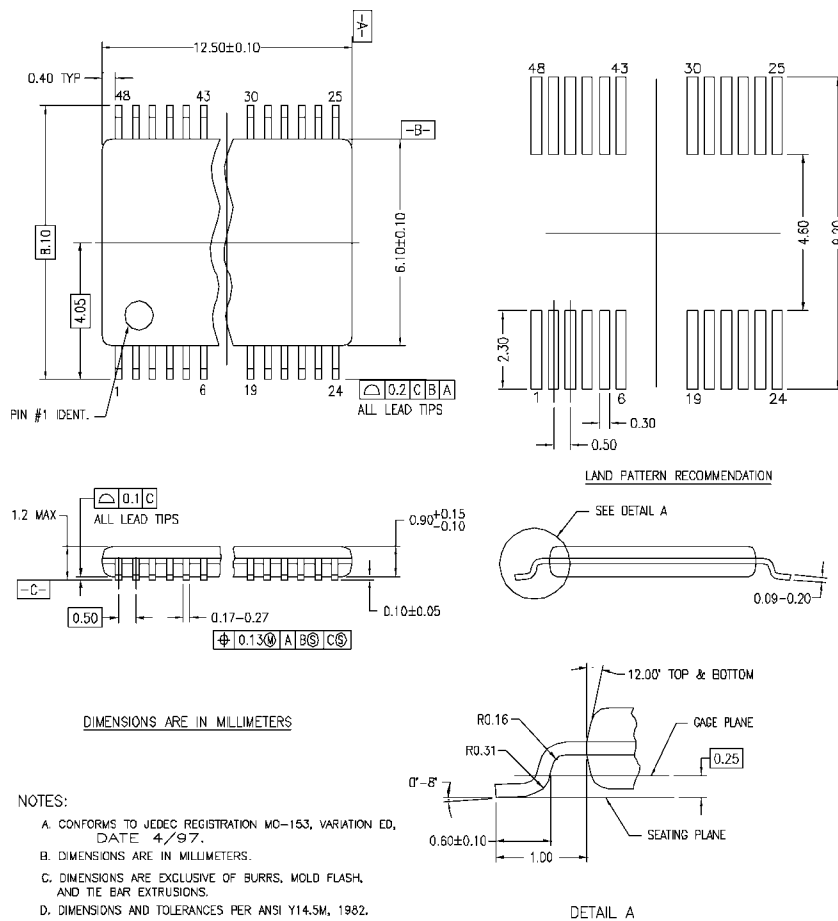


**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide**
**Package Number MTD48**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**www.fairchildsemi.com**

## PUBLICATION ORDERING INFORMATION

© Semiconductor Components Industries, LLC

www.onsemi.com