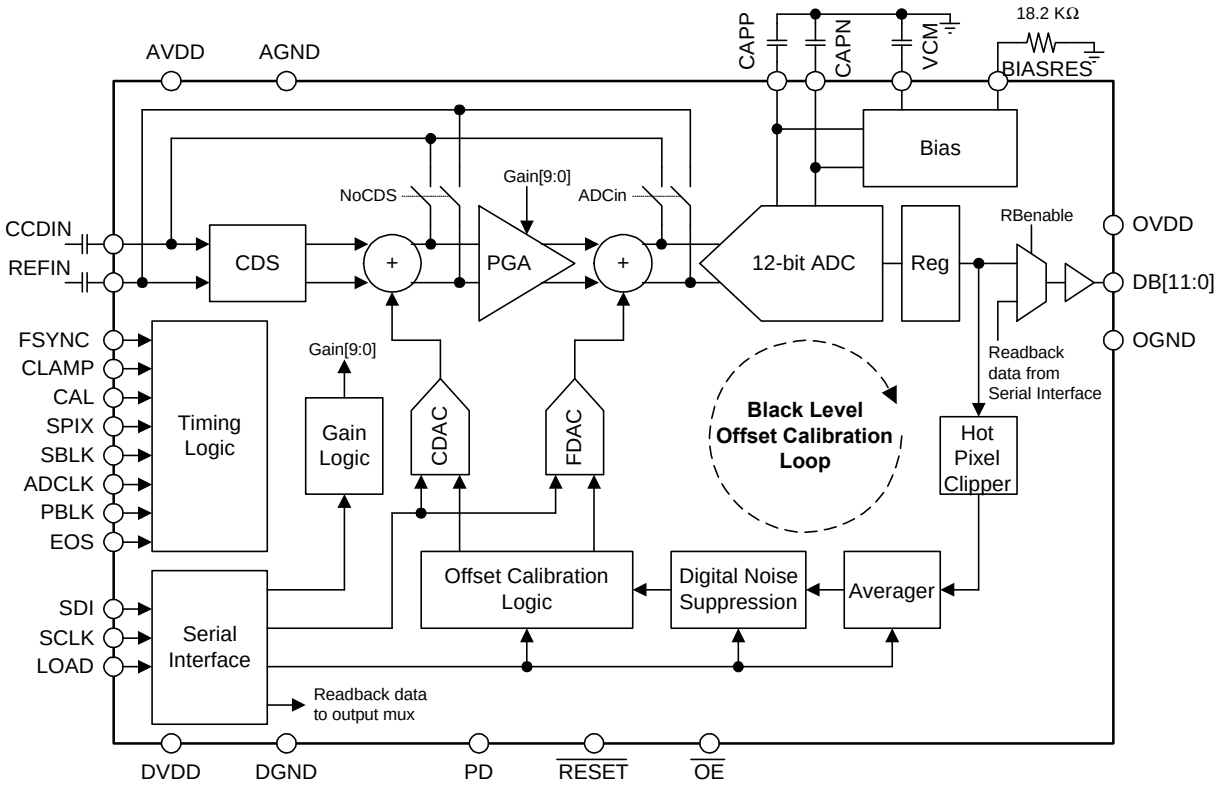


Figure 1. XRD98L63 Block Diagram

PIN CONFIGURATION

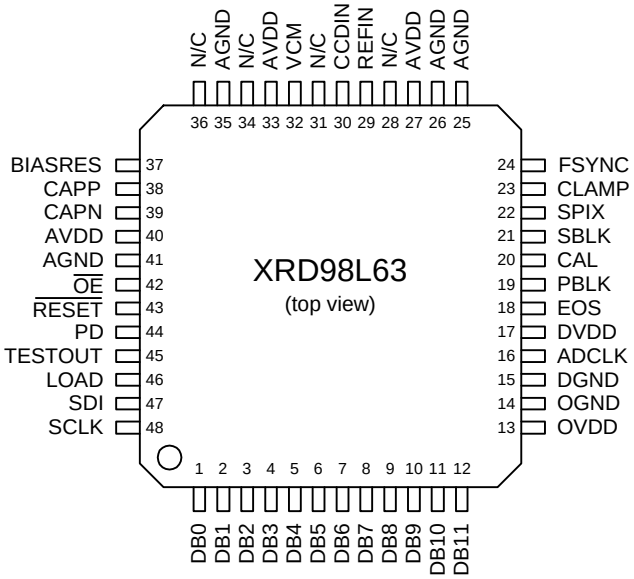


Figure 2. XRD98L63 Pinout

PIN DESCRIPTION

Pin #	Name	Type	Description
1	DB0	Digital out	ADC Output (LSB)
2	DB1	Digital out	ADC Output
3	DB2	Digital out	ADC Output
4	DB3	Digital out	ADC Output
5	DB4	Digital out	ADC Output
6	DB5	Digital out	ADC Output
7	DB6	Digital out	ADC Output
8	DB7	Digital out	ADC Output
9	DB8	Digital out	ADC Output
10	DB9	Digital out	ADC Output
11	DB10	Digital out	ADC Output
12	DB11	Digital out	ADC Output (MSB)
13	OVDD	Power	Digital Output Power Supply (must be $\leq$ AVDD)
14	OGND	Ground	Digital Output Ground
15	DGND	Ground	On chip Logic Ground
16	ADCLK	Digital in	ADC Clock
17	DVDD	Power	On chip Logic Power Supply (must = AVDD)
18	EOS	Digital in	Even/Odd Line select
19	PBLK	Digital in	Pre-Blanking clock
20	CAL	Digital in	Calibration Control Clock (clamp OB)
21	SBLK	Digital in	CDS Sample Black Clock
22	SPIX	Digital in	CDS Sample Pixel Clock
23	CLAMP	Digital in	DC-Restore Input Clamp Control Clock
24	FSYNC	Digital in	Frame Sync Clock
25	AGND	Ground	Analog Ground
26	AGND	Ground	Analog Ground
27	AVDD	Power	Analog Power Supply
28	N/C		(Not used)
29	REFIN	Analog	CCD Reference Signal
30	CCDIN	Analog	CCD Input Signal
31	N/C		(Not used)
32	VCM	Analog	Common mode bias by-pass
33	AVDD	Power	Analog Power Supply
34	N/C		(Not used)
35	AGND	Ground	Analog Ground
36	N/C		(not used)
37	BIASRES	Analog	External Reference Resistor (connect 18.2KΩ resistor to ground)
38	CAPP	Analog	ADC Reference By-Pass
39	CAPN	Analog	ADC Reference By-Pass
40	AVDD	Power	Analog Power Supply
41	AGND	Ground	Analog Ground
42	$\overline{OE}$	Digital in	Output Enable Control, 1=high-Z, 0=enable, internal pull down
43	$\overline{RESET}$	Digital in	Reset Control, 1=convert, 0=reset, internal pull up
44	PD	Digital in	Power Down Control, 1=Power Down, 0=convert, internal pull down
45	TESTOUT	Digital out	Factory Test Output
46	LOAD	Digital in	Serial Interface Data Load
47	SDI	Digital in	Serial Interface Data Input
48	SCLK	Digital in	Serial Interface Shift Clock

DC ELECTRICAL CHARACTERISTICS – XRD98L63

Unless otherwise specified: $0V_{DD}$ = DV_{DD} = AV_{DD} = 3.0V, Pixel Rate = 30MSPS, T_A = 25°C Rext = 18.2 KΩ

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CDS Performance						
$CDSV_{IN}$	Input Range		0.8	1.0	V_{PP}	Pixel (V_{BLK} - V_{VIDEO}), (See Figure 3).
V_{DARK}	Maximum Dark Voltage Offset			300	mV	At any gain. (See Figure 3).
Vrst	Reset Pulse			500	mV	
r_{CLAMP}	Clamp On Resistance	25	40	75	Ω	
PGA Parameters						
AV_{MIN}	Minimum Gain		6		dB	Gain Code = 0
AV_{MAX}	Maximum Gain		36		dB	Gain Code ≥ 640
PGA n	Resolution		10		bits	Transfer function is linear steps in dB
PGA Step	Gain Step Size		0.047		dB	
ADC Parameters (Measured in ADC Test Mode, ADCin=1)						
ADC n	Resolution	12			bits	
f_s	Max Sample Rate	30			MSPS	
DNL	Differential Non-Linearity		±0.5	±1.0	LSB	
V_{ID}	Full Scale Differential Input		±0.9			
ΔV_{REF}	ADC Reference Voltage		0.9		V	ΔV_{REF} = CapP - CapN

DC ELECTRICAL CHARACTERISTICS – XRD98L63 (cont'd)
Unless otherwise specified: OV_{DD} = DV_{DD} =AV_{DD} = 3.0V, Pixel Rate = 30MSPS, T_A = 25°C
Rext = 18.2 KΩ

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
System Specifications						
DNL_S	System DNL		±0.6	±1.0	LSB	No missing codes, monotonic
f_{smax}	Maximum Sample Rate	30			MSPS	
f_{smin}	Minimum Sample Rate		500		KSPS	Not tested
$e_{n\ MAXAV}$	Input ref. Noise, max.Gain		180		μV_{rms}	Gain Code = 640 (36db)
$e_{n\ MINAV}$	Input ref. Noise, min.Gain		400		μV_{rms}	Gain Code = 0 (6dB)
Latency	Pipeline Delay			7.5	cycles	
Digital Inputs (Digital Input Thresholds are Set by DV_{DD})						
V_{IH}	Digital Input High Voltage	V_{DD}-0.5			V	
V_{IL}	Digital Input Low Voltage			GND+0.5	V	
I_L	DC Leakage Current		0.05	±1.0	µA	V_{IN} between GND and V_{DD}.
I_L	Input Leakage, PD and $\overline{OE}$	-5		100	µA	PD and $\overline{OE}$ have internal pull-down resisters
I_L	Input Leakage, $\overline{RESET}$	-100		5	µA	$\overline{RESET}$ has an internal pull-up resister
I_L	Input Leakage, All Other Digital Inputs	-100		100	nA	Input = V_{DD} or GND
C_{IN}	Input Capacitance		5		pF	
Digital Outputs						
V_{OH}	Digital Output High Voltage	OV_{DD}-0.5			V	While sourcing 2mA
V_{OL}	Digital Output Low Voltage			0.5	V	While sinking 2mA
I_{OZ}	High–Z Leakage		0.05	±1.0	µA	$\overline{OE}$ = 1 or PD = 1 or OE bit = 0

DC ELECTRICAL CHARACTERISTICS – XRD98L63 (cont'd)
Unless otherwise specified: OV_{DD} = DV_{DD} =AV_{DD} = 3.0V, Pixel Rate = 30MSPS, T_A = 25°C
Rext = 18.2 KΩ

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Digital I/O Timing						
t_{DL}	Data Valid Delay		20	27	ns	10 pF load, Note1
t_{PW1}	Pulse Width of SPIX	10			ns	
t_{PW2}	Pulse Width of SBLK	10			ns	
t_{PIX}	Pixel Period	33			ns	
t_{BK}	Sample Black (SBLK), Aperture Delay		5	7	ns	SBdly[5:0] = 0, Note 1
t_{VD}	Sample Video (SPIX), Aperture Delay		6	8	ns	SPdly[8:0] = 0, Note 1
t_{SCLK}	Shift Clock Period	100			ns	
t_{SET}	Shift Register Setup Time	10			ns	
t_{HOLD}	Shift Register Hold Time			0	ns	
t_{L1}	Load Set-up Time	10			ns	
t_{L2}	Load Hold Time			0	ns	
Power Supplies						
AV_{DD}	Analog Supply Voltage	2.7	3.0	3.6	V	
DV_{DD}	Digital Supply Voltage	2.7	3.0	3.6	V	Set DV_{DD} = AV_{DD}
OV_{DD}	Digital Output Supply Voltage	2.7	3.0	3.6	V	$OV_{DD} \leq AV_{DD}$
I_{DD}	Supply Current		40	45	mA	OV_{DD} = AV_{DD} = DV_{DD} = 3.0V
I_{DDPD}	Power Down Supply Current		0.02	0.1	mA	PD = 1 or CHIPpd register bit = 1

Note 1. *Guaranteed by design, not tested*

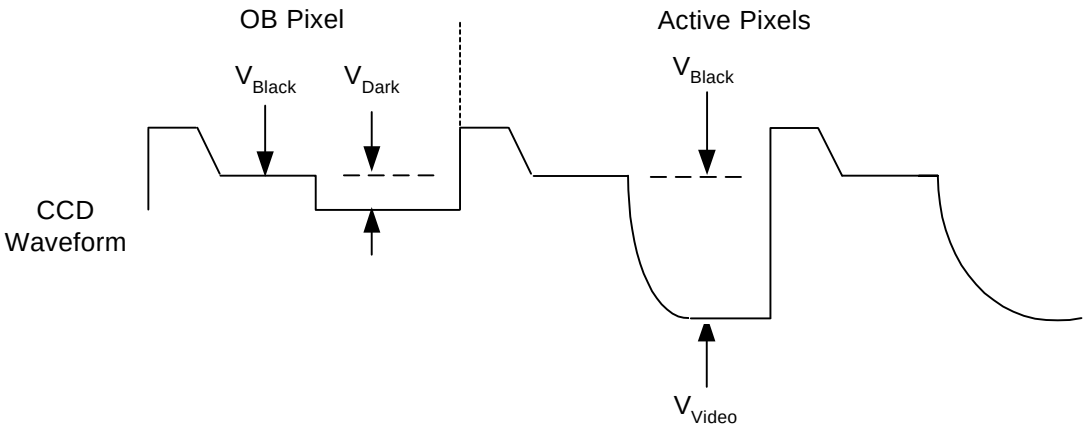


Figure 3. Definition of terms for V_{Out} of the CCD waveform: $CDSV_{IN} = (V_{Black} - V_{Video})$

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND	+6.6V
V_{RT} & V_{RB}	V_{DD} +0.5 to GND -0.5V
V_{IN}	V_{DD} +0.5 to GND -0.5V
All Inputs	V_{DD} +0.5 to GND -0.5V
All Outputs	V_{DD} +0.5 to GND -0.5V
Storage Temperature	-65°C to 150°C
Lead Temperature (Soldering 10 seconds)	300°C
Maximum Junction Temperature	150°C
Package Power Dissipation Ratings (T_A= +70°C)	
TQFP	θ_{JA} = 105°C/W
ESD	2000V

Notes:

1 *Stresses above those listed as "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*

2 *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.*

3 *V_{DD} refers to AV_{DD}, OV_{DD} and DV_{DD}. GND refers to AGND, OGND and DGND.*

SERIAL INTERFACE

The XRD98L63 uses a three wire serial interface (LOAD, SDI & SCLK) to access the programmable features and controls of the chip. The serial interface uses a 16-bit shift register. The first 6 bits shifted in are the address bits, the next 10 bits are the data bits. The address bits select which of the internal registers will receive the 10 data bits.

The interface will only load data from the shift register into the register array if there are exactly 16 rising edges of SCLK while LOAD is low. If more or less rising edges are present, the data is discarded. There is no checking of the address bits to ensure a valid register is written to. If the address bits select an undefined register, the data will be discarded. There is a readback function (see the Serial Interface Read Back section) that outputs the contents of a selected register on pins DB[11:2] of the digital output bus.

The following is the procedure for writing to the serial interface:

1) Force LOAD pin low to enable shift register.
2) Shift in 16 bits, 6 address bits (msb first), followed by 10 data bits (msb first).
3) Force LOAD pin high to transfer data from the shift register to the serial interface register array.

Note: *There must be exactly 16 rising edges of SCLK while LOAD is low.*

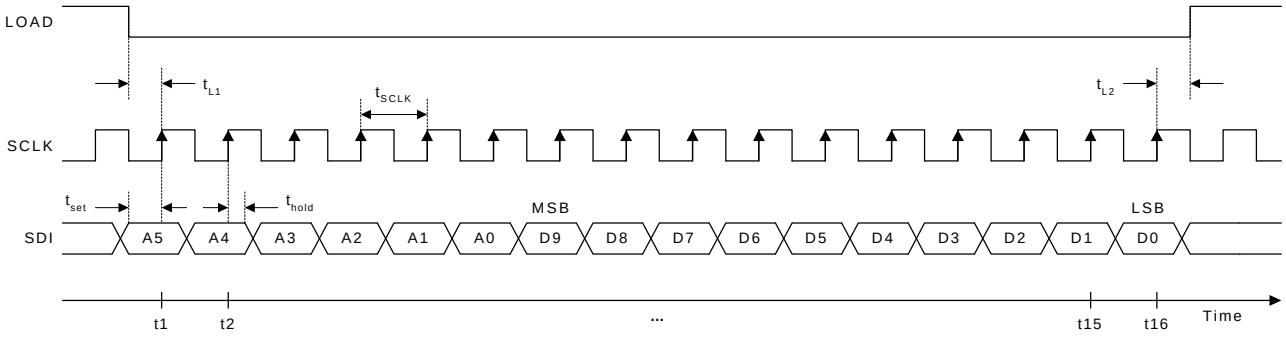


Figure 4. Serial Interface Timing Diagram

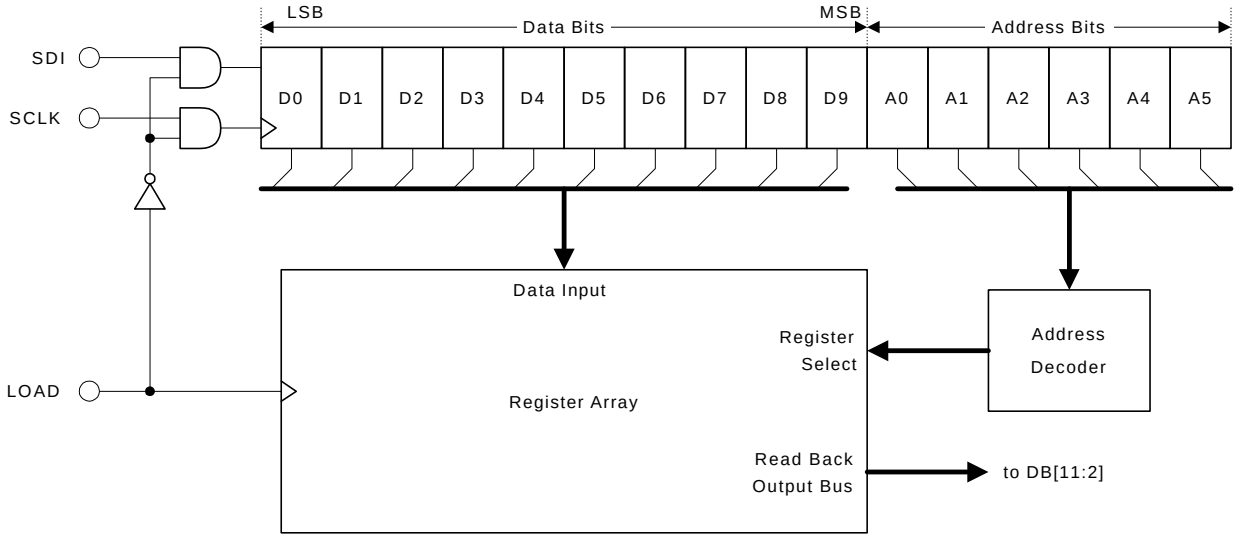


Figure 5. Serial Interface Block Diagram

	Address bits						Data bits									
Reg. Name	A5	A4	A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PGA00	0	0	0	0	0	0	PGA00[9] 0	0	0	0	0	0	0	0	0	PGA00[0] 0
Offset	0	0	0	0	0	1			OB[7] 1	0	0	0	0	0	0	OB[0] 0
PGA01	0	0	0	0	1	0		PGA01[8] 0	0	0	0	0	0	0	0	PGA01[0] 0
PGA10	0	0	0	0	1	1		PGA10[8] 0	0	0	0	0	0	0	0	PGA10[0] 0
PGA11	0	0	0	1	0	0		PGA11[8] 0	0	0	0	0	0	0	0	PGA11[0] 0
OB Even Gain	0	0	0	1	0	1		OBE[8] 0	0	0	0	0	0	0	0	OBE[0] 0
OB Odd Gain	0	0	0	1	1	0		OBO[8] 0	0	0	0	0	0	0	0	OBO[0] 0
Even Line	0	0	0	1	1	1	PRE[1] 0	PRE[0] 1	ELP4[1] 0	ELP4[0] 0	ELP3[1] 0	ELP3[0] 0	ELP2[1] 1	ELP2[0] 1	ELP1[1] 1	ELP1[0] 0
Odd Line	0	0	1	0	0	0	PRO[1] 0	PRO[0] 1	OLP4[1] 0	OLP4[0] 0	OLP3[1] 0	OLP3[0] 0	OLP2[1] 0	OLP2[0] 0	OLP1[1] 0	OLP1[0] 1
Calibration	0	0	1	0	0	1		OBdel[1] 0	OBdel[0] 0	Avg[1] 1	Avg[0] 0	DNS[1] 0	DNS[0] 1	Mode 0	Hold 0	ManCal 0
Wait A	0	0	1	0	1	0	WL[11] 0	0	0	0	0	0	0	0	0	WL[2] 0
Wait B	0	0	1	0	1	1									WL[1] 0	WL[0] 1
OB Lines	0	0	1	1	0	0			OBL[7] 0	0	0	0	0	0	1	OBL[0] 0
CDAC Even	0	0	1	1	0	1		CDE[8] 0	0	0	0	0	0	0	0	CDE[0] 0
CDAC Odd	0	0	1	1	1	0		CDO[8] 0	0	0	0	0	0	0	0	CDO[0] 0
FDAC Even	0	0	1	1	1	1	FDE[9]	0	0	0	0	0	0	0	0	FDE[0] 0
FDAC Odd	0	1	0	0	0	0	FDO[9]	0	0	0	0	0	0	0	0	FDO[0] 0
Control	0	1	0	0	0	1	ADCpd 0	AFEpd 0	CHIPpd 0	OE 1	MultGain 0	MGsel[1] 0	MGsel[0] 0	MGstart 0	MinClip 1	OneV 0
Test	0	1	0	0	1	0		nofs2 0	*Reserved 0	*Reserved 0	*Reserved 1	*Reserved 0	ADCin 0	NoCDS 0	*Reserved 0	*Reserved 0
Polarity	0	1	0	0	1	1			PBLKpol 0	EOSpol 1	SBLKpol 0	SPIXpol 0	CALpol 0	CLAMPpol 0	FSYNCpol 0	ADCpol 0
Clock	0	1	0	1	0	0					ADCLKsel 0	CLAMPopt 0	CALonly 0	SPIXopt 0	RSTreject 0	DOclamp 1
SBLKdly	0	1	0	1	0	1					SBdly[5] 0	0	0	0	0	SBdly[0] 0
SPIXdly	0	1	0	1	1	0		SPdly[8] 0	0	0	0	0	0	0	0	SPdly[0] 0
ADCdly	0	1	0	1	1	1			ADCdly[7] 0	0	0	0	0	0	0	ADCdly[0] 0
ReadBack	1	1	1	1	1	0	RBenable 0	RBreg[8] 0	0	0	0	0	0	0	0	RBreg[0] 0
Reset	1	1	1	1	1	1										Reset 0

Note: Shaded cells represent unused bits.

* Reserved Test register bits. Used for factory test only. Please do not modify.

Table 1. Serial Interface Register Address Map & default values

PGA00 Register

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PGA00	PGA00[9]	PGA00[8]	PGA00[7]	PGA00[6]	PGA00[5]	PGA00[4]	PGA00[3]	PGA00[2]	PGA00[1]	PGA00[0]
default	0	0	0	0	0	0	0	0	0	0

PGA00[9:0] is used to set the gain of the Programmable Gain Amplifier (PGA).
Code = 0000000000 is minimum gain (6dB). Code ≥ 1001111111 is maximum gain (36dB).
See the “Programmable Gain Amplifier” (pg. 16) and the “Multiple Gain Mode” (pg. 30) sections for more information.

Offset Register

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Offset			OB[7]	OB[6]	OB[5]	OB[4]	OB[3]	OB[2]	OB[1]	OB[0]
default	0	0	1	0	0	0	0	0	0	0

OB[7:0] is used by the Offset Calibration logic as the target output code for Optical Black pixels.
See the “Black Level Offset Calibration” section (pg. 19) for more information.

PGA01, PGA10 and PGA11 Registers

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PGA01		PGA01[8]	PGA01[7]	PGA01[6]	PGA01[5]	PGA01[4]	PGA01[3]	PGA01[2]	PGA01[1]	PGA01[0]
default	0	0	0	0	0	0	0	0	0	0
PGA10		PGA10[8]	PGA10[7]	PGA10[6]	PGA10[5]	PGA10[4]	PGA10[3]	PGA10[2]	PGA10[1]	PGA10[0]
default	0	0	0	0	0	0	0	0	0	0
PGA11		PGA11[8]	PGA11[7]	PGA11[6]	PGA11[5]	PGA11[4]	PGA11[3]	PGA11[2]	PGA11[1]	PGA11[0]
default	0	0	0	0	0	0	0	0	0	0

PGA01[8:0], PGA10[8:0] and PGA11[8:0] are used in the Multiple Gain mode to program the gain ratios for different pixel colors. See the “Multiple Gain Mode” section (pg. 30) for more information.

OB Even Gain & OB Odd Gain Registers

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OB Even Gain		OBE[8]	OBE[7]	OBE[6]	OBE[5]	OBE[4]	OBE[3]	OBE[2]	OBE[1]	OBE[0]
default	0	0	0	0	0	0	0	0	0	0

OBE[8:0] is used in the Multiple Gain mode to program the gain to be applied to Optical Black pixels on Even lines during Offset Calibration. OBO[8:0] is used in the Multiple Gain mode to program the gain to be applied to Optical Black pixels on Odd lines during Offset Calibration. See the “Multiple Gain Mode” section (pg. 30) for more information.

Even Line and Odd Line Registers

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Even Line	PRE[1]	PRE[0]	ELP4[1]	ELP4[0]	ELP3[1]	ELP3[0]	ELP2[1]	ELP2[0]	ELP1[1]	ELP1[0]
default	0	1	0	0	0	0	1	1	1	0
Odd Line	PRO[1]	PRO[0]	OLP4[1]	OLP4[0]	OLP3[1]	OLP3[0]	OLP2[1]	OLP2[0]	OLP1[1]	OLP1[0]
default	0	1	0	0	0	0	0	0	0	1

The Even Line and Odd Line Registers are used to program the pixel patterns for Even and Odd lines in the Multiple Gain mode. See the “Multiple Gain Mode” section (pg. 30) for more information.

Calibration Register

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Calibration		OBdel[1]	OBdel[0]	Avg[1]	Avg[0]	DNS[1]	DNS[0]	Mode	Hold	ManCal
default	0	0	0	1	0	0	1	0	0	0

The Calibration register is used to program various options for the Offset Calibration logic.
OBdel[1:0], sets the number of Fringe pixels which should not be used for Black Level Calibration.
Avg[1:0], sets the number of OB pixels to average, 00=32 pix, 01=64 pix, 10=128 pix, 11=256 pix.
DNS[1:0], sets the Digital Noise Suppression filter width, 00=no filter, 01=narow, 10=med, 11=wide.
Mode, sets Calibration mode. 0=Line mode, 1=Frame mode (not supported at this time).
Hold, used to stop calibration updates. 0=Calibration active. 1=stop, hold current Calibration values.
ManCal, used to manually program the Offset DACs. 0=automatic mode. 1=manual mode.
See the “Black Level Offset Calibration” section (pg. 19) for more information.

Wait A, Wait B and OB Lines Registers

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WaitA	WL[11]	WL[10]	WL[9]	WL[8]	WL[7]	WL[6]	WL[5]	WL[4]	WL[3]	WL[2]
default	0	0	0	0	0	0	0	0	0	0
WaitB									WL[1]	WL[0]
default	0	0	0	0	0	0	0	0	0	1
OB Lines			OBL[7]	OBL[6]	OBL[5]	OBL[4]	OBL[3]	OBL[2]	OBL[1]	OBL[0]
default	0	0	1	0	0	0	0	0	1	0

WL[11:0] and OBL[7:0] are used by the Black Level Calibration logic in the Frame mode to determine which lines to use for Calibration. (Frame mode is not currently supported)
See the “Black Level Offset Calibration” section (pg. 19) for more information.

CDAC Even and CDAC Odd Registers

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CDAC Even		CDE[8]	CDE[7]	CDE[6]	CDE[5]	CDE[4]	CDE[3]	CDE[2]	CDE[1]	CDE[0]
default	0	0	0	0	0	0	0	0	0	0
CDAC Odd		CDO[8]	CDO[7]	CDO[6]	CDO[5]	CDO[4]	CDO[3]	CDO[2]	CDO[1]	CDO[0]
default	0	0	0	0	0	0	0	0	0	0

CDE[8:0] and CDO[8:0] are used to program the internal Coarse Offset DAC in the Manual Calibration mode. In the normal, single gain mode the value in CDE[8:0] is used. In the Multiple Gain mode, CDE[8:0] is used for Even lines and CDO[8:0] is used for Odd lines.
See the “Black Level Offset Calibration” section (pg. 19) for more information.

FDAC Even and FDAC Odd Registers

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FDAC Even	FDE[9]	FDE[8]	FDE[7]	FDE[6]	FDE[5]	FDE[4]	FDE[3]	FDE[2]	FDE[1]	FDE[0]
default	0	0	0	0	0	0	0	0	0	0
FDAC Odd	FDO[9]	FDO[8]	FDO[7]	FDO[6]	FDO[5]	FDO[4]	FDO[3]	FDO[2]	FDO[1]	FDO[0]
default	0	0	0	0	0	0	0	0	0	0

FDE[9:0] and FDO[9:0] are used to program the internal Fine Offset DAC in the Manual Calibration mode. In the normal, single gain mode the value in FDE[9:0] is used. In the Multiple Gain mode, FDE[9:0] is used for Even lines and FDO[9:0] is used for Odd lines.
See the “Black Level Offset Calibration” section (pg. 19) for more information.

Control Register

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Control	ADCpd	AFEpd	CHIPpd	OE	MultGain	MGsel[1]	MGsel[0]	MGstart	MinClip	OneV
default	0	0	0	1	0	0	0	0	1	0

The Control register is used to program various options.
ADCpd, power down the ADC block. 0=normal operation. 1=ADC power down.
AFEpd, power down the AFE block. 0=normal operation. 1=AFE power down.
OE, output enable control. 0=DB[11:0] in high Z mode. 1=DB[11:0] in active drive mode.
MultGain, enable the Multiple Gain mode. 0=single gain mode. 1= Multiple Gain mode.
MGsel[1:0], Multiple Gain timing mode select.
MGstart, Even or Odd starting condition for MGsel[1:0]=11. 0=start with Even line, 1=start with Odd line.
MinClip, minimum clip option. 0=minimum clip disabled, 1=minimum clip enabled.
OneV, 1 volt input range option. 0=0.8V maximum input range. 1=1.0V maximum input range.
See the “Chip Power Down” section (pg. 34) for information about ADCpd, AFEpd, CHIPpd and OE.
See the “Multiple Gain Mode” section (pg. 30) for information about MultGain, MGsel[1:0] and MGstart.
See the “Other Chip Controls and Features” section (pg. 34) for information about MinClip.
See the “One Volt Input Option” section (pg. 16) for information about OneV.

Test Register

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Test		nofs2	*Reserved	*Reserved	*Reserved	*Reserved	ADCin	NoCDS	*Reserved	*Reserved
default	0	0	0	0	1	0	0	0	0	0

The Test register is used to program various special modes of the chip.
* Reserved bits are for Exar Factory test only, do not modify these bits.
nofs2, analog ½ scale offset control. 0=normal CCD signal conversion. 1=no ½ scale offset at PGA.
ADCin, ADC direct analog input mode. 0=normal operation. 1=CCDin & REFin connect directly to ADC.
NoCDS, CDS By-Pass mode. 0=normal operation. 1=CCDin & REFin connect directly to PGA.
See the "Analog Front End" section (pg. 15) for information about nofs2 and NoCDS
See the "Analog to Digital Converter" section (pg. 18) for information about ADCin,

Polarity Register

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Polarity			PBLKpol	EOSpol	SBLKpol	SPIXpol	CALpol	CLAMPpol	FSYNCpol	ADCpol
default	0	0	0	1	0	0	0	0	0	0

The Polarity register is used to program the polarity of the clock inputs. All the clock inputs (except the serial interface SCLK) can be programmed to be active high or active low. 0=active low. 1=active high.
See the "Clock Polarity" section (pg. 22) for more information.

Clock Register

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Clock					ADCLKsel	CLAMPopt	CALonly	SPIXopt	RSTreject	DOclamp
default	0	0	0	0	0	0	0	0	0	1

The Clock register is used for programming various clocking options.
ADCLKsel, select internal or external ADC clock. 0=external ADCLK pin. 1=internal ADCLK.
CLAMPopt, DC restore biasing. 0=bias powered only when CLAMP is active. 1=bias always powered.
CALonly, line timing option. 0=CAL & CLAMP signals required. 1=only CAL signal required.
SPIXopt, ϕ2 signal generation option. 0=ϕ2 is a function of SPIX. 1=ϕ2 is a function of SBLK & SPIX.
RSTreject, reset pulse rejection option. 0=ϕ3 always ON. 1=ϕ3 switched to reject CCD reset pulse.
DOclamp, digital output clamp option. 0=disable clamp function. 1=PBLK forces digital outputs to OB[7:0]
See the "Analog Front End" section (pg. 15) for information about CLAMPopt.
See the "Pixel Rate Clocks, SBLK, SPIX, and ADCLK" section (pgs. 22-25) for information about ADCLKsel, CAL only, SPIXopt and RSTreject.
See the "Other Chip Controls and Features" section (pg. 34) for information about DOclamp.

SBLK Delay, SPIX Delay and ADC Delay Registers

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SBLK Delay					SBdly[5]	SBdly[4]	SBdly[3]	SBdly[2]	SBdly[1]	SBdly[0]
default	0	0	0	0	0	0	0	0	0	0
SPIX Delay		SPdly[8]	SPdly[7]	SPdly[6]	SPdly[5]	SPdly[4]	SPdly[3]	SPdly[2]	SPdly[1]	SPdly[0]
default	0	0	0	0	0	0	0	0	0	0
ADC Delay			ADCdly[7]	ADCdly[6]	ADCdly[5]	ADCdly[4]	ADCdly[3]	ADCdly[2]	ADCdly[1]	ADCdly[0]
default	0	0	0	0	0	0	0	0	0	0

SBdly[5:0], SPdly[8:0] and ADCdly[7:0] are used to program the internal aperture delay options. Each register is divided into 2 or 3 delay parameters. For each delay parameter, minimum delay is all 0's, and maximum delay is all 1's.
See the "Aperture Delays" section (pg. 26) for information about the Programmable Aperture Delays.

Readback Register

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Readback	RBenable	RBreg[8]	RBreg[7]	RBreg[6]	RBreg[5]	RBreg[4]	RBreg[3]	RBreg[2]	RBreg[1]	RBreg[0]
default	0	0	0	0	0	0	0	0	0	0

RBenable, used to enable the Readback feature. 0=Readback OFF. 1=ReadBacK ON.
RBreg[8:6], used to select internal Calibration or Multiple Gain registers for Readback.
RBreg[5:0], used to select internal Serial Interface registers for Readback.
See the “Serial Interface Readback” section (pg. 14) for more information.

Reset Register

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reset										Reset
default	0	0	0	0	0	0	0	0	0	0

The Reset bit is used to reset the chip to power-up default conditions.
Program Reset=1 to reset the chip. After all internal registers are reset, the Reset bit will clear itself.
See the “Chip Reset” section (pg. 34) for more information.

Serial Interface Readback

The readback function is used to view the content of the serial interface registers as well as several key registers in the ofset calibration logic. Readback is enabled by writing a 1 to the RBenable bit (D9) of the Readback register.

In the readback mode, the content of the selected register is output on the 10 MSBs of the ADC output bus pins DB[11:2]. As long as valid clocks and CCD signal are applied, the calibration will continue to function properly during readback (internally the ADC data is still sent to the calibration logic).

Registers are selected for readback by writing to the RBreg[8:0] bits in the Readback register, bits D8 to D0. If RBreg[8:6]=000, then RBreg[5:0] are used to address the serial interface registers. Currently only register addresses 0 to 23, 62 and 63 are defined. If RBreg[8:6]≠000, then RBreg[5:0] are ignored and RBreg[8:6] are used to address registers in the calibration logic.

RBenable	RBreg[8]	RBreg[7]	RBreg[6]	RBreg[5]	RBreg[4]	RBreg[3]	RBreg[2]	RBreg[1]	RBreg[0]	Selected Register	Register Number
0	x	x	x	x	x	x	x	x	x	none (ADC data output)	
1	0	0	0	0	0	0	0	0	0	PGA00	0
1	0	0	0	0	0	0	0	0	1	Offset	1
1	0	0	0	0	0	0	0	1	0	PGA01	2
1	0	0	0	0	0	0	0	1	1	PGA10	3
1	0	0	0	0	0	0	1	0	0	PGA11	4
1	0	0	0	0	0	0	1	0	1	OB Even Gain	5
1	0	0	0	0	0	0	1	1	0	OB Odd Gain	6
1	0	0	0	0	0	0	1	1	1	Even Line	7
1	0	0	0	0	0	1	0	0	0	Odd Line	8
1	0	0	0	0	0	1	0	0	1	Calibration	9
1	0	0	0	0	0	1	0	1	0	Wait A	10
1	0	0	0	0	0	1	0	1	1	Wait B	11
1	0	0	0	0	0	1	1	0	0	OB Lines	12
1	0	0	0	0	0	1	1	0	1	CDAC Even	13
1	0	0	0	0	0	1	1	1	0	CDAC Odd	14
1	0	0	0	0	0	1	1	1	1	FDAC Even	15
1	0	0	0	0	1	0	0	0	0	FDAC Odd	16
1	0	0	0	0	1	0	0	0	1	Control	17
1	0	0	0	0	1	0	0	1	0	Test	18
1	0	0	0	0	1	0	0	1	1	Polarity	19
1	0	0	0	0	1	0	1	0	0	Clock	20
1	0	0	0	0	1	0	1	0	1	SBLKdly	21
1	0	0	0	0	1	0	1	1	0	SPIXdly	22
1	0	0	0	0	1	0	1	1	1	ADCdly	23
1	0	0	0	1	1	1	1	1	0	ReadBack	62
1	0	0	0	1	1	1	1	1	1	Reset	63
1	0	0	1	x	x	x	x	x	x	Average Even (internal)	Cal 1
1	0	1	0	x	x	x	x	x	x	Average Odd (internal)	Cal 2
1	0	1	1	x	x	x	x	x	x	CDAC Even (internal)	Cal 3
1	1	0	0	x	x	x	x	x	x	CDAC Odd (internal)	Cal 4
1	1	0	1	x	x	x	x	x	x	FDAC Even (internal)	Cal 5
1	1	1	0	x	x	x	x	x	x	FDAC Odd (internal)	Cal 6
1	1	1	1	x	x	x	x	x	x	Gain (internal)	Cal 7

Table 2. Readback Register Selection

ANALOG FRONT END (AFE)

Correlated Double Sample/Hold (CDS)

The function of the CDS block is to sense the voltage difference between the black level and video level for each pixel. The PGA amplifies the difference to the desired level for the ADC. The CDS and PGA are fully differential. The CCDIN pin should be connected, via a capacitor, to the CCD output signal. The REFIN pin should be connected, via a capacitor, to the CCD "Common" voltage (typically the CCD ground is used as the "Common" voltage). These capacitors, C1 and C2, are typically 0.01µF ± 10% or better matching.

The internal timing signals ϕ1, ϕ2, and ϕ3, which are generated from SBLK and SPIX, control the sampling switches shown in Fig. 6. ϕ3 (reset reject switches) are closed to simplify the operation described below.

At the beginning (or end) of every video line, the DC restore switch forces one side of the external capacitors to an internal bias level (Vbias1=1.2V). The DC restore switch is controlled by the combination of the CLAMP input signal ANDed with the ϕ2 clock.

The CLAMPopt bit in the Clock register controls the circuit which generates the Vbias1 level. When CLAMPopt=0 (the default condition), the Vbias1 level is only generated while CLAMP is active. When CLAMP is not active, the Vbias1 circuit is put in a stand-by mode, reducing the supply current by about 1 mA. When CLAMPopt=1, the Vbias1 circuit always runs at full power.

During the black reference phase of each CCD pixel, the ϕ1 (Sample Black Reference) switches are turned on, shorting the CDSamp inputs to a second bias level (Vbias2). The Coarse Offset DAC adds an adjustment to the bias level (Vbias2) to cancel black level offset in the CCD signal. When the ϕ1 switches turn off, the pixel black reference level is held on the internal black sample capacitors, and the CDSamp is ready to gain up the CCD video signal.

During the video phase of each CCD pixel, the difference between the pixel black level and video level is transmitted through the internal black sample capacitors and converted to a fully differential signal by the CDSamp. At this time, the ϕ2 (Sample Pixel value) switches turn on, and the internal video sample capacitors track the amplified difference. The Fine Offset DAC adds offset adjustment to the PGA2 output (post gain).

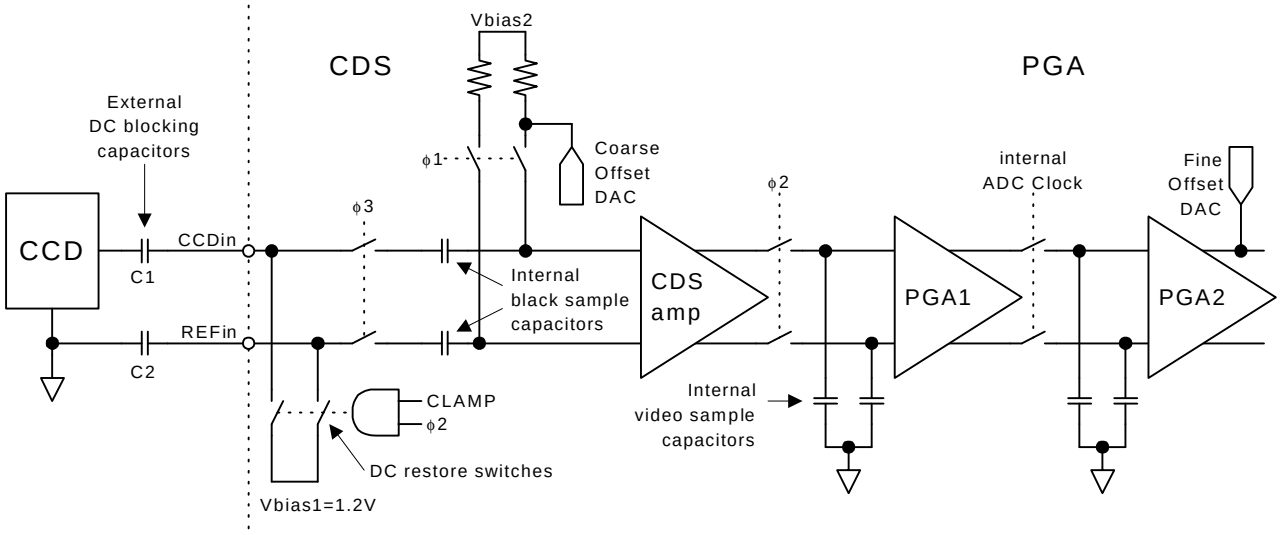


Figure 6. CDS and PGA Block Diagram

One Volt Input Option

The CDS amp is designed to normally handle a maximum signal of 800mV (V_{BLACK} - V_{VIDEO}). The One Volt option allows the CDS amp to handle up to 1.0V with no distortion. The One Volt option is enabled by writing a 1 to the "OneV" bit in the Control register.

Programmable Gain Amplifier (PGA)

The PGA provides gains from 6 dB to 36 dB in approximately 0.047 dB steps. The desired gain setting is programmed via the 10 bit gain register in the Serial Interface.

For gain codes between 0 and 639, the gain can be calculated by the following equation:

$$\text{Gain}[\text{dB}] = \left(\frac{Code}{640} \times 30\right) + 6$$

For gain codes ≥ 640, the gain is fixed at 36 dB. The gain increases by 6dB (a factor of 2x) every 128 codes. This should help simplify DSP algorithms and control.

An example of setting the gain is as follows: if the CCD input is limited to 800mVpp ($CDSV_{IN}$) and the ADC full scale differential input (VID) is 1.8Vpp, then a minimum gain is calculated by:

$$\text{Gain} = 20\log\left(\frac{VID}{CDSVin}\right) = 20\log\left(\frac{1.8\text{V}}{0.8\text{V}}\right) = 7.04\text{dB}$$

The gain code would be set to 22 (decimal) for a PGA gain of 7.03 dB.

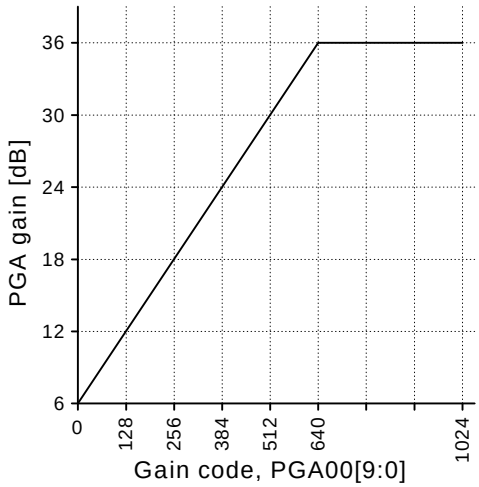


Figure 7. PGA Gain vs. Gain Code

CDS By-Pass Mode

The CDS By-Pass mode connects the CCDin and REFin pins directly to the CDS amp inputs, by-passing the CDS switching function. This mode is useful for testing the PGA/ADC with a simple differential or a single-ended signal.

To enable the CDS By-Pass mode, write a "1" to the No CDS bit in the Test register. This will disable the CDS switching functions and turn on switches which connect the CCDin & REFin pins directly to the CDS amp inputs.

In the CDS By-Pass mode, the SPIX signal is required to clock the switched-capacitor PGA stages, and ADCLK is required to clock the ADC. The PGA analog output does not come out to any pin; the ADC digital output must be monitored instead.

When using the CDS By-Pass mode, the calibration logic must be put in either the Hold mode or the ManCal mode. In the CDS By-Pass mode, the Coarse Offset DAC does not affect the input, but the Fine Offset DAC does affect the PGA output. The calibration logic is not aware that the Coarse Offset DAC is not active, and will cause errors if left operating in the automatic mode.

To simplify signal interfacing when using the CDS By-Pass mode, write a "1" to the nofs2 bit in the Test register. This will disable the ½ scale offset introduced at the PGA ouput (this offset is required for CCD signal digitization).

When using the CDS By-Pass mode, the ADC digital output code will be related to the inputs by the transfer function below:

$$\text{ADCout} = 2048 + \left[\text{PGAgain} \times \left(REFin - CCDin\right) + \text{FineOffsetDAC}\right] \times \frac{4096}{2\left(\text{CapP} - \text{CapN}\right)}$$

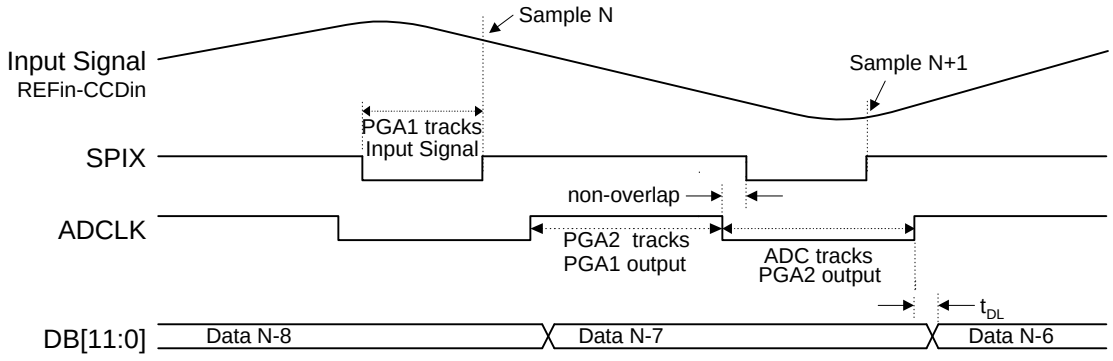


Figure 8. CDS By-Pass Mode Timing

ANALOG TO DIGITAL CONVERTER (ADC)

The analog-to-digital converter is based on pipeline architecture with a built in track & hold input stage. The track & hold and ADC conversion are controlled by the externally supplied ADCLK.

The polarity of the ADCLK is programmable. If ADCpol=low, the track & hold circuit tracks the PGA output while ADCLK is high and holds while ADCLK is low. If ADCpol=high, the track & hold circuit tracks the PGA output while ADCLK is low and holds while ADCLK is high. ADCLK should be a 50% duty cycle clock, and should be synchronized with SBLK such that ADC tracking ends at the same time as the CDS sample black ends. (See Figure 16).

The ADC reference levels, Vcm, CapP & CapN, are generated from an internal voltage reference. To minimize noise, these pins should have high frequency bypass capacitors to AGND. The value of these capacitors will affect the time required for the reference to charge up and settle after power-down mode.

The ADC output bus, DB[11:0], has 3-state capability controlled by the OE bit of the Control register and pin 42, $\overline{OE}$. The output bus is enabled when both the OE bit is high and the $\overline{OE}$ pin is low. The outputs become high impedance when either the OE bit is low or the $\overline{OE}$ pin is high.

Direct ADC Input Mode

The Direct ADC Input mode connects the CCDin & REFin pins directly to the ADC inputs, by-passing the CDS & PGA circuits. To enable the Direct ADC Input mode, use the Serial Interface to program:

ADCin=1 in the Test register,
DOclamp=0 in the Clock register, and
MinClip=0 in the Control register.

In this mode, the PGA outputs are disabled so there is no contention at the ADC input nodes. For best performance, we recommend using fully differential signals with a common mode level around 1.2V.

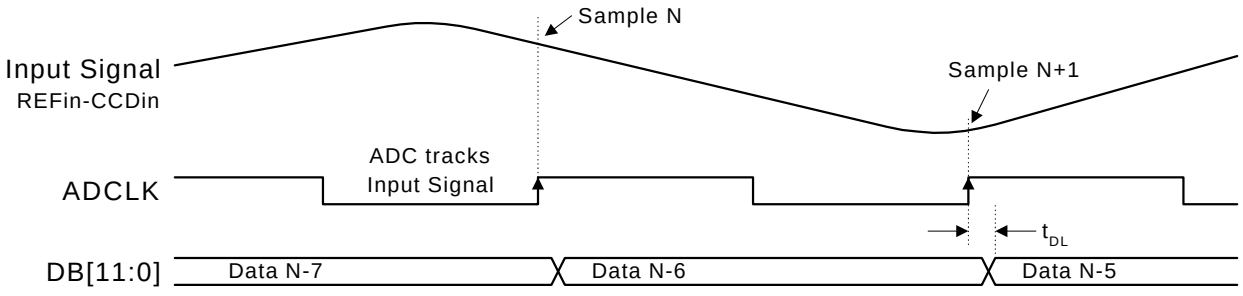


Figure 9. Direct ADC Input Mode Timing

BLACK LEVEL OFFSET CALIBRATION

To get the maximum color resolution and dynamic range, the XRD98L63 uses a digitally controlled calibration circuit to correct for offset in the CCD signal as well as offset in the CDS, PGA & ADC signal path. This calibration is done while the CCD outputs Optical Black (OB) pixels.

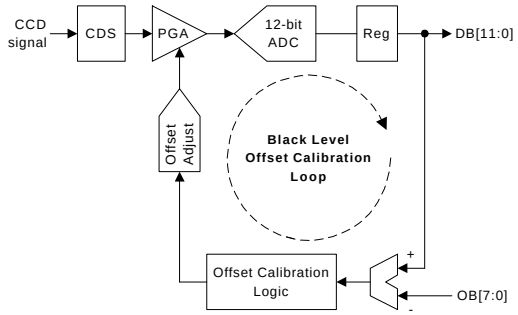


Figure 10. Simplified Block Diagram of Black Level Offset Calibration Loop

In the default "Line" timing mode, OB pixels are sampled when CAL is active at the start, or end, of each CCD scan line. CAL can be programmed to be active high or active low; please see the Timing section for more details about clock polarity. Averaging will span as many lines as needed to get the number of OB pixels programmed by Avg[1:0]. Updates to the offset DACs occur during the Optical Black pixel time after a complete iteration. A complete iteration includes the pixel clipping, averaging, calculation of the offset difference, and calculation of the DAC update values. After a complete iteration, the averager is reset, and the logic waits for the number of lines programmed in the “Wait A” & “Wait B” registers, WL[11:0], before starting the next iteration.

Offset Register										ADC Output
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Black Level (LSB)
X	X	0	0	0	0	0	0	0	0	0
X	X	0	0	0	0	0	0	0	1	1
					.					.
					.					.
					.					.
X	X	1	1	1	1	1	1	1	0	254
X	X	1	1	1	1	1	1	1	1	255

Table 3. Black Level Output Control

Hot Pixel Clipper

CCD’s occasionally have hot pixels. These are defective pixels, which always output a bright level. To ensure the Black Level is not affected by hot pixels in the OB area, the Hot Pixel Clipper limits pixel data from the ADC to a maximum value of 511 (1FFh). This clipping only affects the data used by the internal calibration logic. Data on the ADC output bus, DB[11:0], is not clipped.

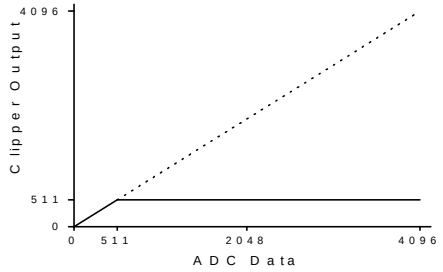


Figure 11. Hot Pixel Clipper

Pixel Averager

After the clipper, the logic takes an average of the Optical Black pixels. The number of pixels to be averaged can be selected as one of the following: 32, 64, 128, or 256. The Avg[1:0] bits in the Calibration register are used to program the number of pixels to average. This averaging function filters out noise and prevents image artifacts. The calibration logic will average OB pixels over as many lines as required to get the programmed number of pixels to average.

In the Multiple Gain Mode, the logic keeps separate avarages for even and odd lines.

Avg[1]	Avg[0]	# of Pixels to Average
0	0	32
0	1	64
1	0	128 (default)
1	1	256

Table 4. Programming the Pixel Averager

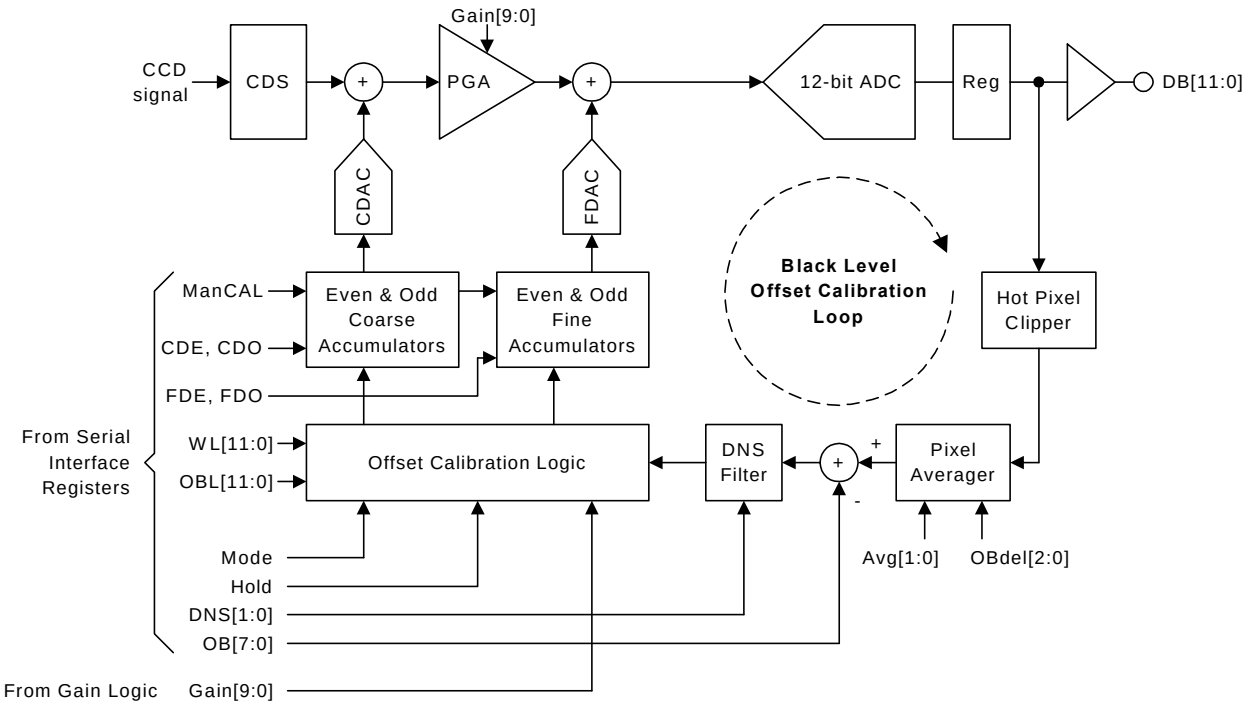


Figure 12. Detailed Block Diagram of the Black Level Offset Calibration Logic

Offset Difference

Next, the Offset register value, OB[7:0], is subtracted from the OB pixel average. If the difference is positive, the offset DACs are adjusted to reduce the effective ADC output code. If the difference is negative, the offset DACs are adjusted to increase the effective ADC output code. The DNS option will affect how the DAC adjustments are made.

Coarse & Fine Accumulators

The Coarse and Fine Accumulators are the registers which hold the digital codes for the Coarse and Fine Offset DACs. The Offset DAC adjustments are made by adding to or subtracting from the value in the Fine accumulator. If there is an overflow or underflow in the Fine Accumulator, the Fine Accumulator is reset to it's mid-scale value, and the Coarse Accumulator is incremented or decremented accordingly.

In the Multiple Gain Mode, there are separate accumulators for even and odd lines.

Calibration Options

Digital Noise Suppression (DNS) Filter

The purpose of this option is to eliminate small changes in the Black Level offset by making the calibration system less sensitive to small changes in the measured offset. In this mode, the user has the option of selecting from three filter settings, see Table 5.

DNS[1]	DNS[0]	DNS Filter Width
0	0	OFF
0	1	Narrow (default)
1	0	Medium
1	1	Wide

Table 5. DNS Threshold Programming

To activate the Digital Noise Suppression mode, write to the DNS[1:0] bits in the Calibration register.

By default, the Digital Noise Suppression is ON and set to the narrow filter width.

Hold Mode

The purpose of this mode is to prevent any changes in the Fine or Coarse accumulators. This mode is intended to optimize digital still camera applications (DSC). The idea is to first run the calibration normally so the Fine and Coarse accumulators converge on the correct values to achieve the programmed Offset Code. Then, just before acquiring the final image data, activate the Hold mode. This will ensure the black level offset of the CDS/PGA does not change while the final image is being transferred out of the CCD. Once the image has been acquired from the CCD, turn off the Hold mode so the chip can continue to compensate for any changes in offset due to temperature drift or other effects.

To activate the Hold mode, write a "1" to the CAL Hold bit in the Calibration register. By default, the Hold mode is not active.

Manual Mode

The purpose of the Manual Mode is to disable the automatic calibration feature and allow a system to write directly to the Coarse and Fine Offset Adjust DACs. When Manual mode is enabled, the Coarse Offset DAC (CDAC) is programmed by writing to the CDAC Even register, CDE[8:0]; the Fine Offset DAC is programmed by writing to the FDAC Even register, FDE[9:0].

If the Multiple Gain Mode is enabled, then the CDAC Odd register and the FDAC Odd register are also used to program the Offset Adjust DACs.

To activate the Manual mode, write a "1" to the ManCal bit in the Calibration register. By default, the Manual mode is not active.

Ignoring Fringe Pixels

Fringe pixels are the first few OB pixels at the edge of the metal shield. Usually, these pixels receive some reflected and/or scattered light, so they do not represent true "Optical Black". If the CAL signal is active while the CCD outputs Fringe pixels, the Calibration logic will not converge properly. The OBdel[1:0] parameter can be used to tell the Calibration logic to ignore (or delete) the first 0-3 OB pixels every time the CAL signal is activated.

OBdel[1:0]	Number of Fringe Pixels to Ignore
00	0
01	1
10	2
11	3

Table 6. Ignoring Fringe Pixels

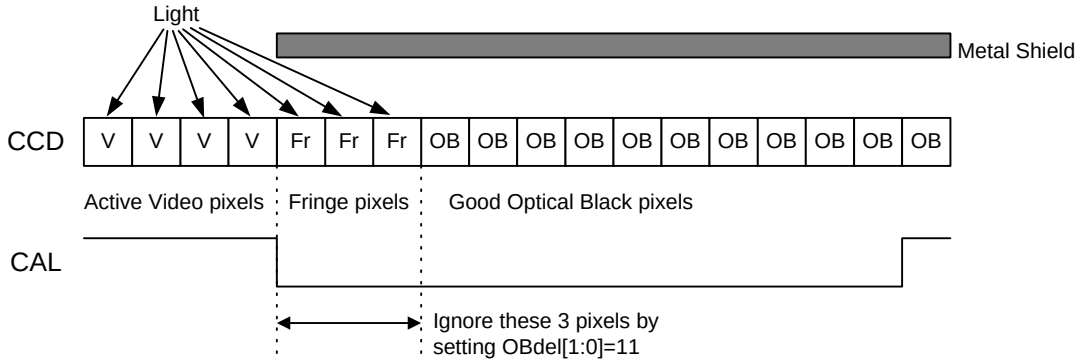


Figure 13. Example of Ignoring Fringe Pixels Using OBdel[2:0]

TIMING: CLOCK BASICS

There are 8 clock signals SBLK, SPIX, ADCLK, CLAMP, CAL, PBLK, EOS and Fsync.

The pixel rate clocks are SBLK, SPIX, and ADCLK. SBLK controls sampling of the Black reference level for each pixel. SPIX controls sampling of the Video level for each pixel. ADCLK controls the ADC sampling of the PGA output and ADC operation.

The line rate clocks are CLAMP, CAL, PBLK and EOS. CLAMP controls the DC restore function for the external AC coupling capacitors. CAL controls the Black level calibration by defining the OB pixels at the start or end of each line. In the One Shot mode (CAL only), CLAMP is not used. PBLK is used to disconnect the CDS from the CCDin & REFin pins during vertical shift time. If the DOclamp bit in the Clock register is high, PBLK will also force the digital output bus, DB[11:0], to output the value in the Offset register, OB[7:0]. EOS is used in the Multiple Gain mode to indicate if a line (or field) is even or odd.

Clock Polarity

Each of the 8 clock pins has a separate polarity control bit in the Polarity register. If the polarity bit for a clock is low, then the clock is active low. If the polarity bit for a clock is high, then the clock is active high. After reset (by POR, Reset bit or XRESET pin), all clocks default to active low; EOS defaults to active high.

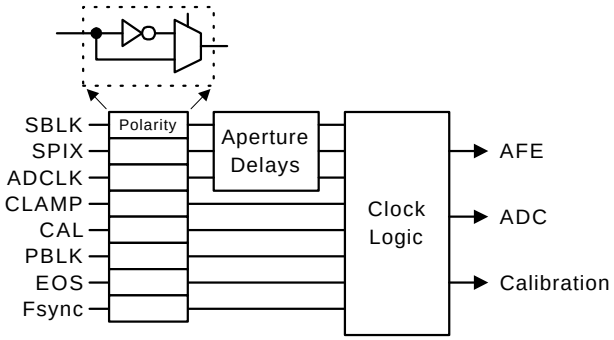


Figure 15. Clock Polarity & Aperture Delays

Pipeline Delay

The digital outputs, DB[11:0] and OVER, are synchronized to ADCLK. When ADCLKpol=0 (default), the digital outputs change on the rising edge of ADCLK. Figure 14 shows the pipeline delay (latency) from sampling a pixel at the CDS input, until the corresponding data is available at the digital output.

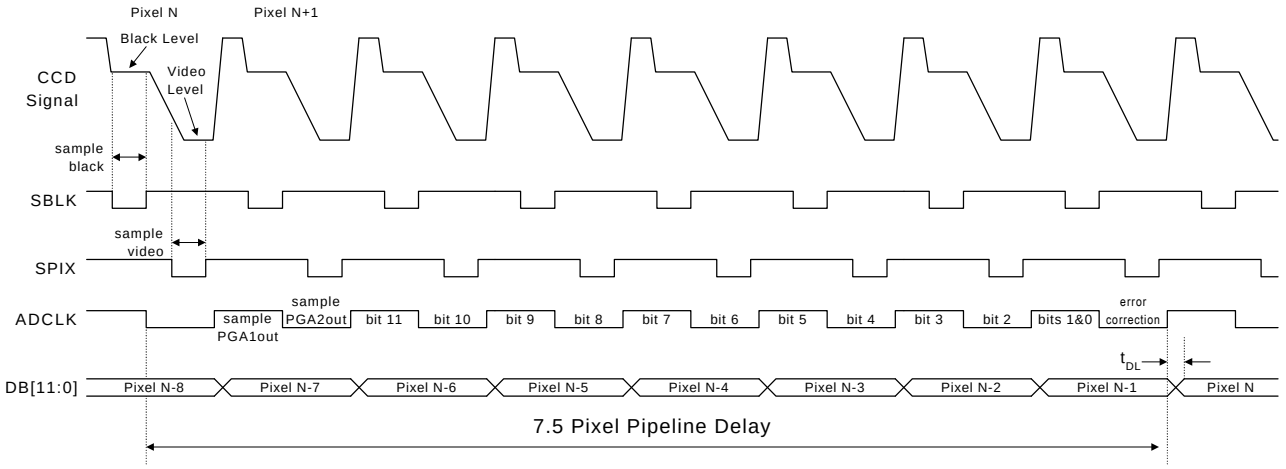


Figure 14. Pixel Timing Showing Pipeline Delay

PIXEL RATE CLOCKS SBLK, SPIX & ADCLK

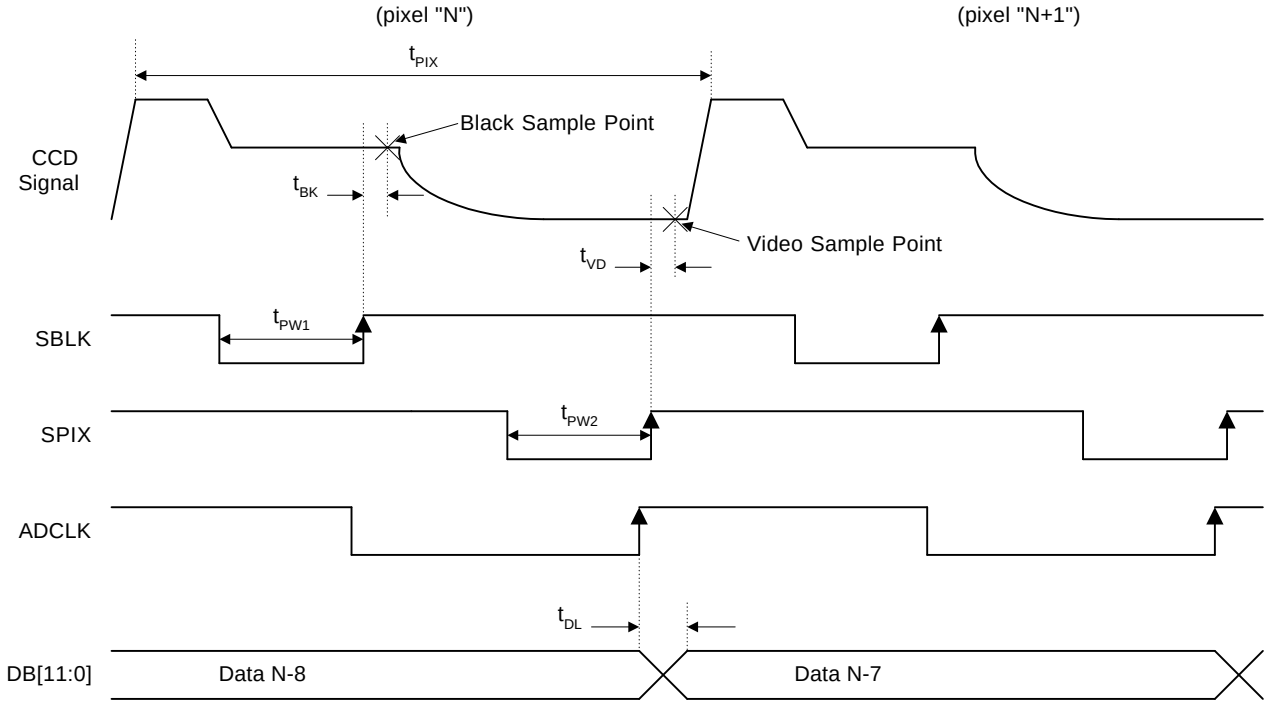


Figure 16. Detailed Pixel Rate Clock Timing for Default Register Settings

Note:

The timing descriptions in this section are correct for the default conditions:
All Polarity bits = 0,
RSTreject = 0 (switch always ON),
SPIXopt = 0

Sampling of the pixel black level is controlled by the SBLK pulse. When SBLK is low, t_{PW1}, the internal sample black switches in the CDS are ON, sampling the pixel black level on the internal black sample capacitors.

Sampling of the pixel video level is controlled by the SPIX pulse. When SPIX is low, t_{PW2}, the video signal propagates through the CDS amp and is sampled on the internal video sampling capacitors. When SPIX goes high, PGA1 gains up the signal from the video sample capacitors.

PGA2 and the ADC form an analog pipeline controlled by ADCLK. When ADCLK is high, PGA2 is sampling the output of PGA1. When ADCLK goes low, PGA2 gains up the sampled signal and the first stage of the ADC samples the output of PGA2. ADCLK should be as close as possible to 50% duty cycle.

If your timing generator does not provide a clock signal suitable for ADCLK, there is an option to generate ADCLK internally. Write a "1" to the "ADCLKsel" bit in the Clock register. This will generate an internal ADCLK based on the SBLK and SPIX clock signals. We recommend that the ADCLK pin be tied to ground when the ADCLKsel option is used.

SPIXopt

In the default case (Figure 17) SPIXopt=0, the signal controlling the internal Sample Video switches, $\phi 2$, is generated from only the SPIX pulse. This mode is intended for camera systems where the designer has the ability to externally fine tune both the rising and falling edges of SPIX to achieve the best performance.

When SPIXopt = 1 (Figure 18), $\phi 2$ is generated from a combination of SBLK and SPIX. $\phi 2$ will turn ON the internal sample video switches by a programmed delay after the SBLK pulse ends. The turn ON delay is programmed by the addition of SBdly[5:3] and SPdly[8:6]. $\phi 2$ will turn OFF the sample video switches at the end of the SPIX pulse.

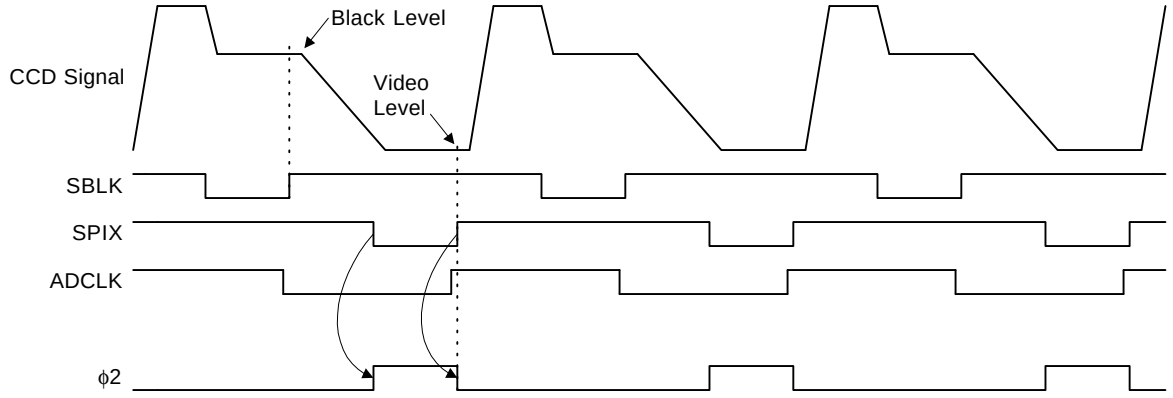


Figure 17. Pixel Rate Clock Timing with SPIXopt=0 (Default)

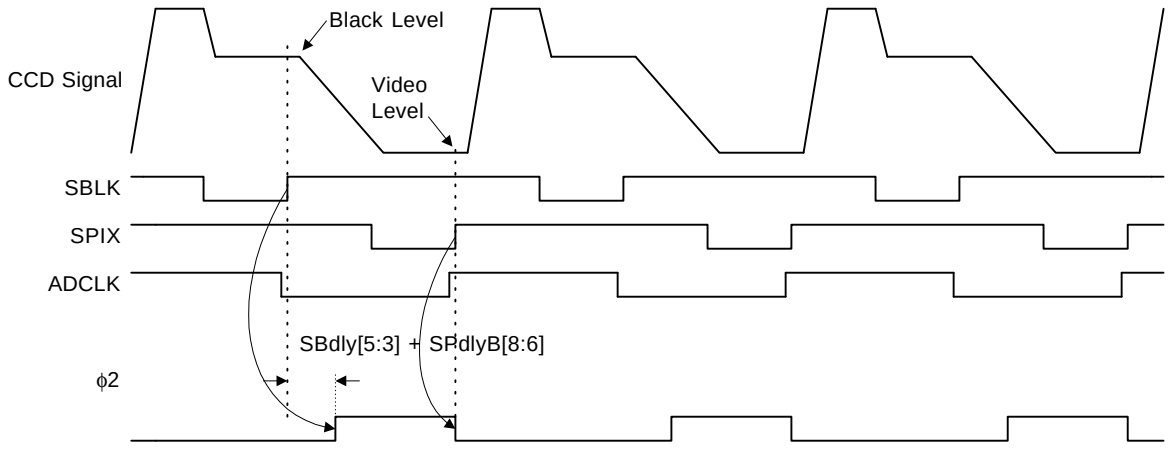


Figure 18. Pixel Rate Clock Timing with SPIXopt=1

Reset Reject

In the default state, the reset reject switches (ϕ3) are always ON; they are not clocked. The reset pulse of each pixel is transmitted to the first stage of the PGA. Depending on the PGA gain and the actual voltage level of the reset pulse, this could cause the first stage of the PGA to rail. During the Black Level sampling, the PGA should have enough time to recuperate, but as a precaution, we have included the Reset Reject option.

When RSTreject = 1, the reset reject switches are turned OFF at the end of the SPIX pulse and turned ON again at the start of the SBLK pulse. This will effectively reject the reset pulse and prevent it from railing the PGA.

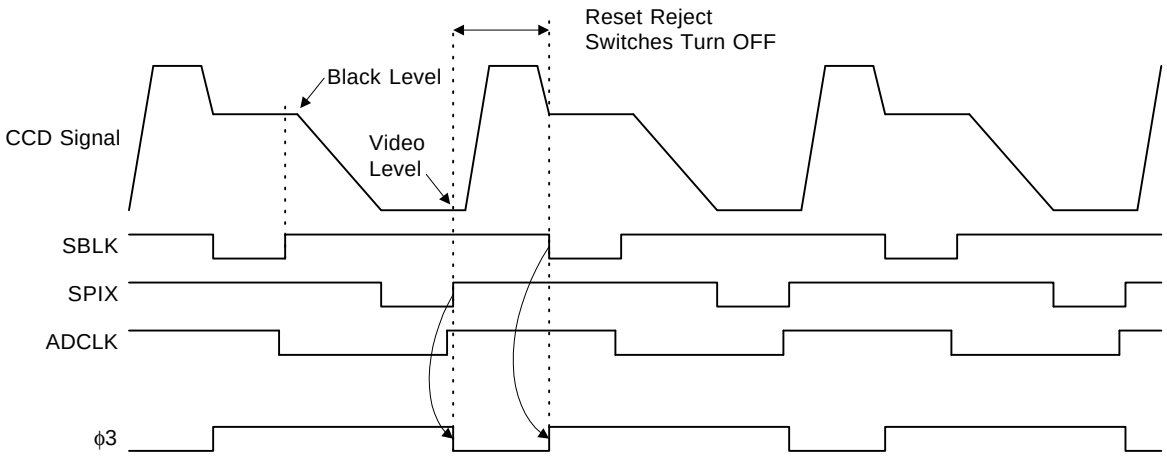


Figure 19. Pixel Rate Clock Timing with RSTreject=1

Aperture delays

One of the most difficult tasks in designing a digital camera is optimizing the pixel timing for the CCD, CDS and ADC. We have included the programmable aperture delay function to help simplify this job.

There are three serial interface registers, SBLKdly, SPIXdly, and ADCdly, used to program the aperture delays. Each register is divided into 2 or 3 delay parameters.

The delays are added to the clock signals after the polarity control. This means the definition of leading edge and trailing edge of the external clock signals (SBLK, SPIX & ADCLK) depends on the polarity control bit for each clock. For the default case, SBLKpol=0, SPIXpol=0 & ADCpol=0, the leading edge is the falling edge and the trailing edge is the rising edge.

The SBLKdly register is divided into two 3-bit delay parameters, SBdly[2:0] and SBdly[5:3]. Each can add from 0 to 7 ns of delay in 1 ns steps.

SBdly[2:0] controls the delay added to the leading edge of SBLK. This positions the rising edge of the internal signal ϕ1.

SBdly[5:3] controls the delay added to the trailing edge of SBLK. This positions the falling edge of the internal signal ϕ1.

The SPIXdly register is divided into three 3-bit delay parameters, SPdly[2:0], SPdly[5:3] and SPdly[8:6]. Each can add from 0 to 7 ns of delay in 1 ns steps.

SPdly[2:0] controls the delay added to the leading edge of SPIX. This positions the rising edge of the internal signal ϕ2.

SPdly[5:3] controls the delay added to the trailing edge of SPIX. This positions the falling edge of the internal signal ϕ2.

SPdly[8:6] is only used when SPIXopt=1. It controls the delay from the trailing edge of SBLK to the rising edge of the internal signal ϕ2. This delay is in addition to SBdly[5:3], the SBLK trailing edge delay.

The ADCdly register is divided into two 4-bit delay parameters, ADCdly[3:0] and ADCdly[7:5]. Each can add from 0 to 7.5 ns of delay in 0.5 ns steps.

ADCdly[3:0] controls the delay added to the leading edge of ADCLK. This positions the falling edge of the internal signal ϕ4.

ADCdly[7:4] controls the delay added to the trailing edge of ADCLK. This positions the rising edge of the internal signal ϕ4.

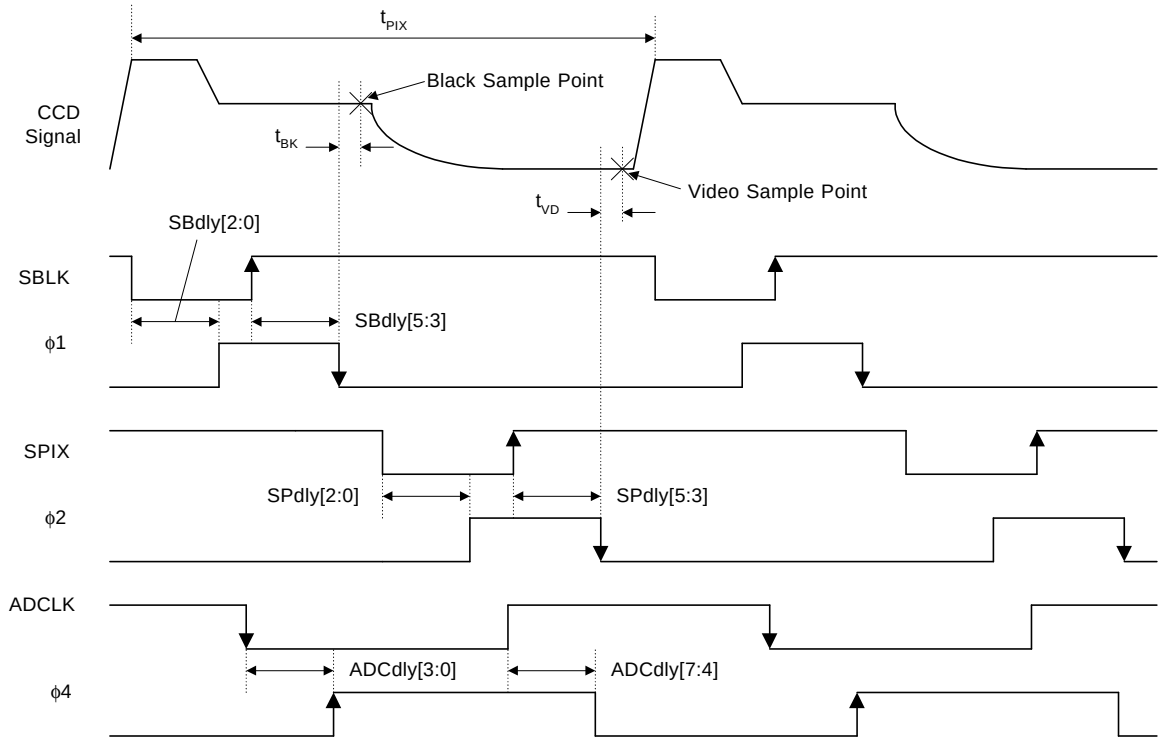


Figure 20. Effects of Aperture Delays with SPIXopt=0 (Default)

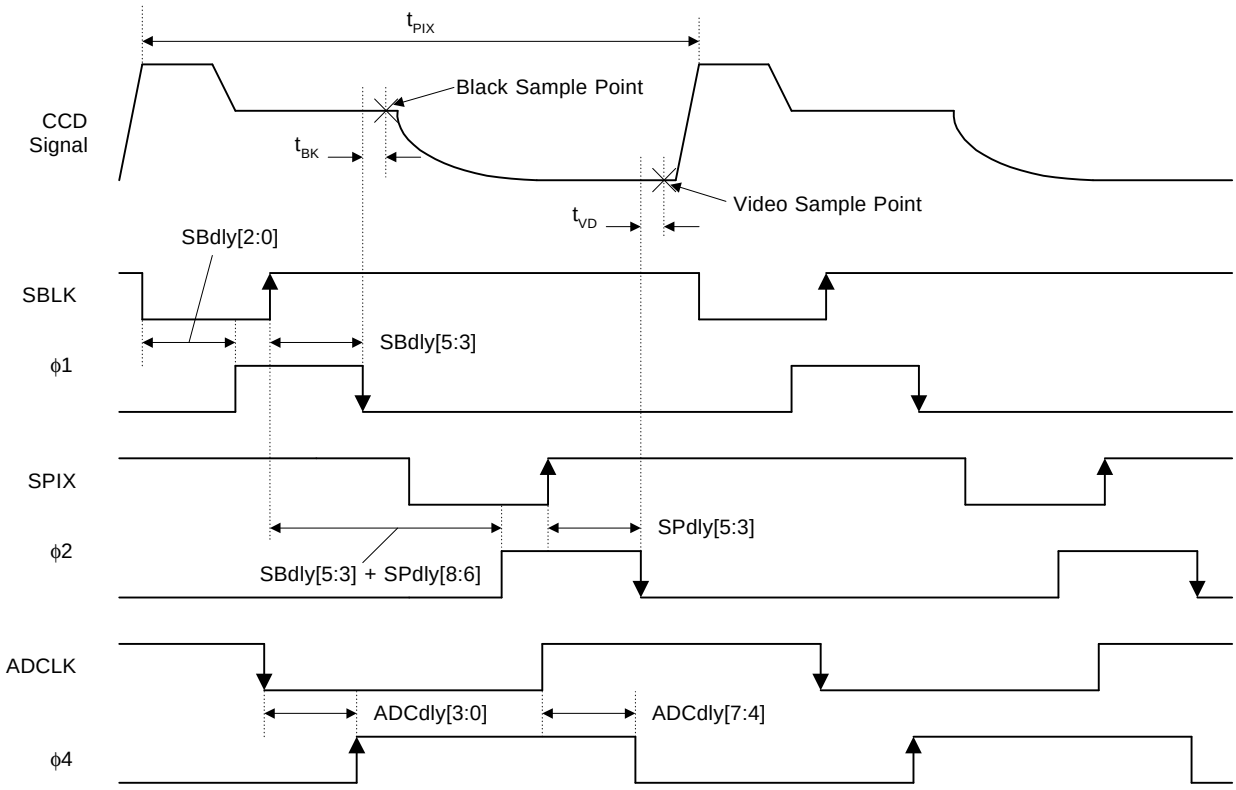


Figure 21. Effects of Aperture Delays with SPIXopt=1

LINE RATE CLOCKS

CLAMP, CAL & PBLK are the three line rate clock signals. There are two modes of operation for these clocks, the CAL & CLAMP mode, and the CALonly mode.

EOS can be a line rate clock as well, but it is only used in the Multiple Gain mode. Please refer to the Multiple Gain mode section for information about EOS.

CAL & CLAMP Mode

CAL & CLAMP is the default line timing mode (CALonly=0). In this mode, the CLAMP signal is used to activate the DC restore Clamp at the CDS input, and the CAL signal is used to define the Optical Black pixels to be used for the Black Level calibration function. Typically the CLAMP pulse comes during the dummy or optical black pixels at the beginning of each scan line, and the CAL pulse comes during the longer string of optical black pixels at the end of each scan line. CLAMP & CAL must not be active at the same time.

CAL-Only (OneShot) Mode

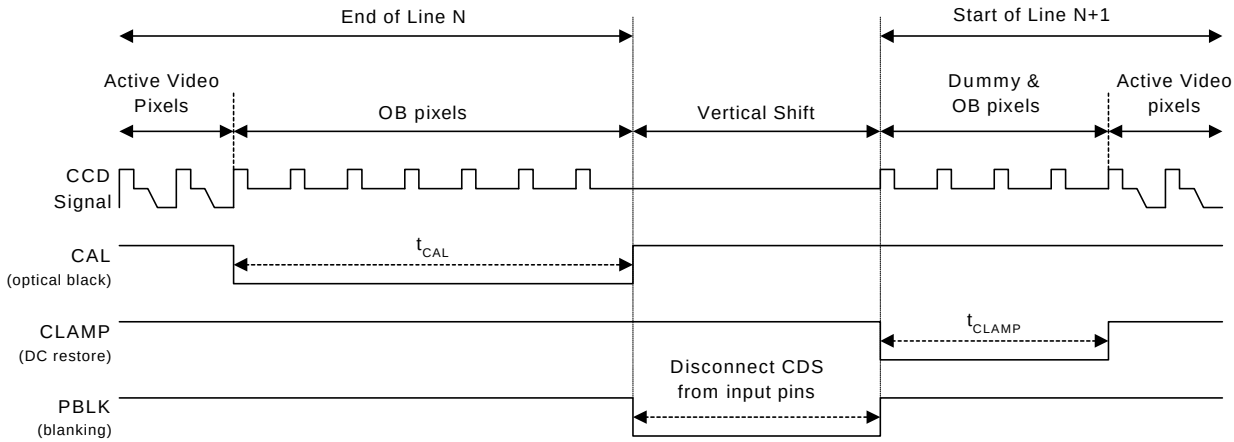
In this mode, the CAL signal is used to activate the DC restore clamp and to define the optical black pixels for calibration. The CAL pulse should frame the longest group of OB pixels at either the end or beginning of each line. The DC restore Clamp switch is turned ON during the first four pixels of each CAL pulse. The remaining pixels under the CAL pulse are used for black level calibration.

Enable the CAL-Only mode by writing a "1" to the "CALonly" bit in the Clock register.

PBLK (Pre-Blanking Clock)

The function of PBLK is the same in both CAL and CLAMP mode and CAL-Only (One Shot) mode. It is used to disconnect the CDS from the CCD input signal during the vertical shift time between CCD lines. If PBLK and CAL overlap, the CAL signal will overide so that black level calibration can take place.

If the DOclamp (digital output clamp) option is enabled, PBLK will also force the digital output bus, DB[11:0], to the value in the Serial Interface Offset register, OB[7:0].



If PBLK overlaps with CAL and/or CLAMP, it will not affect the optical black calibration and DC restore functions. Internally, CAL & CLAMP will overwrite PBLK.

Figure 22. Line Rate Timing with CALonly=0 (CLAMPpol=0, CALpol=0, PBLKpol=0)

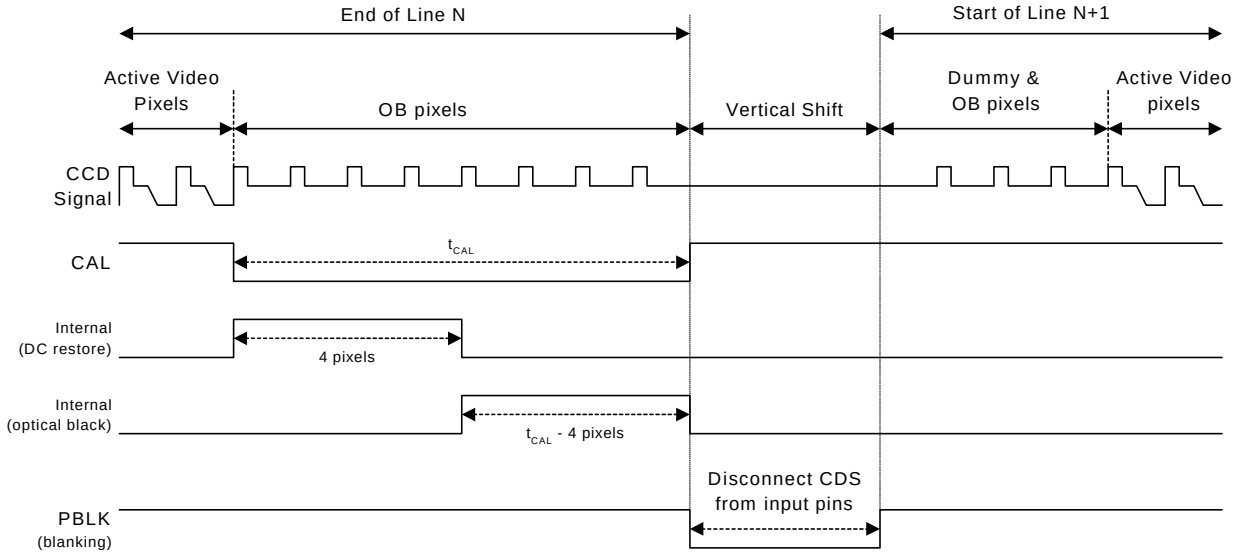


Figure 23. Line Rate Timing with CALonly=1 (CALpol=0, PBLKpol=0)

MULTIPLE GAIN MODE

The Benefits of Multiple Gain Mode

The Multiple Gain mode switches the gain of the Programmable Gain Amplifier (PGA) at the pixel rate. The Multiple Gain logic will switch the PGA gain according to two user defined patterns. Each pattern can be from one to four pixels long.

This allows a color digital camera system to set different PGA (analog) gains for the different color pixels. Most CCDs with RGB Color Filter Arrays (CFA) have weaker signal response for the Blue pixels than for Red or Green pixels. Using the Multiple Gain mode, the Blue pixels can be amplified with higher gain than the Red or Green pixels before being digitized by the ADC. This allows all colors to take advantage of the full ADC resolution.

Enable the Multiple Gain mode by writing a "1" to the "MultGain" bit in the Control register.

Overview of Multiple Gain Mode

The Multiple Gain mode is designed assuming the color filter array is made up of lines (rows) which alternate between two different pixel patterns. We will refer to the two patterns as the Even pattern and the Odd pattern. In a typical camera design using an RGB CFA, the even lines will have Red & Green alternating pixels, while the Odd lines will have Green & Blue alternating pixels. The XRD98L63 allows the patterns to be defined with a single Green gain used on both Even and Odd lines, or with two different Green gains for Even and Odd lines.

There are three main steps to setting up and using the Multiple Gain mode:

1) Select the appropriate Interlaced or Progressive scan clocking mode.
2) Program the Even and Odd Line Pattern registers to match the color filter array used on the CCD.
3) Program the Gain Registers.

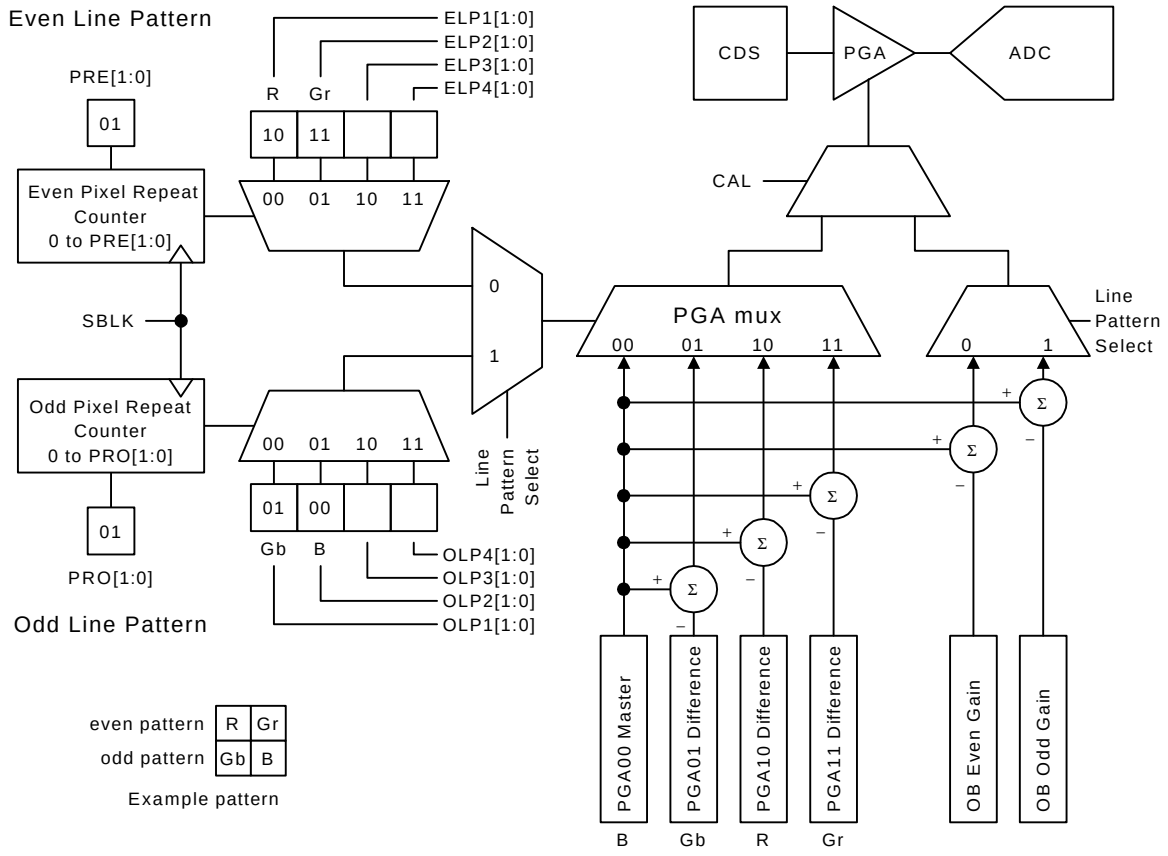


Figure 24. Block Diagram of the Multiple Gain Logic

Select Clocking Mode

The Multiple Gain Mode logic needs to know if the current scan line is using the Even or the Odd line pattern. You will select one of four clocking modes depending on the signals available from your timing generator and whether the CCD is being clocked in a progressive or interlaced mode.

Progressive Scanning
In the Progressive scan mode, the CCD outputs alternating Even and Odd lines. Set MGsel[0]=1.

If your timing generator provides a Line ID signal which is low for Even lines and high for Odd lines, then connect this signal to EOS, pin 18, and set MGsel[1]=0.

If your timing generator does not provide a Line ID signal, then connect EOS (pin 18) to the Horizontal sync signal (typically called HD), connect Fsync (pin 24) to the Vertical Sync signal (typically called VD), and set MGsel[1]=1. This mode uses an internal line counter. At the start of every frame, the Fsync signal resets this counter to the value of the MGstart bit in the Control register. Then on every scan line, the PBLK pulse will toggle the value in the counter.

Interlaced Scanning
In the interlaced scan mode, the CCD outputs all the Even lines during one field, and all the Odd lines during the next field. Set MGsel[0]=0.

If your timing generator provides a Line ID signal which is low for Even lines and high for Odd lines, then connect this signal to EOS, pin 18, and set MGsel[1]=0.

If your timing generator changes the timing relationship of the Vertical and Horizontal sync signals to indicate which fields are Even and which are Odd, then connect EOS (pin 18) to the Horizontal sync signal (typically called HD), connect Fsync (pin 24) to the Vertical Sync signal (typically called VD), and set MGsel[1]=1.

Programming the Line Pattern Registers

Even Line & Odd Line are the Line Pattern registers. Each is divided into 5 parameters. The default values work with RGB CFAs which have Red-Green pixel lines alternating with Green-Blue pixel lines.

PRE[1:0] (Even Line) and PRO[1:0] (Odd Line) are the pixel repeat parameters. The number of pixels in the repeated pattern for Even/Odd lines is selected by programming PRE[1:0]/PRO[1:0] as shown in table 5.

PRE[1] PRO[1]	PRE[0] PRO[0]	Number of pixels in pattern
0	0	1
0	1	2 (default, typ RGB CCD)
1	0	3
1	1	4

Table 7. Pattern Repeat Programming

ELP1[1:0] through ELP4[1:0] are used to define which gain register is used for each pixel in the repeated pattern for Even lines. Each of these 2 bit wide parameters is a pointer to one of the four PGA gain registers. Likewise, OLP1[1:0] through OLP4[1:0] are used to define which gain register is used for each pixel in the repeated pattern for Odd lines.

Programming the Gain Registers

The Multiple Gain mode can switch between any of four different PGA gains. In a typical digital camera, using a CCD with a standard RGB CFA, the Even lines will use 2 gains and the Odd line will used 2 gains.

The Multiple Gain logic includes 6 gain registers.

PGA00 is the 10-bit wide, Master Gain register. It should be assigned to the color which will require the highest gain (usually this is Blue).

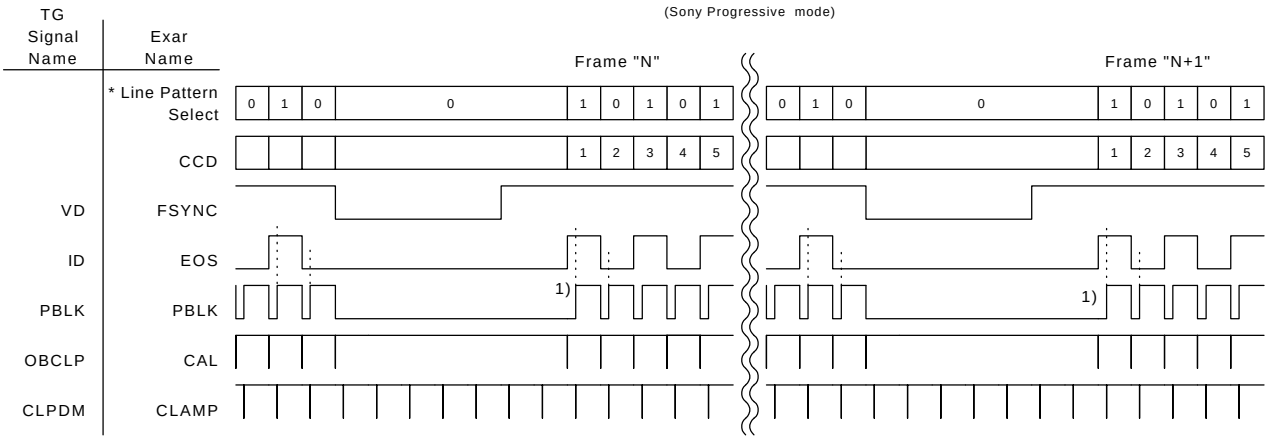
PGA01, PGA10, & PGA11 are the 9-bit wide Gain Difference registers. The value programmed into any of these registers is first subtracted from the value in the PGA00 register before being sent to the analog PGA.

OBE (OB Even) and OBO (OB Odd) are also 9-bit wide Gain Difference registers. These registers are used to set the gain applied to the Optical Black pixels during Black Level Calibration.

As described in the Programmable Gain Amplifier section, the PGA is programmed on a dB scale, where 1 LSB = 0.047 dB. A constant gain difference on a dB scale is a constant gain ratio on a linear scale.

This system of a Master Gain register along with multiple Gain Difference registers on a dB scale, allows a camera system to set the desired gain ratios between all the different colors. Then, the camera can write values to the Master Gain register (to compensate for changes in the ambient light level), and the gains of all the other colors will automatically be adjusted to maintain the desired gain ratios.

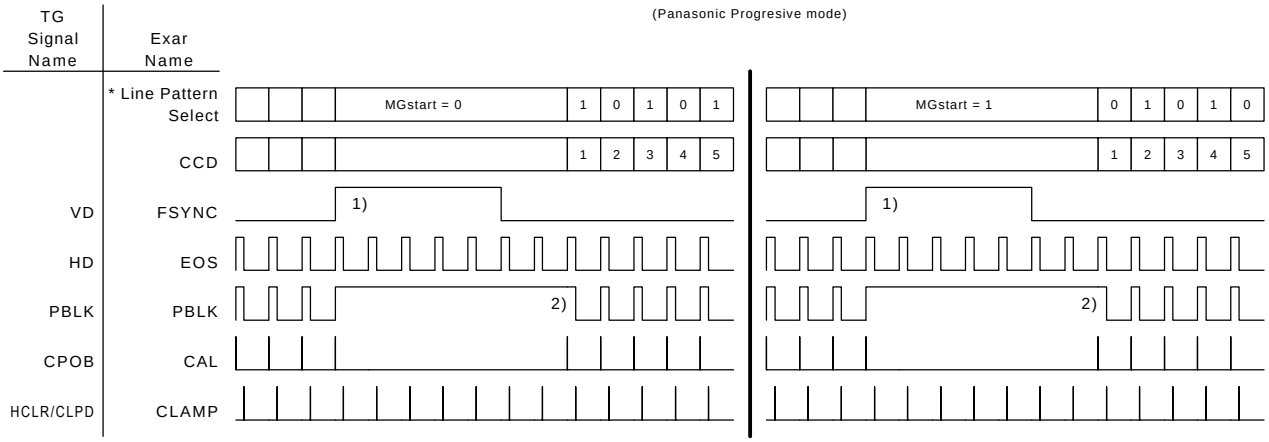
MGsel	Functions
00	Sony Interlaced
01	Sony Progressive
10	Panasonic Interlaced
11	Panasonic Progressive



CONDITIONS: FSYNCpol=0, PBLKpol=0, CALpol=0, CLAMPpol=0, EOSpol=1
* Internal signals

1) PBLK latches EOS value into Line Pattern Select.

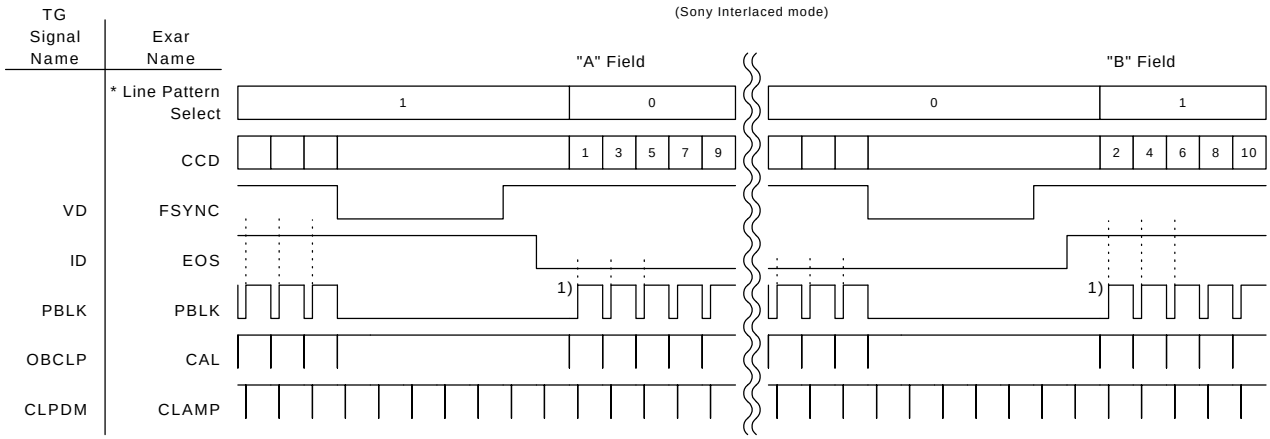
Figure 25. Multiple Gain Mode Timing, Progressive, MGsel[1:0] = 01



CONDITIONS: FSYNCpol=1, PBLKpol=1, CALpol=1, CLAMPpol=1, EOSpol=1
* Internal signals

1) FSYNC resets Line Pattern Select to "MGstart" bit value.
2) PBLK toggles Line Pattern Select value.

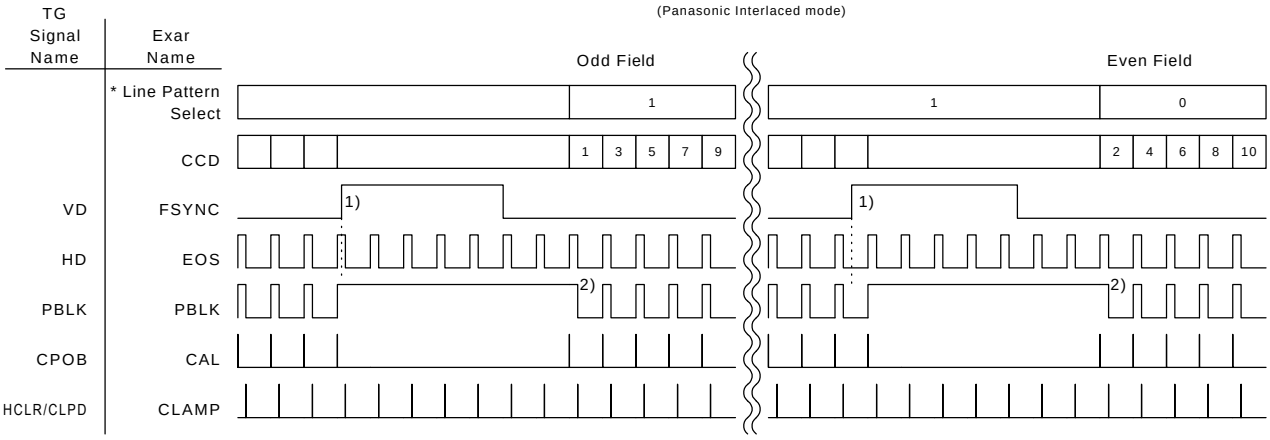
Figure 26. Multiple Gain Mode Timing, Progressive, MGsel[1:0] = 11



CONDITIONS: FSYNCpol=0, PBLKpol=0, CALpol=0, CLAMPpol=0, EOSpol=1
* Internal signals

1) PBLK latches EOS value into Line Pattern Select.

Figure 27. Multiple Gain Mode Timing, Interlaced, MGsel[1:0] = 00



CONDITIONS: FSYNCpol=1, PBLKpol=1, CALpol=1, CLAMPpol=1, EOSpol=1
* Internal signals

1) FSYNC latches EOS value.
2) PBLK updates Line Pattern Select to the latched EOS value.

Figure 28. Multiple Gain Mode Timing, Interlaced, MGsel[1:0] = 10

OTHER CHIP CONTROLS & FEATURES

Chip Power Down

The Power Down mode can be activated by forcing the PD pin high, or by writing a "1" to the CHIPpd bit in the Control register. For normal operation, the PD pin must be low and the CHIPpd bit must be "0". In the Power Down mode, all analog circuits are turned off, and the output bus, DB[11:0], is put in the high impedance mode. All the digital registers retain their values, so the PGA gain, offset, and calibration will return to their previous states. The serial interface pins remain active in the Power Down mode. The PD pin and the CHIPpd bit do not reset any internal registers.

In addition to the CHIPpd bit, there are two other power down bits which only turn off portions of the chip. AFEpd controls the CDS & PGA circuits. ADCpd controls the ADC. AFEpd & ADCpd are included for factory test and characterization purposes, they are not intended for use in digital camera applications.

Digital Output Enable Control

The ADC digital output bus, DB[11:0], has 3-state capability. When the OE bit in the control register is high, and the $\overline{OE}$ Pin (pin 42) is low, the digital output drivers are enabled and active. When the OE bit is low, or the $\overline{OE}$ pin is high, the digital output drivers are disabled and the bus is in the high impedance state.

The OE bit and $\overline{OE}$ pin only control the digital output drivers, all other circuits on the chip will remain active. The black level calibration can still run properly when the outputs are in the high impedance state.

Chip Reset

The chip includes a Power-On-Reset function (POR), so when the power supplies are turned on, the chip will always power up with default values in all registers.

There are two methods to force a chip reset. The first is to write a "1" to the RESET bit in the reset register. This will reset the chip, and after a delay of about 10 ns, the reset bit will automatically clear itself. The second reset method is to force the $\overline{RESET}$ pin (pin # 43) low. This will reset the chip until the $\overline{RESET}$ pin goes high again. The $\overline{RESET}$ pin has an internal pull up.

Minimum Clip

The Minimum Clip feature helps reduce noise in black areas of a digitized image by clipping ADC output data, such that the minimum code out is the code programmed in to the Offset register, OB[7:0].

When MinClip=1 (the default condition), the digital output data will be clipped such that:

$$DB[11:0] \geq OB[7:0]$$

This feature does not clip the data used by the internal Black level Calibration Logic.

Digital Output Clamp

The PBLK (Pre-Blanking) clock is used to disconnect the CDS inputs from the CCD signal during vertical shift time. When DOclamp=1 (the default condition), PBLK is also used to force the digital output data to the code stored in the Offset register, OB[7:0].

If (DOclamp=1) AND (PBLK=active)
THEN DB[11:0] = OB[7:0]

Setting Power and Performance with Rext

The power and performance levels of the XRD98L63 are set by the value of Rext. Rext sets the current bias level for the entire chip. Rext is connected between pin 37 (BiasRes) and analog ground (see Figure 29). This resistor should be placed as close as possible to the pin and routed directly to a ground plane in a PCB layout. A surface mount carbon resistor is recommended.

Increasing the value of Rext will decrease the power, linearity and noise performance of the XRD98L63. Reducing the value of Rext will improve the linearity and noise performance while increasing power. The tested default value for Rext is 18.2KΩ.

In order to match system to system performance and set consistent manufacturable performance levels between cameras, it is recommended that the Rext resistor have <1% tolerance.

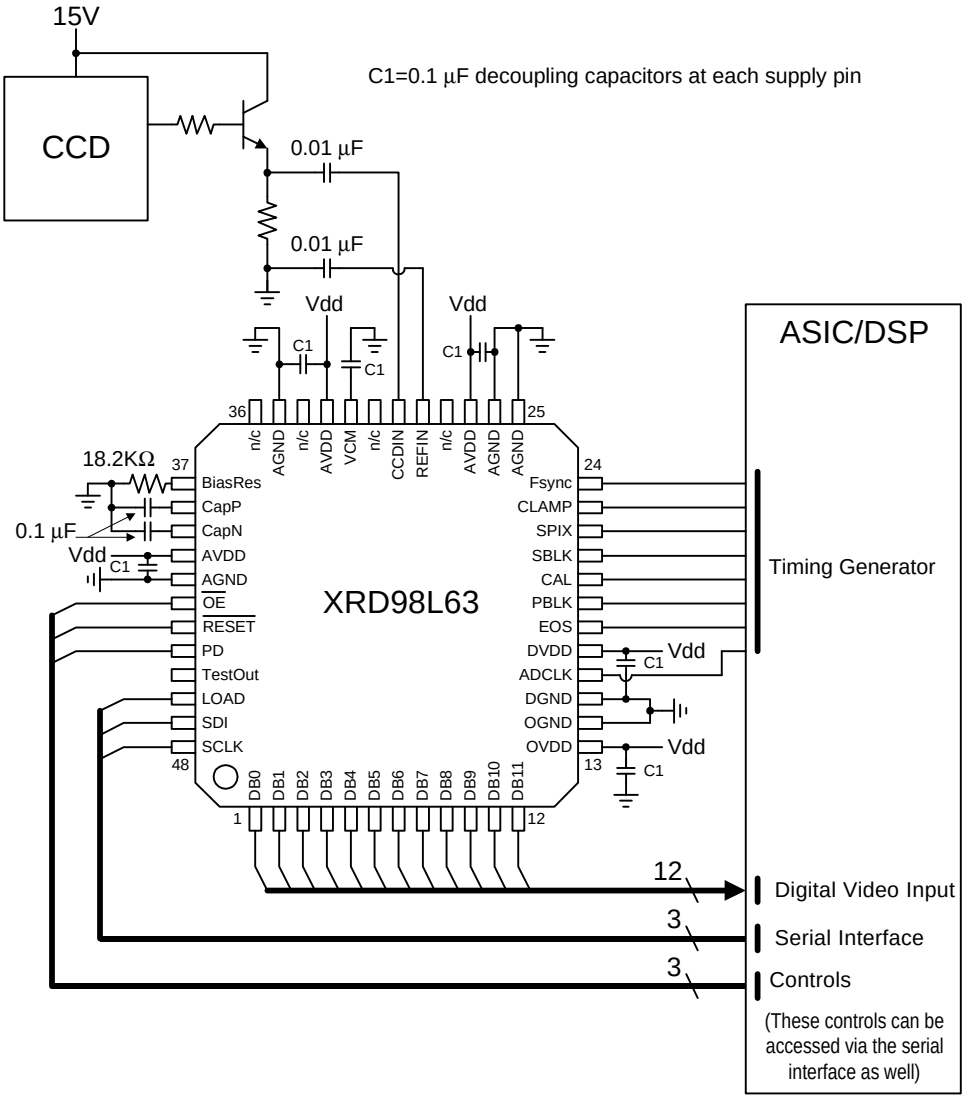


Figure 29. Application Schematic

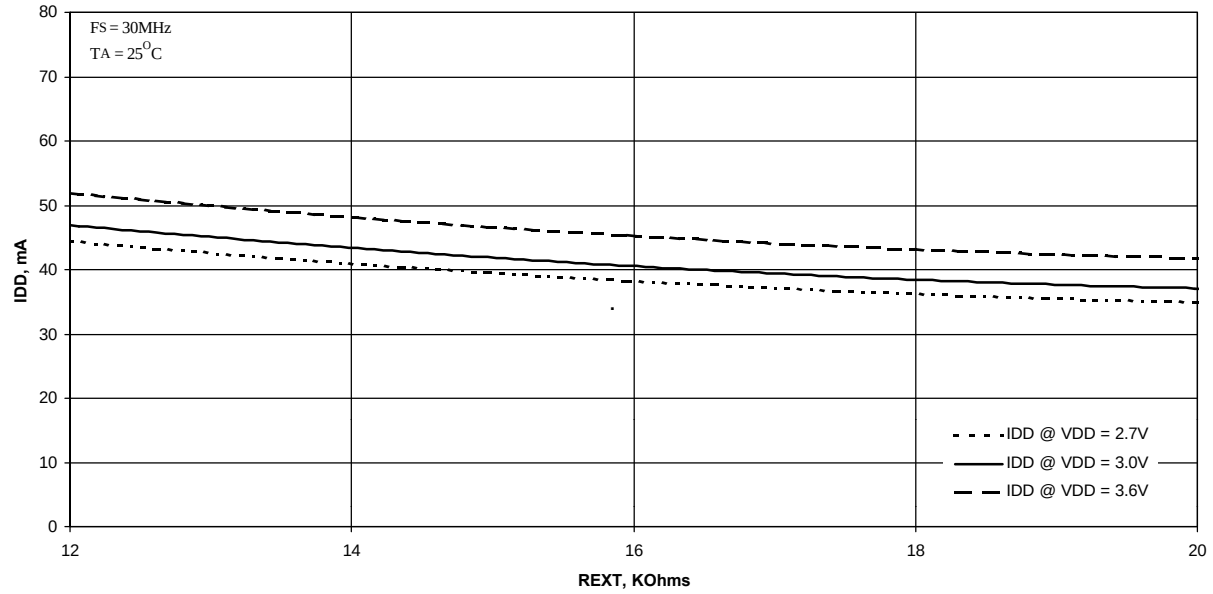


Figure 30. IDD vs Rext

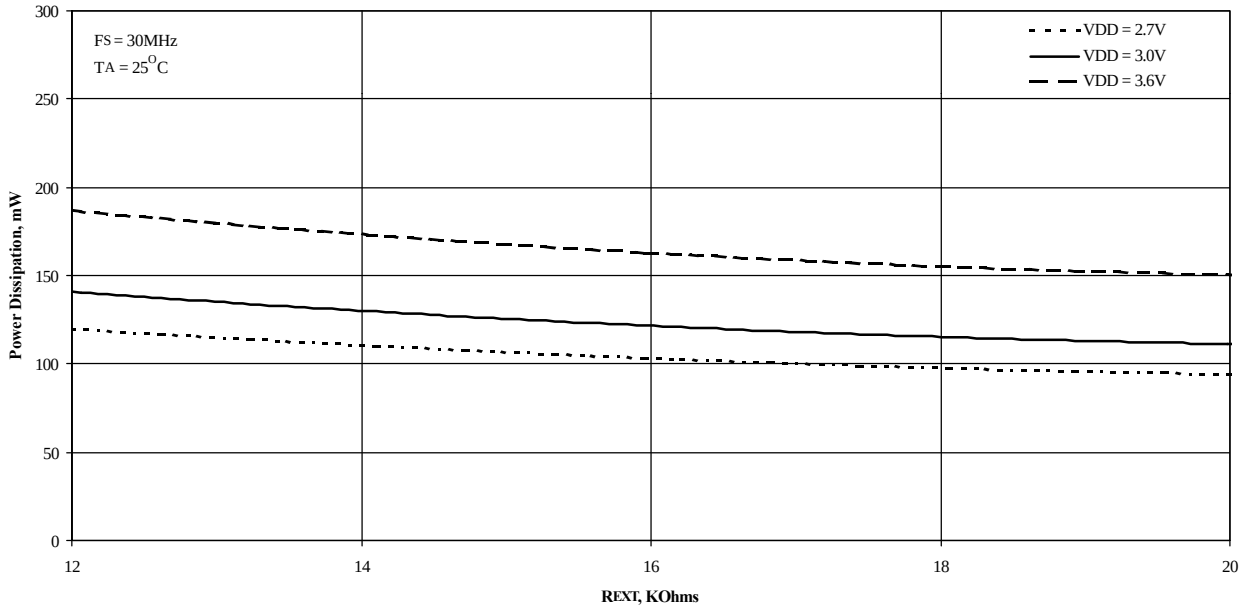


Figure 31. Power Dissipatin vs Rext

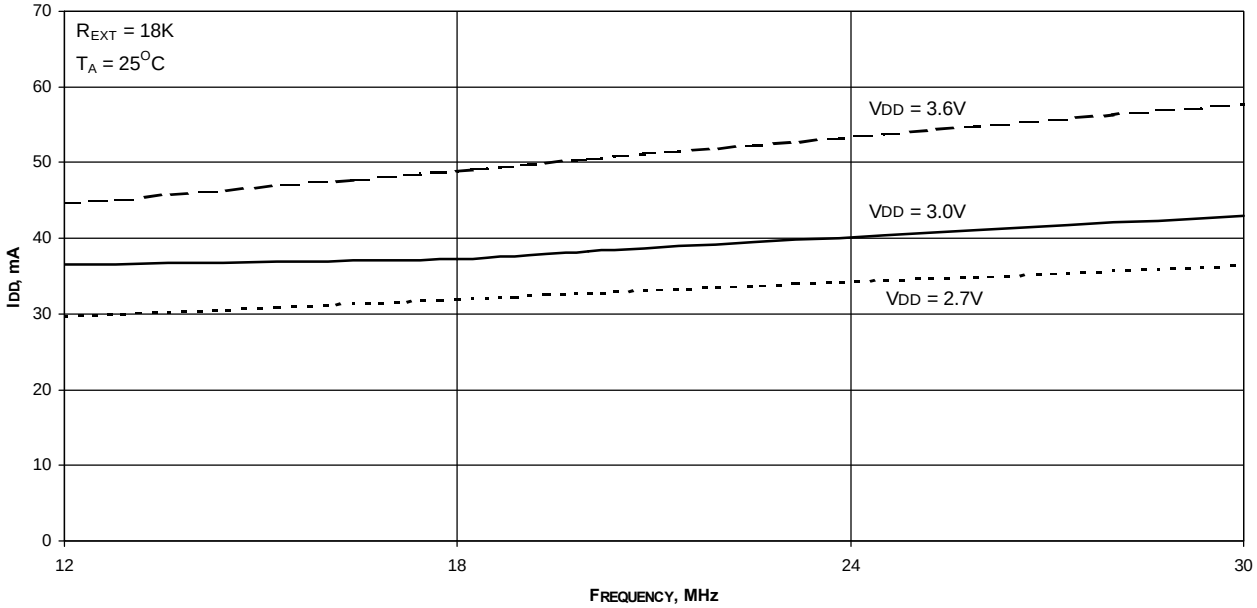


Figure 32. IDD vs Frequency

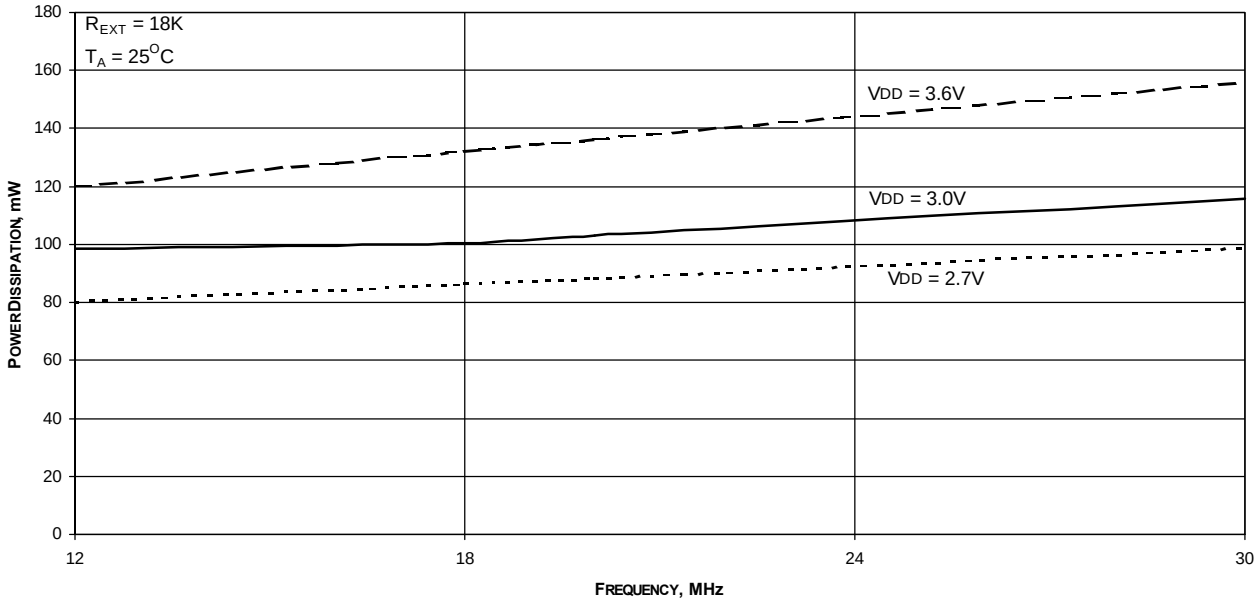


Figure 33. Power Dissipation vs Frequency

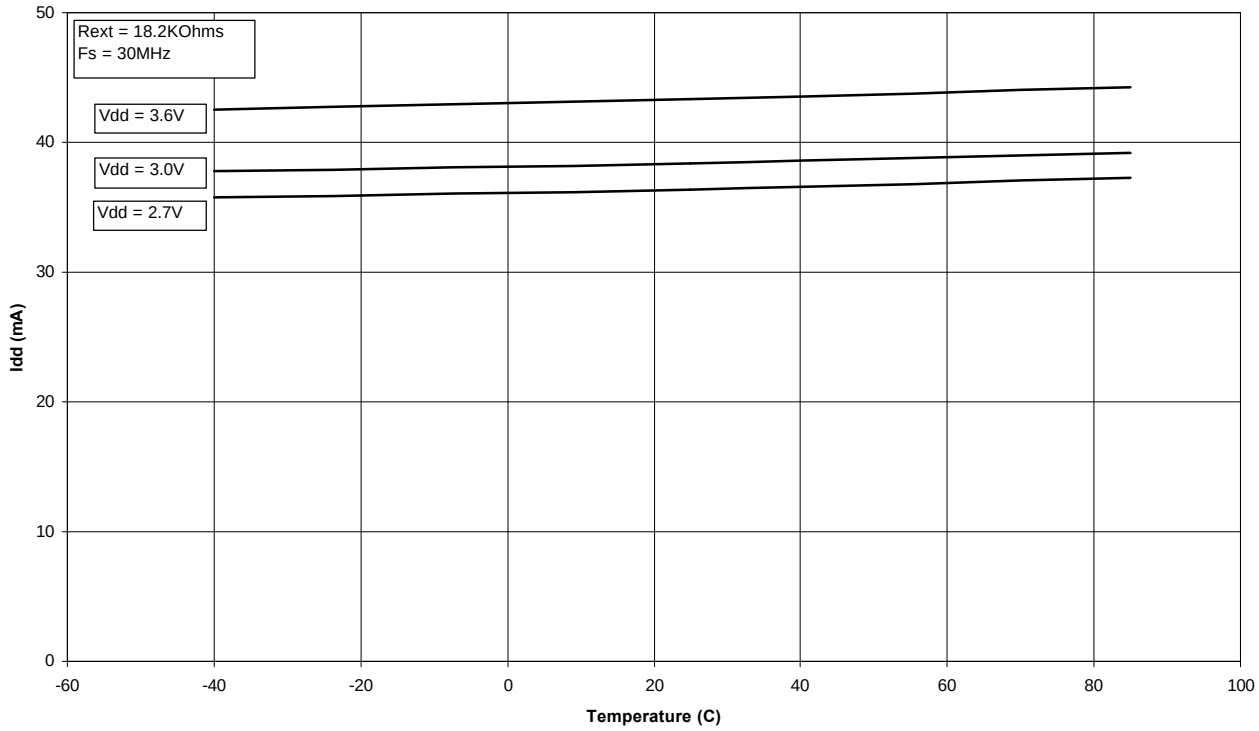


Figure 34. IDD vs Temperature

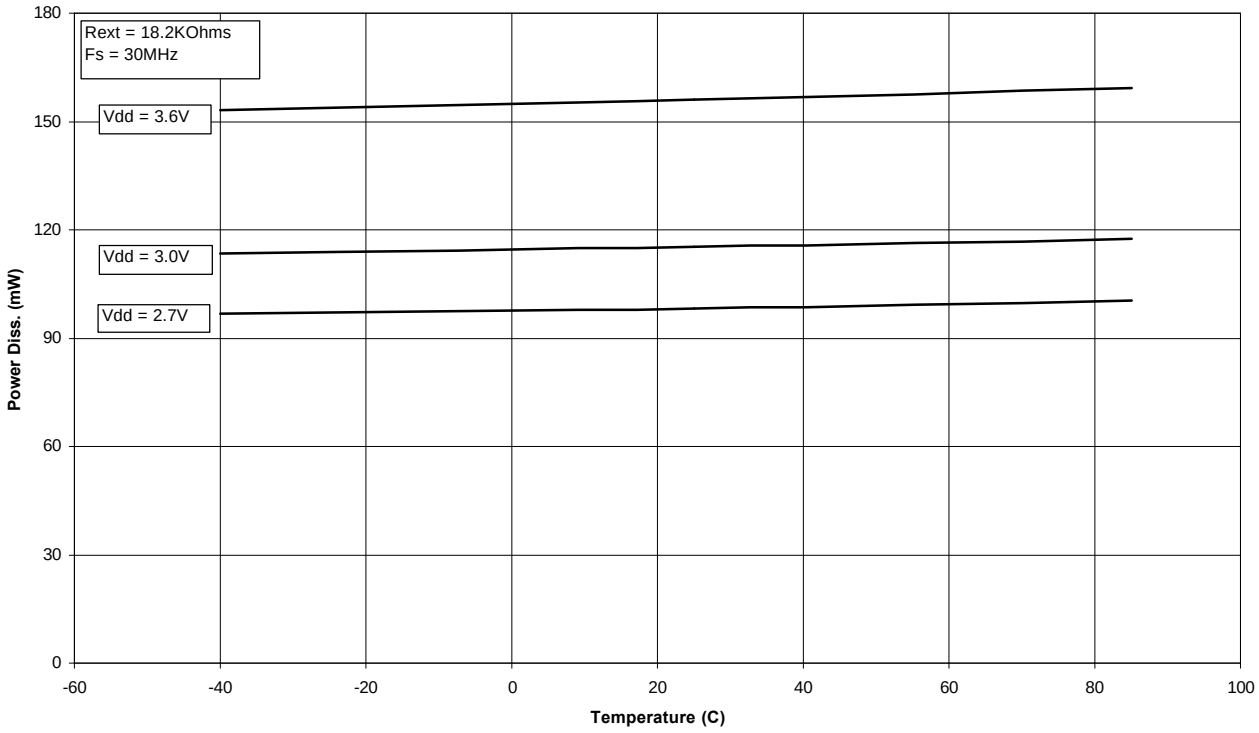


Figure 35. Power Dissipation vs Temperature

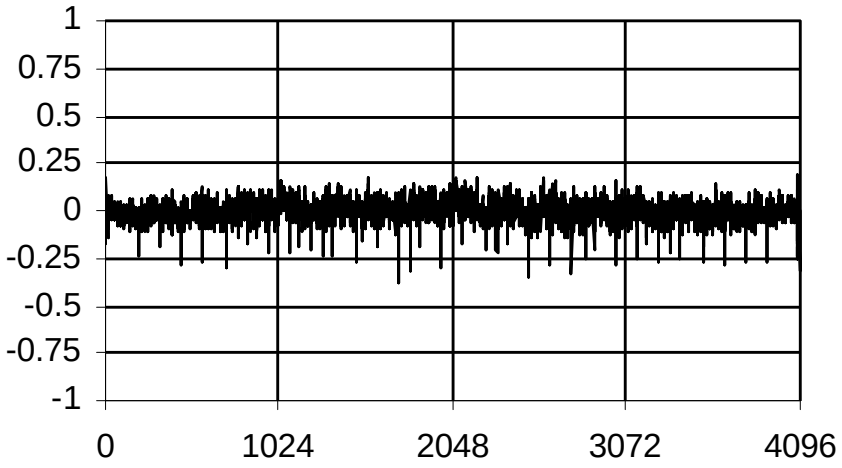


Figure 36. System DNL

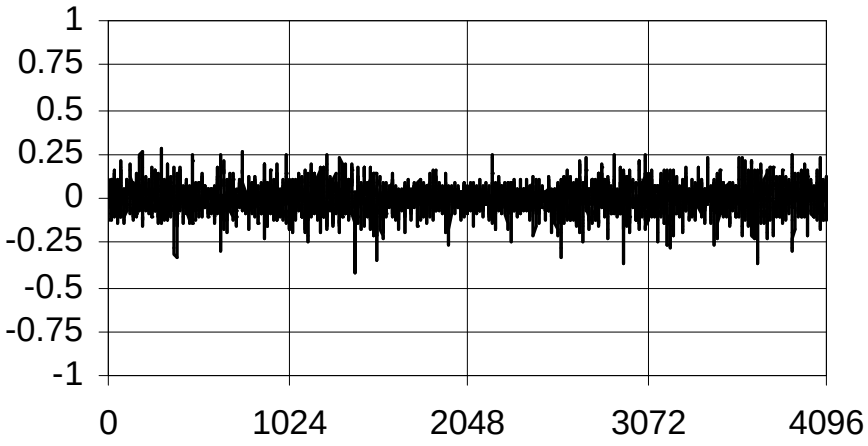
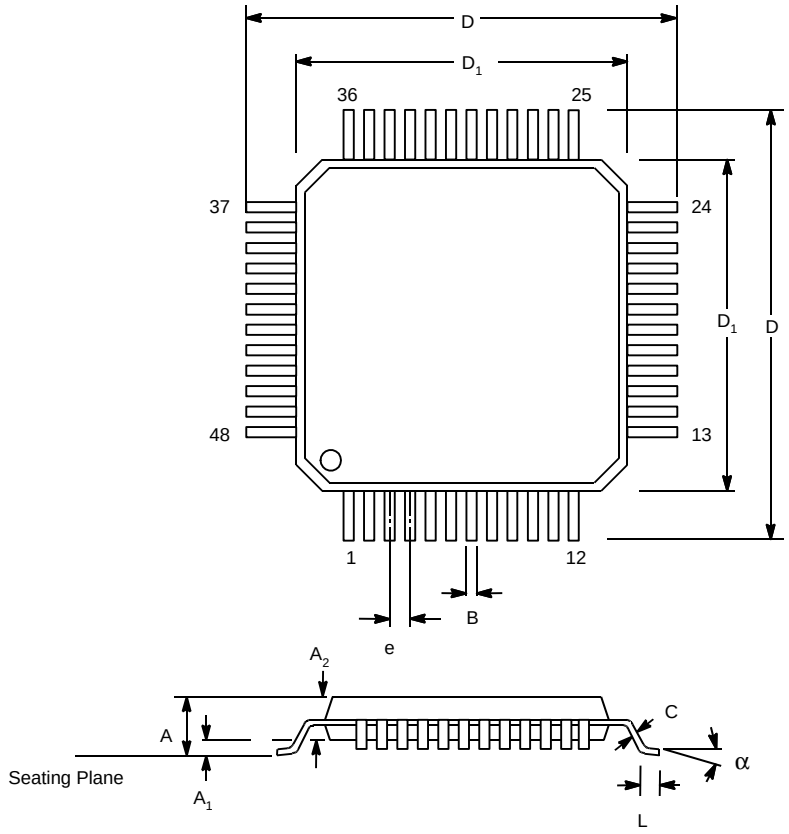


Figure 37. ADC DNL

48 LEAD THIN QUAD FLAT PACK

(7 x 7 x 1.4 mm TQFP)

REV. 2.00



	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.055	0.063	1.4	1.6
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.2
D	0.346	0.362	8.8	9.2
D_1	0.272	0.28	6.9	7.1
e	0.020 BSC		0.50 BSC	
L	0.018	0.03	0.45	0.75
a	0°	7°	0°	7°

Note: *The control dimension is the millimeter column*

NOTICE

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