1 Pin configuration

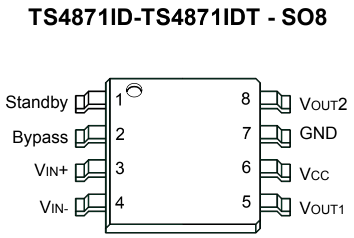


Figure 1. Pin connections (top view)

2 Maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_i	Input voltage (2)	GND to V_{CC}	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction-to-ambient (3) SO8	175	°C/W
	Thermal resistance junction-to-ambient (3) MiniSO8	215	
P_d	Power dissipation	Internally limited (4)	
ESD	Human body model	2	kV
ESD	Machine model	200	V
Latch-up	Latch-up immunity	Class A	
	Lead temperature (soldering, 10 s)	260	°C

1. *All voltages values are measured with respect to the ground pin.*
2. *The magnitude of input signal must never exceed V_{CC} + 0.3 V / GND - 0.3 V*
3. *The device is protected in case of overtemperature by a thermal shutdown active @ 150 °C.*
4. *Exceeding the power derating curves during a long period, involves abnormal operating conditions.*

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.5 to 5.5	V
V_{ICM}	Common mode Input voltage range	GND to V_{CC} - 1.2 V	V
V_{STB}	Standby voltage input: device ON	GND ≤ V_{STB}≤ 0.5 V	V
	Standby voltage input: device OFF	V_{CC} - 0.5 V ≤ V_{STB} ≤ V_{CC}	
R_L	Load resistor	4 - 32	Ω
R_{thja}	Thermal resistance junction-to-ambient (1) SO8	150	°C/W
	Thermal resistance junction-to-ambient (1) MiniSO8	190	

1. *This thermal resistance can be reduced with a suitable PCB layout (see power derating curves).*

3 Electrical characteristics

Table 3. **Electrical characteristics V_{CC} = +5 V, GND = 0 V, T_{amb} = 25 °C (unless otherwise specified).**

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		6	8	mA
$I_{STANDBY}$ [(1)]	Standby current No input signal, V_{STDBY} = V_{CC}, R_L = 8 Ω		10	1000	nA
V_{OO}	Output offset voltage No input signal, R_L = 8 Ω		5	20	mV
P_O	Output power THD = 1% max., f = 1 kHz, R_L = 8 Ω		1		W
THD + N	Total harmonic distortion + noise P_O = 250 mW_{rms}, Gv = 2, 20 Hz < f < 20 kHz, R_L = 8 Ω		0.15		%
PSRR [(2)]	Power supply rejection ratio f = 217 Hz, R_L = 8 Ω, R_{Feed} = 22 K V_{ripple} = 200 mV_{rms}		75		dB
ϕ_M	Phase margin at unity gain R_L = 8 Ω, C_L = 500 pF		70		Degrees
GM	Gain margin R_L = 8 Ω, C_L = 500 pF		20		dB
GBP	Gain bandwidth product R_L = 8 Ω		2		MHz

1. *Standby mode is actived when Vstdby is tied to V_{CC}.*
2. *Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the surimposed sinus signal to V_{CC} @ f = 217 Hz.*

Table 4. **Electrical characteristics V_{CC} = +3.3 V, GND = 0 V, T_{amb} = 25 °C (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		5.5	8	mA
$I_{STANDBY}$ (1)	Standby current No input signal, V_{STDBY} = V_{CC}, R_L = 8 Ω		10	1000	nA
V_{OO}	Output offset voltage No input signal, R_L = 8 Ω		5	20	mV
P_O	Output power THD = 1% max., f = 1 kHz, R_L = 8 Ω		450		mW
THD + N	Total harmonic distortion + noise P_O = 250 mW_{rms}, Gv = 2, 20 Hz < f < 20 kHz, R_L = 8		0.15		%
PSRR (2)	Power supply rejection ratio f = 217 Hz, R_L = 8 Ω, R_{Feed} = 22 kΩ V_{ripple} = 200 mV_{rms}		75		dB
ϕ_M	Phase margin at unity gain R_L = 8 Ω, C_L = 500 pF		70		Degrees
GM	Gain margin R_L = 8 Ω, C_L = 500 pF		20		dB
GBP	Gain bandwidth product R_L = 8 Ω		2		MHz

1. *Standby mode is actived when V_{stdby} is tied to V_{CC}*
2. *Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the surimposed sinus signal to V_{CC} @ f = 217 Hz*

Note: *All electrical values are made by correlation between 2.6 V and 5 V measurements.*

Table 5. **Electrical characteristics V_{CC} = +2.6 V, GND = 0 V, T_{amb} = 25 °C (unless otherwise specified).**

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		5.5	8	mA
$I_{STANDBY}$ (1)	Standby current No input signal, V_{STDBY} = V_{CC}, R_L = 8 Ω		10	1000	nA
V_{OO}	Output offset voltage No input signal, R_L = 8 Ω		5	20	mV
P_O	Output power THD = 1% max.., f = 1 kHz, R_L = 8 Ω		260		mW
THD + N	Total harmonic distortion + noise P_O = 250 mW_{rms}, Gv = 2, 20 Hz < f < 20 kHz, R_L = 8 Ω		0.15		%
PSRR (2)	Power supply rejection ratio f = 217 Hz, R_L = 8 Ω, R_{Feed} = 22 kΩ, V_{ripple} = 200 mV_{rms}		75		dB

Symbol	Parameter	Min.	Typ.	Max.	Unit
ϕ_M	Phase margin at unity gain R_L = 8 Ω, C_L = 500 pF		70		Degrees
GM	Gain margin R_L = 8 Ω, C_L = 500 pF		20		dB
GBP	Gain bandwidth product R_L = 8 Ω		2		MHz

1. *Standby mode is actived when Vstdby is tied to V_{CC}*
2. *Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the surimposed sinus signal to V_{CC} @ f = 217 Hz*

Table 6. Bill of material

Components	Functional description
R_{in}	Inverting input resistor which sets the closed loop gain in conjunction with R_{feed}. This resistor also forms a high pass filter with C_{in} [f_c = 1 / (2 x P_i x R_{in} x C_{in})]
C_{in}	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal
R_{feed}	Feed back resistor which sets the closed loop gain in conjunction with Rin
C_s	Supply bypass capacitor which provides power supply filtering
C_b	Bypass pin capacitor which provides half supply filtering
C_{feed}	Low pass filter capacitor allowing to cut the high frequency [low pass filter cut-off frequency 1 / (2 x P_i x R_{feed} x C_{feed})]
R_{stb}	Pull-up resistor which fixes the right supply level on the standby pin
G_v	Closed loop gain in BTL configuration = 2 x (R_{feed} / R_{in})

Remarks

1. All measurements, except PSRR measurements, are made with a supply bypass capacitor C_s = 100 µF.
2. External resistors are not needed for having better stability when supply @ V_{CC} down to 3 V. By the way, the quiescent current remains the same.
3. The standby response time is about 1 µs.

4 Electrical characteristics curves

Figure 2. Open loop frequency response Vcc=5 V

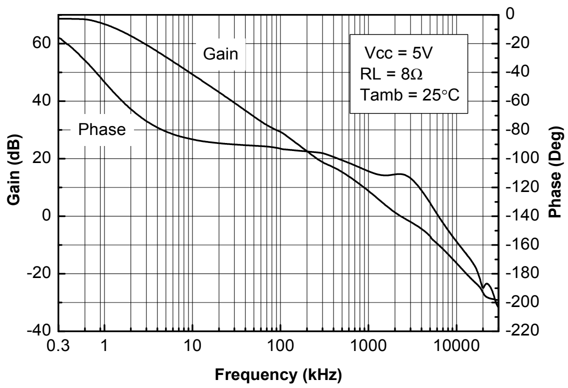


Figure 3. Open loop frequency response ZL=8 Ω

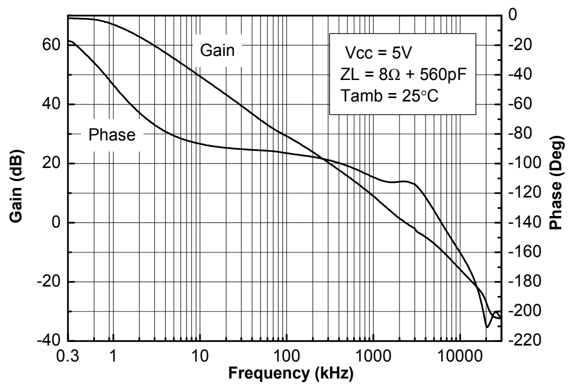


Figure 4. Open loop frequency response Vcc=3.3 V

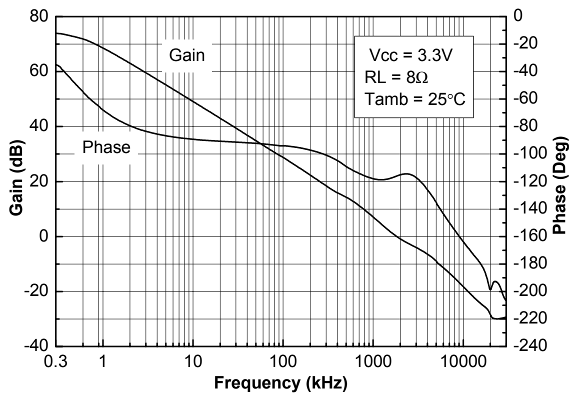


Figure 5. Open loop frequency response Vcc=3.3 V, ZL=8 Ω

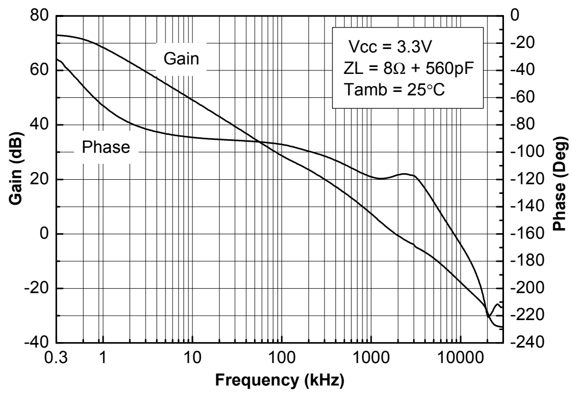


Figure 6. Open loop frequency response Vcc=2.6 V

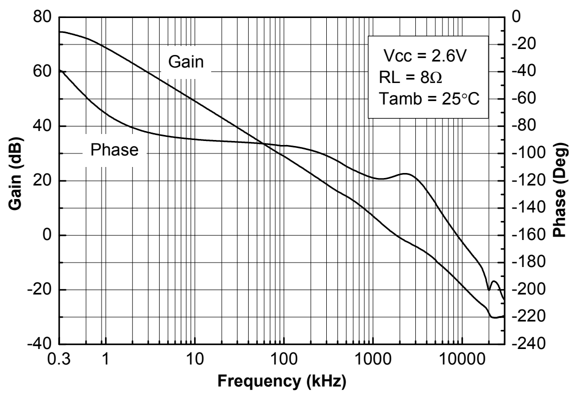


Figure 7. Open loop frequency response Vcc=2.6 V, ZL=8 Ω

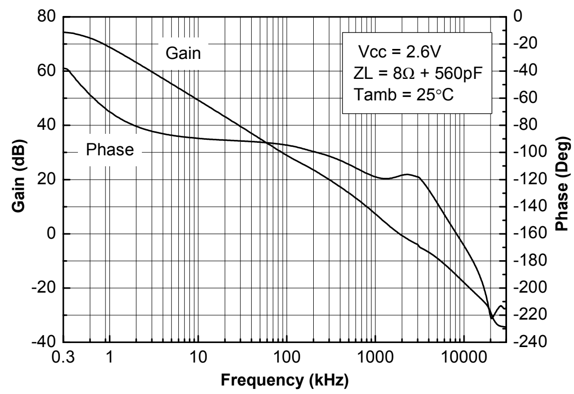


Figure 8. Open loop frequency response Vcc=5 V, CL=560 pF

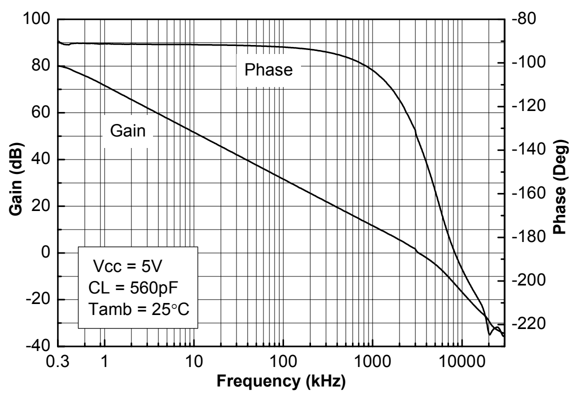


Figure 9. Open loop frequency response Vcc=3.3 V, CL=560 pF

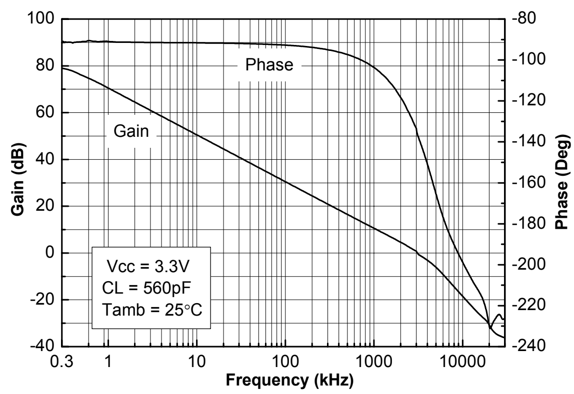


Figure 10. Open loop frequency response Vcc=2.6 V, CL=560 pF

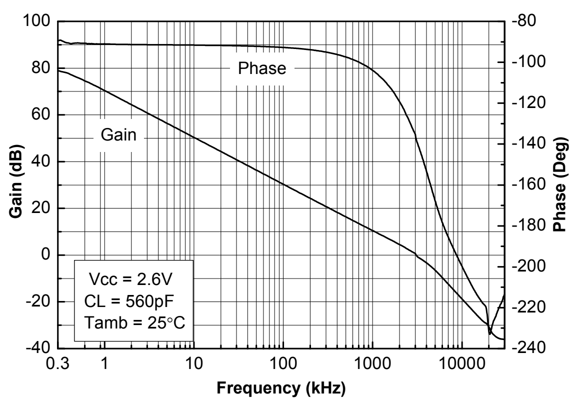


Figure 11. Power supply rejection ratio (PSRR) vs power supply

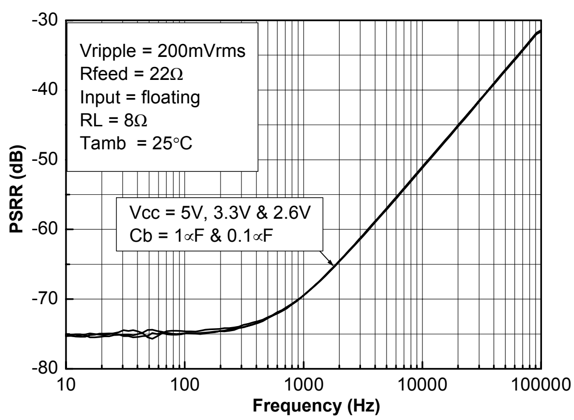


Figure 12. Power supply rejection ratio (PSRR) vs feedback capacitor

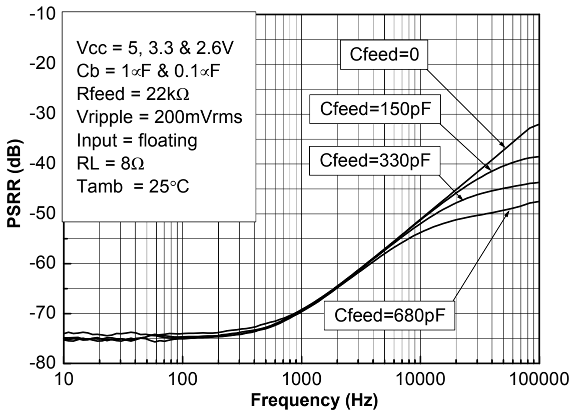


Figure 13. Power supply rejection ratio (PSRR) vs bypass capacitor

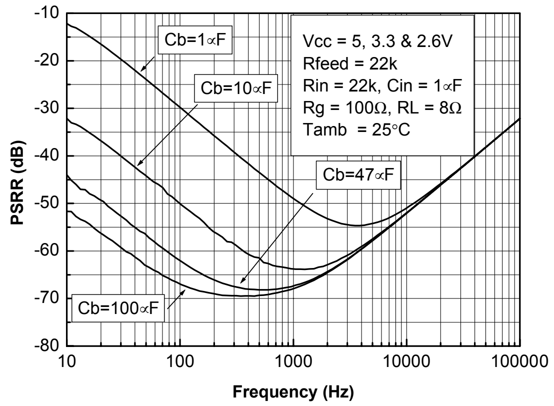


Figure 14. Power supply rejection ratio (PSRR) vs input capacitor

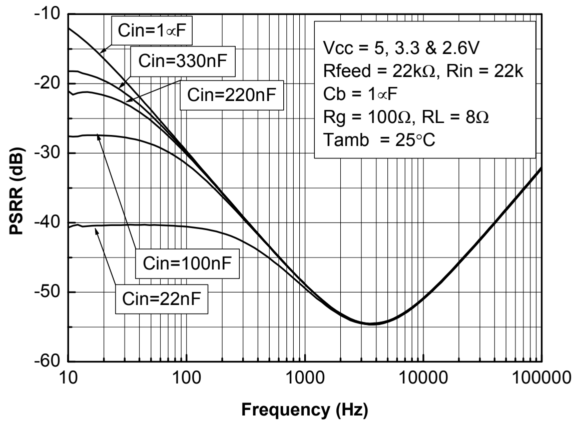


Figure 15. Power supply rejection ratio (PSRR) vs feedback resistor

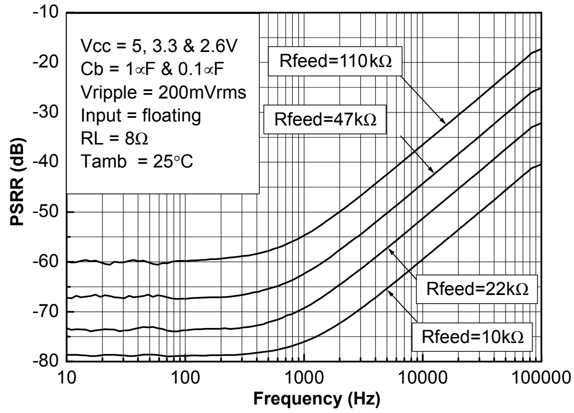


Figure 16. **Pout @ THD + N = 1% vs supply voltage vs RL**

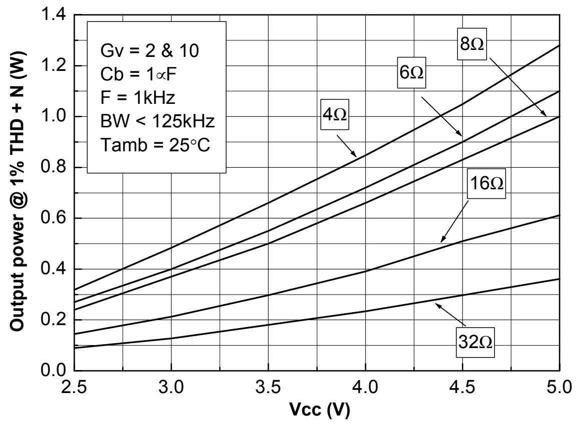


Figure 17. **Pout @ THD + N = 10% vs supply voltage vs RL**

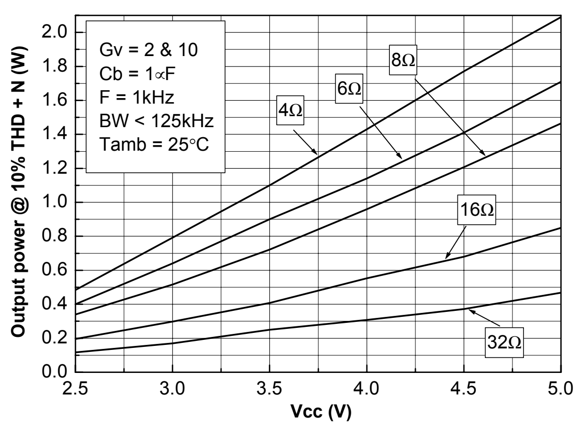


Figure 18. **Power dissipation vs Pout Vcc=5 V**

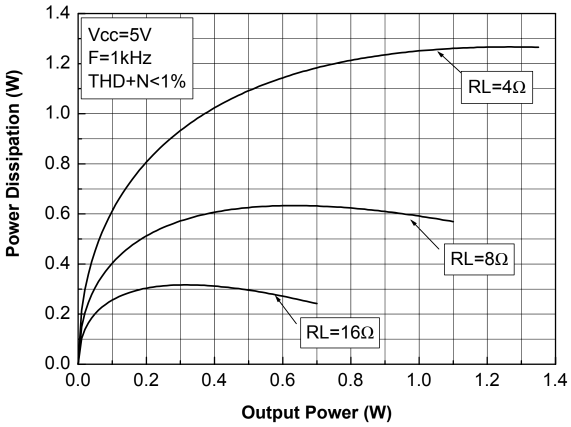


Figure 19. **Power dissipation vs Pout Vcc=3.3 V**

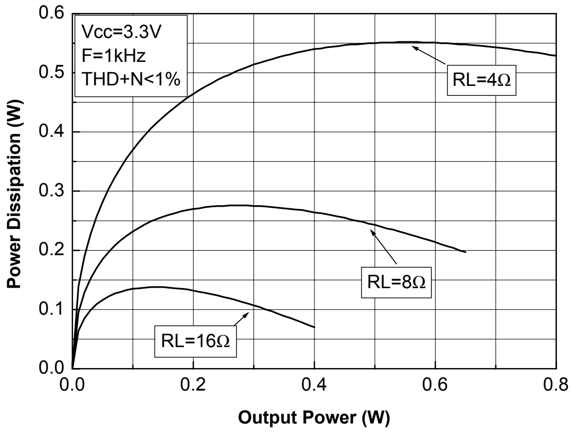


Figure 20. **Power dissipation vs Pout Vcc=2.6 V**

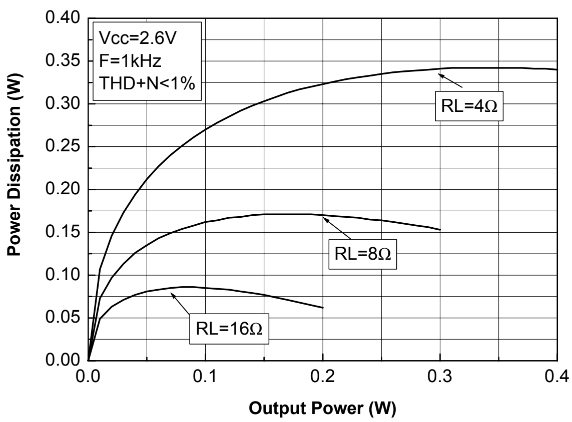


Figure 21. **Power derating curves**

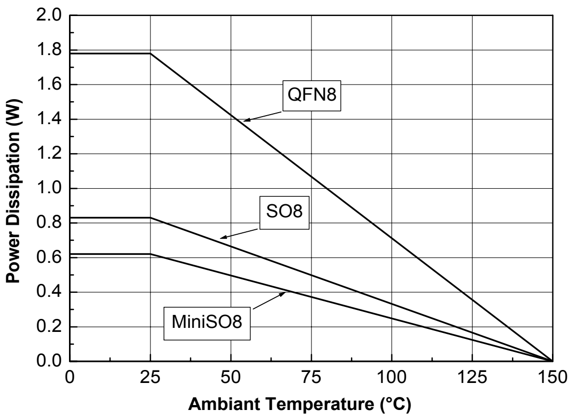


Figure 22. **THD + N vs output power Gv=2, Vcc= 5 V**

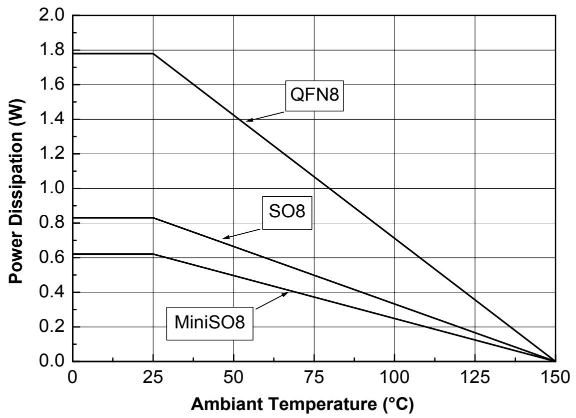


Figure 23. **THD + N vs output power Gv=10, Vcc =5 V**

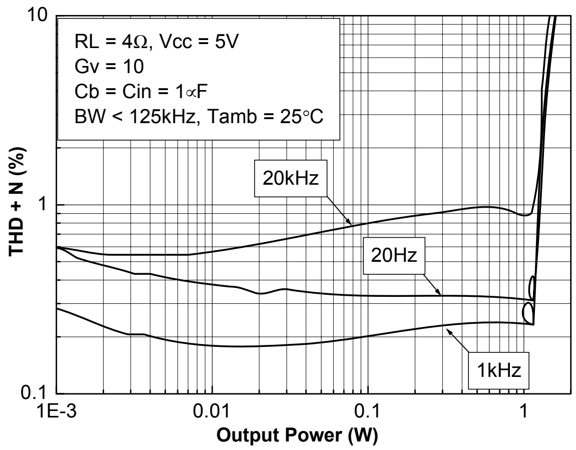


Figure 24. **THD + N vs output power Gv=2, Vcc = 3.3 V**

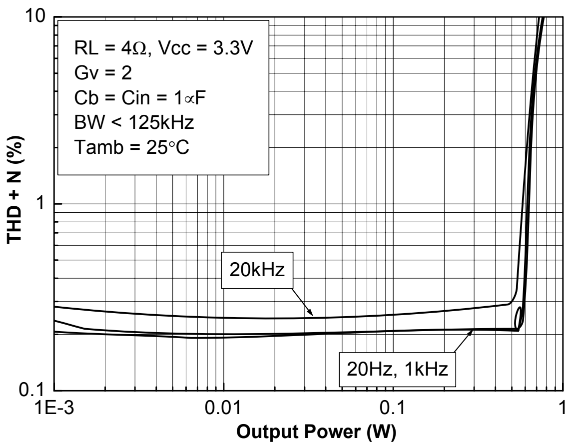


Figure 25. **THD + N vs output power Gv=10, Vcc = 3.3 V**

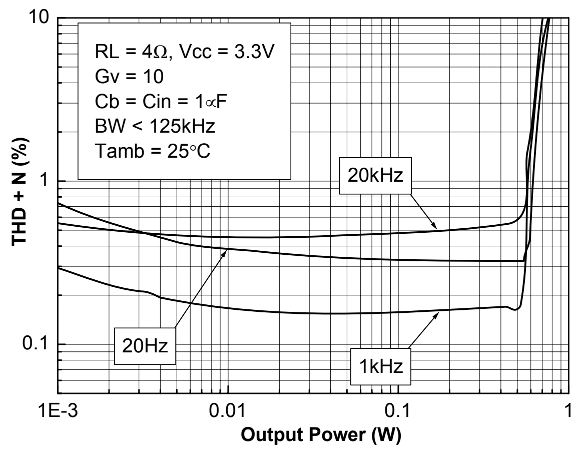


Figure 26. THD + N vs output power Gv=2, Vcc = 2.6 V

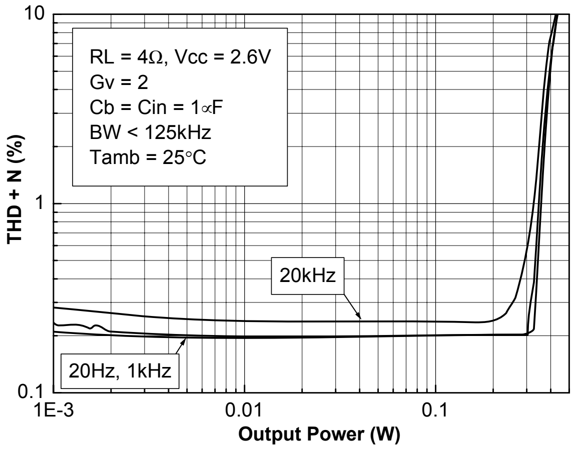


Figure 27. THD + N vs output power Gv=10, Vcc = 2.6 V

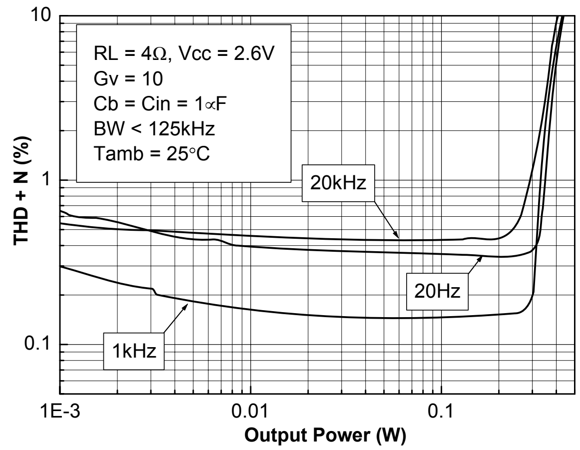


Figure 28. THD + N vs output power Gv=2, Vcc= 5 V, RL=8 Ω

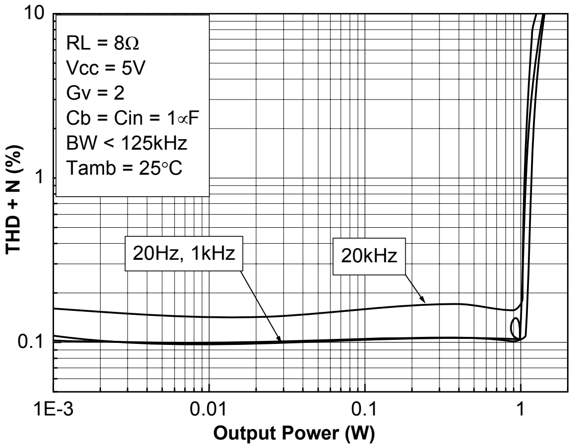


Figure 29. THD + N vs output power Gv=10, Vcc = 5 V

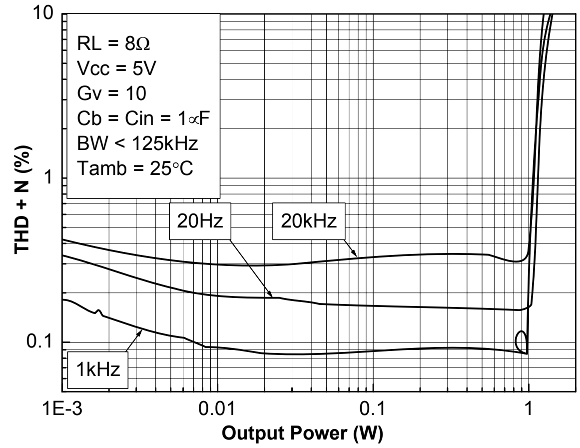


Figure 30. THD + N vs output power RL= 8 Ω

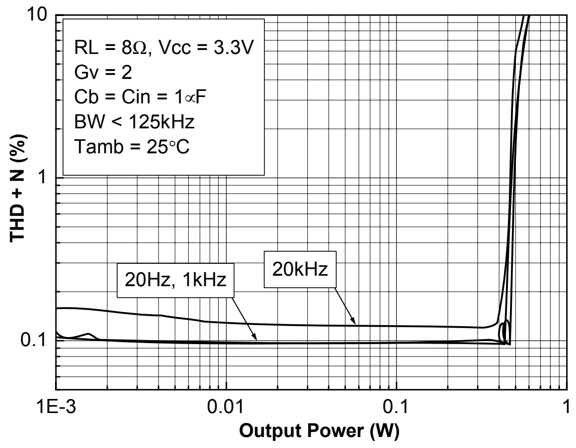


Figure 31. THD + N vs output power RL= 8 Ω, Vcc=3.3 V

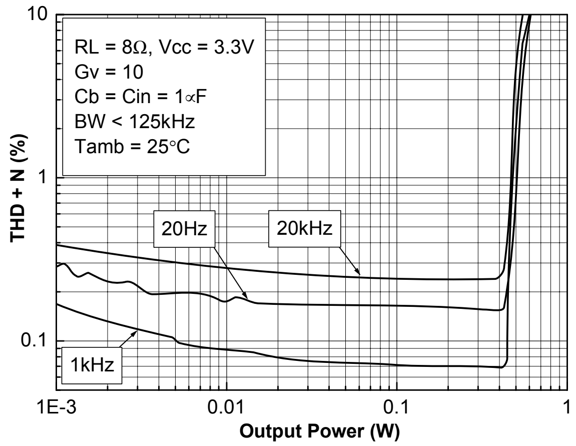


Figure 32. THD + N vs output power RL= 8 Ω, Vcc=2.6 V

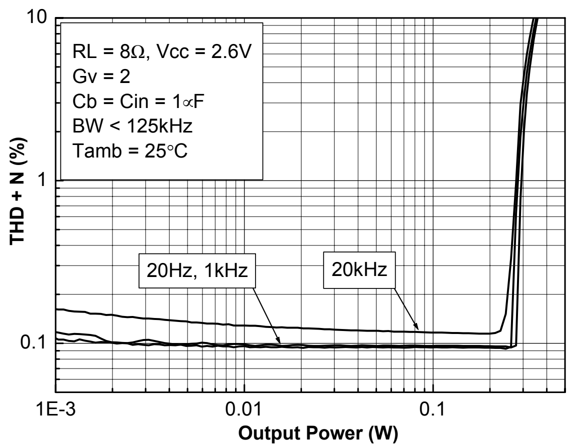


Figure 33. THD + N vs output power RL= 8 Ω, Gv=10

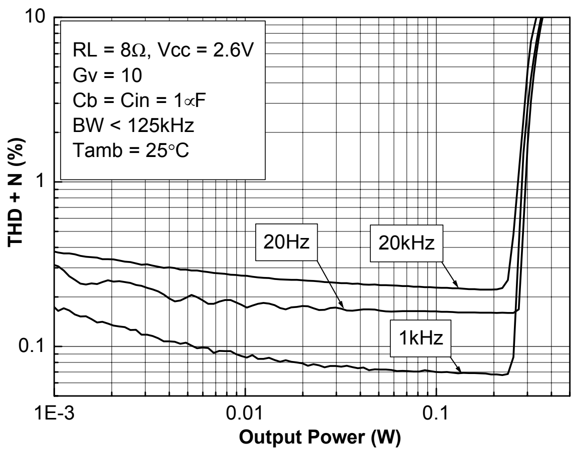


Figure 34. THD + N vs output power Gv=2, Vcc=5 V, Cb=0.1 µF

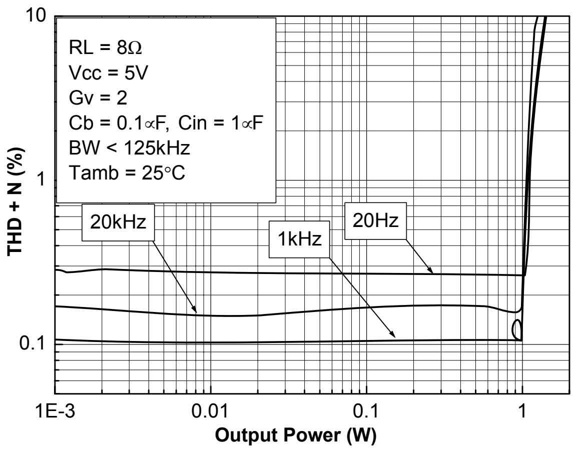


Figure 35. THD + N vs output power Gv=10, Vcc = 5 V, Cb=0.1 µF

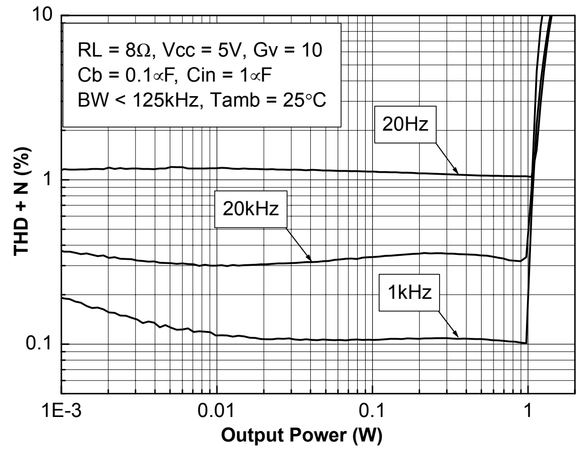


Figure 36. THD + N vs output power Gv=2, Vcc = 3.3 V, Cb=0.1 µF

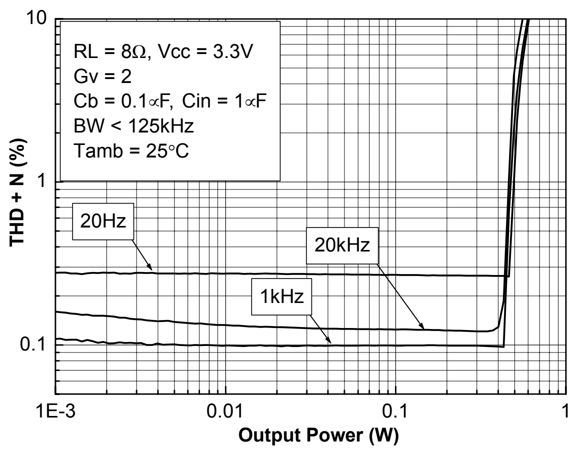


Figure 37. THD + N vs output power Gv=10, Vcc=3.3 V, Cb=0.1 µF

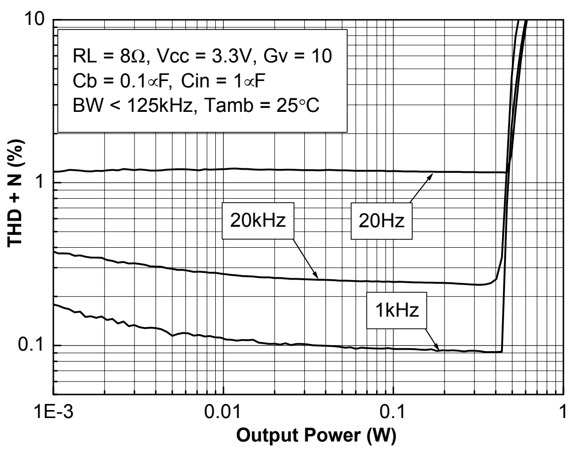


Figure 38. THD + N vs output power Gv=2, Vcc = 2.6 V, Cb=0.1 µF

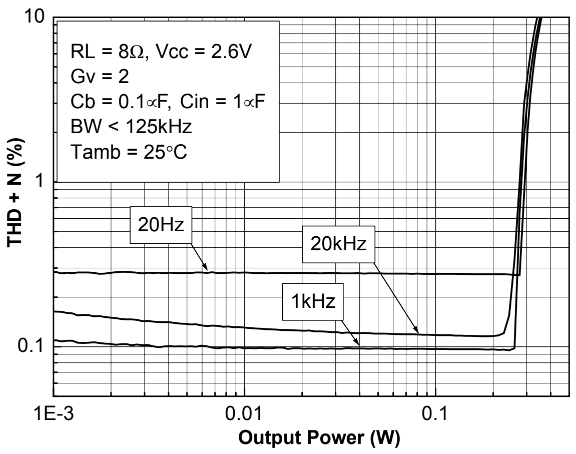


Figure 39. THD + N vs output power Gv=10, Vcc=2.6 V, Cb=0.1 µF

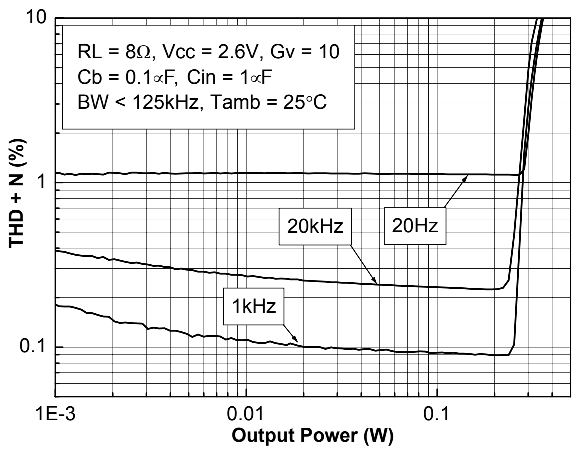


Figure 40. THD + N vs output power RL=16 Ω Vcc=0 5 V

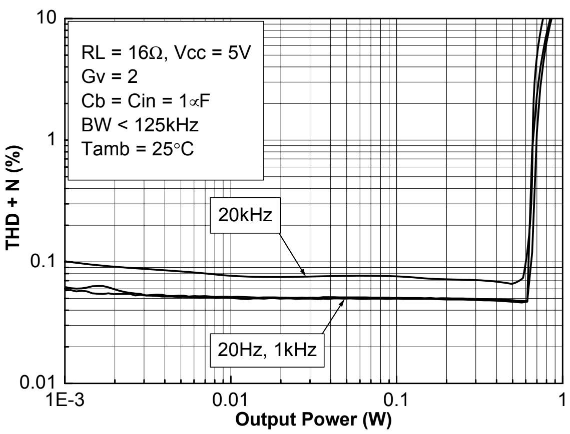


Figure 41. THD + N vs output power RL=16 Ω Gv=10

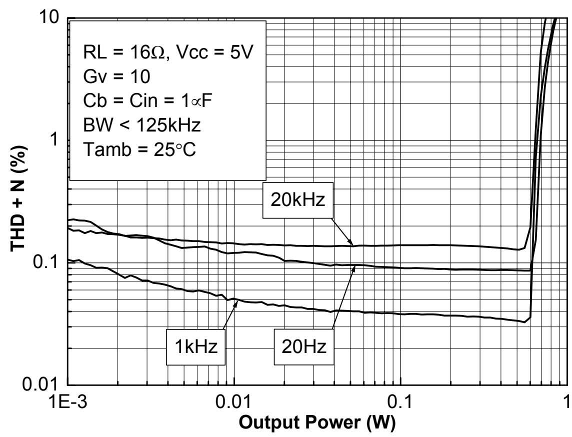


Figure 42. **THD + N vs output power RL=16 Ω, Gv=2**

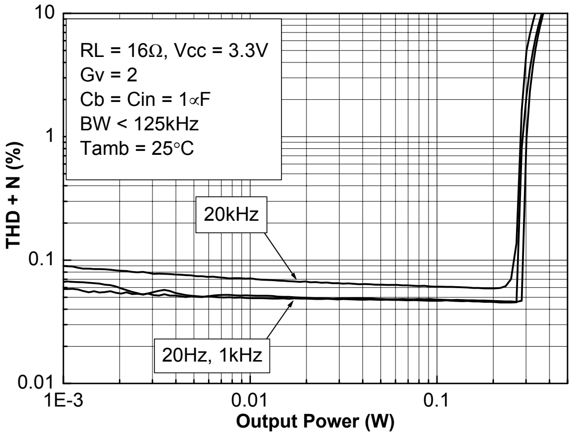


Figure 43. **THD + N vs output power RL=16 Ω, Gv=10, V_{CC}=3.3 V**

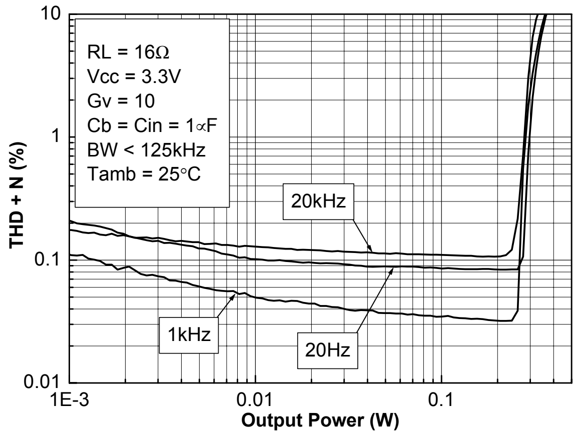


Figure 44. **THD + N vs output power RL=16 Ω Vcc=2.6 V**

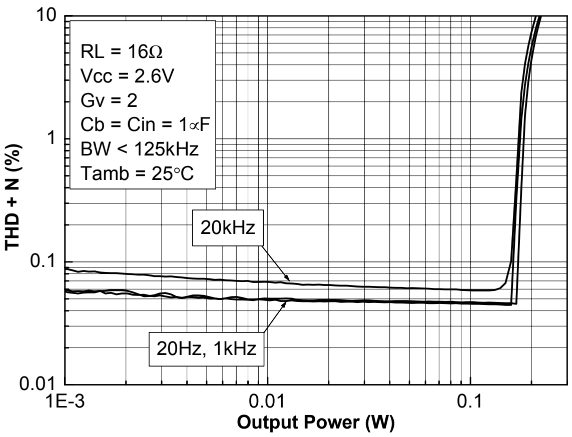


Figure 45. **THD + N vs output power RL=16 Ω, Vcc=2.6 V , Gv=10**

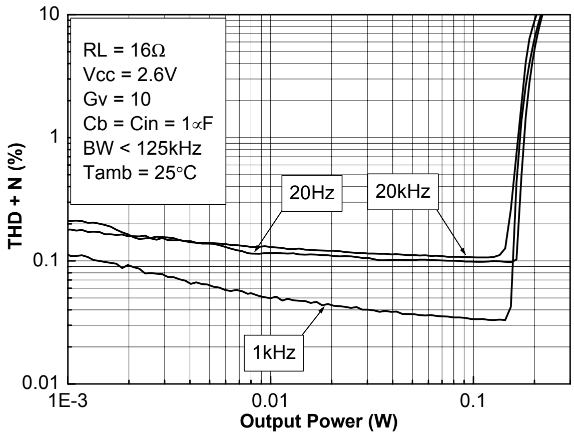


Figure 46. THD + N vs frequency

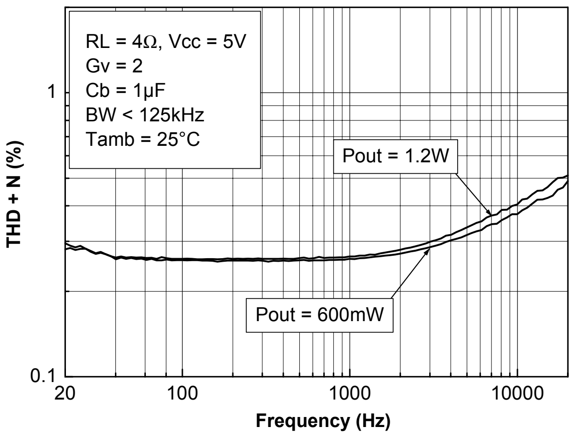


Figure 47. THD + N vs frequency, Vcc=5 V

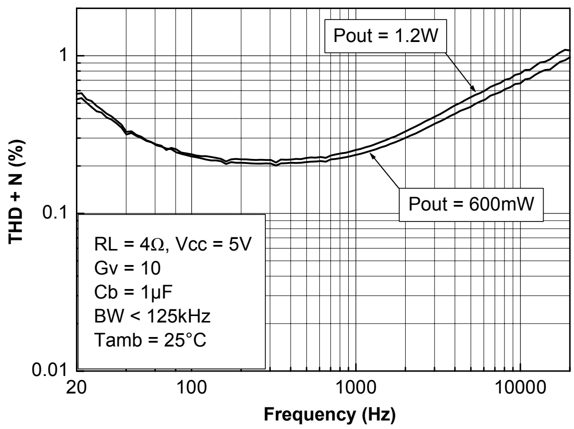


Figure 48. THD + N vs frequency, Vcc=3.3 V

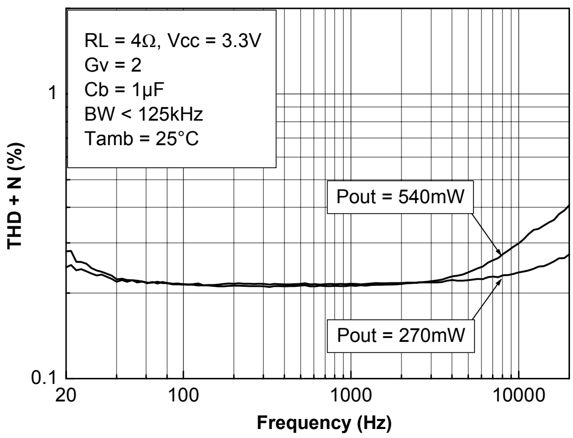


Figure 49. THD + N vs frequency, Gv=10

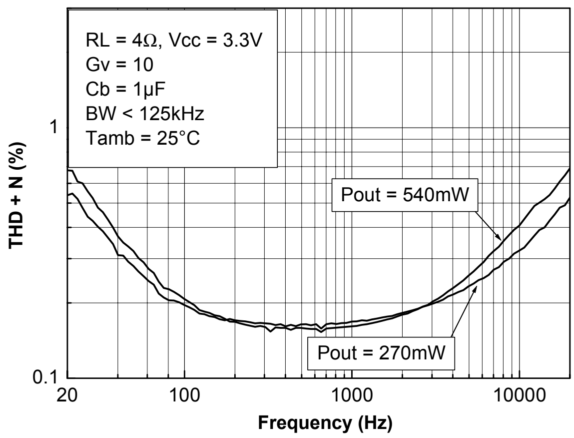


Figure 50. **THD + N vs frequency, Vcc=2.6 V**

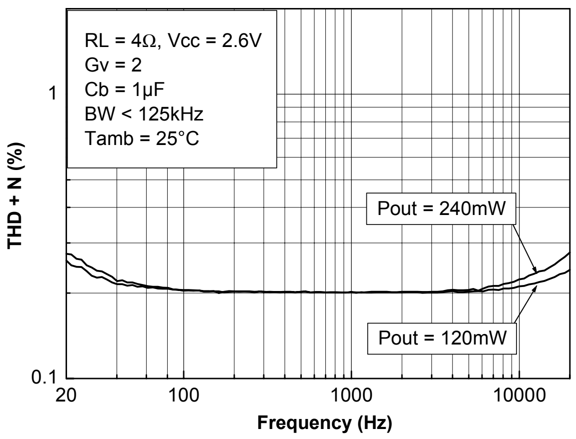


Figure 51. **THD + N vs frequency, Vcc=2.6 V, RL = 4 Ω**

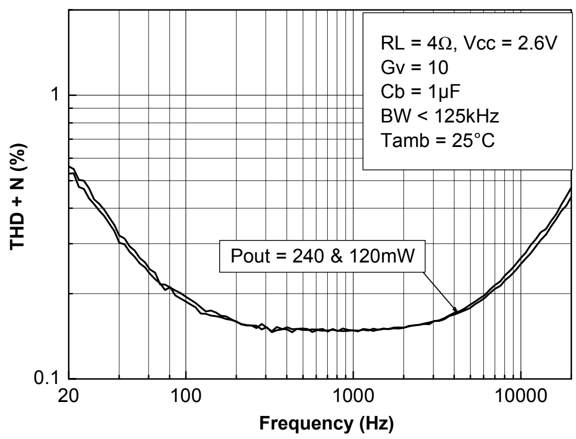


Figure 52. **THD + N vs frequency, Vcc=5 V, RL=8 Ω**

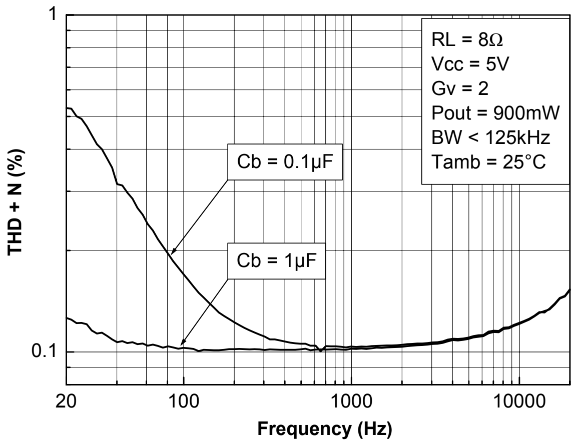


Figure 53. **THD + N vs frequency, Pout=450 mW**

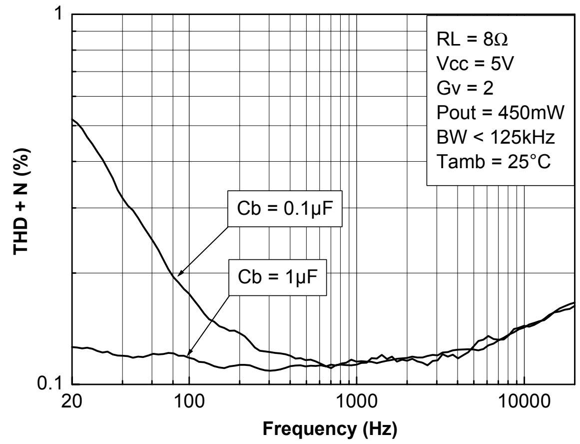


Figure 54. THD + N vs frequency, Pout=900 mW

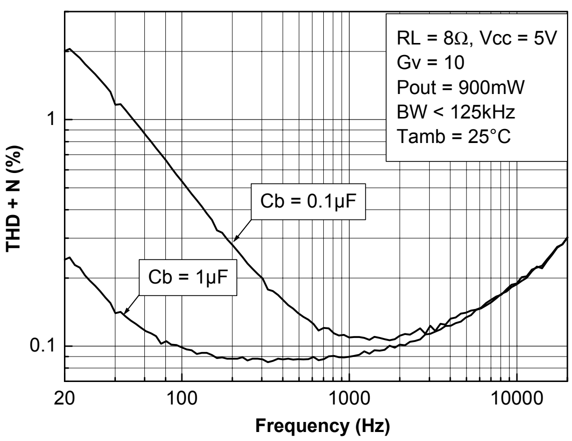


Figure 55. THD + N vs frequency, Pout=450 mW, RL=8 Ω

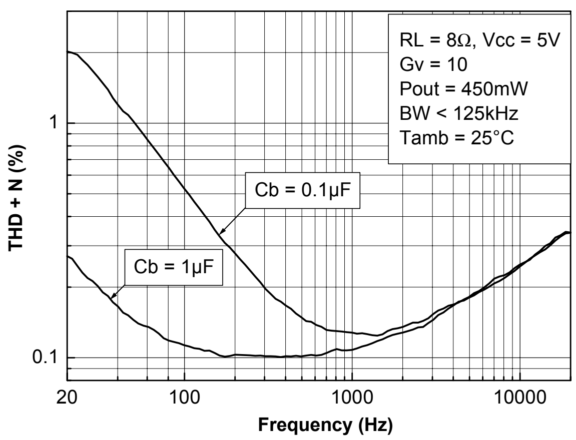


Figure 56. THD + N vs frequency, Pout=400 mW

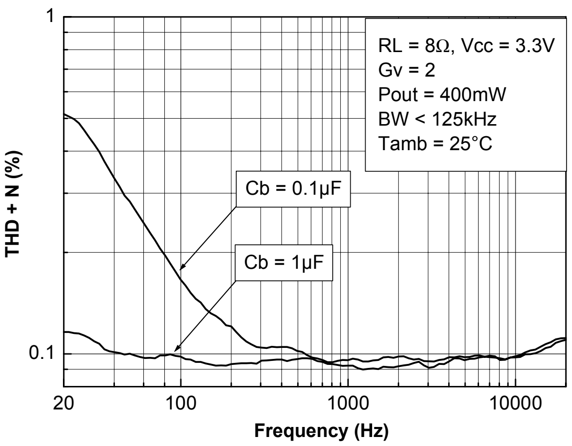


Figure 57. THD + N vs frequency, Pout=200 mW

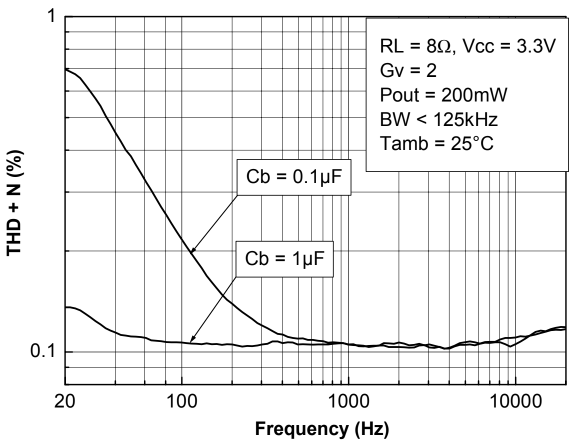


Figure 58. THD + N vs frequency, Pout=400 mW, Gv=010

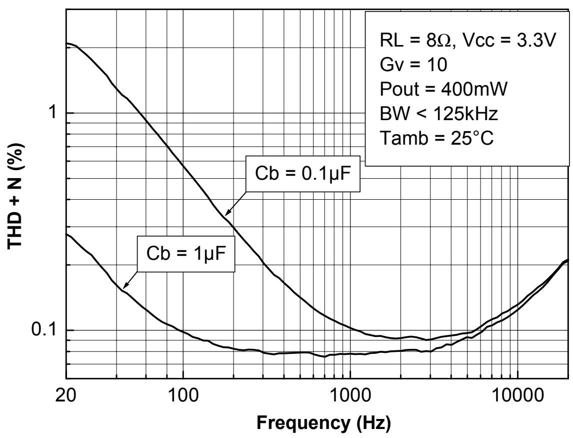


Figure 59. THD + N vs frequency, Pout=200 mW

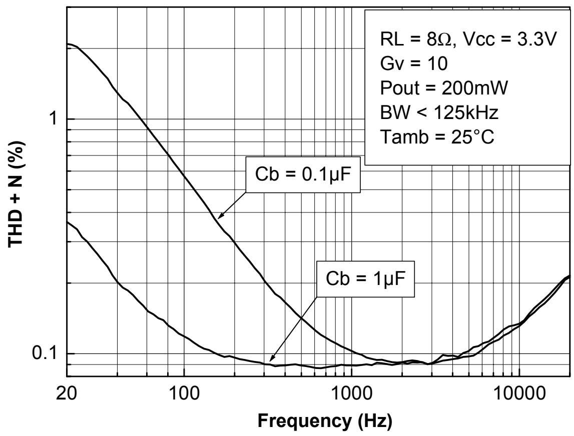


Figure 60. THD + N vs frequency, Pout=220 mW

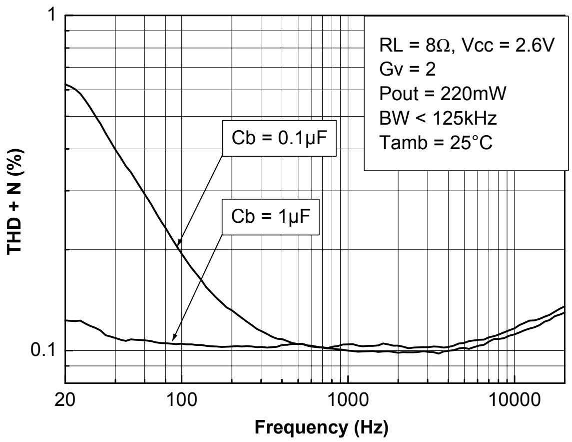


Figure 61. THD + N vs frequency, Pout=110 mW

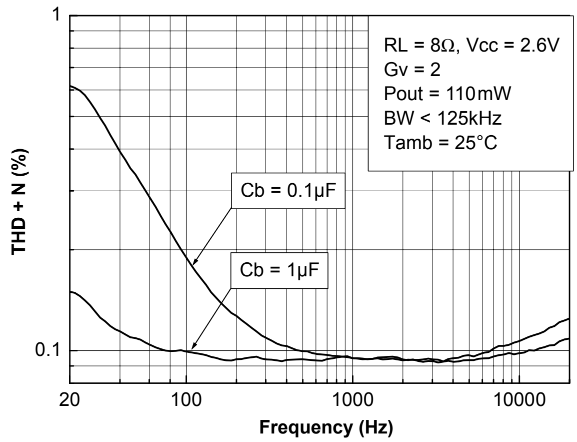


Figure 62. THD + N vs frequency, Pout=220 mW, Vcc= 2.6 V

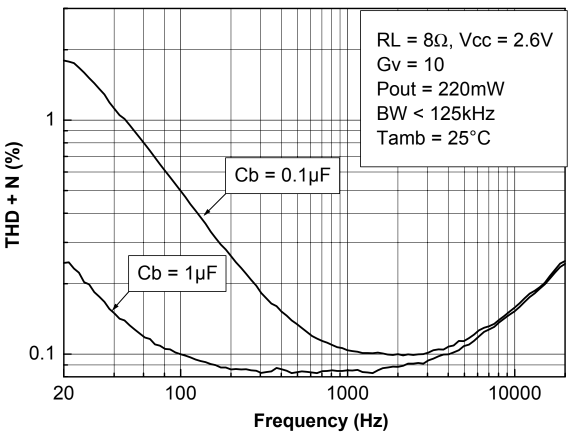


Figure 63. THD + N vs frequency, Pout=110 mW, Vcc= 2.6 V

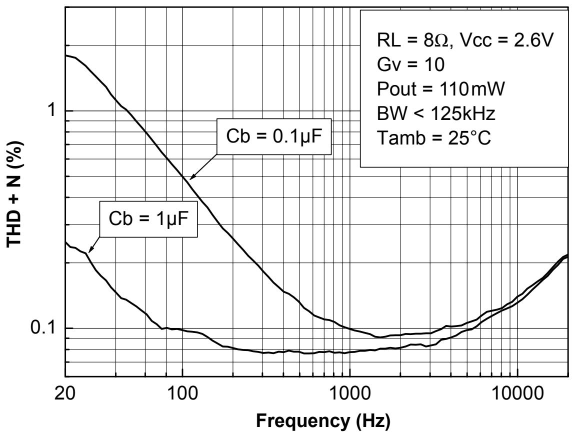


Figure 64. THD + N vs frequency, RL=16 Ω

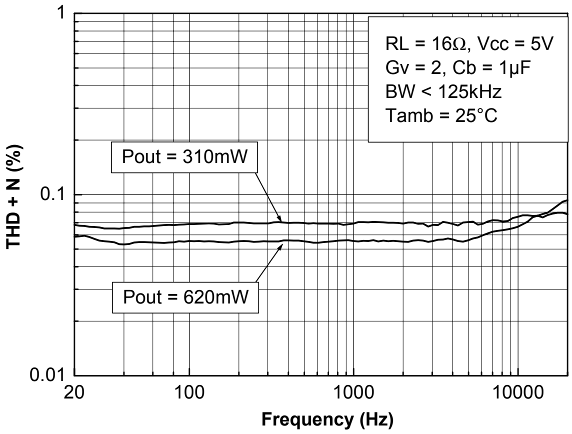


Figure 65. THD + N vs frequency, RL=16 Ω , Gv=10

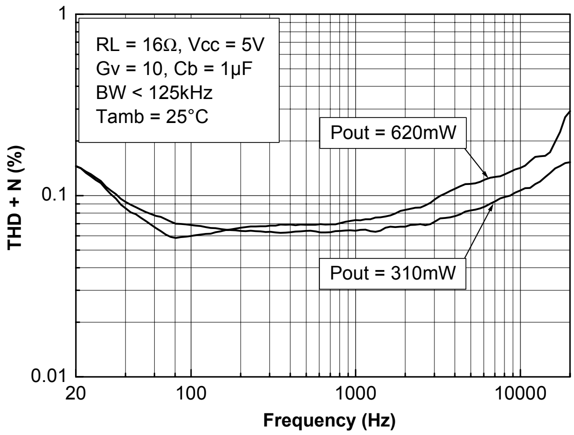


Figure 66. THD + N vs frequency, RL=16 Ω , Gv=2

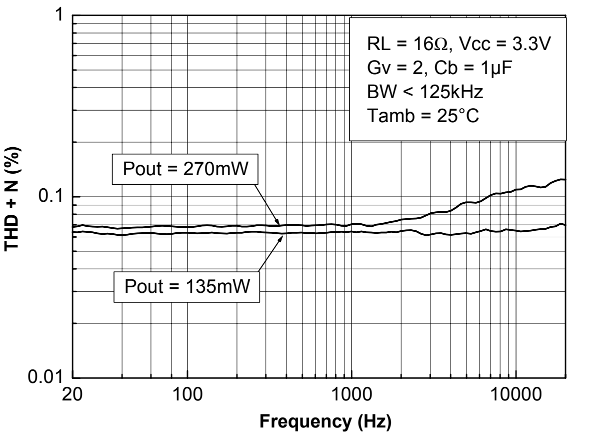


Figure 67. THD + N vs frequency, RL=16 Ω , Gv=10, Vcc=3.3 V

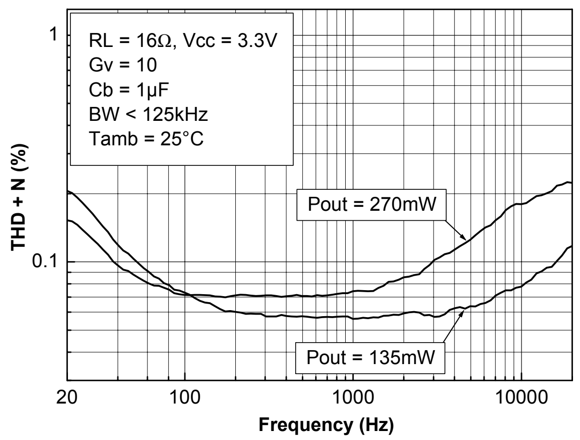


Figure 68. THD + N vs frequency, RL=16 Ω , Gv=2, Vcc=2.6 V

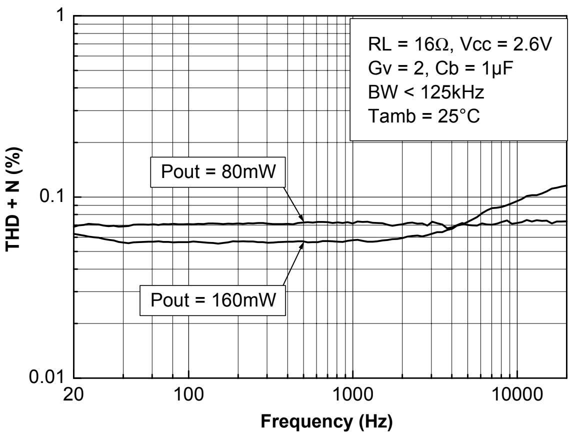


Figure 69. THD + N vs frequency, RL=16 Ω , Gv=10, Pout= 160 mW

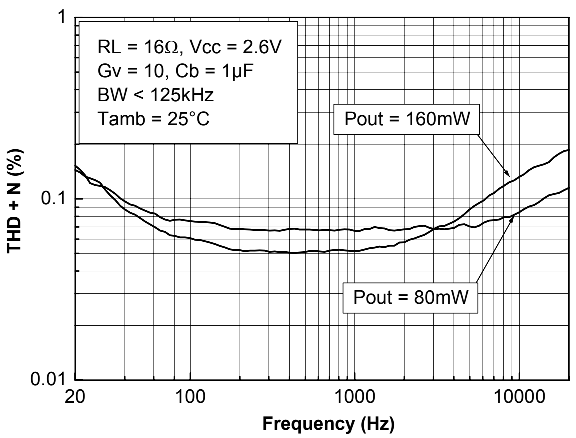


Figure 70. Signal-to-noise ratio vs power supply with unweighted filter (20 Hz to 20 kHz)

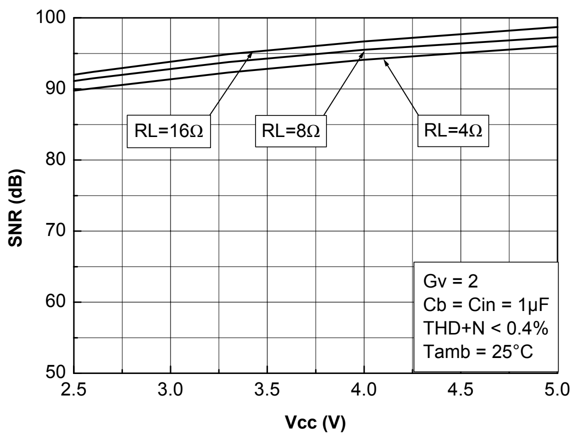


Figure 71. Signal-to-noise ratio vs power supply with weighted filter type A

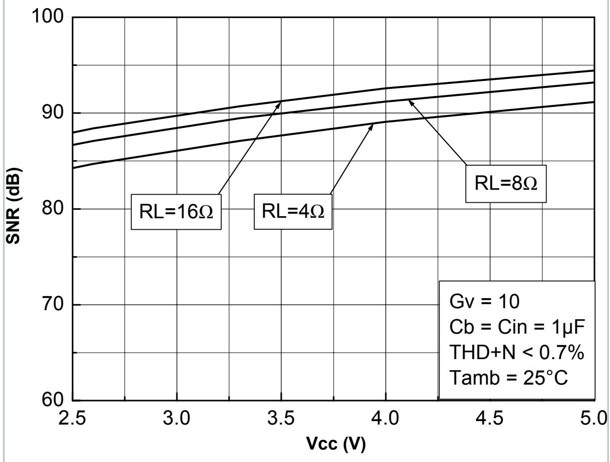


Figure 72. Signal-to-noise ratio vs power supply with weighted filter type A Gv=2

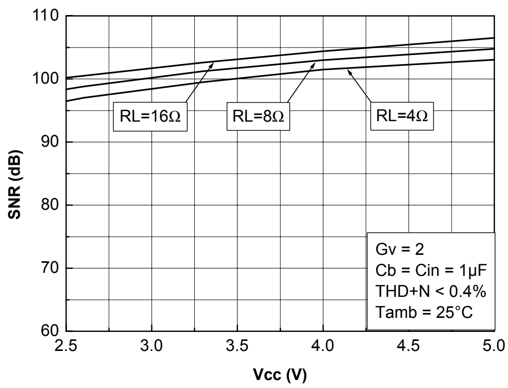


Figure 73. Current consumption vs power supply voltage

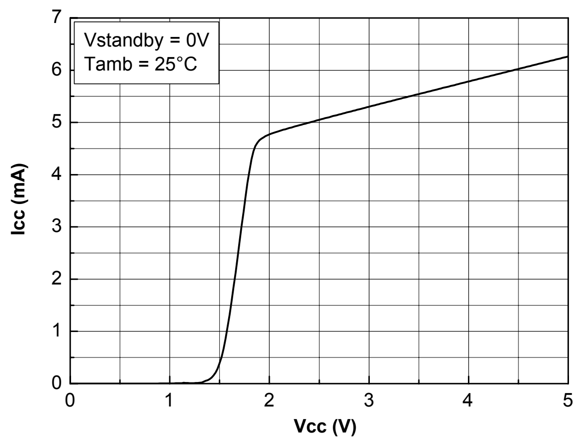


Figure 74. **Signal-to-noise ratio vs power supply with unweighted filter (20 Hz to 20 kHz) Gv=10**

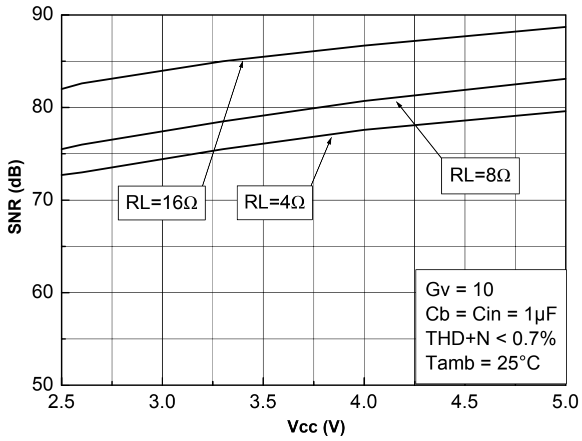


Figure 75. **Current consumption vs standby voltage @ Vcc = 5 V**

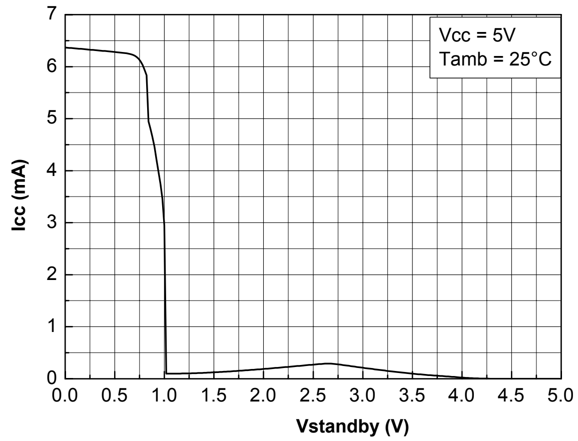


Figure 76. **Current consumption vs standby voltage @ Vcc = 2.6 V**

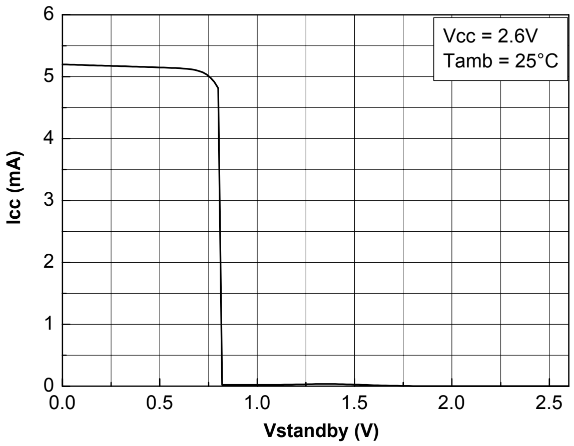


Figure 77. **Current consumption vs standby voltage @ Vcc = 3.3 V**

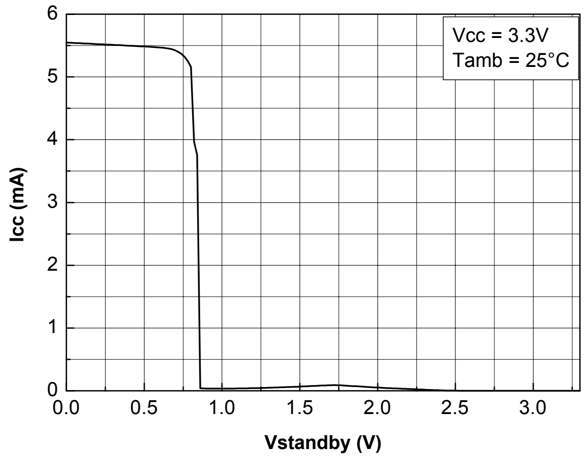


Figure 78. Clipping voltage vs power supply voltage and load resistor

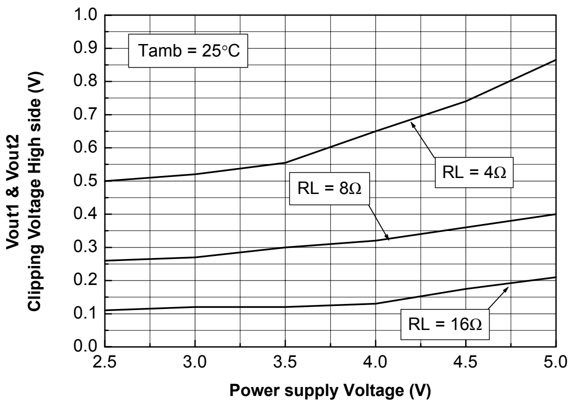


Figure 79. Clipping voltage low-side vs power supply voltage and load resistor

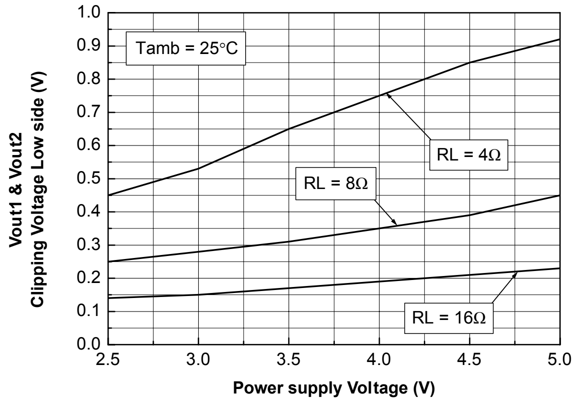


Figure 80. Vout1+Vout2 unweighted noise floor

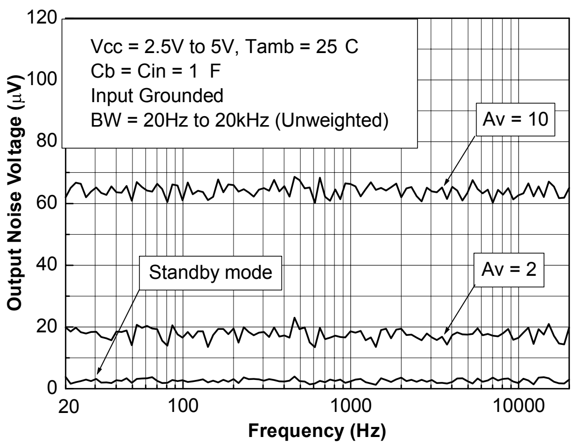
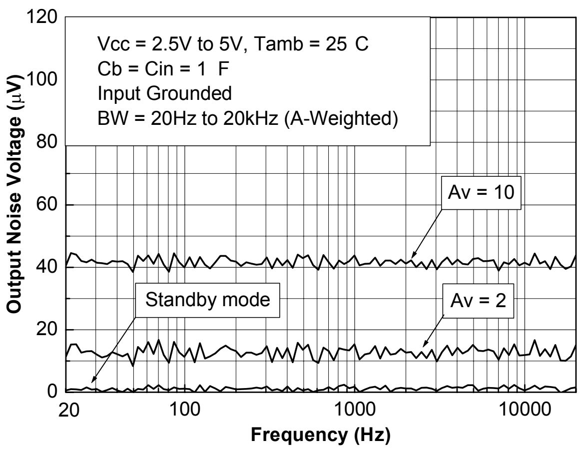


Figure 81. Vout1+Vout2 A-weighted noise floor



5 Application information

Figure 82. Demoboard schematic

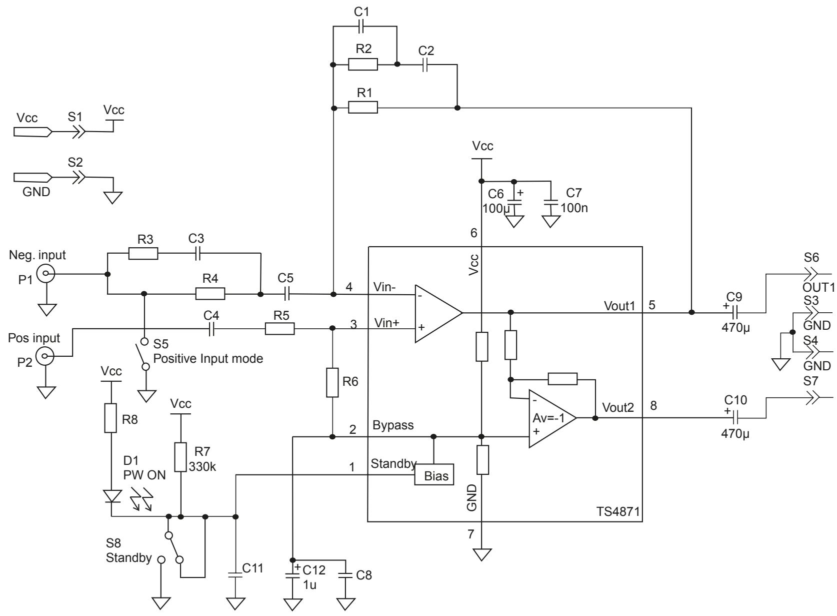
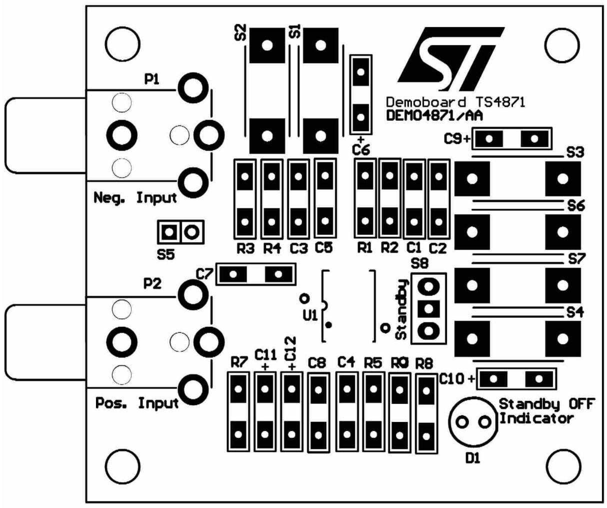


Figure 83. SO8 & MiniSO8 demoboard components side



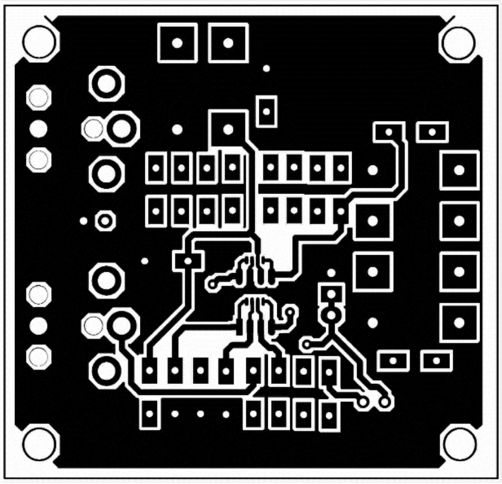


Figure 84. **SO8 and MiniSO8 demoboard top solder layer**

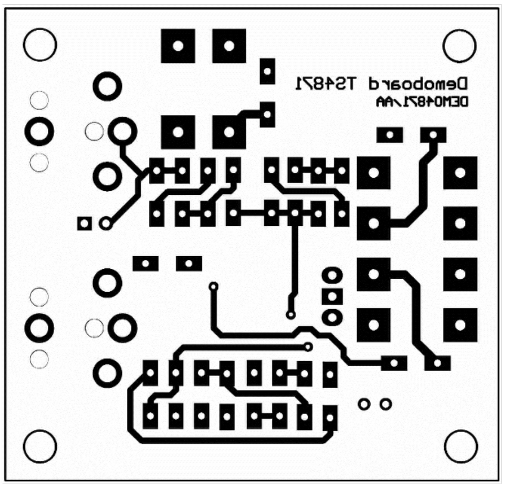


Figure 85. **SO8 and MiniSO8 demoboard bottom solder layer**

5.1 BTL configuration principle

The TS4871 is a monolithic power amplifier with a BTL output type. BTL (bridge tied load) means that each end of the load is connected to two single ended output amplifiers. Thus, we have:

Single ended output 1 = Vout1 = Vout (V)

Single ended output 2 = Vout2 = -Vout (V)

And Vout1 - Vout2 = 2Vout (V)

The output power is:

$$Pout = \frac{(2Vout_{RMS})^2}{R_L}(W) \quad (1)$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

5.2 Gain In typical application schematic

In flat region (no effect of Cin), the output voltage of the first stage is:

$$Vout1 = -Vin\frac{Rfeed}{Rin}(V)$$

For the second stage : Vout2 = -Vout1 (V)

The differential output voltage is:

$$Vout2 - Vout1 = 2Vin\frac{Rfeed}{Rin}(V)$$

The differential gain named gain (Gv) for more convenient usage is:

$$Gv = \frac{Vout2 - Vout1}{Vin} = 2\frac{Rfeed}{Rin}$$

Remark : Vout2 is in phase with Vin and Vout1 is 180 phased with Vin. It means that the positive terminal of the loud speaker should be connected to Vout2 and the negative to Vout1.

5.3 Low and high frequency response

In low frequency region, the effect of Cin starts. Cin with Rin forms a high pass filter with a -3 dB cut-off frequency

$$F_{CL} = \frac{1}{2\pi RinCin}(Hz)$$

In high frequency region, you can limit the bandwidth by adding a capacitor (Cfeed) in parallel on Rfeed. Its form a low pass filter with a -3 dB cut-off frequency.

$$F_{CH} = \frac{1}{2\pi RfeedCfeed}(Hz)$$

5.4 Power dissipation and efficiency

Hypothesis:

- Voltage and current in the load are sinusoidal (Vout and Iout)
- Supply voltage is a pure DC source (Vcc)

Regarding the load we have:

$$V_{OUT} = V_{PEAK}\sin\,\omega t(t)$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L}(A)$$

$$P_{OUT} = \frac{V_{PEAK}2}{2R_L}(W)$$

Then, the average current delivered by the supply voltage is:

$$Icc_{AVG} = 2\frac{V_{PEAK}}{\pi R_L}(A)$$

The power delivered by the supply voltage is Psupply = Vcc Icc_{AVG} (W)

Then, the power dissipated by the amplifier is Pdiss = Psupply - Pout (W)

$$Pdiss = \frac{2\sqrt{2Vcc}}{\pi\sqrt{R_L}}\sqrt{P_{OUT}} - P_{OUT}(W)$$

and the maximum value is obtained when:

$$\frac{\partial Pdiss}{\partial P_{OUT}} = 0$$

and its value is:

$$Pdissmax = \frac{2V_{CC}{}^2}{\pi^2 R_L}(W)$$

Remark : This maximum value is only depending on power supply voltage and load values.

The efficiency is the ratio between the output power and the power supply

$$\eta = \frac{P_{OUT}}{P_{supply}} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when

Vpeak = Vcc, so

$$\frac{\pi}{4} = 78.5\,\%$$

5.5 Decoupling of the circuit

Two capacitors are needed to bypass properly the TS4871, a power supply bypass capacitor Cs and a bias voltage bypass capacitor Cb.

Cs has especially an influence on the THD+N in high frequency (above 7 kHz) and indirectly on the power supply disturbances.

With 100 µF, you can expect similar THD+N performances like shown in the datasheet.

If Cs is lower than 100 µF, in high frequency increases, THD+N and disturbances on the power supply rail are less filtered.

To the contrary, if Cs is higher than 100 µF, those disturbances on the power supply rail are more filtered.

Cb has an influence on THD+N in lower frequency, but its function is critical on the final result of PSRR with input grounded in lower frequency.

If Cb is lower than 1 µF, THD+N increase in lower frequency (see THD+N vs frequency curves) and the PSRR worsens up.

If Cb is higher than 1 µF, the benefit on THD+N in lower frequency is small but the benefit on PSRR is substantial (see PSRR vs. Cb curve: fig.12).

Note that Cin has a non-negligible effect on PSRR in lower frequency. Lower is its value, higher is the PSRR (see fig. 13).

5.6 Pop and Click performance

Pop and click performance is intimately linked to the size of the input capacitor Cin and the bias voltage bypass capacitor Cb.

Size of Cin is due to the lower cut-off frequency and PSRR value requested. Size of Cb is due to THD+N and PSRR requested always in lower frequency.

Moreover, Cb determines the speed that the amplifier turns ON. The slower the speed is, the softer the turn ON noise is.

The charge time of Cb is directly proportional to the internal generator resistance 50 kW.

Then, the charge time constant for Cb is

τb = 50 kΩxCb (s)

As Cb is directly connected to the non-inverting input (pin 2 and 3) and if we want to minimize, in amplitude and duration, the output spike on Vout1 (pin 5), Cin must be charged faster than Cb. The charge time constant of Cin is

τin = (Rin+Rfeed)xCin (s)

Thus we have the relation

τin << τb (s)

The respect of this relation allows the pop and click noise to be minimized.

Remark : Minimize Cin and Cb has a benefit on pop and click phenomena but also on cost and size of the application.

Example : your target for the -3 dB cut off frequency is 100 Hz. With Rin = Rfeed = 22 kΩ, Cin = 72 nF (in fact 82 nF or 100 nF).

With Cb = 1 µF, if you choose the one of the latest two values of Cin, the pop and click phenomena at power supply ON or standby function ON/OFF will be very small

50 kΩx1 µF >> 44 kΩ x 100 nF (50 ms >> 4.4 ms).

Increasing Cin value increases the pop and click phenomena to an unpleasant sound at power supply ON and standby function ON/OFF.

Why Cs is not important in pop and click consideration ?

Hypothesis :

Cs = 100 µF

Supply voltage = 5 V

Supply voltage internal resistor = 0.1 Ω

Supply current of the amplifier Icc = 6 mA

At power ON of the supply, the supply capacitor is charged through the internal power supply resistor. So, to reach 5 V you need about five to ten times the charging time constant of Cs (τs = 0.1 x Cs (s)).

Then, this time equal 50 µs to 100 µs << τb in the majority of application.

At power OFF of the supply, Cs is discharged by a constant current Icc. The discharge time from 5 V to 0 V of Cs is:

$$t_{DischCs} = \frac{5C_S}{Icc} = 83\,ms$$

Now, we must consider the discharge time of Cb.

At power OFF or standby ON, Cb is discharged by a 100 kΩ resistor. So the discharge time is about

$\tau b_{Disch} \approx 3 \times Cb \times 100\ k\Omega\ (s)$.

In the majority of application, Cb = 1 µF, then

$\tau b_{Disc}h \approx 300\ ms >> \tau_{dischCs}$.

5.7 Power amplifier design examples

Given :

Load impedance : 8 Ω

Output power @ 1% THD+N : 0.5 W

Input impedance : 10 kΩ min.

Input voltage peak to peak : 1 Vpp

Bandwidth frequency : 20 Hz to 20 kHz (0, -3 dB)

Ambient temperature max = 50 °C

SO8 package

First of all, we must calculate the minimum power supply voltage to obtain 0.5 W into 8 Ω. With curves in fig. 15, we can read 3.5 V. Thus, the power supply voltage value min. is 3.5 V.

Following the maximum power dissipation equation

$$Pdissmax = \frac{2V_{CC}{}^2}{\pi^2 R_L} = (W)$$

with 3.5 V we have Pdissmax = 0.31 W

Refer to power derating curves (fig. 20), with 0.31 W the maximum ambient temperature is 100 °C. This last value could be higher if you follow the example layout shown on the demoboard (better dissipation).

The gain of the amplifier in flat region is:

$$G_V = \frac{V_{OUTPP}}{V_{INPP}} = \frac{2\sqrt{2R_L P_{OUT}}}{V_{INPP}} = 5.65$$

We have Rin > 10 kΩ. Let's take Rin = 10 kΩ, then Rfeed = 28.25 kΩ. We could use for Rfeed = 30 kΩ in normalized value and the gain is Gv = 6.

In lower frequency we want 20 Hz (- 3dB cut-off frequency). Then:

So, we could use for Cin a 1 µF capacitor value

$$C_{IN} = \frac{1}{2\pi R_{in} F_{CL}} = 795\ nF$$

which gives 16 Hz.

In higher frequency we want 20 kHz (- 3dB cut off frequency). The gain bandwidth product of the TS4871 is 2 MHz typical and does not change when the amplifier delivers power into the load.

The first amplifier has a gain of:

$$\frac{R_{feed}}{R_{in}} = 3$$

and the theoretical value of the - 3 dB cut-off higher frequency is 2 MHz/3 = 660 kHz.

We can keep this value or limit the bandwidth by adding a capacitor Cfeed, in parallel on Rfeed.

Then:

$$C_{FEED} = \frac{1}{2\pi R_{FEED} F_{CH}} = 265pF$$

So, we could use for Cfeed a 220 pF capacitor value that gives 24 kHz.

Now, we can calculate the value of Cb with the formula τb = 50 kΩ x Cb >> τin = (Rin+Rfeed) x Cin which permits to reduce the pop and click effects.

Then Cb >> 0.8 µF.

We can choose for Cb a normalized value of 2.2 µF that gives good results in THD+N and PSRR.

In the following tables, you could find three another examples with values required for the demoboard.

Remark : components with (*) marking are optional.

5.8 Application n°1 : 20 Hz to 20 kHz bandwidth and 6 dB gain BTL power amplifier

Table 7. Components

Designator	Part type
R1	22 k / 0.125 W
R4	22 k / 0.125 W
R6	Short-circuit
R7	330 k / 0.125 W
R8*	(Vcc-Vf_led) / If_led
C5	470 nF
C6	100 µF
C7	100 nF
C9	Short-circuit
C10	Short-circuit
C12	1 µF
S1, S2, S6, S7	2 mm insulated plug 10.16 mm pitch
S8	3 pt connector 2.54 mm pitch
P1	PCB phono Jack
D1*	Led 3 mm
U1	TS4871ID or TS4871IS

5.9 Application n°2 : 20 Hz to 20 kHz bandwidth and 20 dB gain BTL power amplifier

Table 8. **Components**

Designator	Part type
R1	110 k / 0.125 W
R4	22 k / 0.125 W
R6	Short-circuit
R7	330 k / 0.125 W
R8*	(Vcc-Vf_led) / If_led
C5	470 nF
C6	100 µF
C7	100 nF
C9	Short-circuit
C10	Short-circuit
C12	1 µF
S1, S2, S6, S7	2 mm insulated plug 10.16 mm pitch
S8	3 pt connector 2.54 mm pitch
P1	PCB phono Jack
D1*	Led 3 mm
U1	TS4871ID or TS4871IS

5.10 Application n° 3: 50 Hz to 10 kHz bandwidth and 10 dB gain BTL power amplifier

Table 9. **Components**

Designator	Part type
R1	33 k / 0.125 W
R2	Short-circuit
R4	22 k / 0.125 W
R6	Short-circuit
R7	330 k / 0.125 W
R8*	(Vcc-Vf_led) / If_led
C2	470 pF
C5	150 nF
C6	100 µF
C7	100 nF
C9	Short-circuit
C10	Short-circuit
C12	1 µF
S1, S2, S6, S7	2 mm insulated plug 10.16 mm pitch
S8	3 pts connector 2.54 mm pitch
P1	PCB phono Jack
D1*	Led 3 mm
U1	TS4871ID or TS4871IS

5.11 Application n°4 : Differential inputs BTL power amplifier

In this configuration, we need to place these components : R1, R4, R5, R6, R7, C4, C5, C12.

We have also : R4 = R5, R1 = R6, C4 = C5.

The gain of the amplifier is:

$$G_{VDIFF} = 2\frac{R1}{R4}$$

For Vcc = 5 V, a 20 Hz to 20 kHz bandwidth and 20 dB gain BTL power amplifier you could follow the bill of material below.

Table 10. Components

Designator	Part type
R1	110 k / 0.125 W
R4	22 k / 0.125 W
R5	22 k / 0.125 W
R6	110 k / 0.125 W
R7	330 k / 0.125 W
R8*	(Vcc-Vf_led) / If_led
C4	470 nF
C5	470 nF
C6	100 µF
C7	100 nF
C9	Short-circuit
C10	Short-circuit
C12	1 µF
D1*	Led 3 mm
S1, S2, S6, S7	2 mm insulated plug 10.16 mm pitch
S8	3 pts connector 2.54 mm pitch
P1, P2	PCB phono Jack
U1	TS4871ID or TS4871IS

5.12 Note on how to use the PSRR curves

We have finished a design and we have chosen the components values

- Rin=Rfeed=22 kΩ
- Cin=100 nF
- Cb=1 µF

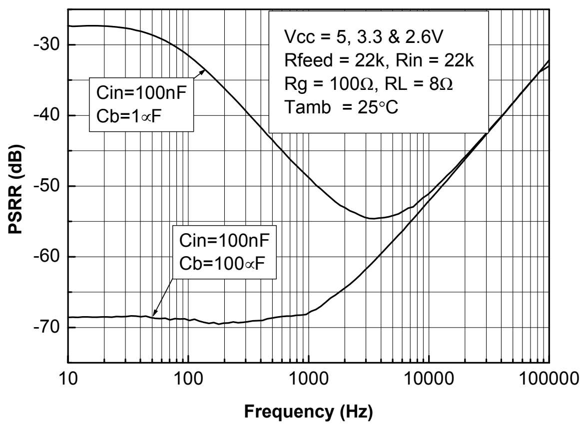
Now, on fig. 13, we can see the PSRR (input grounded) vs. frequency curves. At 217 Hz we have a PSRR value of -36 dB.

In reality we want a value about -70 dB. So, we need a gain of 34 dB.

Now, on fig. 12 we can see the effect of Cb on the PSRR (input grounded) vs. frequency. With Cb=100 µF, we can reach the -70 dB value.

The process to obtain the final curve (Cb=100 µF, Cin=100 nF, Rin=Rfeed=22 kΩ) is a simple transfer point by point on each frequency of the curve on fig. 13 to the curve on fig. 12. The measurement result is shown on the next figure.

Figure 86. **PSRR changes with Cb**



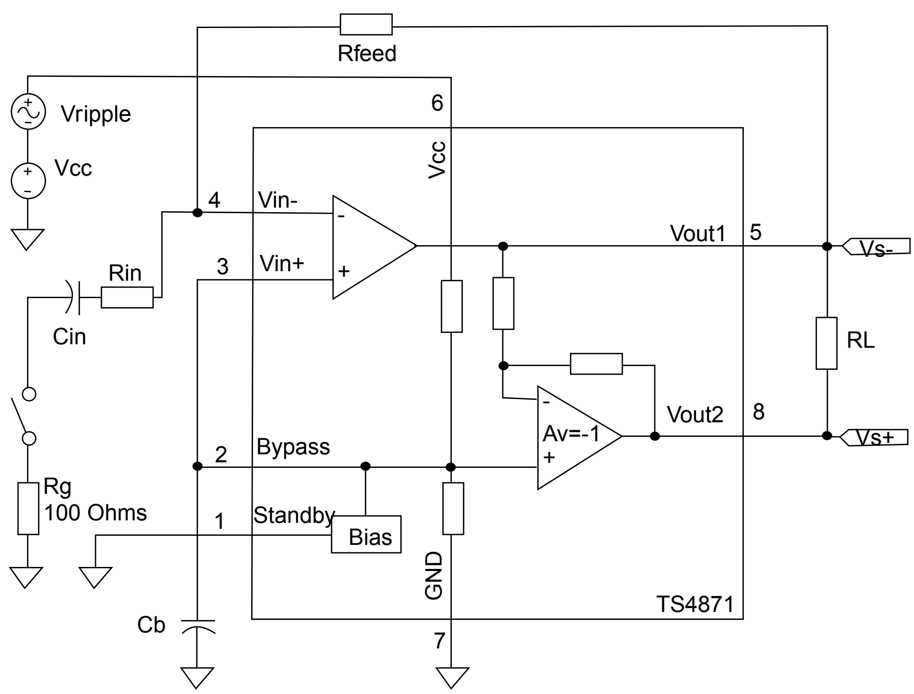
What is the PSRR?

The PSRR is the power supply rejection ratio. It is a kind of SVR in a determined frequency range.

The PSRR of a device, is the ratio between a power supply disturbance and the result on the output. We can say that the PSRR is the ability of a device to minimize the impact of power supply disturbances to the output.

How do we measure the PSRR?

Figure 87. **PSRR measurement schematic**



5.13 Principle of operation

We fixed the DC voltage supply (Vcc), the AC sinusoidal ripple voltage (Vripple) and no supply capacitor Cs is used.

The PSRR value for each frequency is:

$$PSRR(dB) = 20xLog_{10}\left[\frac{Rms(Vripple)}{Rms(Vs_{+} - Vs_{-})}\right]$$

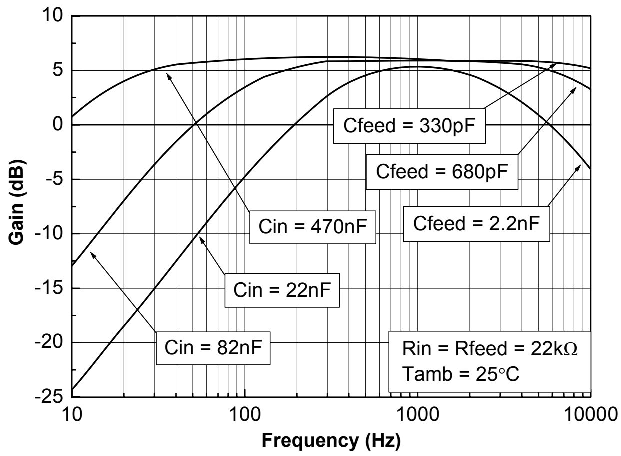
Remark : The measure of the Rms voltage is not a Rms selective measure but a full range (2 Hz to 125 kHz) Rms measure.

It means that we measure the effective Rms signal + the noise.

5.14 High/low cut-off frequencies

For their calculation, please check the figure below:

Figure 88. Frequency response gain vs Cin and Cfeed



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 MiniSO8 package information

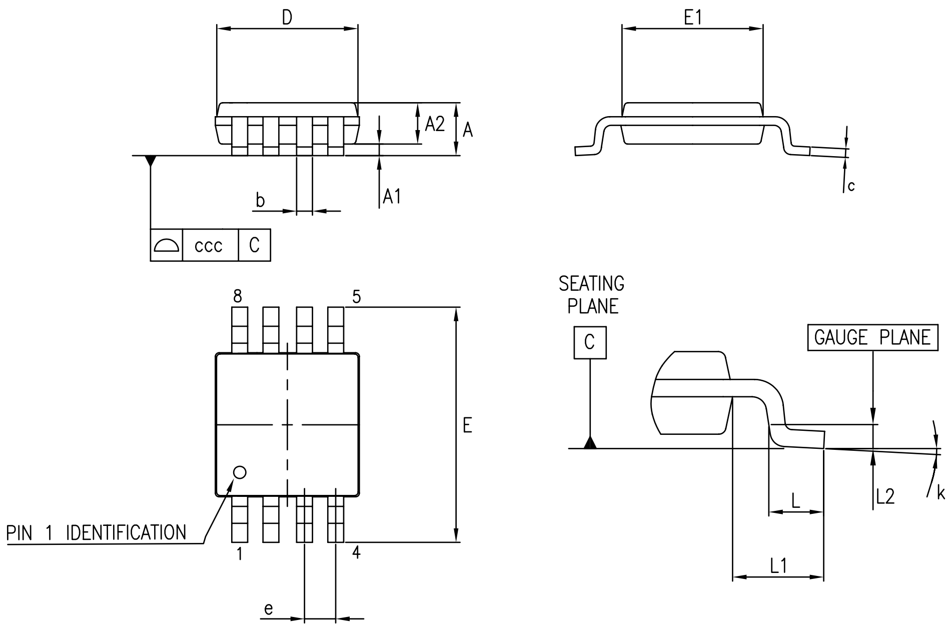


Figure 89. MiniSO8 package outline

Table 11. MiniSO8 mechanical data

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.03	0.033	0.037
b	0.22		0.4	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.8	3	3.2	0.11	0.118	0.126
E	4.65	4.9	5.15	0.183	0.193	0.203
E1	2.8	3	3.1	0.11	0.118	0.122
e		0.65			0.026	
L	0.4	0.6	0.8	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.01	
k	0°		8°	0°		8°
ccc			0.1			0.004

6.2 SO8 package information

Figure 90. **SO-8 package outline**

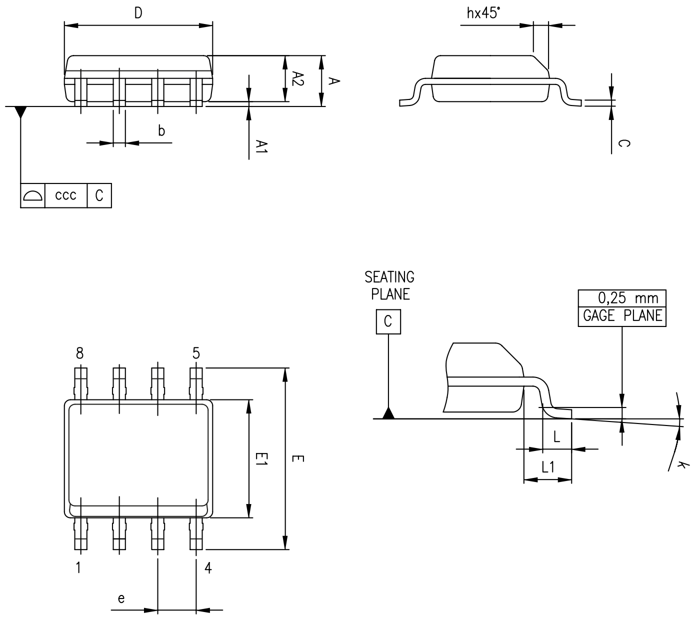


Table 12. **SO-8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.04		0.010
A2	1.25			0.049		
b	0.28	0.40	0.48	0.011	0.016	0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40	0.635	1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

7 Ordering information

Table 13. Ordering information

Order code	Temperature range	Package	Packing	Marking
TS4871IST	-40, +85°C	MiniSO8	Tape and reel	4871I
TS4871IDT		SO8		4871
TS4871ID		SO8	Tube	4871

Revision history

Table 14. Document revision history

Date	Revision	Changes
08-May-2019	9	No history because of migration. Removed the part number TS4871IQT and all its reference throughout the document.

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