Single-Wire-Transceiver TLE 6259-2

Final Datasheet

1 Overview

P-DSO-8-3

1.1 Features

- Single-wire transceiver, suitable for **LIN** protocol
- Transmission rate up to 20 kBaud
- Compatible to LIN specification 1.2
- Compatible to ISO 9141 functions
- Very low current consumption in sleep mode
- Control output for voltage regulator
- Bus short to GND protection
- Short circuit proof to ground and battery
- Overtemperature protection

Type	Ordering Code	Package
TLE 6259-2G	Q 67006 - A 9596	P-DSO-8-3

Description

The TLE 6259-2 is a monolithic integrated circuit in a P-DSO-8-3 package. It works as an interface between the protocol controller and the physical bus. The TLE 6259-2 is especially suitable to drive the bus line in LIN systems in automotive and industrial applications. Further it can be used in standard ISO9141 systems. The TLE6259-2 has a BUS short to GND feature implemented, to avoid a battery decharge.

In order to reduce the current consumption, the TLE 6259-2 offers a sleep operation mode. In this mode a voltage regulator can be controlled to minimize the current consumption of the whole application. A wake-up caused by a message on the bus, enables the voltage regulator and sets the RxD output LOW until the device is switched to normal operation mode.

The IC is based on the Smart Power Technology SPT® which allows bipolar and CMOS control circuitry in accordance with DMOS power devices existing on the same monolithic circuit.

The TLE 6259-2 is designed to withstand the severe conditions of automotive applications.

1.2 Pin Configuration (top view)

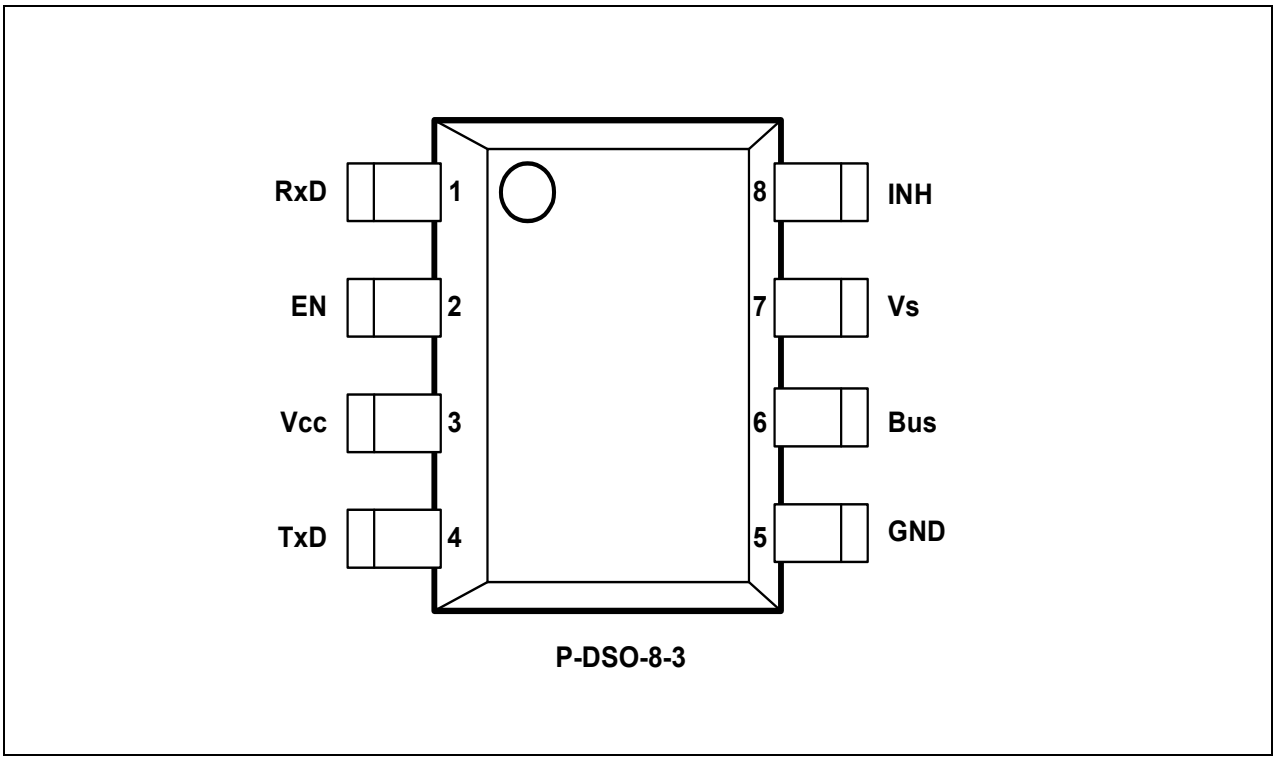


Figure 1

1.3 Pin Definitions and Functions:

Pin No.	Symbol	Function
1	RxD	**Receive data output;** integrated pull up, LOW in dominant state,
2	EN	**Enable input;** integrated 30 kΩ pull down, transceiver in normal operation mode when HIGH
3	V_{CC}	**5V supply input;**
4	TxD	**Transmit data input;** integrated pull up, LOW in dominant state
5	GND	**Ground;**
6	Bus	**Bus output/input;** internal 30 kΩ pull up, LOW in dominant state
7	Vs	**Battery supply input;**
8	INH	**Inhibit output;** to control a voltage regulator, becomes HIGH when wake-up via LIN bus occurs

1.4 Functional Block Diagram

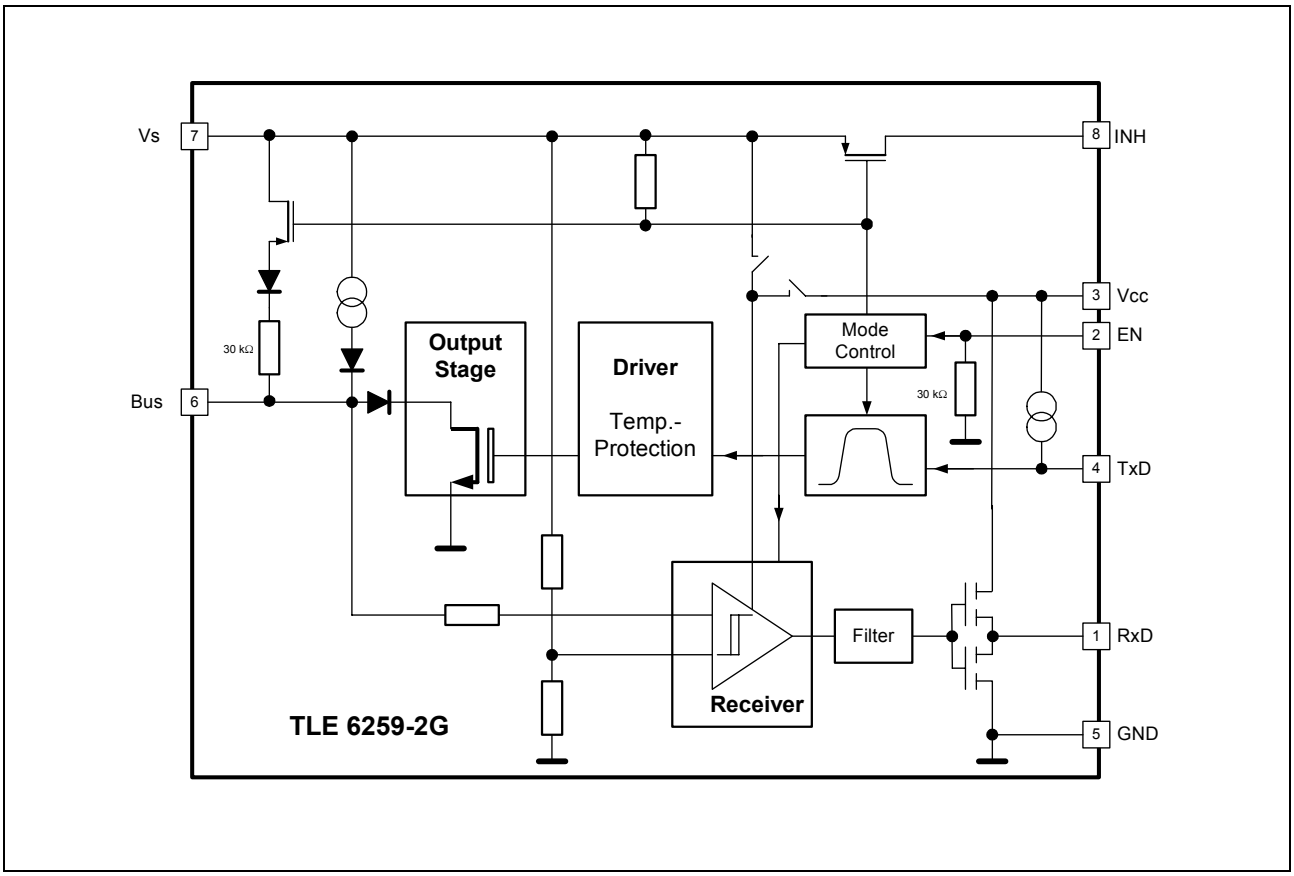


Figure 2

1.5 Application Information

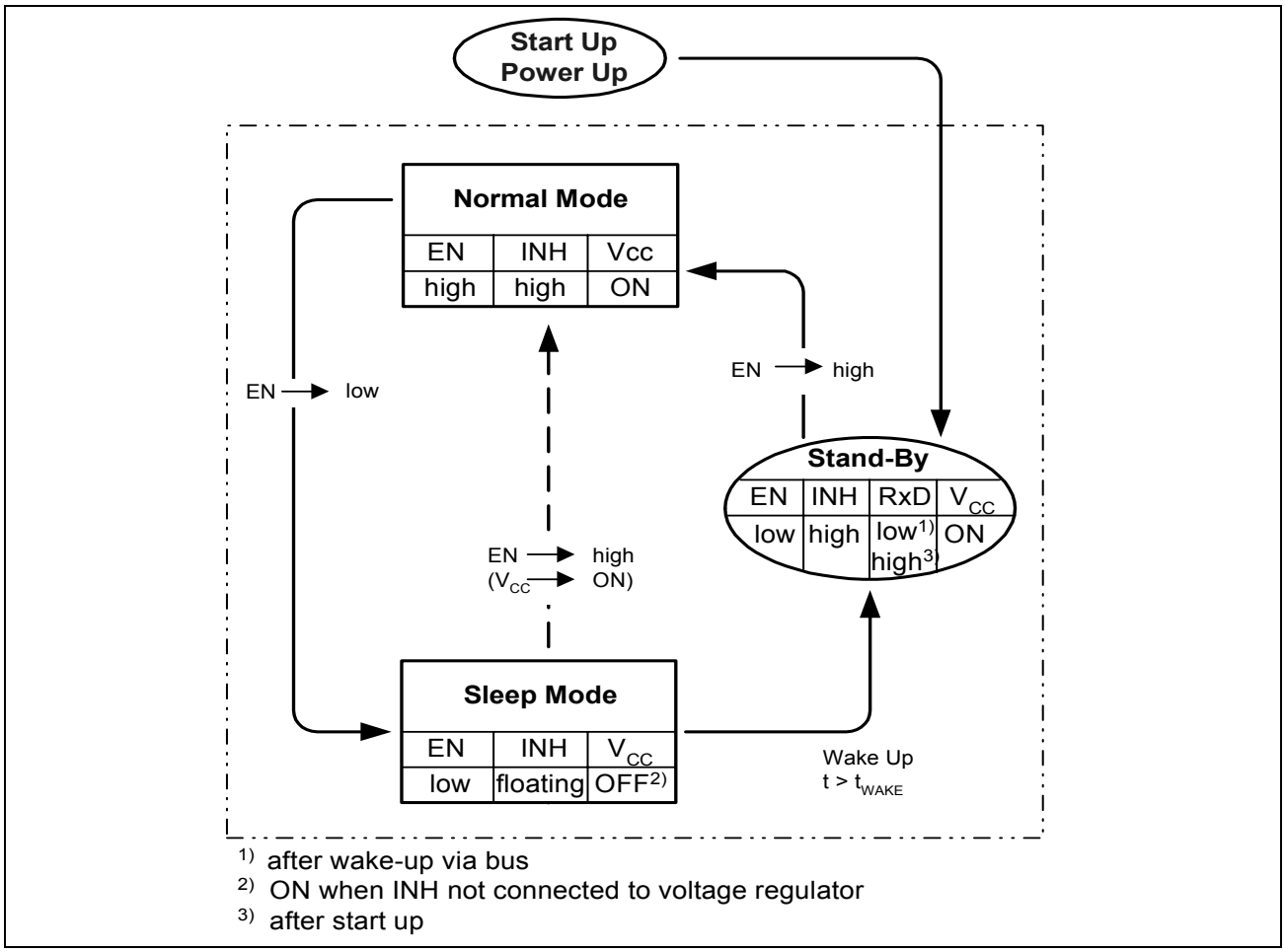


Figure 3: operation mode state diagram

Master Termination

For fail safe reasons, the TLE6259-2 already has a pull up resistor of 30kΩ implemented. To achieve the required timings for the dominant to recessive transition of the bus signal an additional external termination resistor of 1kΩ is required. It is recommended to place this resistor in the master node. To avoid reverse currents from the bus line into the battery supply line in case of an unpowered node, it is recommended to place a diode in series to the external pull up. For small systems (low bus capacitance) the EMC performance of the system is supported by an additional capacitor of at least 1nF in the master node (see figure 6 and 7, application circuit).

External Capacitors

An capacitor of 22µF at the supply voltage input V_S buffers the input voltage. In combination with the required reverse polarity diode this prevents the device from detecting power down conditions in case of negative transients on the supply line.

The 100nF capacitors close to the V_S pins of the 6259-2 and the voltage regulator help to improve the EMC behavior of the system.

Sleep Mode

In order to reduce the current consumption the TLE 6259-2 offers a sleep operation mode. This mode is selected by switching the enable input EN low (see figure 3, state diagram). In the sleep mode, a voltage regulator can be controlled via the INH output in order to minimize the current consumption of the whole application. A wake-up caused by a message on the communication bus, automatically enables the voltage regulator by switching the INH output high. In parallel the wake-up is indicated by setting the RxD output LOW. When entering the normal mode this wake-up flag is reset and the RxD output is released to transmit the bus data.

In case the voltage regulator control input is not connected to INH output or the microcontroller is active respectively, the TLE6259-2 can be set in normal operation mode without a wake-up via the communication bus.

Bus Short to GND Feature

The TLE6259-2 also has a BUS short to GND feature implemented, in order to protect the battery from running out of charge. A normal master termination connection like described above, 1kΩ resistor and diode between bus and V_S, whould cause a constantly drawn current via this path. The resulting resistance of this short to GND is lower than 1kΩ. To avoid this current during a generator off state, like a parked car, the sleep mode has a bus short to GND feature implemented in the 6259-2. This feature is only applicable, if the master termination is connected with the INH pin, instead of the V_S. For a more detailed information see the application circuit in figure 6 and 7.

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_{CC}	-0.3	6	V	
Battery supply voltage	V_S	-0.3	40	V	
Bus input voltage	V_{bus}	-20	32	V	
Bus input voltage	V_{bus}	-20	40	V	t < 1s
Logic voltages at EN, TxD, RxD	V_I	-0.3	V_{CC} + 0.3	V	0 V < V_{CC} < 5.5 V
Input voltages at INH	V_{INH}	-0.3	V_S + 0.3	V	
Output current at INH	I_{INH}		20	mA	
Electrostatic discharge voltage at Vs, Bus	V_{ESD}	-4	4	kV	human body model (100 pF via 1.5 kΩ)
Electrostatic discharge voltage	V_{ESD}	-2	2	kV	human body model (100 pF via 1.5 kΩ)
Temperatures					
Junction temperature	T_j	-40	150	°C	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

2.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{CC}	4.5	5.5	V	
Battery Supply Voltage	V_S	6	35	V	
Junction temperature	T_j	– 40	150	°C	–

Thermal Resistances

Junction ambient	$R_{thj\text{-}a}$	–	185	K/W	–

Thermal Shutdown (junction temperature)

	Symbol	Limit Values			Unit
		min.	typ.	max.	
Thermal shutdown temp.	T_{jSD}	150	170	190	°C
Thermal shutdown hyst.	ΔT	–	10	–	K

2.3 Electrical Characteristics

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 27 V; R_L =500 Ω; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Current Consumption						
Current consumption inNormal Mode	I_{CC}		0.3	0,7	mA	recessive state; $V_{TxD} = V_{CC}$
			0.4	0.8	mA	dominant state; V_{TxD} = 0 V
	I_S		0.8	1.5	mA	recessive state, without R_{load}; $V_{TxD} = V_{CC}$
			1.3	2	mA	dominant state, without R_{load}; V_{TxD} = 0 V
Current consumption in Standby Mode	I_{CC}		3	10	µA	external VR activated INH=H
	I_S		18	30	µA	
Current consumption in Sleep Mode	I_{CC}		-	-	µA	external VR deactivated INH=L
	I_S		18	30	µA	

2.3 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 27 V; R_L =500 Ω; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Receiver Output R×D						
HIGH level output current	$I_{RD,H}$	-1.2	-0.8	-0.5	mA	V_{RD} = 0.8 x V_{CC},
LOW level output current	$I_{RD,L}$	0.5	0.8	1.2	mA	V_{RD} = 0.2 x V_{CC},
Transmission Input T×D						
HIGH level input voltage threshold	$V_{TD,H}$		2.9	0.7 x V_{CC}	V	recessive state
TxD input hysteresis	$V_{TD,hys}$	300	700	900	mV	
LOW level input voltage threshold	$V_{TD,L}$	0.3 x V_{CC}	2.1		V	dominant state
TxD pull up current	I_{TD}	-150	-110	-70	µA	V_{TxD}<0.3Vcc
Enable input (pin EN)						
HIGH level input voltage threshold	$V_{EN,on}$		2.8	0.7 x V_{CC}	V	normal mode
LOW level input voltage threshold	$V_{EN,off}$	0.3 x V_{CC}	2.2		V	low power mode
EN input hysteresis	$V_{EN,hys}$	300	600	900	mV	
EN pull down resistance	R_{EN}	15	30	60	kΩ	
Inhibit output (pin INH)						
Inhibit R_{on} resistance	R_{onINH}		65	120	Ω	I_{INH} = - 15 mA
Leakage current	$I_{INH,lk}$	- 5.0		5.0	µA	sleep mode; V_{INH} = 0 V

2.3 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 27 V; R_L =500 Ω; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Bus receiver						
Receiver threshold voltage, recessive to dominant edge	$V_{bus,rd}$	0.44 x V_S	0.5 x V_S		V	-8V<V_{bus}<$V_{bus,dom}$
Receiver threshold voltage, dominant to recessive edge	$V_{bus,dr}$		0.56 x V_S	0.6 x V_S	V	$V_{bus,rec}$<V_{bus}<20 V
Receiver hysteresis	$V_{bus,hys}$	0.02 x V_S	0.04 x V_S	0.1 x V_S	mV	$V_{bus,hys}$ = $V_{bus,rec}$ - $V_{bus,dom}$
wake-up threshold voltage	V_{wake}	0.40 x V_S	0.5 x V_S	0.6 x V_S	V	
Bus transmitter						
Bus recessive output voltage	$V_{bus,rec}$	0.9 x V_S		V_S	V	V_{TxD} = V_{CC}
Bus dominant output voltage	$V_{bus,dom}$			0.15 x V_S	V	V_{TxD} = 0 V; 8V<V_S<27V
				1.2	V	6V<V_S<8V
Bus short circuit current	$I_{bus,sc}$	40	100	150	mA	$V_{bus,short}$ = 13.5 V
Leakage current	$I_{bus,lk}$	-150	-70		µA	V_{CC} = 0 V, V_S = 0 V, V_{bus} = -8 V
			10	25	µA	V_{CC} = 0 V, V_S = 0 V, V_{bus} = 20 V
				10	µA	V_{LIN}=V_S=13,5V
Bus pull up resistance	R_{bus}	20	30	47	kΩ	Normal mode
Lin output current	I_{lin}	5	30	60	µA	Sleep mode

2.3 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 27 V; R_L =500 Ω; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Dynamic Transceiver Characteristics						
Slope fall time	t_{fslope}			22,5	µs	100% > V_{bus} > 0% C_{bus}= 10 nF; R_L=500Ω V_{CC} = 5 V; V_S = 13.5 V
Slope rise time	t_{rslope}			22,5	µs	0% > V_{bus} >10 0% C_{bus}= 10 nF; R_L=500Ω V_{CC} = 5 V; V_S = 13.5 V
Slope symmetry	$t_{slopesym}$	-5		5	µs	t_{fslope}-t_{rslope}
Slope fall time	t_{fslope}			22.5	µs	100% > V_{bus} > 0% C_{bus}= 6,8nF;R_L=660Ω $T_{ambient}$ < 85 °C; V_{CC} = 5 V; V_S = 13.5 V
Slope rise time	t_{rslope}			22.5	µs	0% > V_{bus} >100% C_{bus}= 6,8nF;R_L=660Ω V_{CC} = 5 V; V_S = 13.5 V
Slope symmetry	$t_{slopesym}$	-4		4	µs	t_{fslope}-t_{rslope}
Propagation delay TxD LOW to bus	$t_{d(L),T}$		1	3	µs	V_{CC} = 5 V
Propagation delay TxD HIGH to bus	$t_{d(H),T}$		1	3	µs	V_{CC} = 5 V
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$		1	6	µs	V_{CC} = 5V; C_{RxD} = 20pF
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$		1	6	µs	V_{CC} = 5 V; C_{RxD} = 20 pF
Receiver delay symmetry	$t_{sym,R}$	-2		2	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$
Transmitter delay symmetry	$t_{sym,T}$	-2		2	µs	$t_{sym,T}$ = $t_{d(L),T}$ - $t_{d(H),T}$
Wake-up delay time	t_{wake}	30	100	150	µs	$T_j \leq 125°$
				170	µs	$T_j \leq 150°$
Delay time for change sleep/ stand by mode-normal mode	t_{snorm}			10	µs	
Delay time for change normal mode - sleep mode	t_{nsleep}			10	µs	

3 Diagrams

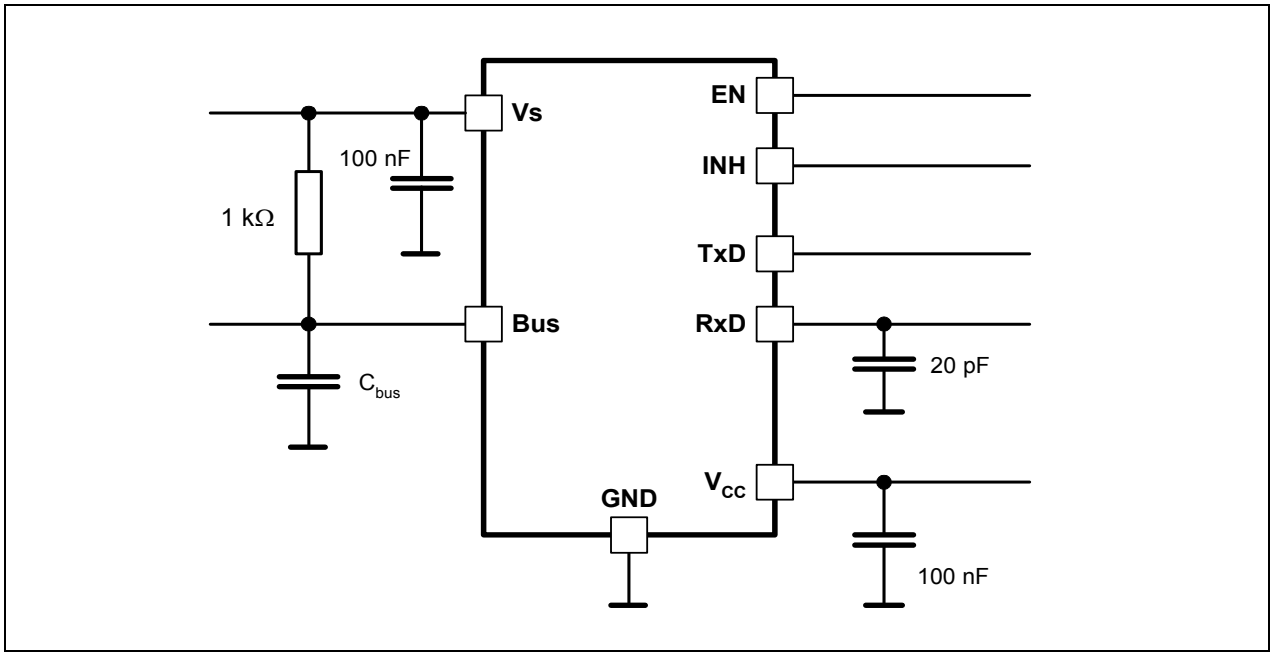


Figure 4: Test circuits

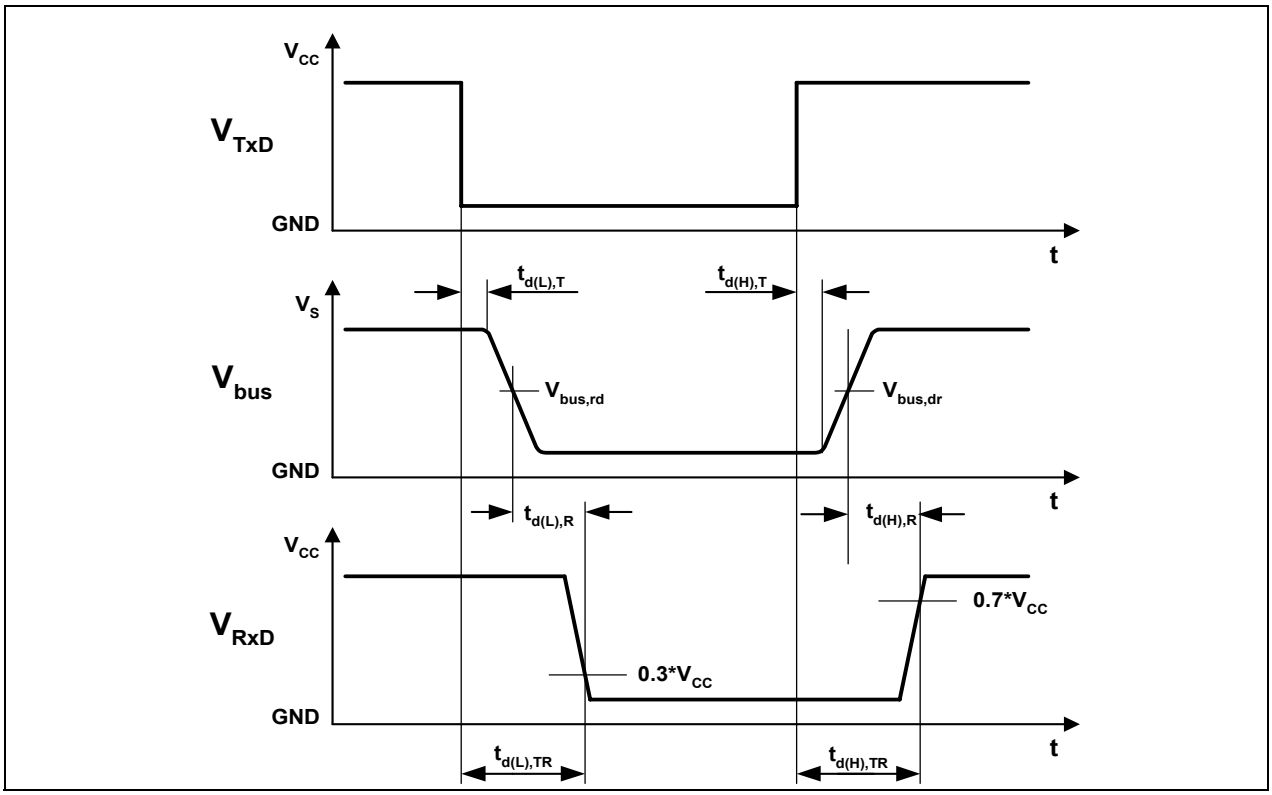


Figure 5: Timing diagrams for dynamic characteristics

4 Application

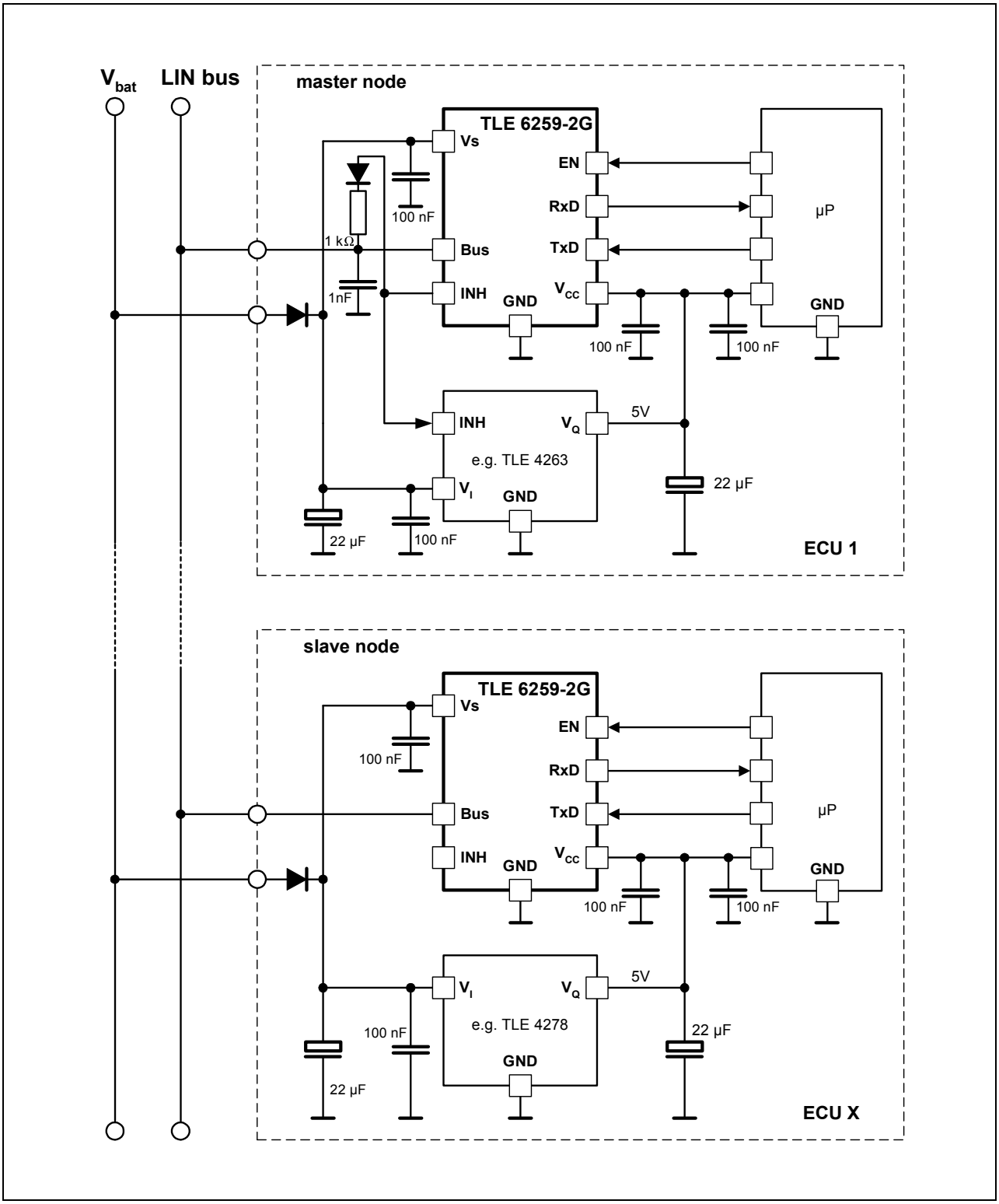


Figure 6
Application circuit with bus short to GND feature applied

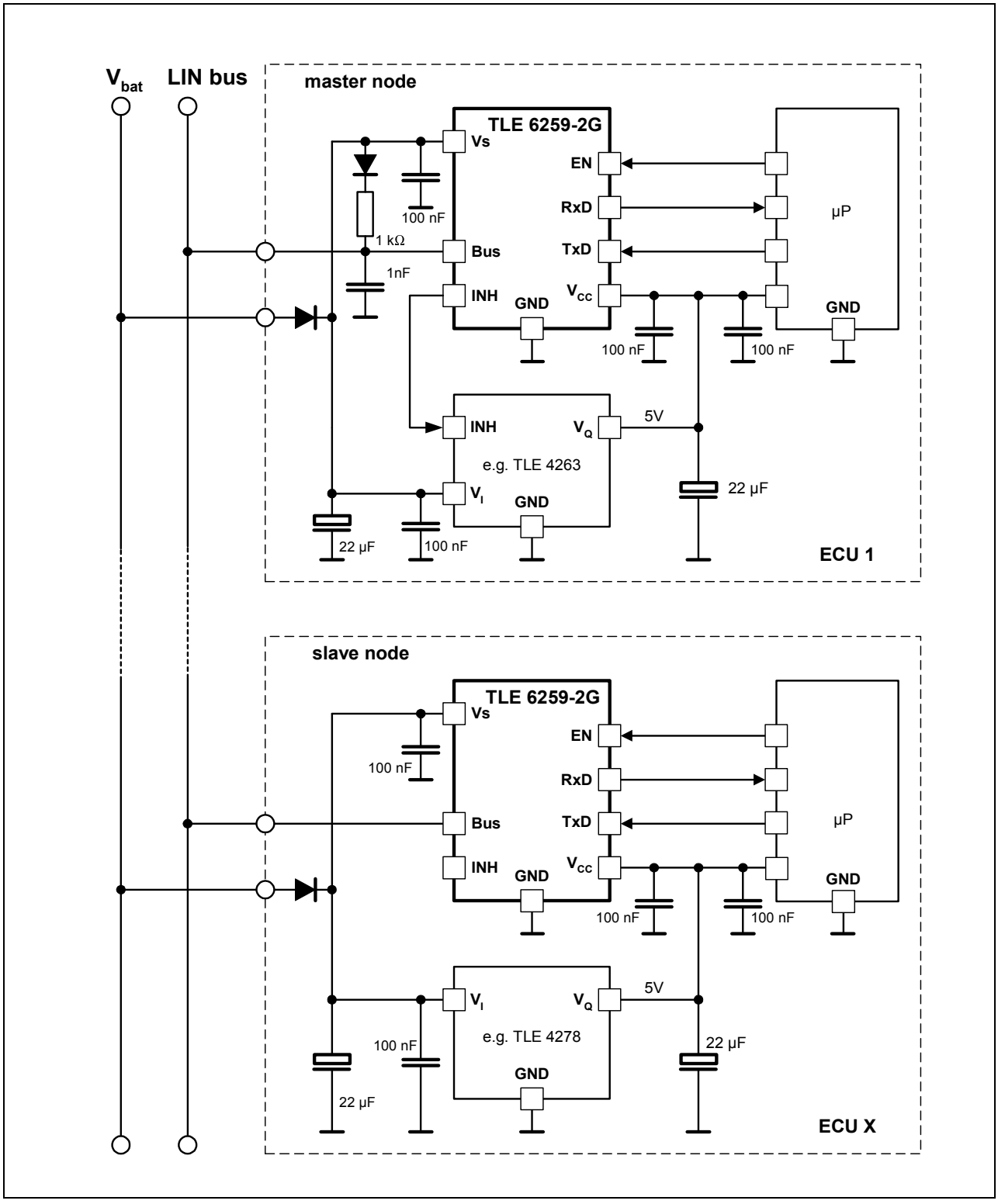
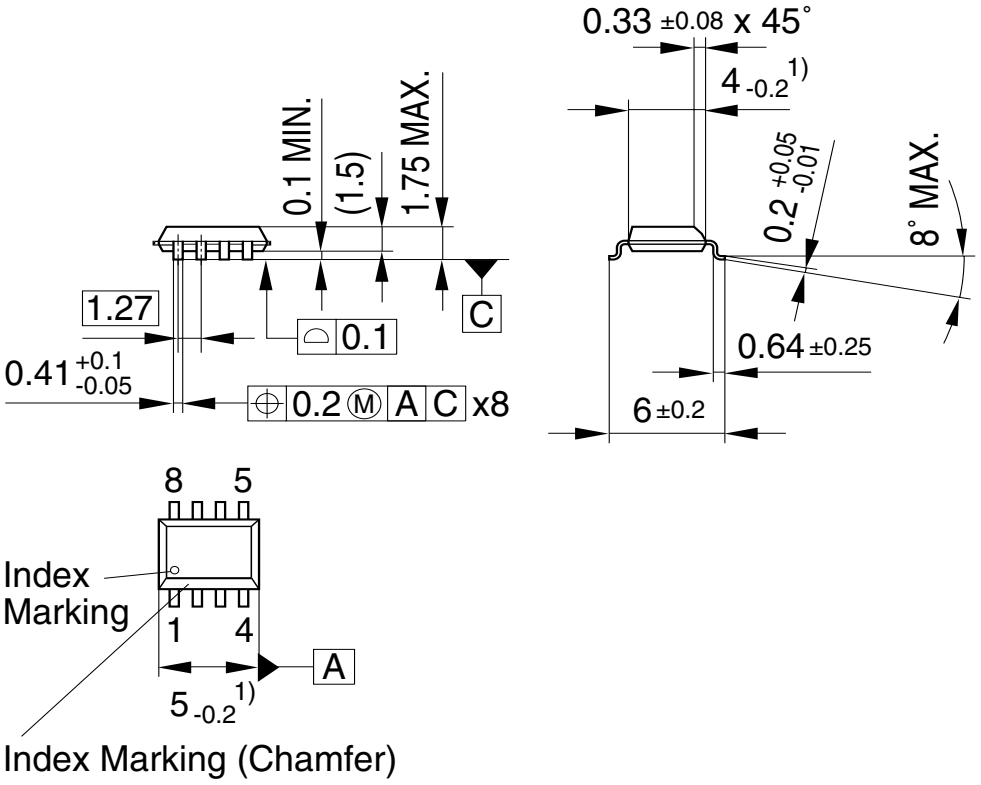


Figure 7
Application circuit without bus short to GND feature

5 Package Outlines

P-DSO-8-3
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

Edition 1999-10-12

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