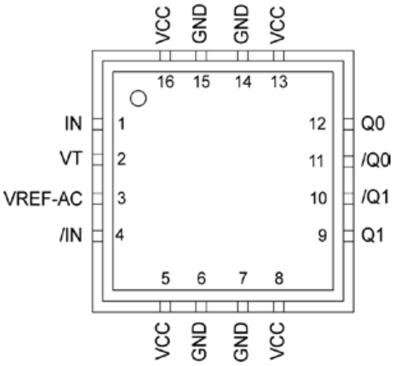
Ordering Information(1)

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89851UMG	QFN-16	Industrial	851U with Pb-Free bar-line indicator	Pb-Free NiPdAU
SY89851UMGTR(2)	QFN-16	Industrial	851U with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



16-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
1,4	IN, /IN	Differential Inputs: This input pair is the differential signal input to the device. Inputs accept AC- or DC-coupled signals as small as 100mV (200mV$_{pp}$). Each pin terminates to a V$_T$ pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the "Input Interface Applications" section for more details.
2	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to a V$_T$ pin. The V$_T$ pins provide a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.
3	VREF-AC	Reference Voltage: This output biases to V$_{CC}$–1.2V. It is used when AC-coupling the inputs (IN, /IN). For AC-coupled applications, connect V$_{REF-AC}$ to the V$_T$ pin and bypass with a 0.01µF low ESR capacitor to V$_{CC}$. Maximum sink/source current is ±1.5mA. See “Input Interface Applications” section for more details.
5,8,13,16	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors and place as close to each V$_{CC}$ pin as possible.
12,11 9,10	Q0, /Q0, Q1, /Q1	Differential Outputs: These 100K LVPECL-compatible output pairs are the precision, low skew copies of the inputs. Unused output pairs may be left open. Terminate with 50Ω to V$_{CC}$–2V. See “LVPECL Output Interface Application” section for more details.
6,7,14,15	GND, Exposed Pad	Ground. GND and exposed pad must both be connected to the same ground plane.

Absolute Maximum Ratings(1)

Supply Voltage (V_{CC})	–0.5V to +4.0V
Input Voltage (IN, /IN)	–0.5V to V_{CC}
LVPECL Output Current (I_{OUT})	
Continuous	±50mA
Surge	±100mA
Termination Current	
Source or sink current on V_T	±100mA
V_{REF-AC} Current	
Source or sink current	±2mA
Input Current	
Source or sink current on IN, /IN	±50mA
Lead Temperature (soldering, 20sec.)	+260°C
Storage Temperature (T_s)	–65°C to 150°C

Operating Ratings(2)

Supply Voltage (V_{CC})	+2.375V to +2.625V
	+3.0V to +3.6V
Ambient Temperature (T_A)	–40°C to +85°C
Package Thermal Resistance(3)	
QFN (θ_{JA})	
Still-Air	60°C/W
QFN (ψ_{JB})	
Junction-to-Board	33°C/W

DC Electrical Characteristics(4)

TA = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375	2.5	2.625	V
			3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		32	45	mA
R_{IN}	Single-Ended Input Resistance (IN-to-V_T)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input High Voltage (IN, /IN)	Note 5	V_{CC} –1.6		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		V_{IH}-0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN-/IN|	See Figure 1b.	0.2			V
V_{T_IN}	IN-to-V_T (IN, /IN)				1.28	V
V_{REF-AC}	Output Reference Voltage		V_{CC} –1.3	V_{CC} –1.2	V_{CC} –1.1	V

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and ψ_{JB} values are for a 4-layer board in still air, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. V_{IH}(min) not lower than 1.2V

100K LVPECL Output DC Electrical Characteristics(6)

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to + 85°C; R_L = 50Ω to V_{CC} –2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage (Q, /Q)		V_{CC}–1.145		V_{CC}–0.895	V
V_{OL}	Output LOW Voltage (Q, /Q)		V_{CC}–1.945		V_{CC}–1.695	V
V_{OUT}	Output Voltage Swing (Q, /Q)	See Figure 1a.	550	800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing (Q, /Q)	See Figure 1b.	1100	1600		mV

Note:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics(7)

V_{CC} = 2.5V ±5% or 3.3V ±10%, R_L = 50Ω to V_{CC} –2V, $V_{IN} \geq$ 100mV (200mV$_{PP}$); T_A = –40°C to + 85°C, unless otherwise stated.

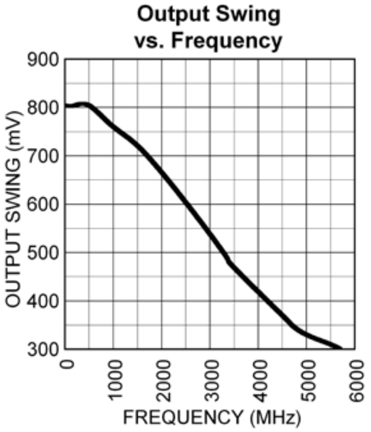
Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	2.5	3.5		Gbps
		Clock	3	4		GHz
t_{pd}	Differential Propagation Delay	IN-to-Q	140	220	340	ps
t_{pd} Tempco	Δt_{pd} Temperature Coefficient			130		fs/°C
t_{SKEW}	Output-to-Output Skew Part-to-Part Skew	Note 8 Note 9		6	20 120	ps ps
t_{JITTER}	Data Random Jitter	Note 10			1	ps$_{RMS}$
	Deterministic Jitter	Note 11			10	ps$_{PP}$
	Clock Cycle-to-Cycle Jitter	Note 12			1	ps$_{RMS}$
	Total Jitter	Note 13			10	ps$_{PP}$
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At full output swing	50	100	180	ps

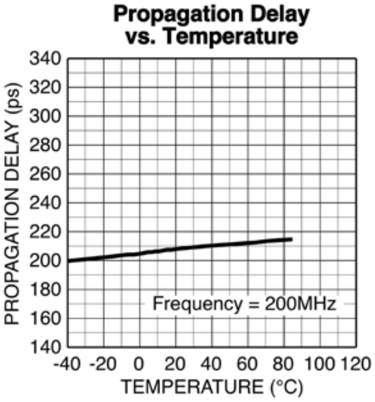
Notes:

7. High-frequency AC-parameters are guaranteed by design and characterization.
8. Output-to-output skew is measured between two different outputs under identical input transitions.
9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
10. Random jitter is measured with a K28.7 character pattern, measured at 2.5Gbps.
11. Deterministic jitter is measured at 2.5Gbps, with both K28.5 and $2^{23} – 1$ PRBS pattern.
12. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n – T_{n-1}$ where T is the time between rising edges of the output signal.
13. Total jitter definition: with an ideal clock input of frequency <f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

Typical Operating Characteristics

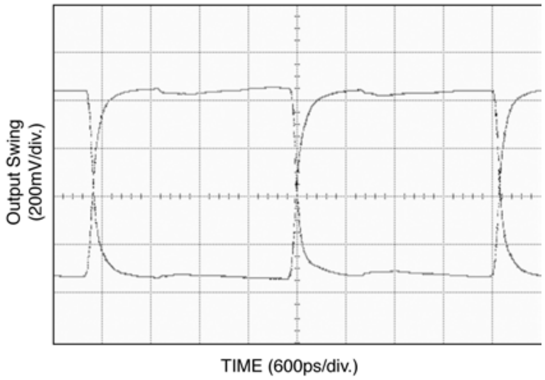
V_{CC} = 3.3V, GND = 0V, V_{IN} = 100mV (200mV_{PP}), R_L = 50Ω to V_{CC} –2V, T_A = 25°C, unless otherwise stated.

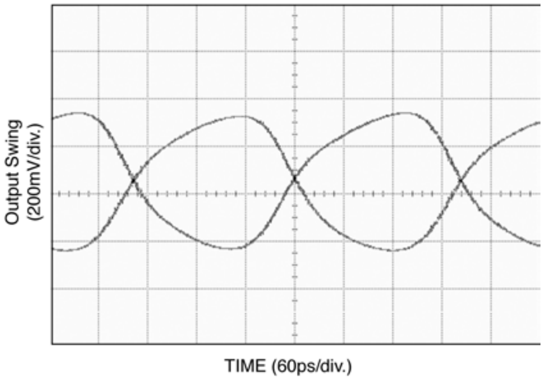


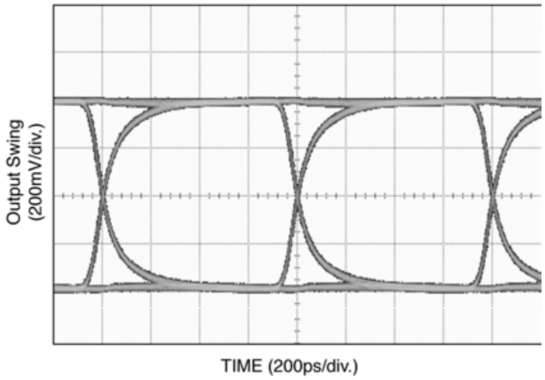


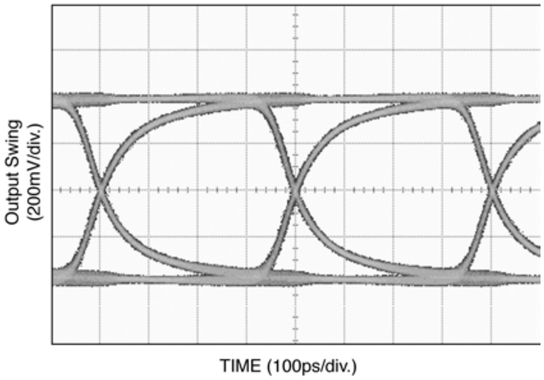
Functional Characteristics

V_{CC} = 3.3V, GND = 0V, V_{IN} = 100mV (200mV_{PP}), R_L = 50Ω to V_{CC} –2V, T_A = 25°C, unless otherwise stated.


200MHz Output


2.5GHz Output


1.25Gbps Output


2.5Gbps Output

Single-Ended and Differential Swings

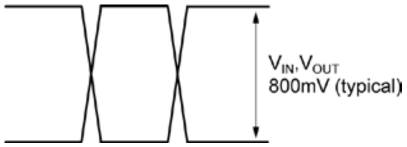


Figure 1a. Single-Ended Voltage Swing

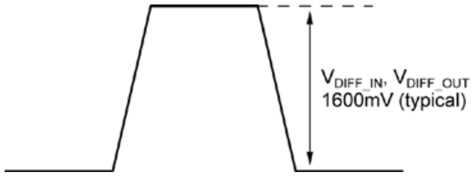
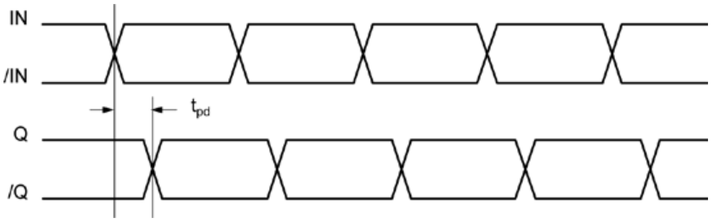


Figure 1b. Differential Voltage Swing

Timing Diagrams



Input and Output Stages

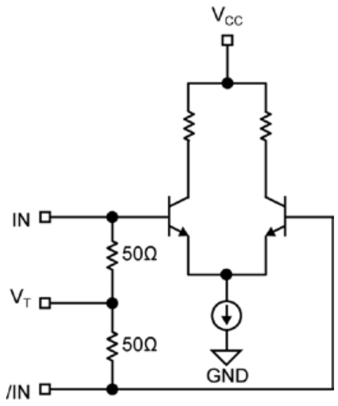


Figure 2a. Simplified Differential Input Stage

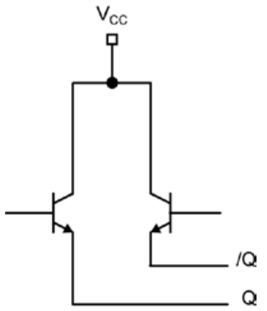
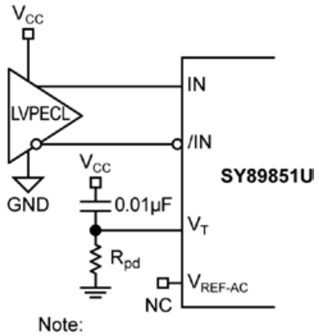


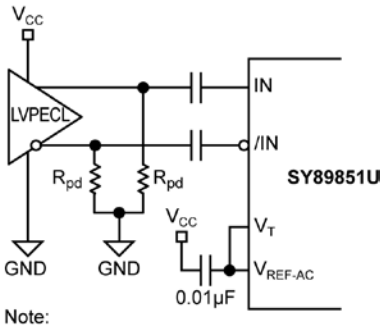
Figure 2b. Simplified LVPECL Output Stage

Input Interface Applications



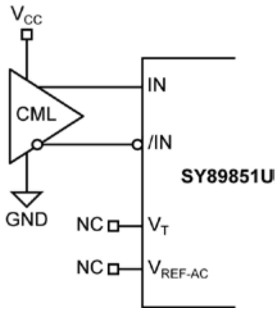
Note:
For 3.3V, R_{pd} = 50Ω.
For 2.5V, R_{pd} = 19Ω.

Figure 3a. LVPECL Interface (DC-Coupled)



Note:
For 3.3V, R_{pd} = 100Ω.
For 2.5V, R_{pd} = 50Ω.

Figure 3b. LVPECL Interface (AC-Coupled)



Optional: may connect V_T to V_{CC}

Figure 3c. CML Interface (DC-Coupled)

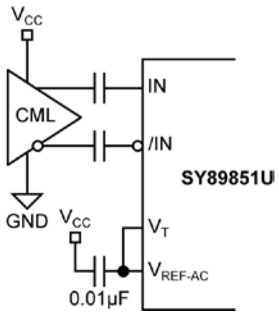


Figure 3d. CML Interface (AC-Coupled)

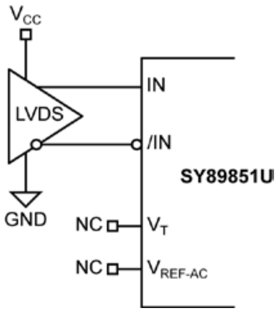
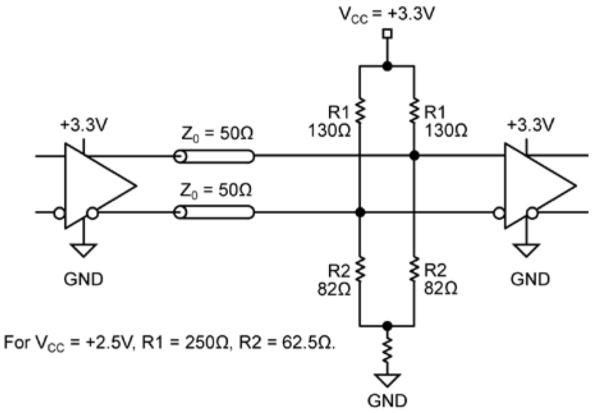


Figure 3e. LVDS Interface

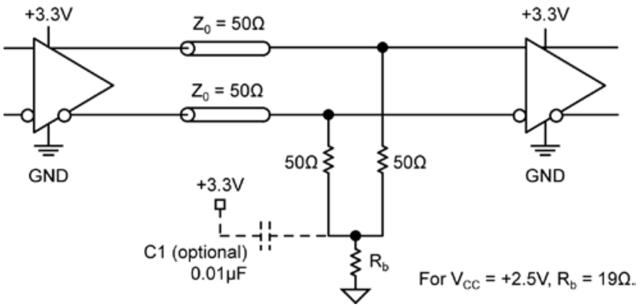
LVPECL Output Interface Applications

LVPECL has high input impedance, very low output (open emitter) impedance, and small signal swing which result in low EMI. LVPECL is ideal for driving 50Ω- and 100Ω-controlled impedance transmission lines. There are several techniques for terminating the LVPECL output including: Parallel Termination-Thevenin Equivalent, Parallel Termination (3-Resistor), and AC-Coupled Termination. Unused output pairs may be left floating. However, single-ended outputs must be terminated, or balanced.



For V_{CC} = +2.5V, R1 = 250Ω, R2 = 62.5Ω.

Figure 4a. Parallel Thevenin-Equivalent Termination



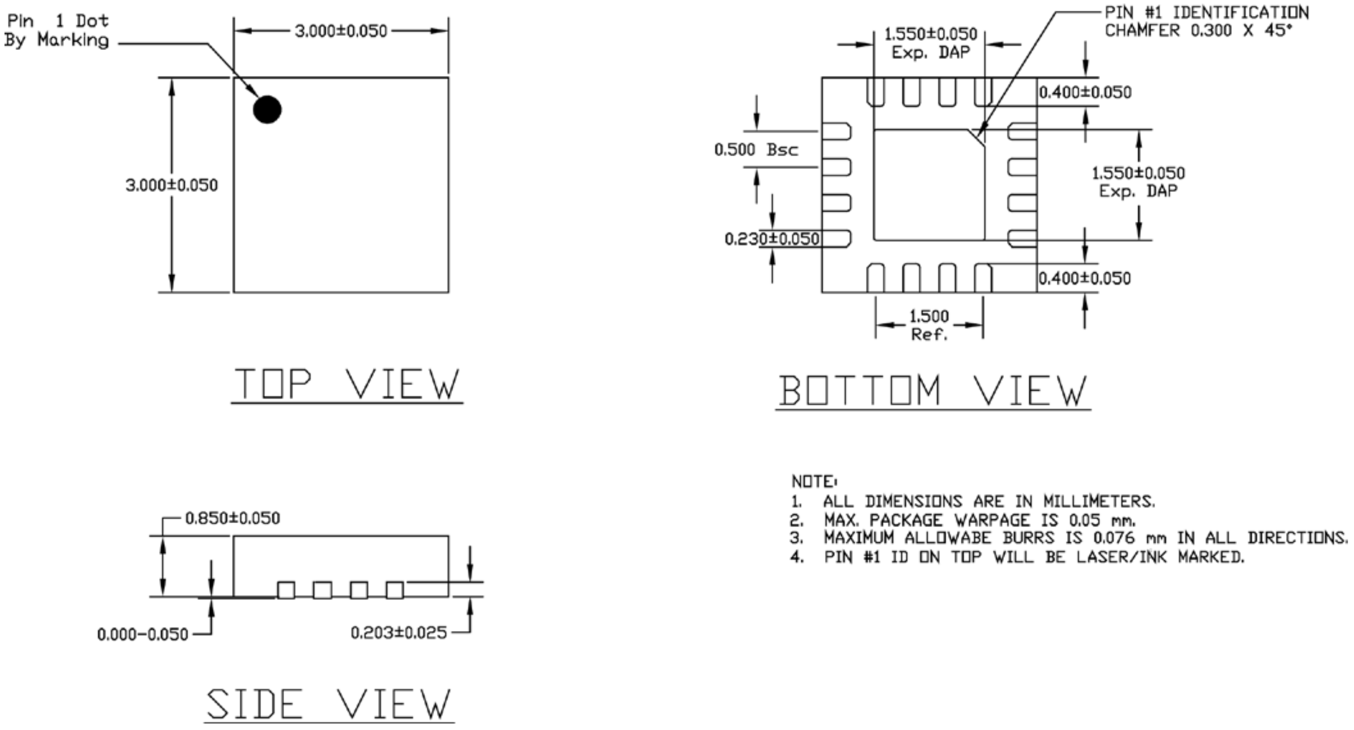
For V_{CC} = +2.5V, R_b = 19Ω.

Figure 4b. Parallel Termination (3-Resistor)

Related Product and Support Documentation

Part Number	Function	Data Sheet Link
SY58012U	5GHz, 1:2 LVPECL Fanout Buffer/Translator with Internal Input Termination	www.micrel.com/product-info/products/sy58012u.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

Package Information



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

16-Pin QFN

Package Notes:

1. Package meets Level 2 Moisture Sensitivity Classification.
2. All parts are dry-packaged before shipment.
3. Exposed pad must be soldered to a ground for proper thermal management.

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