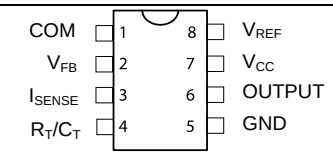
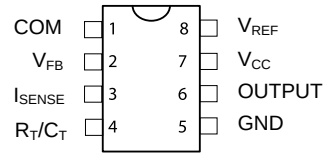
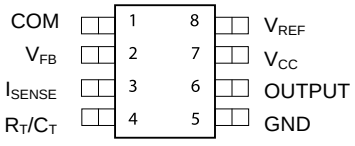
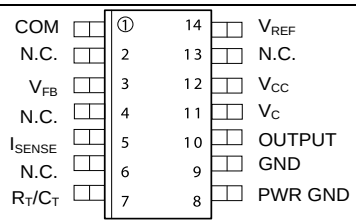
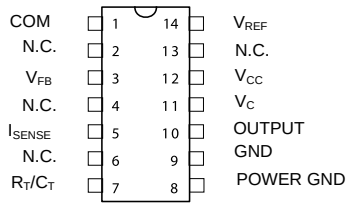
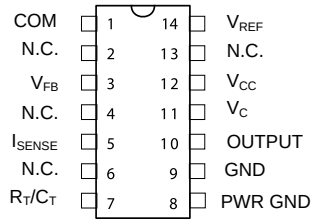
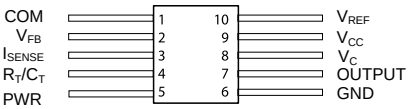
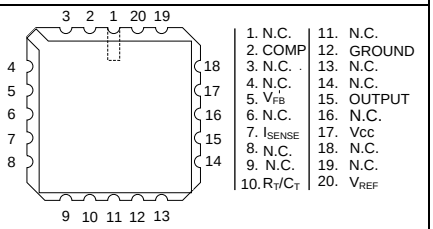
Connection Diagrams and Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type	Connection Diagram
0°C to 70°C	M	8-PIN PLASTIC DUAL INLINE PACKAGE	SG3842M	Plastic DIP	 **M PACKAGE** (Top View) **M Package**: RoHS / Pb-free 100% Matte Tin Lead Finish
			SG3843M		
-25°C to 85°C			SG2842M		
			SG2843M		
0°C to 70°C	Y	8-PIN CERAMIC DUAL INLINE PACKAGE	SG3842Y	CERDIP	 **Y PACKAGE** (Top View) PbSn Tin Lead Finish
			SG3843Y		
-25°C to 85°C			SG2842Y		
			SG2843Y		
-55°C to 125°C			SG1842Y		
			SG1843Y		
MIL-STD/883			SG1842Y-883B		
			SG1843Y-883B		
DESC			SG1842Y-DESC		
			SG1843Y-DESC		
0°C to 70°C	DM	8-PIN SMALL OUTLINE INTEGRATED CIRCUIT	SG3842DM	SOIC	 **DM PACKAGE** (Top View) RoHS / Pb-free 100% Matte Tin Lead Finish
			SG3843DM		
-25°C to 85°C			SG2842DM		
			SG2843DM		
0°C to 70°C	D	14-PIN SMALL OUTLINE INTEGRATED CIRCUIT	SG3842D	SOIC	 **D PACKAGE** (Top View) RoHS / Pb-free 100% Matte Tin Lead Finish
			SG3843D		
-25°C to 85°C			SG2842D		
			SG2843D		
0°C to 70°C	N	14-PIN DUAL INLINE PLASTIC PACKAGE	SG3842N	PLASTIC DIP	 **N PACKAGE** (Top View) **N Package**: RoHS / Pb-free 100% Matte Tin Lead Finish
			SG3843N		
-25°C to 85°C			SG2842N		
			SG2843N		

Connection Diagrams and Ordering Information *(continued)*

Ambient Temperature	Type	Package	Part Number	Packaging Type	Connection Diagram
-55°C to 125°C	J	14-PIN CERAMIC DUAL INLINE PACKAGE	SG1842J	CERDIP	 **J PACKAGE** (Top View) **PbSn** Lead Finish
			SG1843J		
MIL-STD/883			SG1842J-883B		
			SG1843J-883B		
DESC			SG1842J-DESC		
			SG1843J-DESC		
-55°C to 125°C	F	10-PIN CERAMIC FLAT PACK PACKAGE	SG1842F	FLAT PACK	 **F PACKAGE** (Top View) PbSn Lead Finish
			SG1843F		
MIL-STD/883			SG1842F-883B		
			SG1843F-883B		
DESC			SG1842F-DESC		
			SG1843F-DESC		
-55°C to 125°C	L	20-PIN CERAMIC	SG1842L	Ceramic Leadless Chip Carrier (LCC)	 **L PACKAGE** (Top View) PbSn Lead Finish
			SG1843L		
MIL-STD/883			SG1842L-883B		
			SG1843L-883B		
DESC			SG1842L-DESC		
			SG1843L-DESC		

Notes:
1. Contact factory for JAN and DESC part availability.
2. All parts are viewed from the top.
3. Available in Tape & Reel. Append the letters "TR" to the part number (SG3842N-TR).

Absolute Maximum Ratings[1 - 2]

Parameter	Value	Units
Supply Voltage (I_{CC} < 30mA)	Self-limiting	V
Supply Voltage (Low Impedance Source)	30	V
Output Current (Peak)	±1	A
Output Current (Continuous)	350	mA
Output Energy (Capacitive Load)	5	µJ
Analog Inputs (V_{FB}, I_{SENSE})	-0.3 to +6.3	V
Error Amplifier Output Sink Current	10	mA
Power Dissipation at T_A = 25°C (DIL-8)	1	W
Operating Junction Temperature		
Hermetic (J, Y, F, L Packages)	150	°C
Plastic (N, M, D, DM Packages)	150	°C
Storage Temperature Range	-65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)	300	°C
RoHS / Pb-free Peak Package Solder Reflow Temp. (40 second max. exposure)	260 (+0, -5)	°C

Notes:
1. *Exceeding these ratings could cause damage to the device.*
2. *All voltages are with respect to Pin 5. All currents are positive into the specified terminal.*

Thermal Data

Parameter	Value	Units
M Package:		
Thermal Resistance-Junction to Ambient, θ_{JA}	95	°C/W
N Package:		
Thermal Resistance-Junction to Ambient, θ_{JA}	65	°C/W
DM Package:		
Thermal Resistance-Junction to Ambient, θ_{JA}	165	°C/W
D Package:		
Thermal Resistance-Junction to Ambient, θ_{JA}	120	°C/W
Y Package:		
Thermal Resistance-Junction to Ambient, θ_{JA}	130	°C/W
J Package		
Thermal Resistance-Junction to Ambient, θ_{JA}	80	°C/W
F Package		
Thermal Resistance-Junction to Case, θ_{JC}	80	°C/W
Thermal Resistance-Junction to Ambient, θ_{JA}	145	°C/W
L Package		
Thermal Resistance-Junction to Case, θ_{JC}	35	°C/W
Thermal Resistance-Junction to Ambient, θ_{JA}	120	°C/W

Notes:
1. *Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.*
2. *The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.*

Recommended Operating Conditions

Symbol	Parameter	Recommended Operating Conditions			Units
		Min	Typ	Max	
V_S	Supply Voltage Range		30		V
I_{PK}	Output Current (Peak)		±1		A
I_{OUT}	Output Current (Continuous)		200		mA
	Analog Inputs (V_{FB}, I_{SENSE})	0		2.6	V
EA_{SINK}	Error Amp Output Sink Current		5		mA
OSC_{FR}	Oscillator Frequency Range	0.1		500	kHz
R_T	Oscillator Timing Resistor	0.52		150	kΩ
C_T	Oscillator Timing Capacitor	0.001		1.0	µF
Operating Ambient Temperature Range					
	SG1842/43	-55		125	°C
	SG2842/43	-25		85	°C
	SG3842/43	0		70	°C

Note: Range over which the device is functional.

Electrical Characteristics

Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1842/SG1843 with -55°C ≤ T_A ≤ 125°C, SG2842/SG2843 with -25°C ≤ T_A ≤ 85°C, SG3842/SG3843 with 0°C ≤ T_A ≤ 70°C, V_{CC} = 15V, R_T = 10kΩ, and C_T = 3.3nF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

Symbol	Parameter	Test Conditions	SG1842/43			SG2842/43			SG3842/43			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Section												
V_{REF}	Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	4.95	5.00	5.05	4.90	5.00	5.10	V
V_{REG}	Line Regulation	12V ≤ V_{IN} ≤ 25V		6	20		6	20		6	20	mV
I_{REG}	Load Regulation	1 ≤ I_O ≤ 20mA		6	25		6	25		6	25	mV
	Temperature Stability[1]			0.2	0.4		0.2	0.4		0.2	0.4	mV/°C
	Total Output Variation[1]	Line, Load, Temperature	4.90		5.10	4.90		5.10	4.82		5.18	V
V_N	Output Noise Voltage[1]	10Hz ≤ f ≤ 10kHz, T_J = 25°C		50			50			50		µV
	Long Term Stability[1]	T_A = 125°C, 1000hrs		5	25		5	25		5	25	mV
V_{REFOSC}	Output Short Circuit		-30	-100	-180	-30	-100	-180	-30	-100	-180	mA
Oscillator Section[3]												
f	Initial Accuracy[5]	T_J = 25°C	47	52	57	47	52	57	47	52	57	kHz
f_{REG}	Voltage Stability	12V ≤ V_{CC} ≤ 25V		0.2	1		0.2	1		0.2	1	%
	Temperature Stability[1]	T_{MIN} ≤ T_A ≤ T_{MAX}		5			5			5		%
OSC_{PP}	Amplitude	$V_{RT/CT}$ (Peak to Peak)		1.7			1.7			1.7		V
I_{DSG}	Discharge Current	T_J = 25°C	7.8	8.3	8.8	7.5	8.4	9.3	7.5	8.4	9.3	mA
		T_{MIN} ≤ T_A ≤ T_{MAX}	7.0		9.0	7.2		9.5	7.2		9.5	mA
Error Amp Section												
EA_{IN}	Input Voltage	V_{COMP} = 2.5V	2.45	2.50	2.55	2.45	2.50	2.55	2.42	2.50	2.58	V
EA_{IB}	Input Bias Current			-0.3	-1		-0.3	1		-0.3	-2	µA
A_{VOL}	Open Loop Gain	2V ≤ V_O ≤ 4V	65	90		65	90		65	90		dB
EA_{BW}	Unity Gain Bandwidth[1]	T_J = 25°C	0.7	1		0.7	1		0.7	1		MHz
PSRR	Power Supply Rejection Ratio	12V ≤ V_{CC} ≤ 25V	60	70		60	70		60	70		dB
EA_{SINK}	Output Sink Current	V_{VFB} = 2.7V, V_{COMP} = 1.1V	2	6		2	6		2	6		mA
EA_{SRC}	Output Source Current	V_{VFB} = 2.3V, V_{COMP} = 5V	-0.5	-0.8		-0.5	-0.8		-0.5	-0.8		mA
EA_{VOH}	V_{OUT} High	V_{VFB} = 2.3V, R_L = 15k to GND	5	6		5	6		5	6		V
EA_{VOL}	V_{OUT} Low	V_{VFB} = 2.7V, R_L = 15k to V_{REF}		0.7	1.1		0.7	1.1		0.7	1.1	V

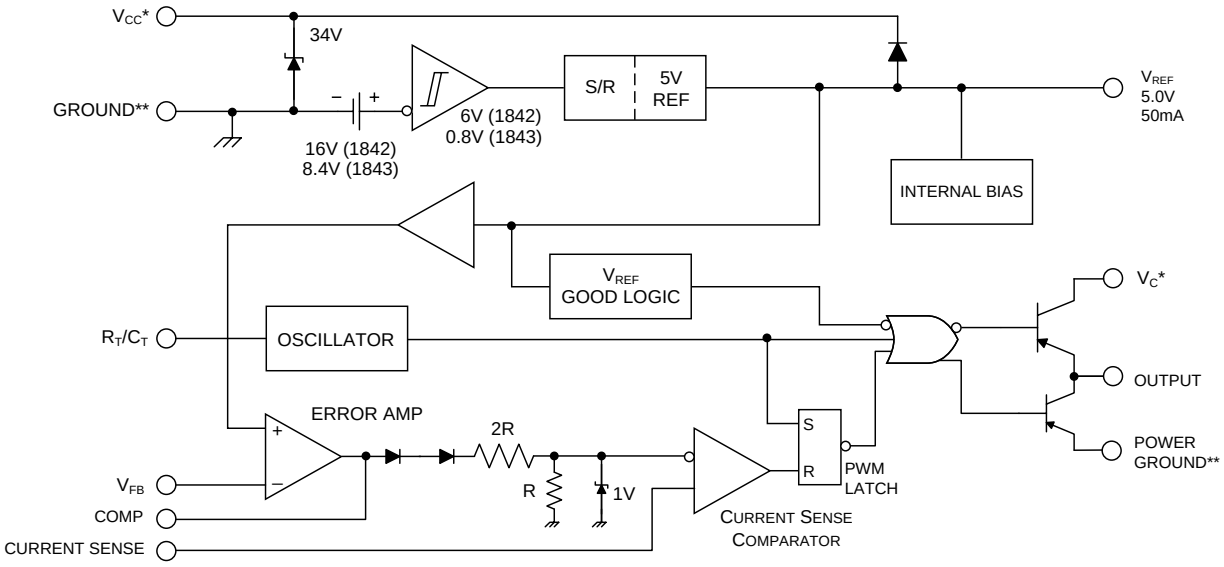
Electrical Characteristics *(continued)*

Symbol	Parameter	Test Conditions	SG1842/43			SG2842/43			SG3842/43			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Current Sense Section												
CS_{AVOL}	Gain [2, 3]		2.85	3	3.15	2.85	3	3.15	2.85	3	3.15	V/V
	Maximum Input Signal[2]	V_{COMP} = 5V	0.9	1	1.1	0.9	1	1.1	0.9	1	1.1	V
PSRR	Power Supply Rejection Ratio[2]	12V ≤ V_{CC} ≤ 25V		70			70			70		dB
CS_{IB}	Input Bias Current			-2	-10		-2	-10		-2	-10	µA
CS_{DELAY}	Delay to Output[1]			150	300		150	300		150	300	ns
Output Section												
V_{OL}	Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4		0.1	0.4	V
		I_{SINK} = 200mA		1.5	2.2		1.5	2.2		1.5	2.2	V
V_{OH}	Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		13	13.5		V
		I_{SOURCE} = 200mA	12	13.5		12	13.5		12	13.5		V
R_S	Rise Time	T_J = 25°C, C_L = 1nF		50	150		50	150		50	150	ns
F_T	Fall Time	T_J = 25°C, C_L = 1nF		50	150		50	150		50	150	ns
Under-Voltage Lockout Section												
UVLO	Start Threshold	1842/2842/3842	15	16	17	15	16	17	14.5	16	17.5	V
		1843/2843/3843	7.8	8.4	9.0	7.8	8.4	9.0	7.8	8.4	9.0	V
V_{SMIN}	Min. Operation Voltage After Turn-On	1842/2842/3842	9	10	11	9	10	11	8.5	10	11.5	V
		1843/2843/3843	7.0	7.6	8.3	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section												
DC_{MAX}	Maximum Duty Cycle		93	95	100	90	95	100	90	95	100	%
DC_{MIN}	Minimum Duty Cycle				0			0			0	%
Power Consumption Section												
I_S	Start-Up Current			0.5	1		0.5	1		0.5	1	mA
I	Operating Supply Current	V_{FB} = V_{ISENSE} = 0V		11	17		11	17		11	17	mA
Z	V_{CC} Zener Voltage	I_{CC} = 25mA		34			34			34		V

Notes:

1. *These parameters, although guaranteed, are not 100% tested in production.*
2. *Parameter measured at trip point of latch with V_{VFB} = 0.*
3. *Gain defined as: $A = \Delta V_{COMP} / \Delta V_{ISENSE}$; $0 \le V_{ISENSE} \le 0.8V$*
4. *Adjust V_{CC} above the start threshold before setting at 15V.*

Block Diagram



* - V_{CC} and V_C are internally connected for 8-pin packages.
** - POWER GROUND and GROUND are internally connected for 8-pin packages.

Figure 2 · Block Diagram

Characteristic Curves

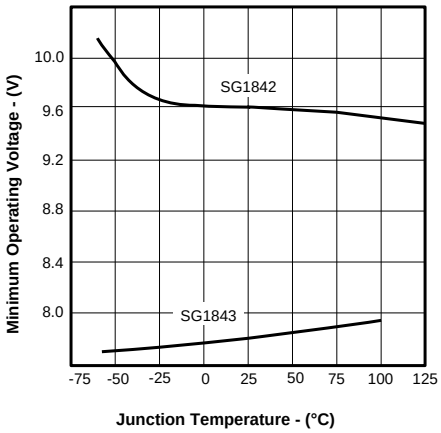


Figure 3 · Dropout Voltage vs. Temperature

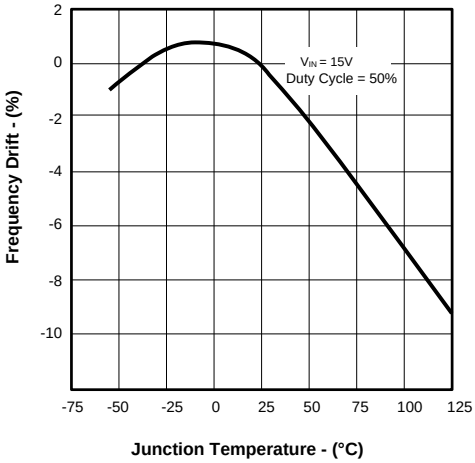


Figure 4 · Oscillator Temperature Stability

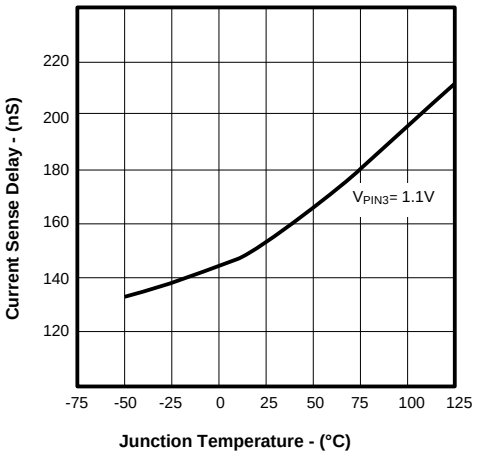


Figure 5 · Current Sense to Output Delay vs. Temperature

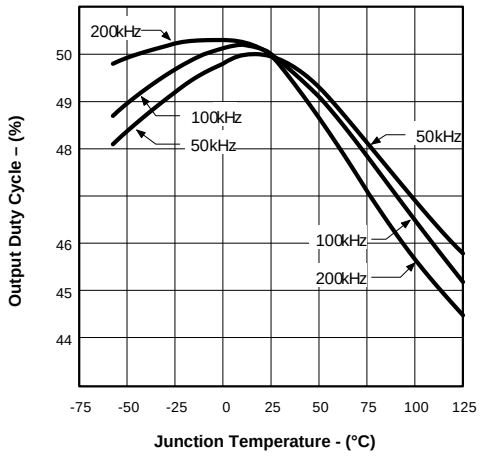


Figure 6 · Output Duty Cycle vs. Temperature

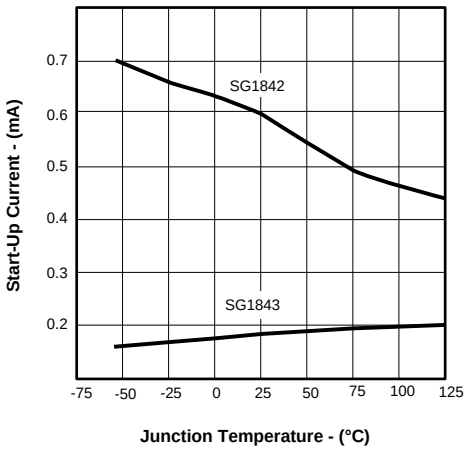


Figure 7 · Start-Up Current vs. Temperature

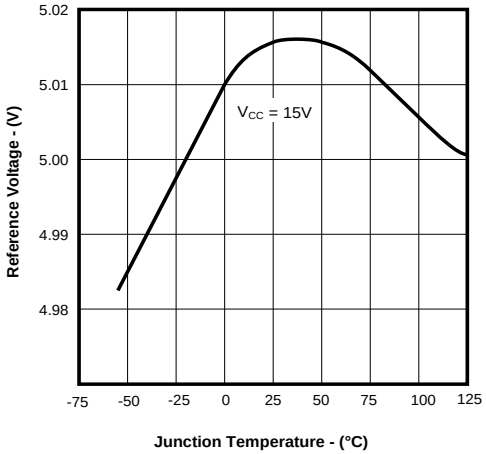


Figure 8 · Reference Voltage vs. Temperature

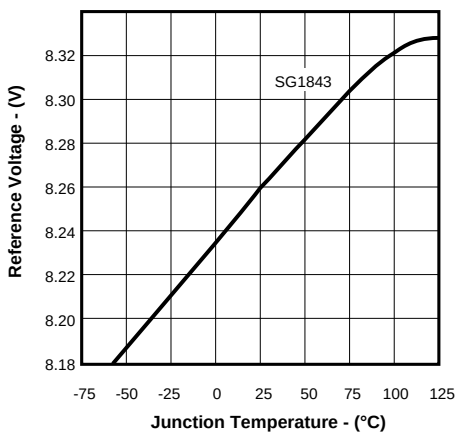


Figure 9 · Start-Up Voltage Threshold vs. Temperature

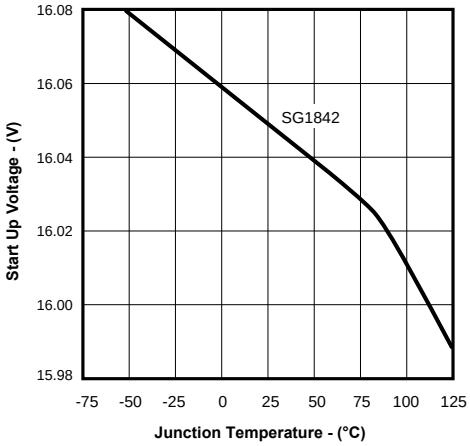


Figure 10 · Start-Up Voltage Threshold vs. Temperature

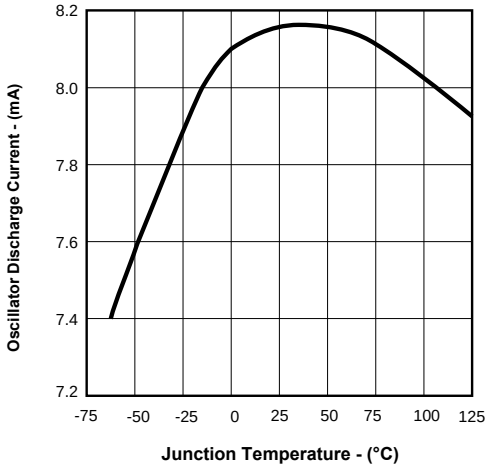


Figure 11 · Oscillator Discharge Current vs. Temperature

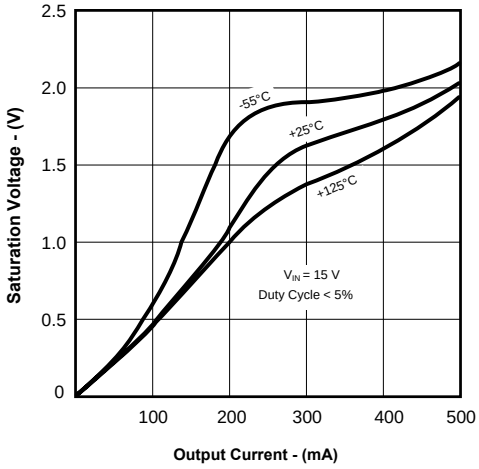


Figure 12 · Output Saturation Voltage vs. Output Current and Temperature (Sink Transistor)

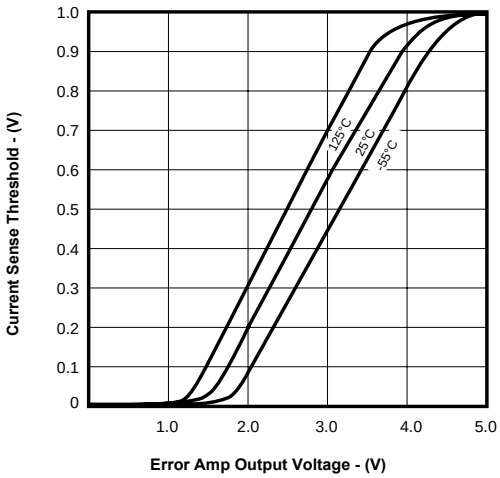


Figure 13 · Current Sense Threshold vs. Error Amplifier Output

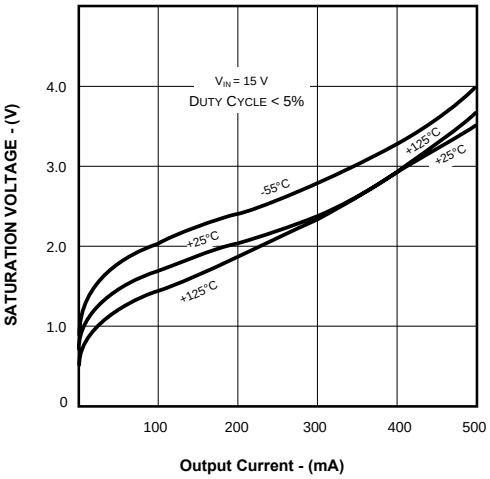


Figure 14 · Output Saturation Voltage vs. Output Current and Temperature

Application Information

The oscillator of the 1842/43 family of PWM's is designed such that many values of R_T and C_T will give the same oscillator frequency, but only one combination will yield a specific duty cycle at a given frequency.

Given:

Frequency ≡ f

Maximum Duty Cycle ≡ D_m

Calculate: $$R_T = 267\left[\frac{(1.76)^{1/D_m}-1}{(1.76)^{(1-D_m)/D_m}-1}\right] (\Omega)$$

where $0.3 < D_m < 0.95$

$$C_T = \frac{1.86 * D_m}{f * R_T} (\mu F)$$

For Duty-Cycles above 95% use:

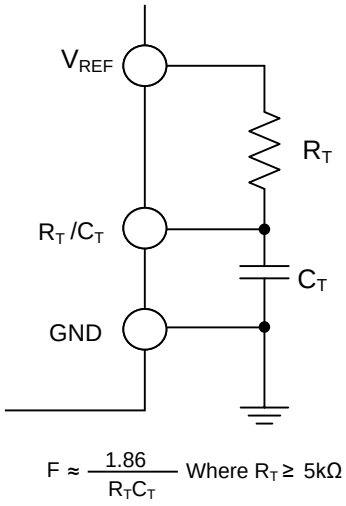


Figure 15 · Oscillator Timing Circuit

A set of formulas are given to determine the values of R_T and C_T for a given frequency and maximum duty cycle. (Note: These formulas are less accurate for smaller duty cycles or higher frequencies. This will require trimming of R_T or C_T to correct for this error.)

Example:

A Flyback power supply requires a maximum of 45% duty cycle at a switching frequency of 50 kHz. What are the values of R_T and C_T?

Given:

f = 50kHz

D_m = 0.45

Calculate: $$R_T = 267\left[\frac{(1.76)^{\frac{1}{.45}} - 1}{(1.76)^{\frac{.55}{.45}} - 1}\right] = 674\ \Omega$$

$$C_T = \frac{1.86\ *\ 0.45}{50000\ *\ 674} = .025\ (\mu F)$$

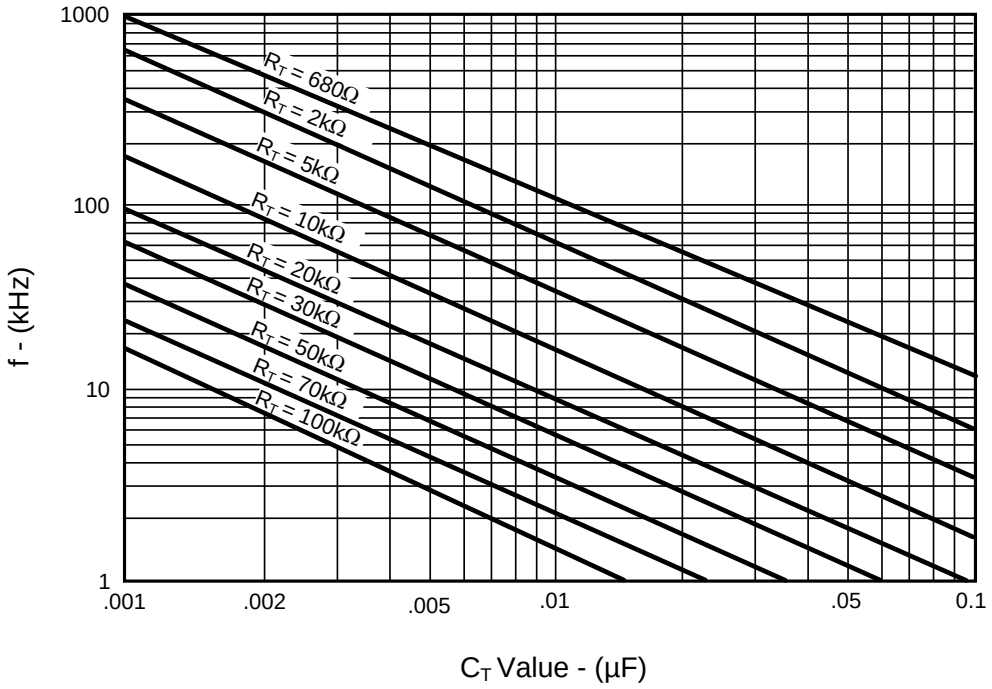


Figure 16 · Oscillator Frequency Vs. R_T For Various C_T

Typical Application Circuits

Pin numbers referenced are for 8-pin package and pin numbers in parenthesis are for 14-pin package.

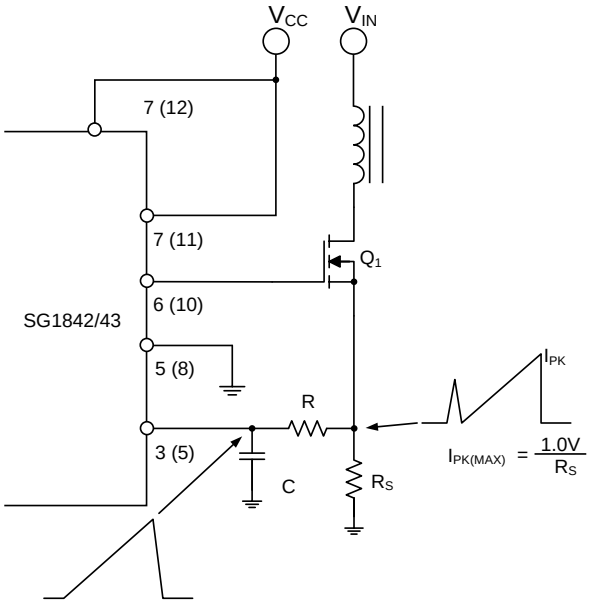


Figure 17 · Current Sense Spike Suppression

The RC low-pass filter eliminates the leading edge current spike caused by parasitic of Power MOSFET.

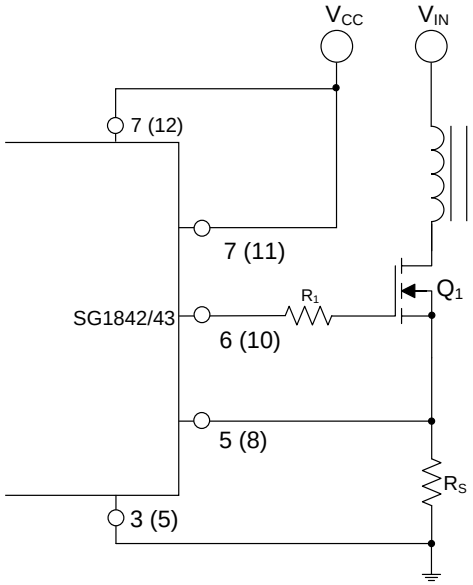


Figure 18 · MOSFET Parasitic Oscillations

A resistor (R1) in series with the MOSFET gate reduce overshoot and ringing caused by the MOSFET input capacitance and any inductance in series with the gate drive. (Note: It is very important to have a low inductance ground path to insure correct operation of the I.C. This can be done by making the ground paths as short and as wide as possible.)

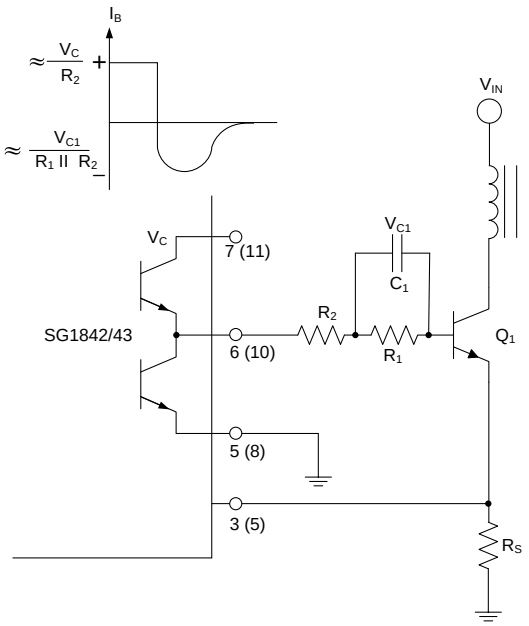


Figure 19 · Bipolar Transistor Drive

The 1842/43 output stage can provide negative base current to remove base charge of power transistor (Q_1) for faster turn off. This is accomplished by adding a capacitor (C_1) in parallel with a resistor (R_1). The resistor (R_1) is to limit the base current during turn on.

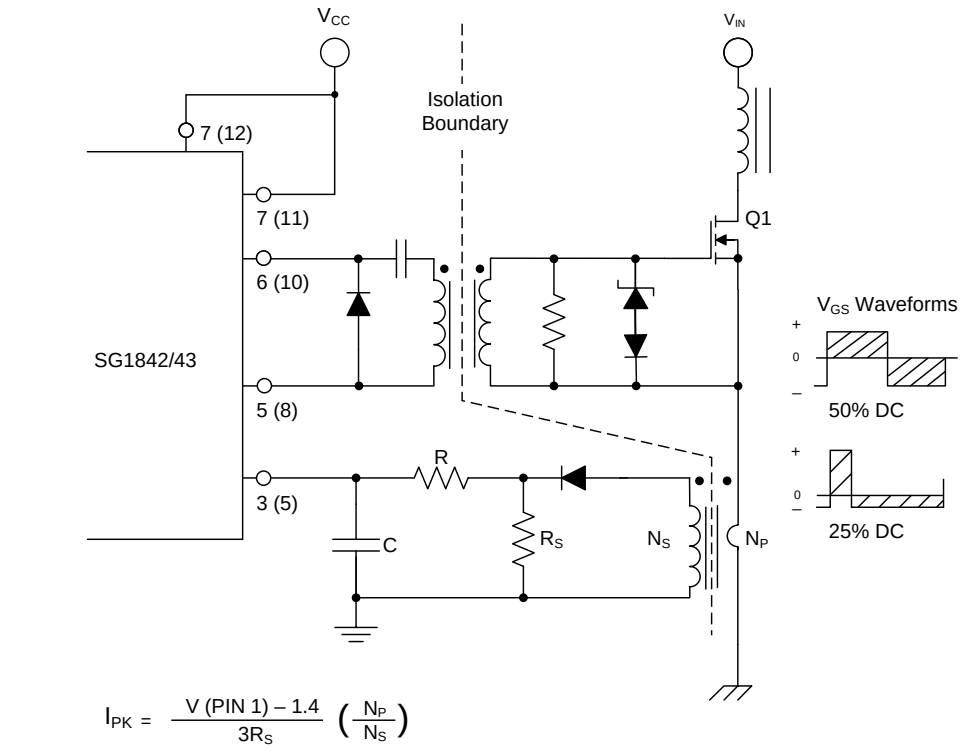


Figure 20 · Isolated MOSFET Drive

Current transformers can be used where isolation is required between PWM and Primary ground. A drive transformer is then necessary to interface the PWM output with the MOSFET.

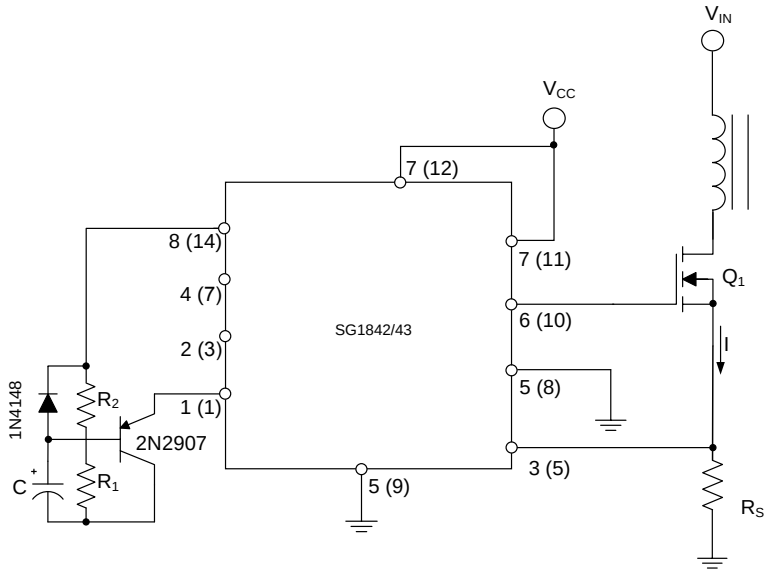


Figure 21 · Adjustable Buffered Reduction of Clamp Level with Softstart

$$I_{PK} = \frac{V_{CS}}{R_S}$$

Where, V_{CS}=1.67 $\left(\frac{R_1}{R_1+R_2}\right)$ and $V_{C.S.MAX}$ = 1V (Typ.)

$$t_{SOFTSTART} = -\ln\left[1 - \frac{V_{EAO} - 1.3}{5\left(\frac{R_1}{R_1+R_2}\right)}\right]\left(\frac{R_1R_2}{R_1+R_2}\right)C$$

Where, V_{EAO} ≡ voltage at the Error Amp Output under minimum line and maximum load conditions

Softstart and adjustable peak current can be done with the external circuitry shown above.

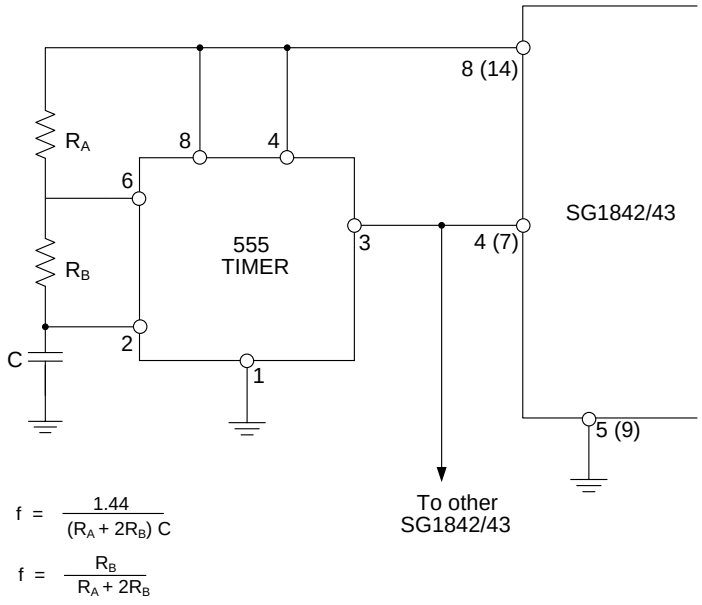


Figure 22 · External Duty Cycle Clamp and Multi-Unit Synchronization

Precision duty cycle limiting as well as synchronizing several 1842/1843's is possible with the above circuitry.

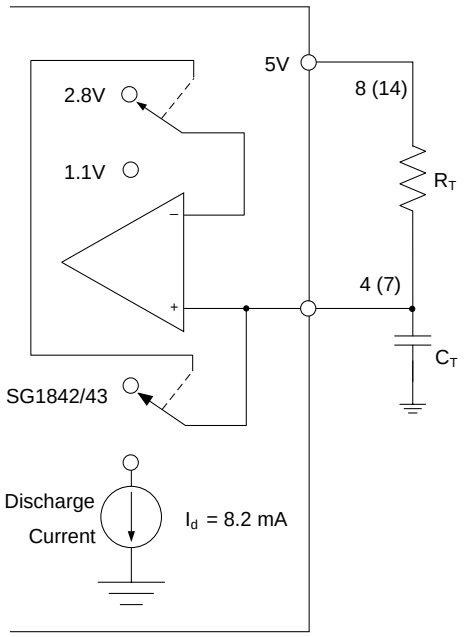


Figure 23 · Oscillator Connection

The oscillator is programmed by the values selected for the timing components R_T and C_T. Refer to application information for calculation of the component values.

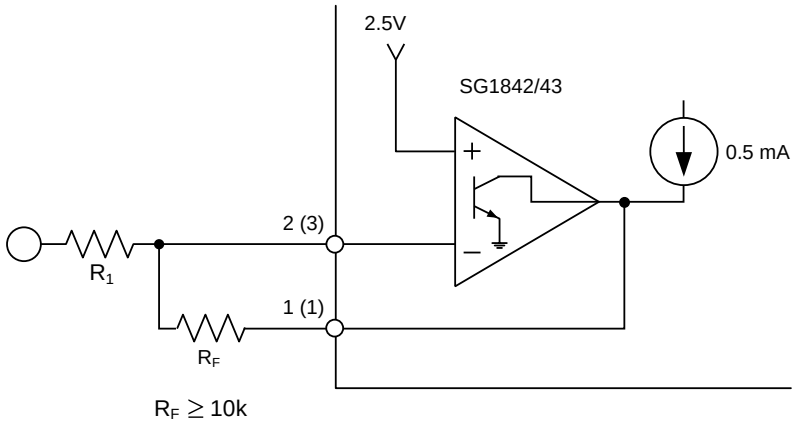


Figure 24 · Error Amplifier Connection

Error amplifier is capable of sourcing and sinking current up to 0.5mA.

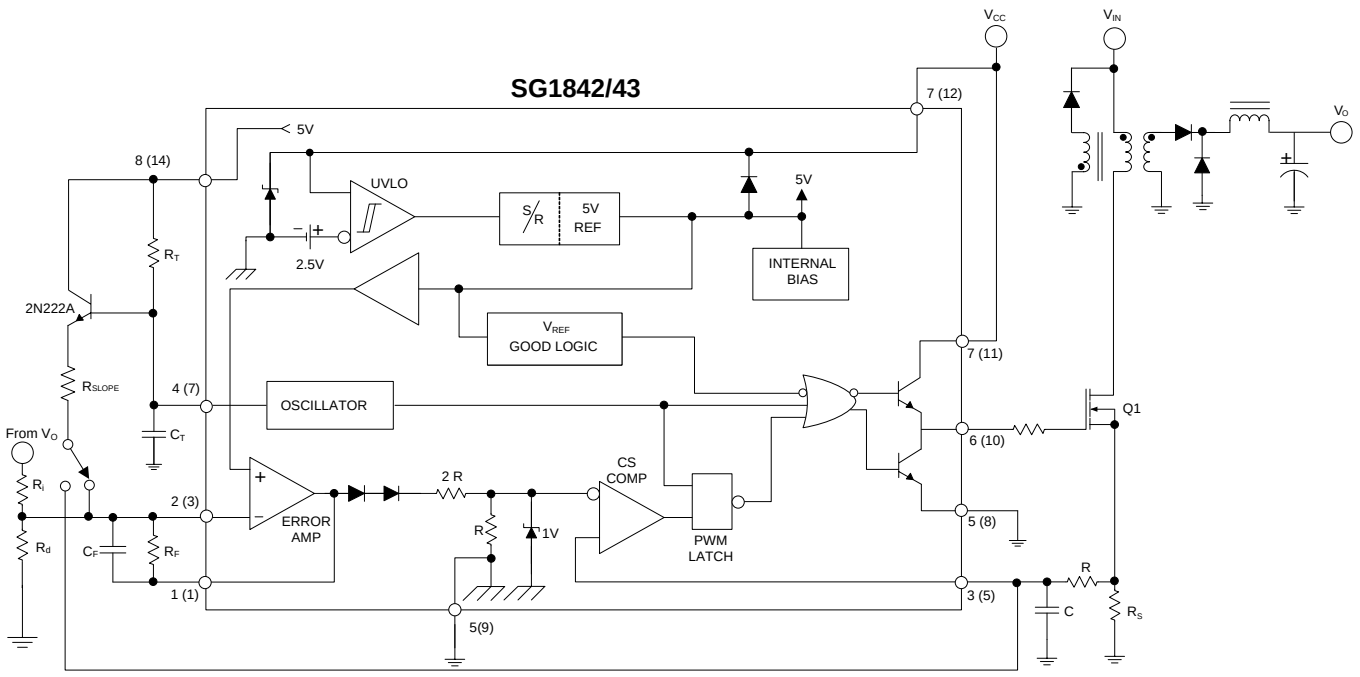


Figure 25 · Slope Compensation

Due to inherent instability of current mode converters running above 50% duty cycle, slope compensation should be added to either current sense pin or the error amplifier. Figure 25 shows a typical slope compensation technique.

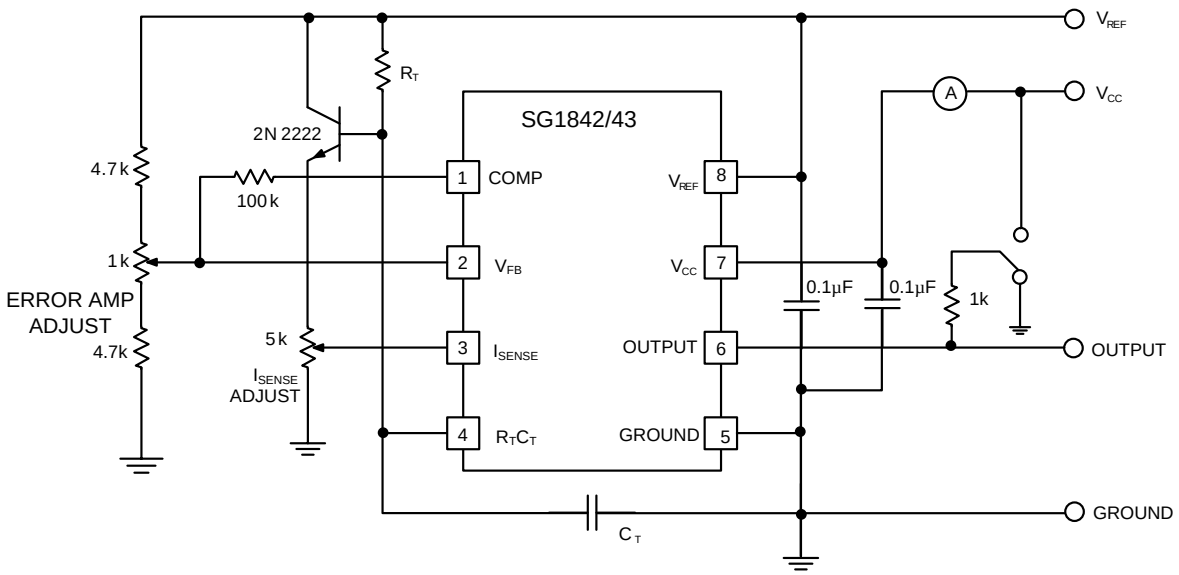


Figure 26 · Open Loop Laboratory Fixture

High-peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected to pin 5 in a single point ground.

The transistor and 5kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

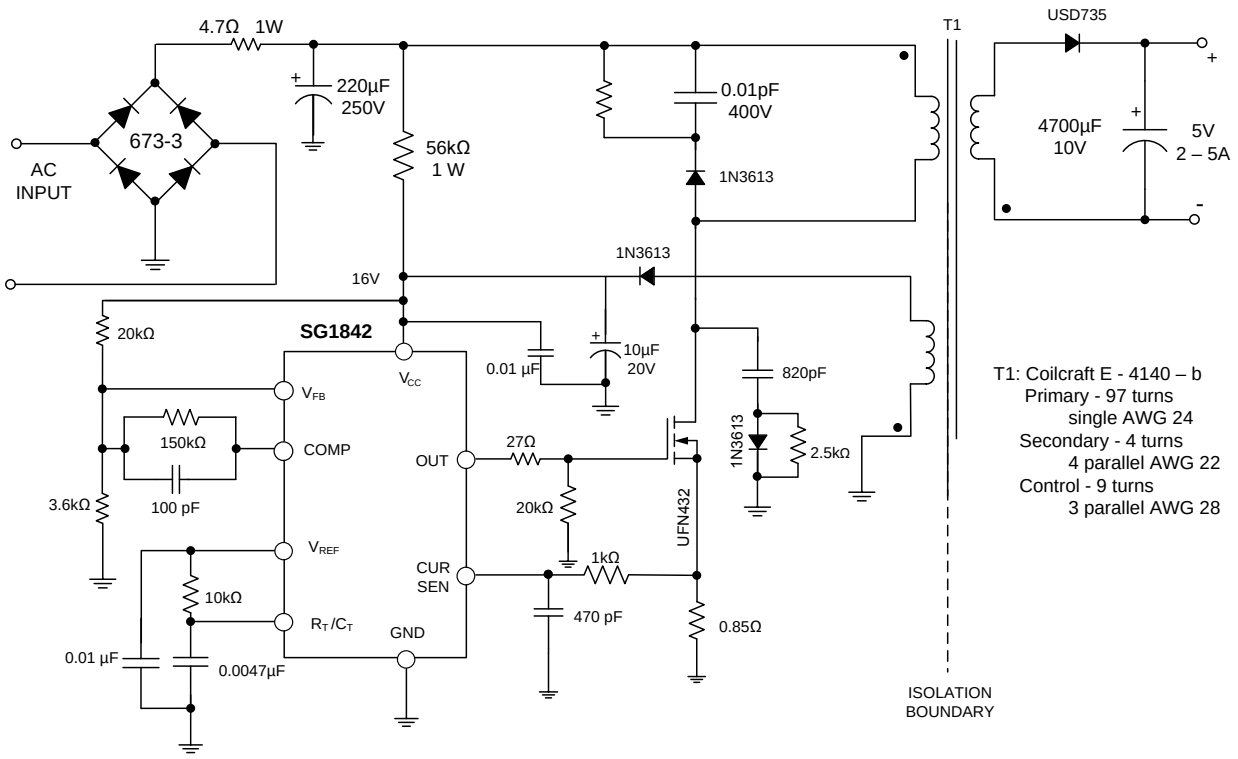


Figure 27 · Off-line Flyback Regulator

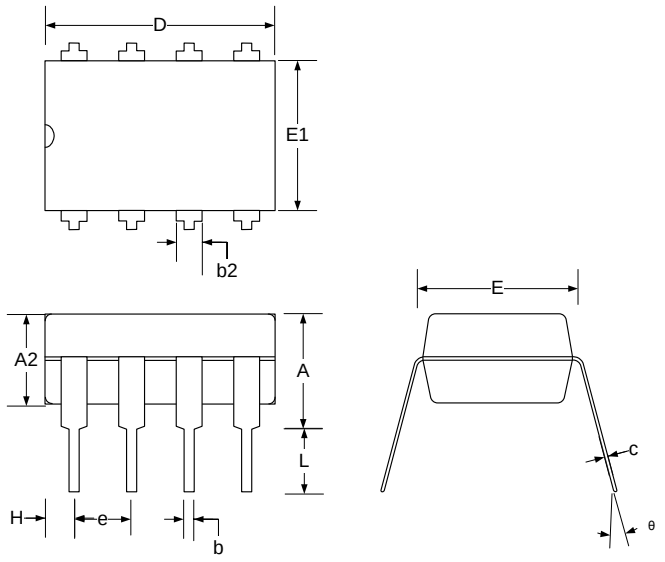
SPECIFICATIONS

Input line voltage:	90VAC to 130VAC
Input frequency:	50 or 60Hz
Switching frequency:	40kHz ±10%
Output power:	25W maximum
Output voltage:	5V +5%
Output current:	2 to 5A
Line regulation:	0.01%/V
Load regulation:	8%/A*
Efficiency @ 25 Watt:	
V_{IN} = 90VAC:	70%
V_{IN} = 130VAC:	65%
Output short-circuit current:	2.5 A average

*This circuit uses a low-cost feedback scheme in which the DC voltage developed from the primary-side control winding is sensed by the SG1842 error amplifier. Load regulation is therefore dependent on the coupling between secondary and control windings, and on transformer leakage inductance.

Package Outline Dimensions

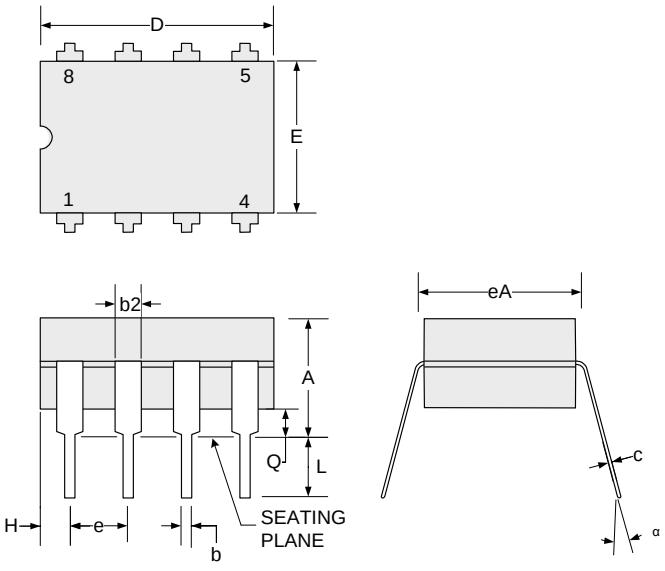
Controlling dimensions are in inches, metric equivalents are shown for general information.



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	5.08	-	0.200
A2	3.30 Typ.		1.30 Typ.	
b	0.38	0.51	0.145	0.020
b2	0.76	1.65	0.030	0.065
c	0.20	0.38	0.008	0.015
D	-	10.16	-	0.400
E	7.62 BSC		0.300 BSC	
e	2.54 BSC		0.100 BSC	
E1	6.10	6.86	0.240	0.270
L	3.05	-	0.120	-
θ	0°	15°	0°	15°

Note:
Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 1 · M 8-Pin PDIP Package Dimensions

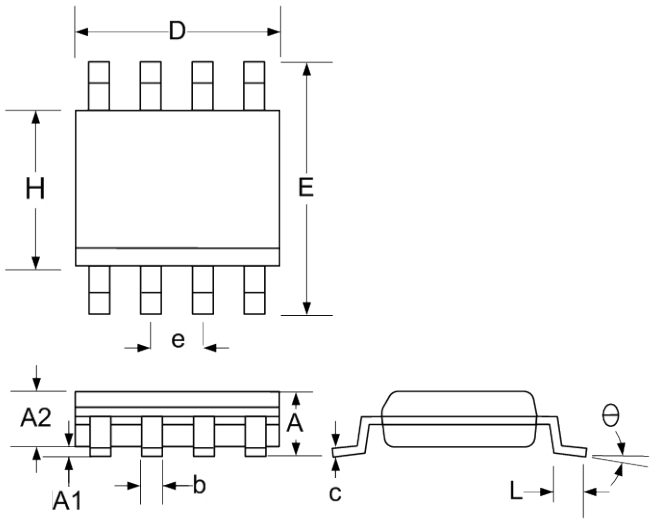


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.08	0.170	0.200
b	0.38	0.51	0.015	0.020
b2	1.04	1.65	0.045	0.065
c	0.20	0.38	0.008	0.015
D	9.52	10.29	0.375	0.405
E	5.59	7.11	0.220	0.280
e	2.54 BSC		0.100 BSC	
eA	7.37	7.87	0.290	0.310
H	0.63	1.78	0.025	0.070
L	3.18	4.06	0.125	0.160
α	-	15°	-	15°
Q	0.51	1.02	0.020	0.040

Note:
Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 2 · Y 8-Pin CERDIP Package Dimensions

Package Outline Dimensions

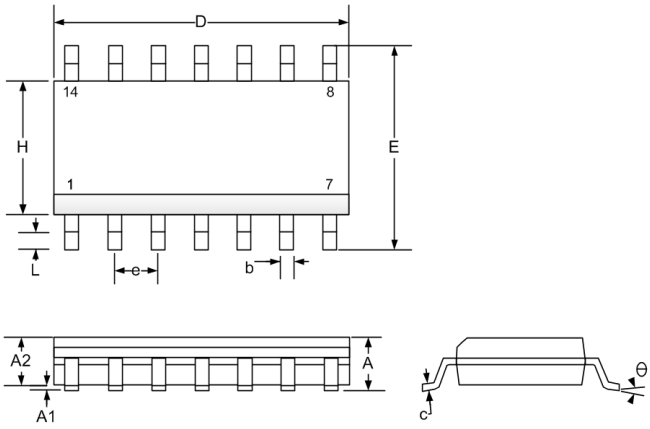


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.52	0.049	0.060
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.007	0.010
D	4.83	5.21	0.189	0.205
E	5.79	6.20	0.228	0.244
e	1.27 BSC		0.050 BSC	
H	3.81	4.01	0.150	0.158
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°
*LC	-	.010	-	0.004

*Lead Co-planarity

Note:
Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage

Figure 3 · DM 8-Pin SOIC Package Dimensions



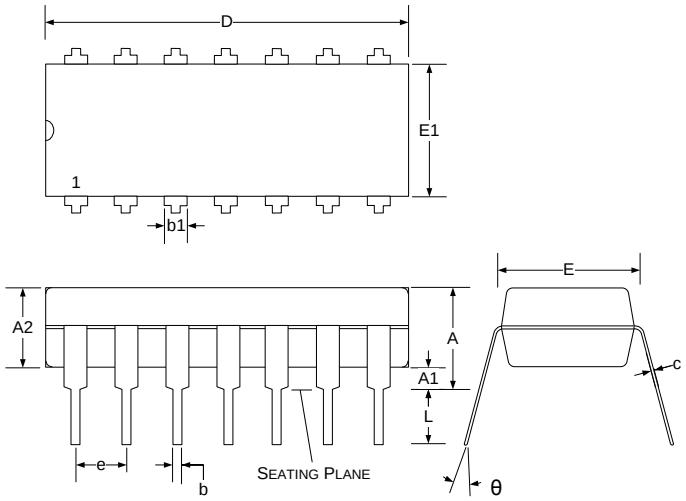
Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.52	0.049	0.060
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.007	0.010
D	8.54	8.74	0.336	0.344
E	5.79	6.20	0.228	0.244
e	1.27 BSC		0.050 BSC	
H	3.81	4.01	0.150	0.158
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°
*LC	-	.010	-	0.004

*Lead Co-planarity

Note:
Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage

Figure 4 · D 14-Pin SOIC Package Dimensions

Package Outline Dimensions

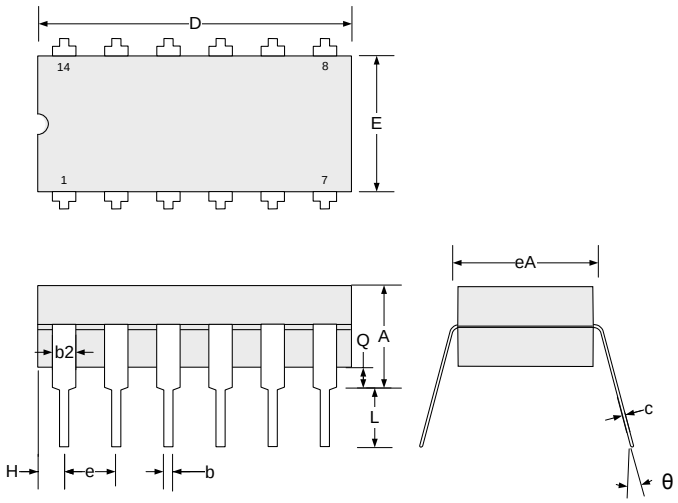


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	5.33	-	0.210
A1	0.38	-	0.015	-
A2	3.30 Typ.		0.130 Typ.	
b	0.36	0.56	0.014	0.022
b1	1.14	1.78	0.045	0.070
c	0.20	0.36	0.008	0.014
D	18.54	20.57	0.730	0.810
e	2.54 BSC		0.100 BSC	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
L	2.92	3.81	0.115	0.150
θ	0°	15°	0°	15°

Note:

Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 5 · N 14-Pin PDIP Package Dimensions



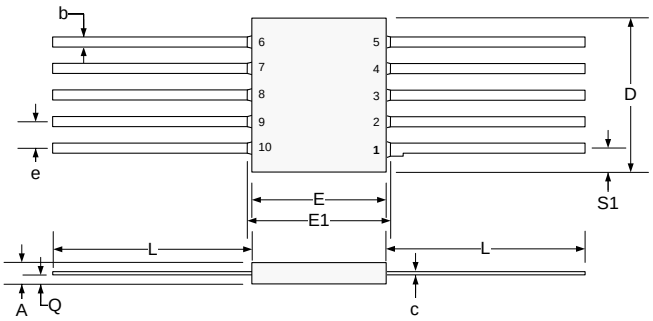
Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.08	0.170	0.200
b	0.38	0.51	0.015	0.020
b2	1.04	1.65	0.045	0.065
c	0.20	0.38	0.008	0.015
D	19.30	19.94	0.760	0.785
E	5.59	7.11	0.220	0.280
e	2.54 BSC		0.100 BSC	
eA	7.37	7.87	0.290	0.310
H	0.63	1.78	0.025	0.070
L	3.18	4.06	0.125	0.160
α	-	15°	-	15°
Q	0.51	1.02	0.020	0.040

Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 6 · J 14-Pin CERDIP Package Dimensions

Package Outline Dimensions

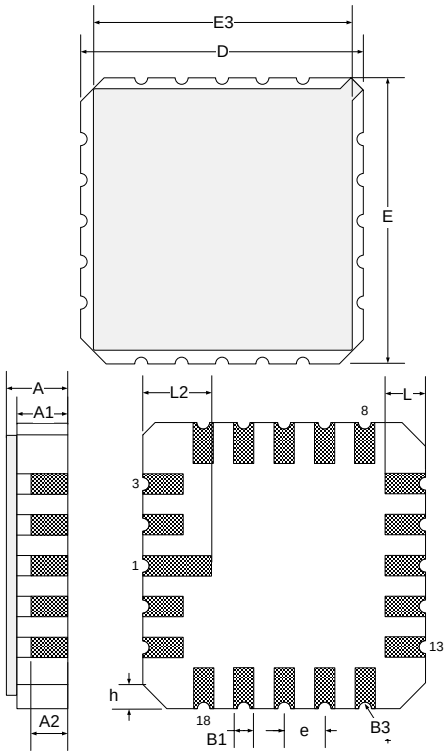


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.45	1.70	0.057	0.067
b	0.25	0.483	0.010	0.019
c	0.102	0.152	0.004	0.006
D	-	7.37	-	0.290
E	6.04	6.40	0.238	0.252
E1	-	6.91	-	0.272
e	1.27 BSC		0.050 BSC	
L	6.35	9.40	0.250	0.370
Q	0.51	1.02	0.020	0.040
S1	0.20	0.38	0.008	0.015

Notes:

1. Lead No. 1 is identified by tab on lead or dot on cover.
2. Leads are within 0.13mm (.0005") radius of the true position (TP) at maximum material condition.
3. Dimension "e" determines a zone within which all body and lead irregularities lie.

Figure 7 · F 10-Pin Ceramic Flatpack Package Dimensions



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
D/E	8.64	9.14	0.340	0.360
E3	-	8.128	-	0.320
e	1.270 BSC		0.050 BSC	
B1	0.635 TYP		0.025 TYP	
L	1.02	1.52	0.040	0.060
A	1.626	2.286	0.064	0.090
h	1.016 TYP		0.040 TYP	
A1	1.372	1.68	0.054	0.066
A2	-	1.168	-	0.046
L2	1.91	2.41	0.075	0.95
B3	0.203R		0.008R	

Note:

All exposed metalized area shall be gold plated 60 micro-inch minimum thickness over nickel plated unless otherwise specified in purchase order.

Figure 8 · L 20-Pin Leadless Chip Carrier Package Dimensions

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