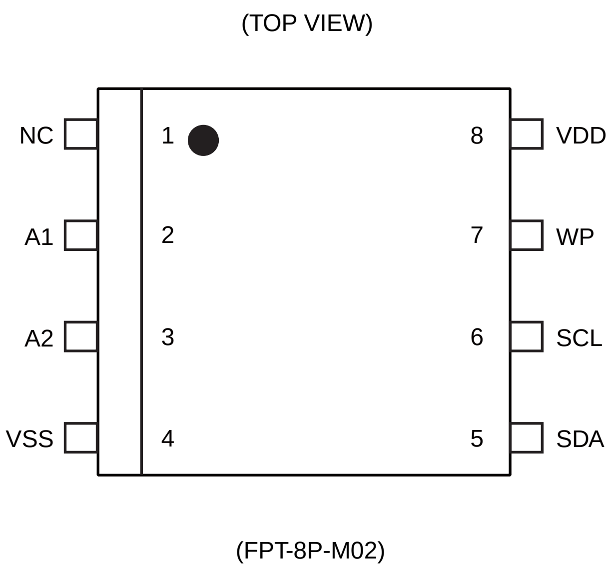
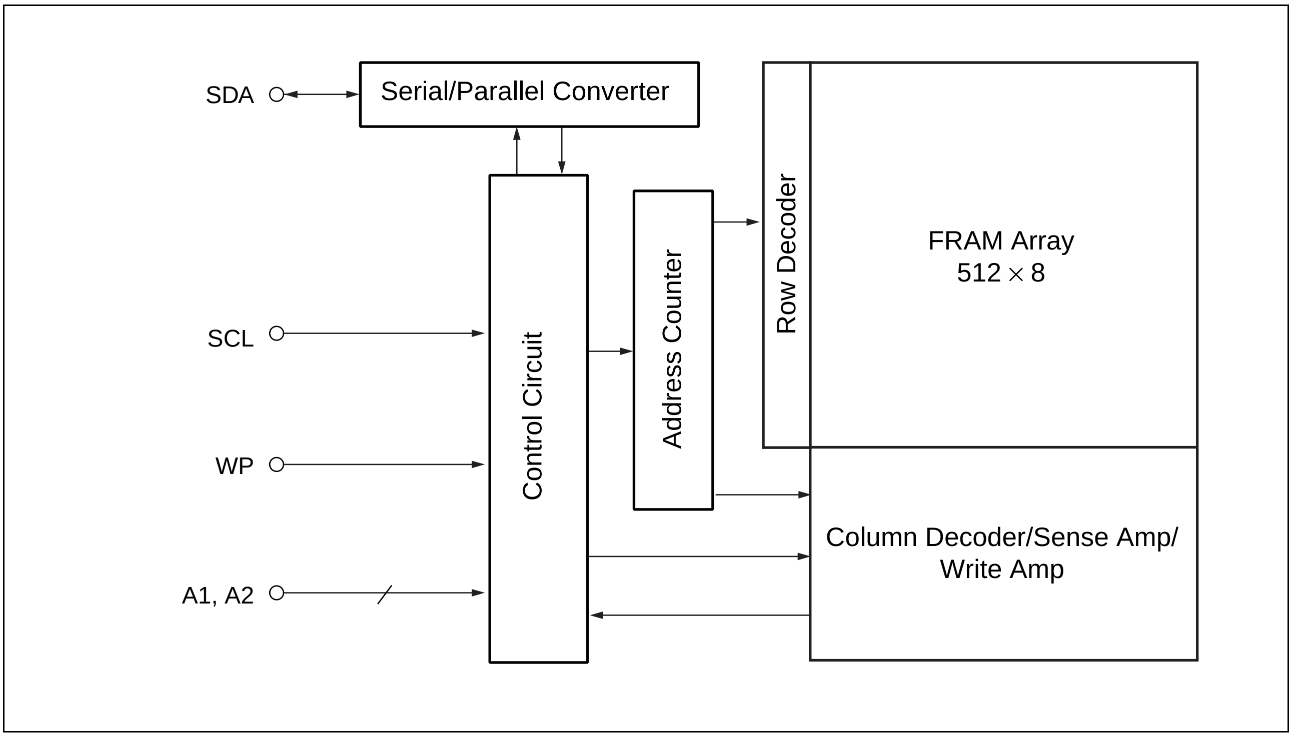
■ PIN ASSIGNMENT



■ PIN FUNCTIONAL DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1	NC	No Connect pin Leave this pin open, or connect to VDD or VSS.
2, 3	A1, A2	Device Address pins The MB85RC04V can be connected to the same data bus up to 4 devices. Device addresses are used in order to identify each of these devices. Connect these pins to VDD pin or VSS pin externally. Only if the combination of VDD and VSS pins matches Device Address Code inputted from the SDA pin, the device operates. In the open pin state, A1 and A2 pins are internally pulled-down and recognized as the "L" level.
4	VSS	Ground pin
5	SDA	Serial Data I/O pin This is an I/O pin which performs bidirectional communication for both memory address and writing/reading data. It is possible to connect multiple devices. It is an open drain output, so a pull-up resistor is required to be connected to the external circuit.
6	SCL	Serial Clock pin This is a clock input pin for input/output timing serial data. Data is sampled on the rising edge of the clock and output on the falling edge.
7	WP	Write Protect pin When the Write Protect pin is the “H” level, the writing operation is disabled. When the Write Protect pin is the “L” level, the entire memory region can be overwritten. The reading operation is always enabled regardless of the Write Protect pin input level. The write protect pin is internally pulled down to VSS pin, and that is recognized as the “L” level (write enabled) when the pin is the open state.
8	VDD	Supply Voltage pin

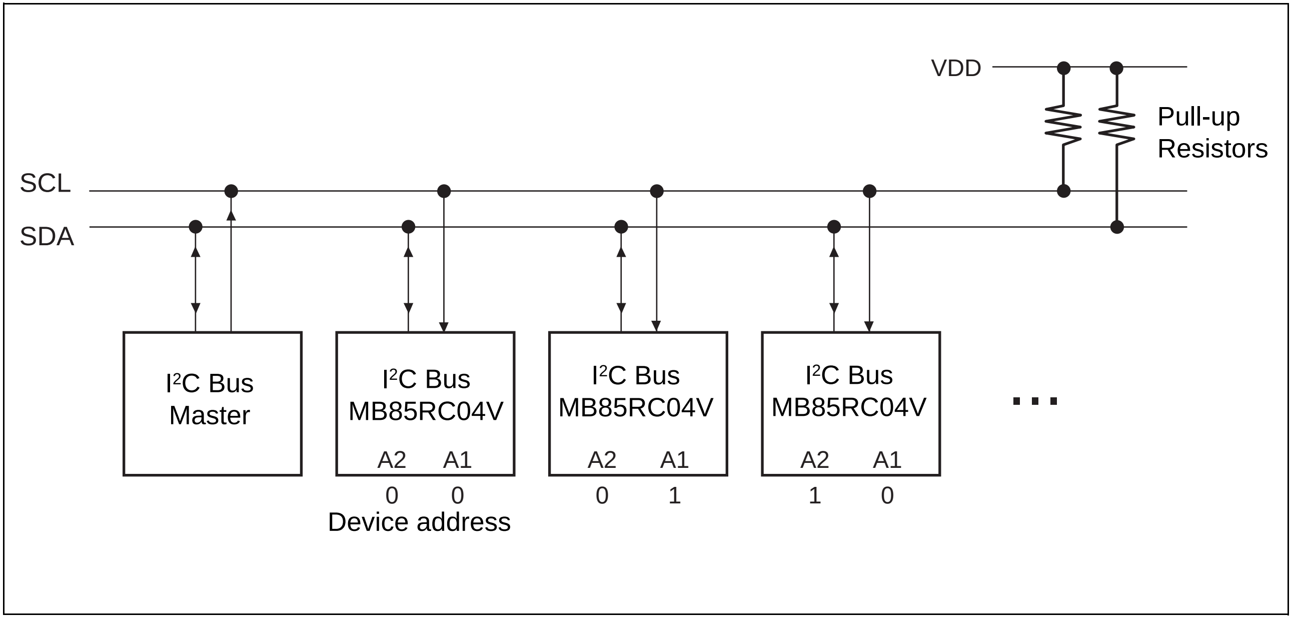
■ BLOCK DIAGRAM



■ I²C (Inter-Integrated Circuit)

The MB85RC04V has the two-wire serial interface; the I²C bus, and operates as a slave device.
The I²C bus defines communication roles of “master” and “slave” devices, with the master side holding the authority to initiate control. Furthermore, the I²C bus connection is possible where a single master device is connected to multiple slave devices in a party-line configuration. In this case, it is necessary to assign a unique device address to the slave device, the master side starts communication after specifying the slave to communicate by addresses.

- **I²C Interface System Configuration Example**



■ I²C COMMUNICATION PROTOCOL

The I²C bus is a two wire serial interface that uses a bidirectional data bus (SDA) and serial clock (SCL). A data transfer can only be initiated by the master, which will also provide the serial clock for synchronization. The SDA signal should change while SCL is the "L" level. However, as an exception, when starting and stopping communication sequence, SDA is allowed to change while SCL is the "H" level.

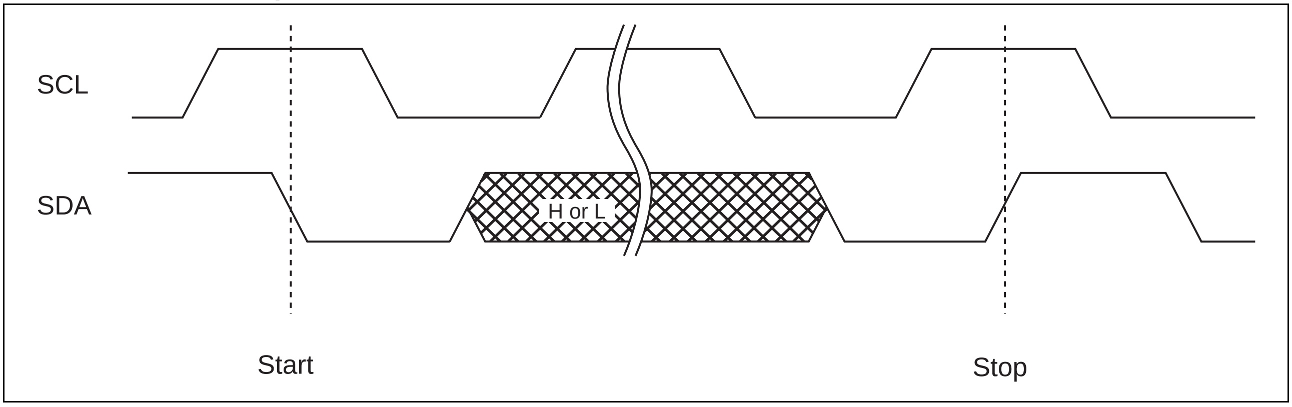
- Start Condition

To start read or write operations by the I²C bus, change the SDA input from the "H" level to the "L" level while the SCL input is in the "H" level.

- Stop Condition

To stop the I²C bus communication, change the SDA input from the "L" level to the "H" level while the SCL input is in the "H" level. In the reading operation, inputting the stop condition finishes reading and enters the standby state. In the writing operation, inputting the stop condition finishes inputting the rewrite data and enters the standby state.

• Start Condition, Stop Condition



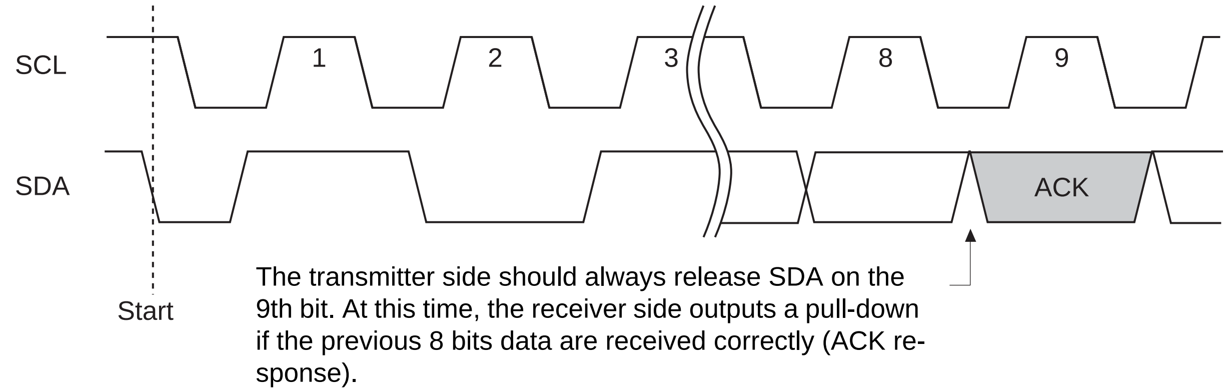
Note : At the write operation, the FRAM device does not need the programming wait time (t_{WC}) after issuing the Stop Condition.

■ ACKNOWLEDGE (ACK)

In the I^{2}C bus, serial data including address or memory information is sent in units of 8 bits. The acknowledge signal indicates that every 8 bits of the data is successfully sent and received. The receiver side usually outputs the “L” level every time on the 9th SCL clock after each 8 bits are successfully transmitted and received. On the transmitter side, the bus is temporarily released to Hi-Z every time on this 9th clock to allow the acknowledge signal to be received and checked. During this Hi-Z released period, the receiver side pulls the SDA line down to indicate the “L” level that the previous 8 bits communication is successfully received.

In case the slave side receives Stop condition before sending or receiving the ACK “L” level, the slave side stops the operation and enters to the standby state. On the other hand, the slave side releases the bus state after sending or receiving the NACK “H” level. The master side generates Stop condition or Start condition in this released bus state.

- **Acknowledge timing overview diagram**



The transmitter side should always release SDA on the 9th bit. At this time, the receiver side outputs a pull-down if the previous 8 bits data are received correctly (ACK response).

■ MEMORY ADDRESS STRUCTURE

The MB85RC04V has the memory address buffer to store the 9-bit information for the memory address.

As for byte write, page write and random read commands, the complete 9-bit memory address is configured by inputting the memory upper address (1 bit) and the memory lower address (8 bits), and saved to the memory address buffer. Then access to the memory is performed.

As for a current address read command, the complete 9-bit memory address is configured and saved to the memory address buffer, by inputting the memory upper address (1 bit) and the memory lower address (8 bits) which has saved in the memory address buffer. Then access to the memory is performed.

■ DEVICE ADDRESS WORD

Following the start condition, the 8 bit device address word is input. Inputting the device address word decides whether writing or reading operation. However, the clock is always driven by the master. The device address word (8 bits) consists of a device Type code (4 bits), device address code (2 bits), memory upper address code (1 bit), and a Read/Write code (1 bit).

- Device Type Code (4 bits)

The upper 4 bits of the device address word are a device type code that identifies the device type, and are fixed at “1010” for the MB85RC04V.

- Device Address Code (2 bits): A1, A2

Following the device type code, the 2 bits of the device address code are input in order of A2 and A1.

The device address code identifies one device from up to 4 devices connected to the bus.

Each MB85RC04V is given a unique 2 bits code on the device address pin (external hardware pin A2 and A1). The slave only responds if the received device address code is equal to this unique 2 bits code.

- Memory Upper Address Code (1 bit): A8

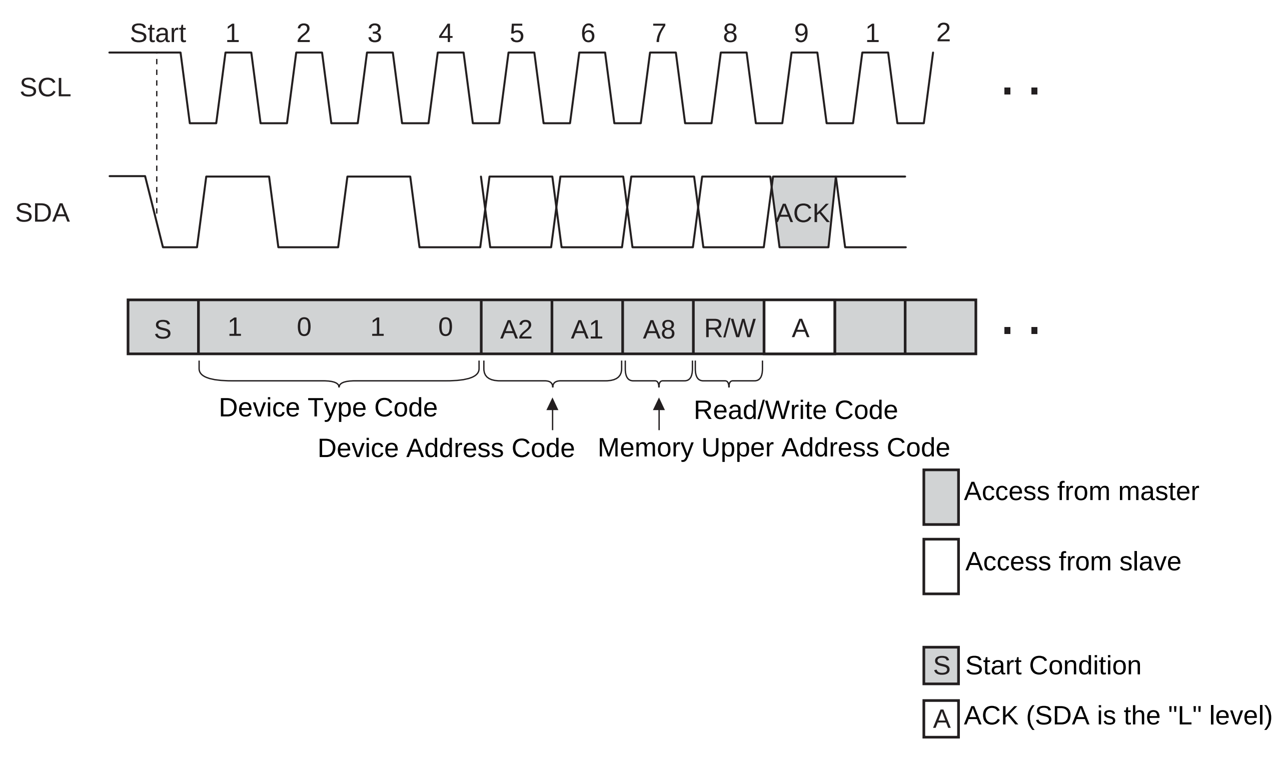
Following the device address code, the 1-bit memory upper address code are input.

This bit is not the setting bit for the slave address, but the upper 1-bit setting bit for the memory address.

- Read/Write Code (1 bit)

The 8th bit of the device address word is the R/W (Read/Write) code. When the R/W code is “0” input, a write operation is enabled, and the R/W code is “1” input, a read operation is enabled for the MB85RC04V. If the device type code is not “1010” or the device address code is not equal to the setting of the external device address pins, the Read/Write operation is not performed and the standby state is chosen.

• Device Address Word



■ DATA STRUCTURE

The master inputs the device address word (8 bits) following the start condition, and then the slave outputs the Acknowledge “L” level on the 9th bit. After confirming the Acknowledge response, the sequential 8-bit memory lower address is input, to the byte write, page write and random read commands.

As for the current address read command, inputting the memory lower address is not performed, and the address buffer lower 8-bit is used as the memory lower address.

When inputting the memory lower address finishes, the slave outputs the Acknowledge “L” level on the 9th bit again.

Afterwards, the input and the output data continue in 8-bit units, and then the Acknowledge “L” level is output for every 8-bit data.

■ FRAM ACKNOWLEDGE -- POLLING NOT REQUIRED

The MB85RC04V performs the high speed write operations, so any waiting time for an ACK* by the acknowledge polling does not occur.

*: In E^2PROM, the Acknowledge Polling is performed as a progress check whether rewriting is executed or not. It is normal to judge by the 9th bit of Acknowledge whether rewriting is performed or not after inputting the start condition and then the device address word (8 bits) during rewriting.

■ WRITE PROTECT (WP)

The entire memory array can be write protected by setting the WP pin to the “H” level. When the WP pin is set to the “L” level, the entire memory array will be rewritten. Reading is allowed regardless of the WP pin's “H” level or “L” level.

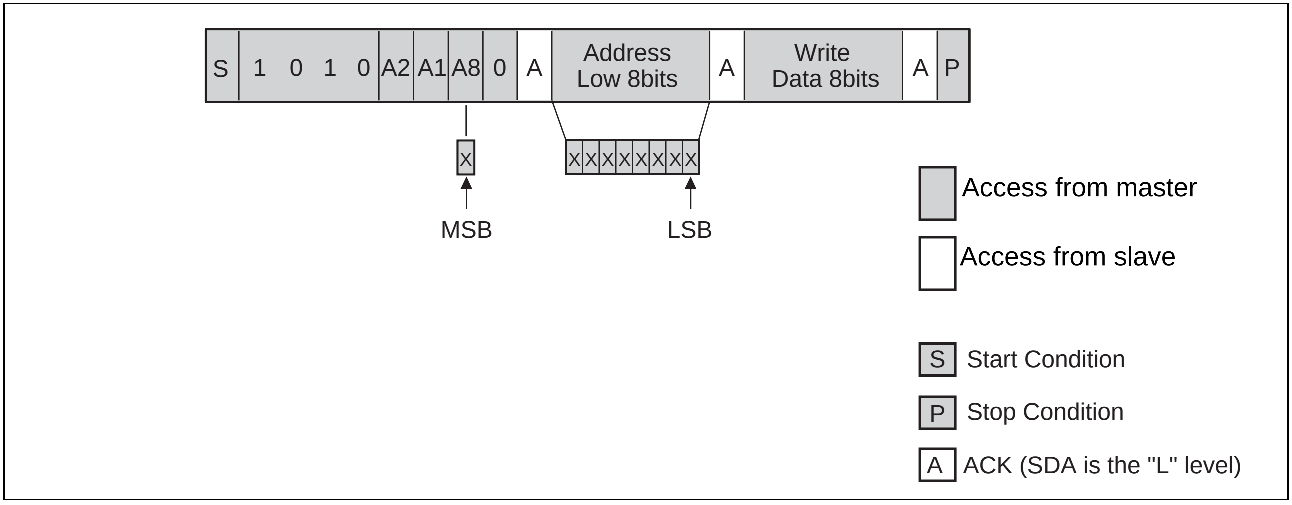
Do not change the WP signal level during the communication period from the start condition to the stop condition.

Note : The WP pin is pulled down internally to the VSS pin, therefore if the WP pin is open, the pin status is recognized as the “L” level (write enabled).

COMMAND

- Byte Write

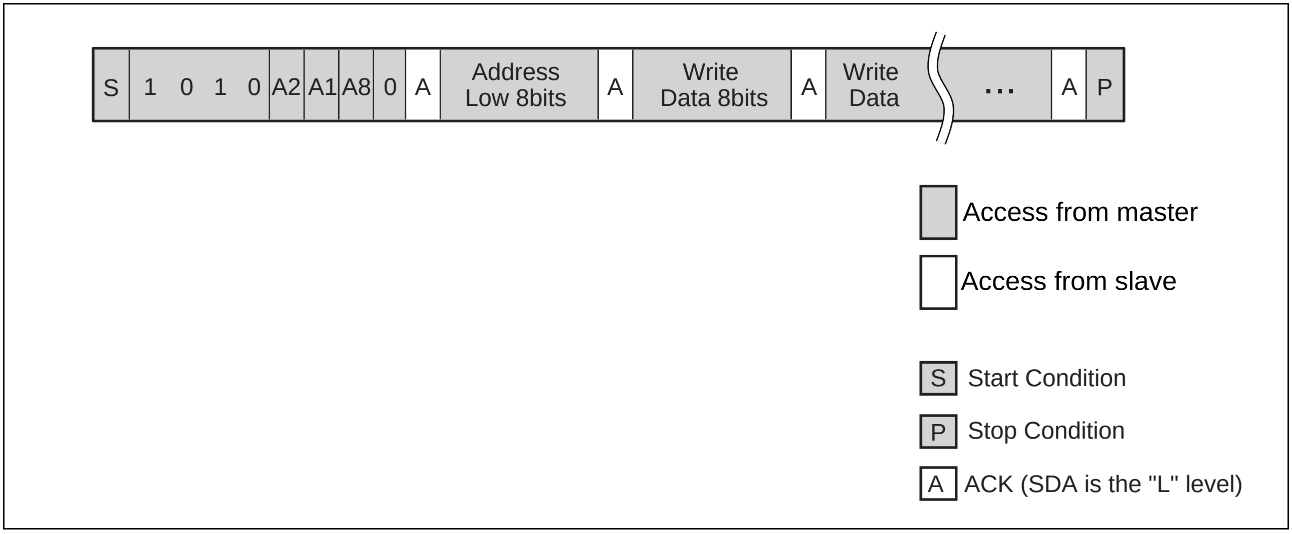
If the device address word (R/W “0” input) is sent after the start condition, the slave responds with an ACK. After this ACK, write memory addresses and write data are sent in the same way, and the write ends by generating a stop condition at the end.



- Page Write

If additional 8 bits are continuously sent after the same command (except stop condition) as Byte Write, a page write is performed. The memory address rolls over to first memory address (000_H) at the end of the address. Therefore, if more than 512bytes are sent, the data is overwritten in order starting from the start of the memory address that was written first.

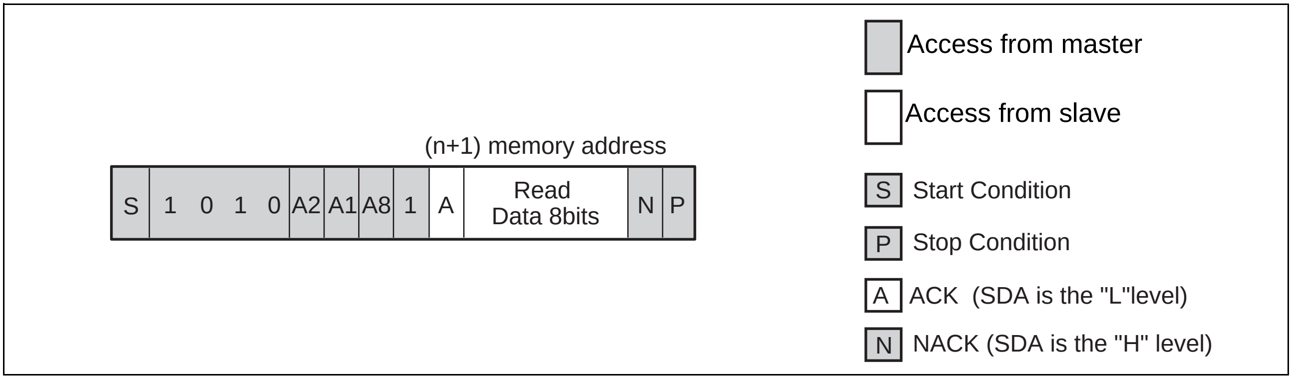
As the FRAM performs the high-speed write operations, the data will be written to FRAM right after the ACK response finished.



- Current Address Read

If the last write or read operation finishes successfully up to the end of stop condition, the memory address that was accessed last remains in the memory address buffer (the length is 9 bits).

When sending this command without turning the power off, it is possible to read from the memory address n+1 which adds 1 to the total 9-bit memory address n, which consists of the 1-bit memory upper address from the device address word input and the lower 8-bit of the memory address buffer. If the memory address n is the last address, it is possible to read with rolling over to the head of the memory address (000H). The current address (address that the memory address buffer indicates) is undefined immediately after turning the power on.

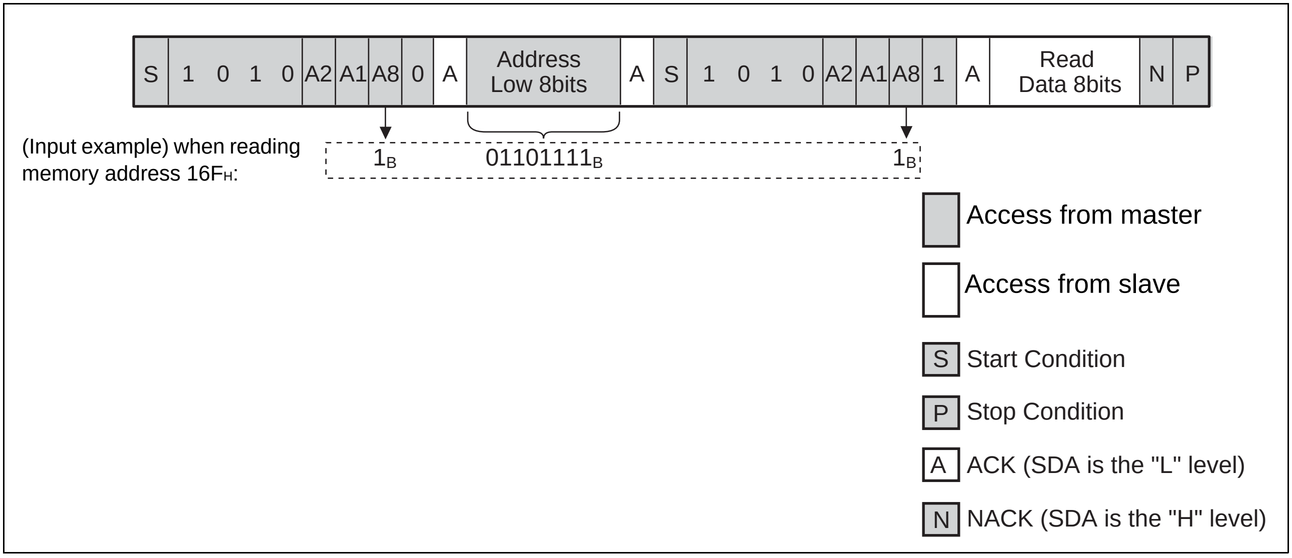


- Random Read

The one byte of data from the memory address saved in the memory address buffer can be read out synchronously to SCL by specifying the address in the same way as for a write, and then issuing another start condition and sending the Device Address Word (R/W “1” input).

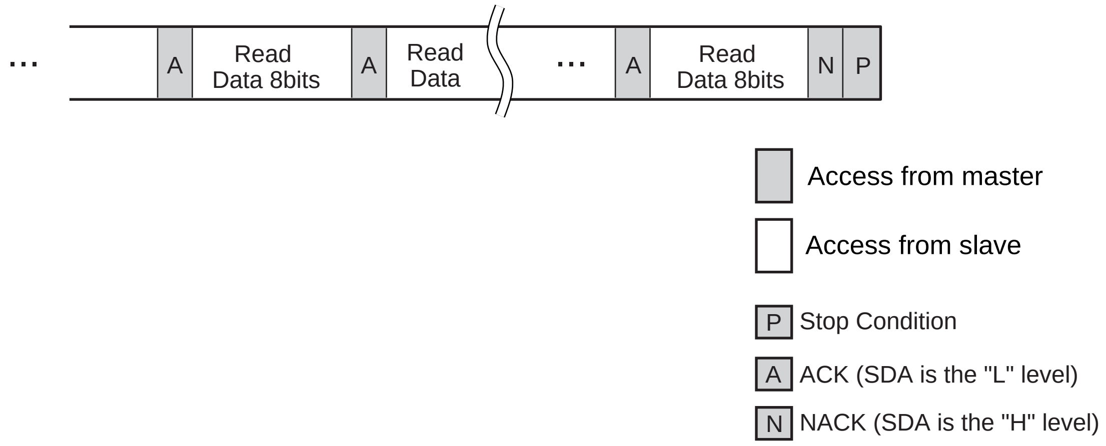
Setting values for the first and the second memory upper address codes should be the same (an example is shown in below).

The final NACK (SDA is the “H” level) is issued by the receiver that receives the data. In this case, this bit is issued by the master side.



- Sequential Read

Data can be received continuously following the Device address word (R/W “1” input) after specifying the address in the same way as for Random Read. If the read reaches the end of address, the read address automatically rolls over to the first memory address (000_H) and keeps reading.



- Device ID

The Device ID command reads fixed Device ID. The size of Device ID is 3 bytes and consists of manufacturer ID and product ID. The Device ID is read-only and can be read out by following sequences.

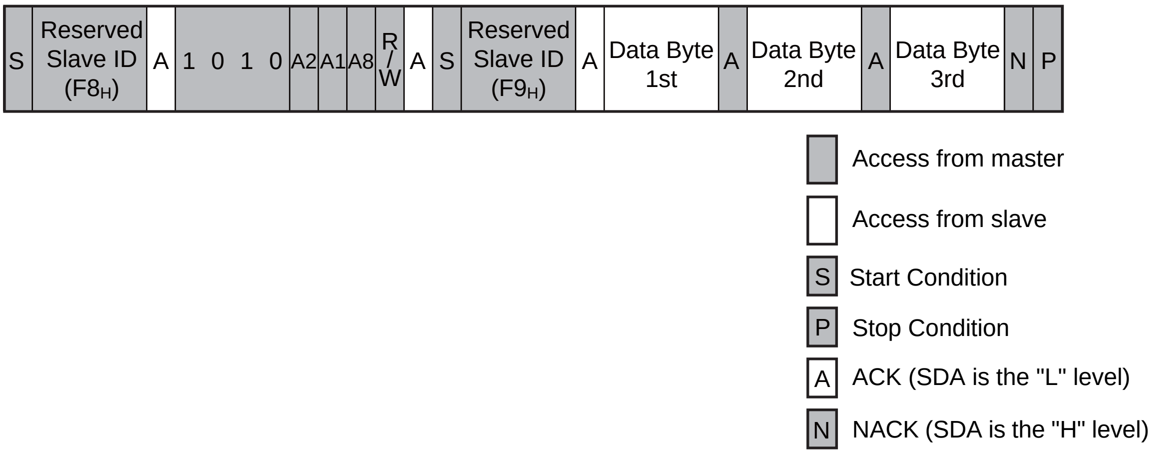
a) The master sends the Reserved Slave ID $F8_H$ after the START condition.

b) The master sends the device address word after the ACK response from the slave.
In this device address word, the memory upper address (one bit) and R/W code are “Don't care” value.

c) The master re-sends the START condition followed by the Reserved Slave ID $F9_H$ after the ACK response from the slave.

d) The master read out the Device ID succeedingly in order of Data Byte 1st / 2nd / 3rd after the ACK response from the slave.

e) The master responds the NACK (SDA is the “H” level) after reading 3 bytes of the Device ID.
In case the master respond the ACK after reading 3 bytes of the Device ID, the master re-reading the Device ID from the 1st byte.



Data Byte 1st								Data Byte 2nd								Data Byte 3rd							
Manufacture ID = $00A_H$												Product ID = 010_H											
11	10	9	8	7	6	5	4	3	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0
Fujitsu Semiconductor												Density = 0_H				Proprietary use							
0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0

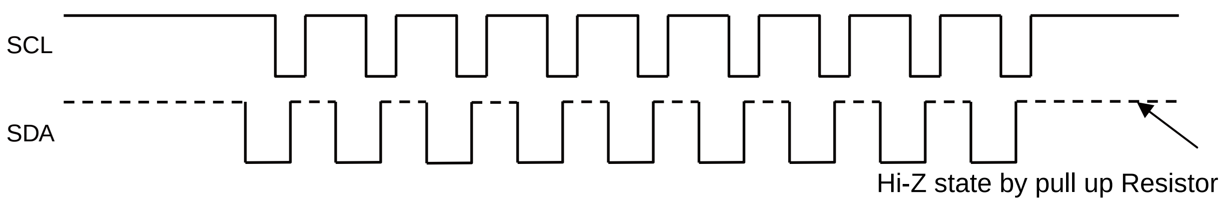
■ SOFTWARE RESET SEQUENCE OR COMMAND RETRY

In case the malfunction has occurred after power on, the master side stopped the I²C communication during processing, or unexpected malfunction has occurred, execute the following (1) software recovery sequence just before each command, or (2) retry command just after failure of each command.

(1) Software Reset Sequence

Since the slave side may be outputting “L” level, do not force to drive “H” level, when the master side drives the SDA port. This is for preventing a bus conflict. The additional hardware is not necessary for this software reset sequence.

9 set of “Start Conditions and one “1” data”



Send “Start Condition and one data “1””.
Repeat these 9 times just before Write or Read command.

(2) Command Retry

Command retry is useful to recover from failure response during I²C communication.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	– 0.5	+6.0	V
Input voltage*	V_{IN}	– 0.5	V_{DD} + 0.5 (≤ 6.0)	V
Output voltage*	V_{OUT}	– 0.5	V_{DD} + 0.5 (≤ 6.0)	V
Operation ambient temperature	T_A	– 40	+ 85	°C
Storage temperature	Tstg	– 55	+ 125	°C

*: These parameters are based on the condition that VSS is 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*	V_{DD}	3.0	—	5.5	V
"H" level input voltage*	V_{IH}	V_{DD} × 0.8	—	5.5	V
"L" level input voltage*	V_{IL}	V_{SS}	—	V_{DD} × 0.2	V
Operation ambient temperature	T_A	– 40	—	+ 85	°C

*: These parameters are based on the condition that VSS is 0 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current*[1]	$\|I_{LI}\|$	V_{IN} = 0 V to V_{DD}	—	—	1	µA
Output leakage current*[2]	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{DD}	—	—	1	µA
Operating power supply current	I_{DD}	SCL = 400 kHz	—	40	80	µA
		SCL = 1000 kHz	—	90	130	µA
Standby current	I_{SB}	SCL, SDA = V_{DD} WP = 0 V or V_{DD} or Open Under Stop Condition T_A = + 25 °C	—	5	10	µA
“L” level output voltage	V_{OL}	I_{OL} = 3 mA	—	—	0.4	V
Input resistance for WP, A1, and A2 pins	R_{IN}	V_{IN} = V_{IL} (Max)	50	—	—	kΩ
		V_{IN} = V_{IH} (Min)	1	—	—	MΩ

*1: Applicable pin: SCL,SDA

*2: Applicable pin: SDA

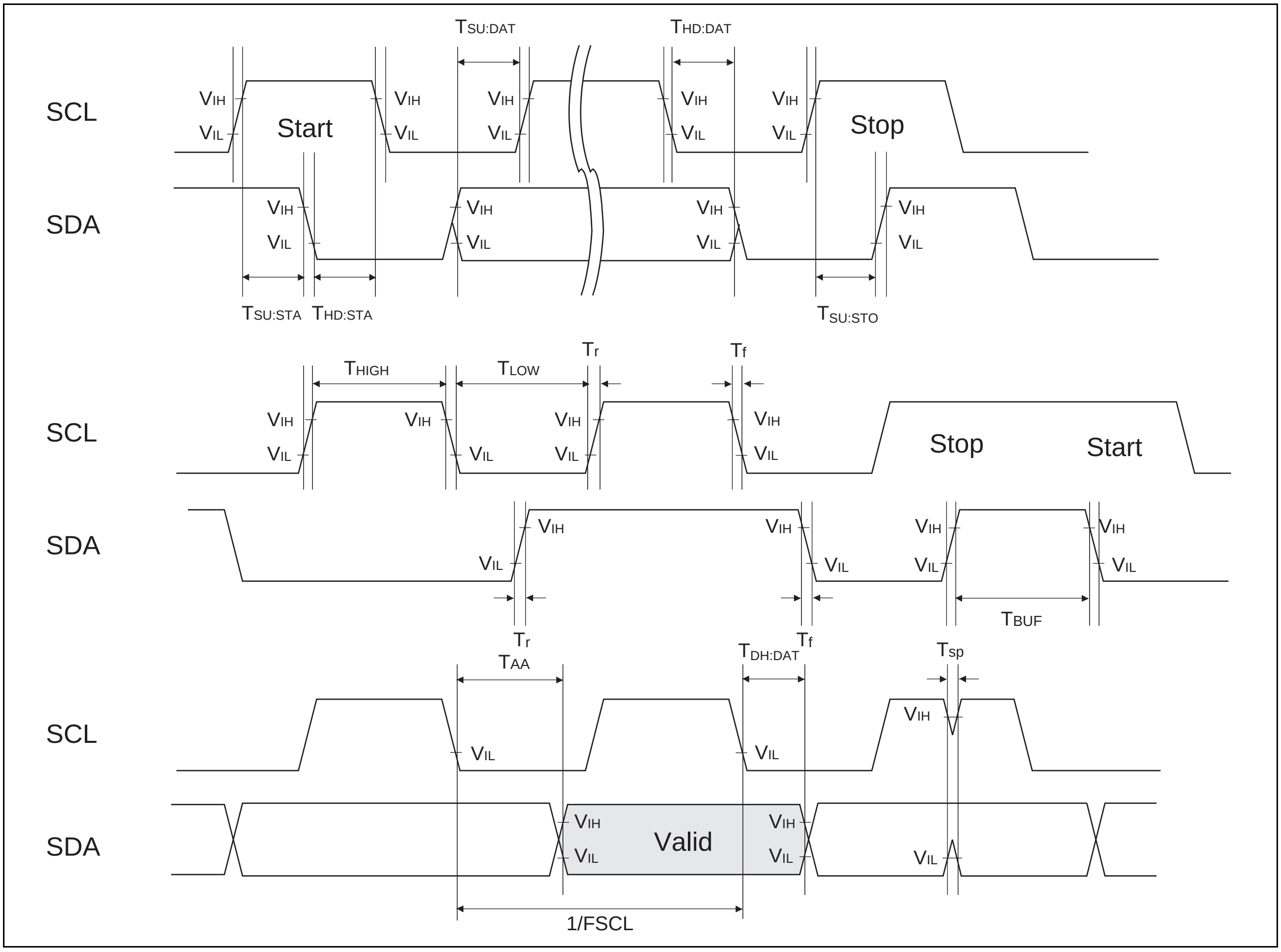
2. AC Characteristics

Parameter	Symbol	Value						Unit
		STANDARD MODE		FAST MODE		FAST MODE PLUS		
		Min	Max	Min	Max	Min	Max	
SCL clock frequency	FSCL	0	100	0	400	0	1000	kHz
Clock high time	T_{HIGH}	4000	—	600	—	400	—	ns
Clock low time	T_{LOW}	4700	—	1300	—	600	—	ns
SCL/SDA rising time	T_r	—	1000	—	300	—	300	ns
SCL/SDA falling time	T_f	—	300	—	300	—	100	ns
Start condition hold	$T_{HD:STA}$	4000	—	600	—	250	—	ns
Start condition setup	$T_{SU:STA}$	4700	—	600	—	250	—	ns
SDA input hold	$T_{HD:DAT}$	0	—	0	—	0	—	ns
SDA input setup	$T_{SU:DAT}$	250	—	100	—	100	—	ns
SDA output hold	$T_{DH:DAT}$	0	—	0	—	0	—	ns
Stop condition setup	$T_{SU:STO}$	4000	—	600	—	250	—	ns
SDA output access after SCL falling	T_{AA}	—	3000	—	900	—	550	ns
Pre-charge time	T_{BUF}	4700	—	1300	—	500	—	ns
Noise suppression time (SCL and SDA)	T_{SP}	—	50	—	50	—	50	ns

AC characteristics were measured under the following measurement conditions.

Power supply voltage : STANDARD MODE and FAST MODE 3.0 V to 5.5 V
: FAST MODE PLUS 4.5 V to 5.5 V
Operation ambient temperature : − 40 °C to + 85 °C
Input voltage magnitude : $V_{DD} \times 0.2$ to $V_{DD} \times 0.8$
Input rising time : 5 ns
Input falling time : 5 ns
Input judge level : $V_{DD}/2$
Output judge level : $V_{DD}/2$

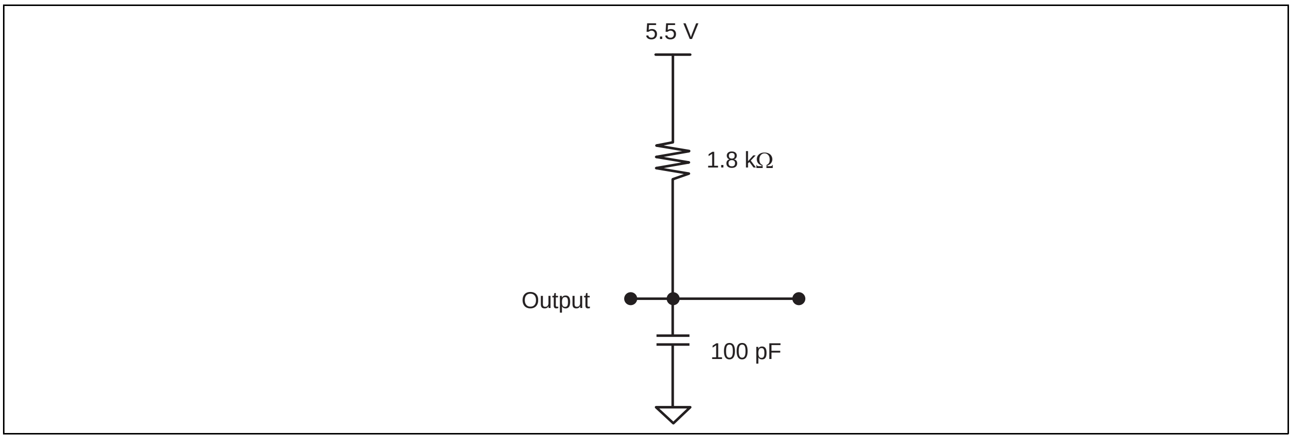
3. AC Timing Definitions



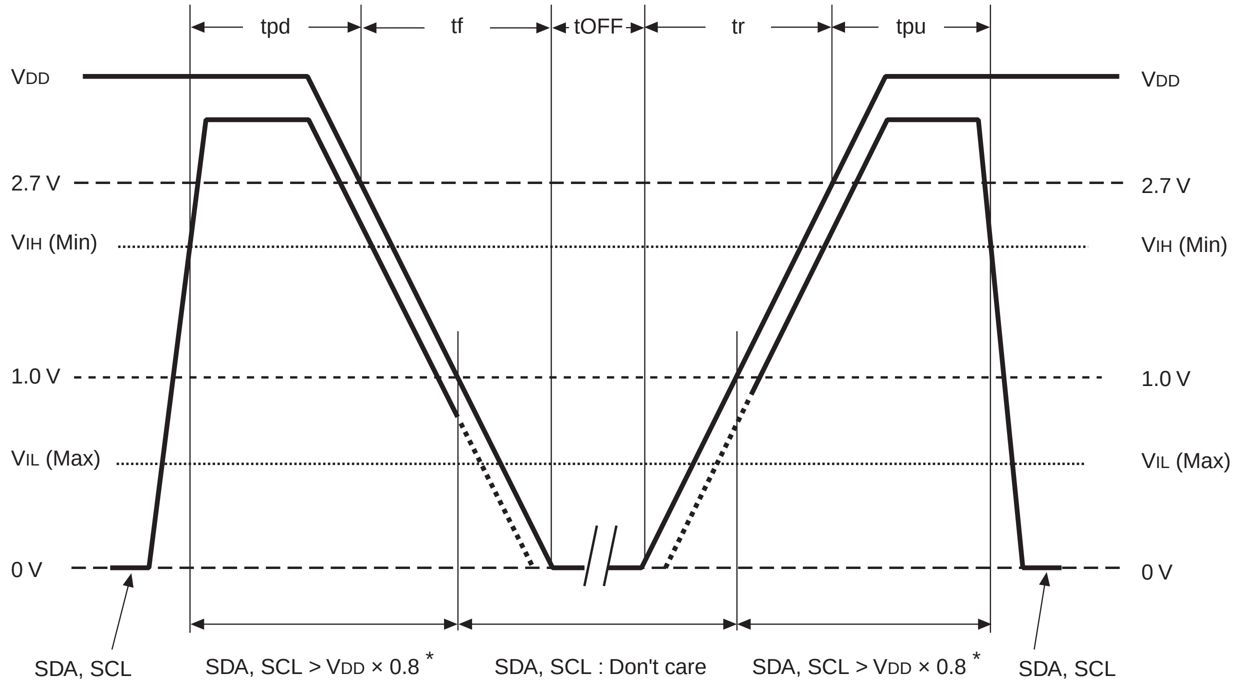
4. Pin Capacitance

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
I/O capacitance	$C_{I/O}$	$V_{DD} = V_{IN} = V_{OUT} = 0$ V, f = 1 MHz, $T_A = +25$ °C	—	—	15	pF
Input capacitance	C_{IN}		—	—	15	pF

5. AC Test Load Circuit



■ POWER ON SEQUENCE



* : SDA, SCL (Max) < V_{DD} + 0.5 V

Parameter	Symbol	Value		Unit	Condition
		Min	Max		
SDA, SCL level hold time during power down	tpd	85	—	ns	—
SDA, SCL level hold time during power up	tpu	85	—	ns	V_{DD} = 5.0V ± 0.5V Operation
		0.5	—	ms	V_{DD} = 3.3V ± 0.3V Operation
Power supply rising time	tr	0.5	50	ms	V_{DD} = 5.0V ± 0.5V Operation
		0.005	50		V_{DD} = 3.3V ± 0.3V Operation
Power supply falling time	tf	0.5	50	ms	—
Power off time	tOFF	50	—	ms	—

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

■ FRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance*1	10^{12}	—	Times/byte	Operation Ambient Temperature T_A = + 85 °C
Data Retention*2	10	—	Years	Operation Ambient Temperature T_A = + 85 °C
	95	—		Operation Ambient Temperature T_A = + 55 °C
	≥ 200	—		Operation Ambient Temperature T_A = + 35 °C

*1 : Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

*2 : Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

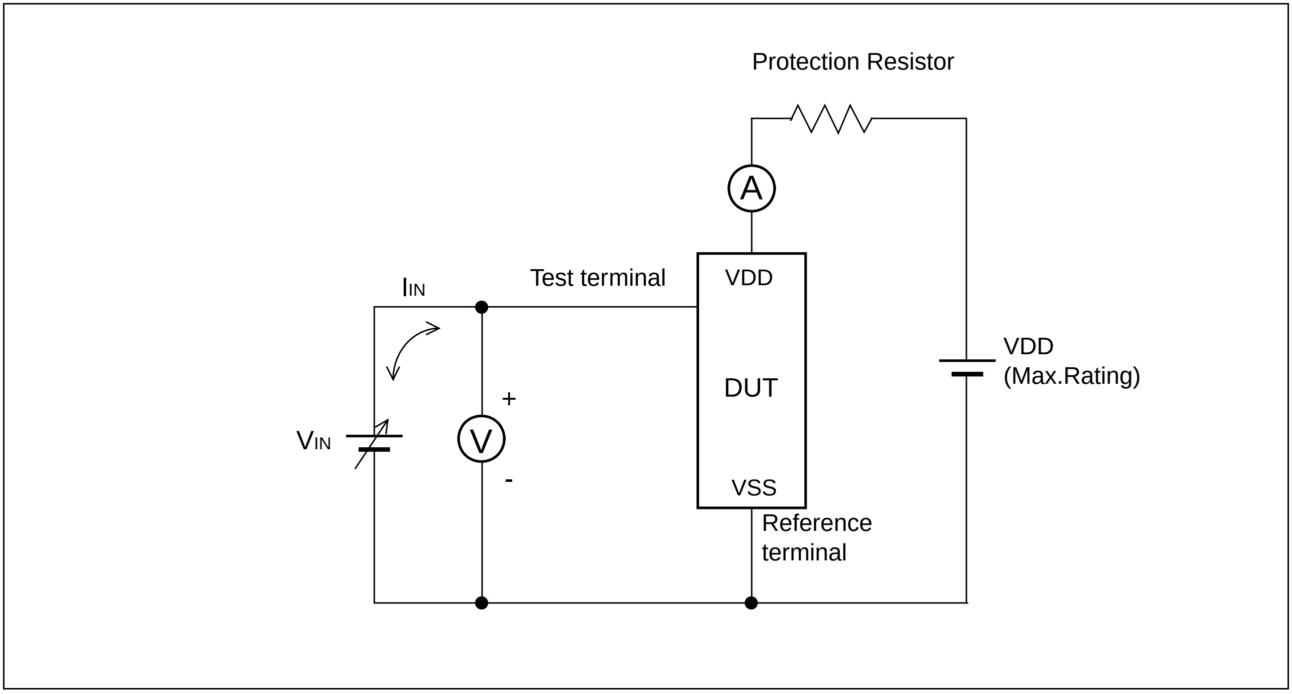
■ NOTE ON USE

- We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.
- During the access period from the start condition to the stop condition, keep the level of WP, A1, and A2 pins to the "H" level or the "L" level.

■ ESD AND LATCH-UP

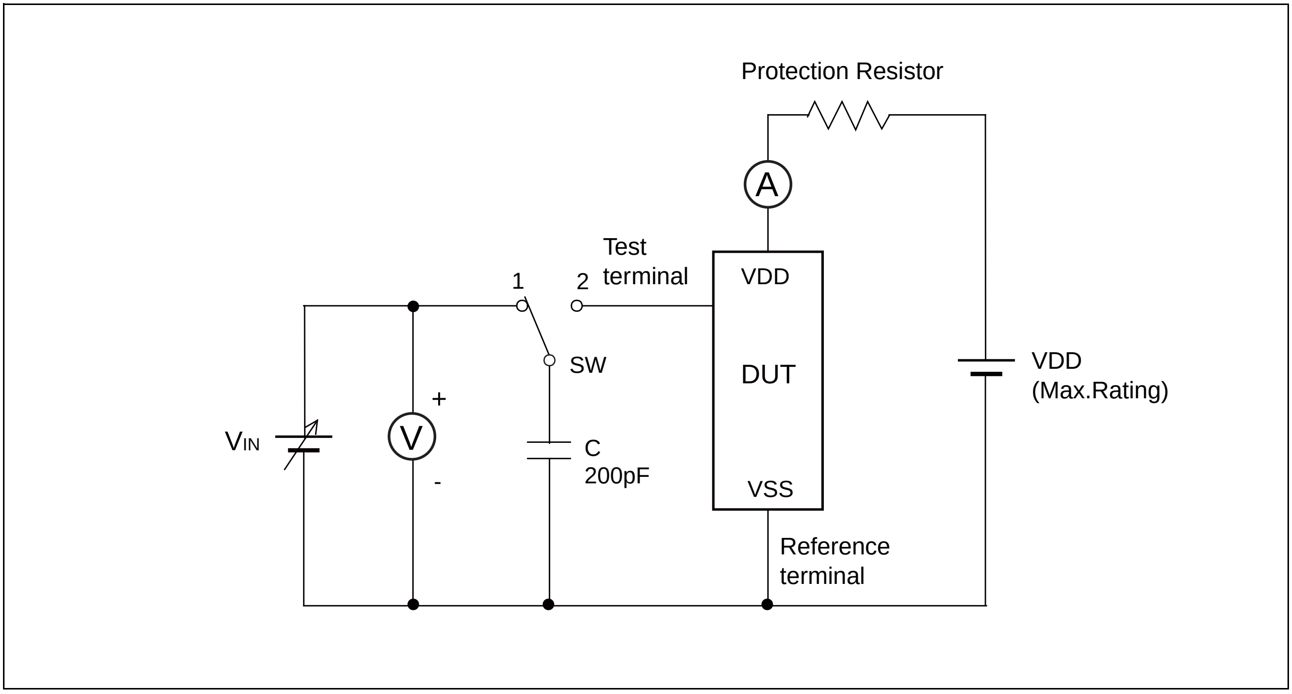
Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85RC04VPNF-G-JNE1	≥ |2000 V|
ESD MM (Machine Model) JESD22-A115 compliant		≥ |200 V|
ESD CDM (Charged Device Model) JESD22-C101 compliant		—
Latch-Up (I-test) JESD78 compliant		—
Latch-Up (V_{supply} overvoltage test) JESD78 compliant		—
Latch-Up (Current Method) Proprietary method		—
Latch-Up (C-V Method) Proprietary method		≥ |200 V|

- Current method of Latch-Up Resistance Test



Note : The voltage V_{IN} is increased gradually and the current I_{IN} of 300 mA at maximum shall flow. Confirm the latch up does not occur under I_{IN} = ± 300 mA.
In case the specific requirement is specified for I/O and I_{IN} cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

- C-V method of Latch-Up Resistance Test



Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle.
Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020D)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS. Please refer to the following web site for more details of current status on contained restricted substances in our products.

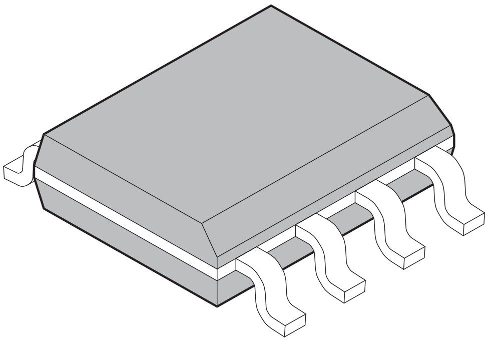
http://www.fujitsu.com/global/services/microelectronics/environment/products/

■ ORDERING INFORMATION

Part number	Package	Shipping form	Minimum shipping quantity
MB85RC04VPNF-G-JNE1	8-pin, plastic SOP (FPT-8P-M02)	Tube	—*
MB85RC04VPNF-G-JNERE1	8-pin, plastic SOP (FPT-8P-M02)	Embossed Carrier tape	1500

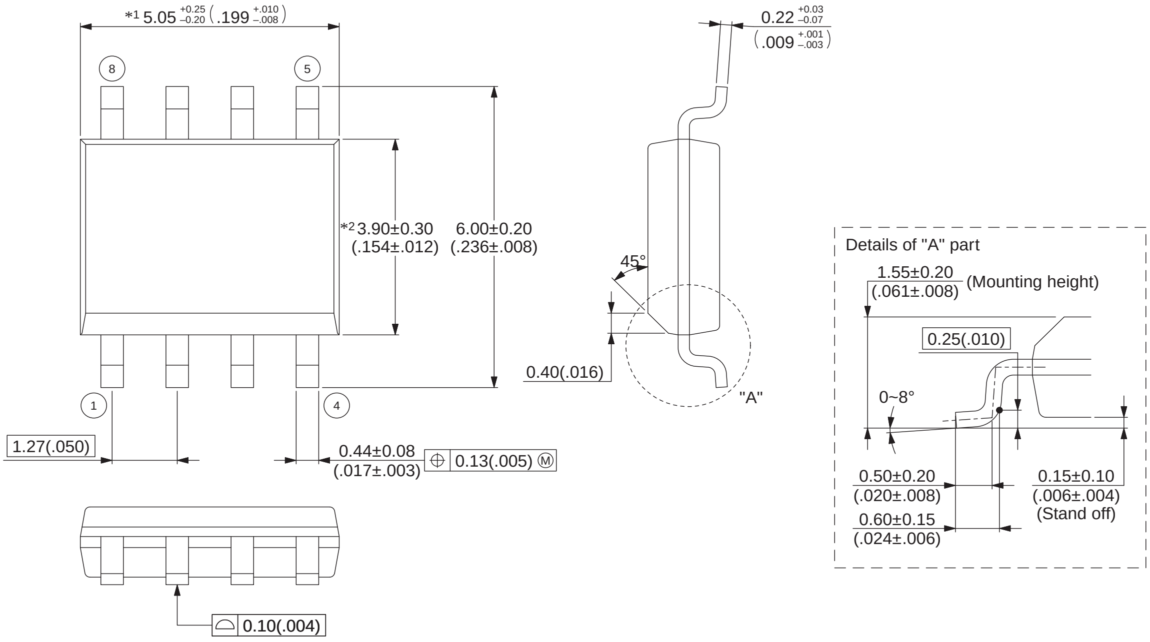
*: Please contact our sales office about minimum shipping quantity.

■ PACKAGE DIMENSION

8-pin plastic SOP  (FPT-8P-M02)	Lead pitch	1.27 mm
	Package width × package length	3.9 mm × 5.05 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.75 mm MAX
	Weight	0.06 g

8-pin plastic SOP
(FPT-8P-M02)

Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.

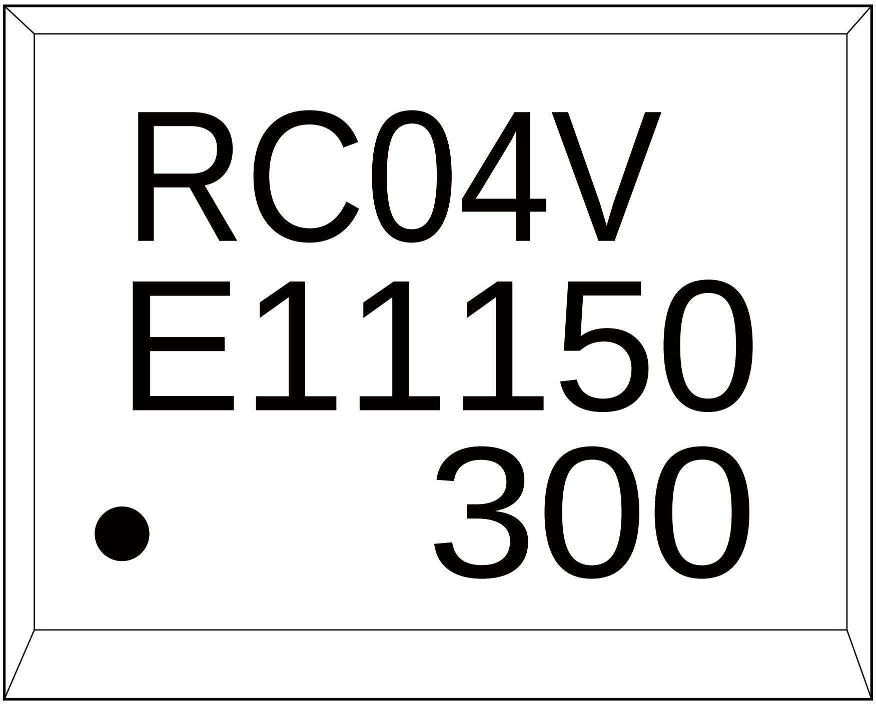


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ MARKING

[MB85RC04VPNF-G-JNE1]
[MB85RC04VPNF-G-JNERE1]



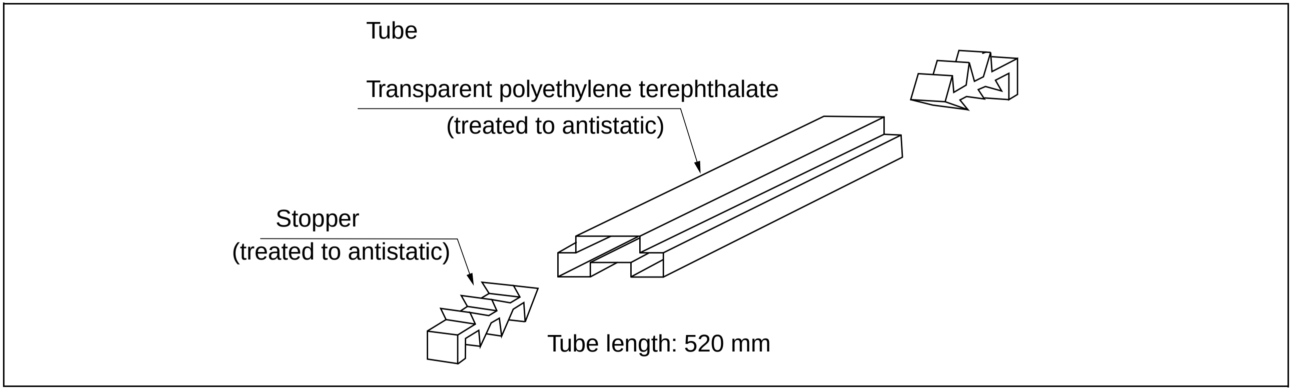
[FPT-8P-M02]

■ PACKING INFORMATION

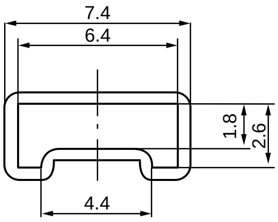
1. Tube

1.1 Tube Dimensions

- Tube/stopper shape

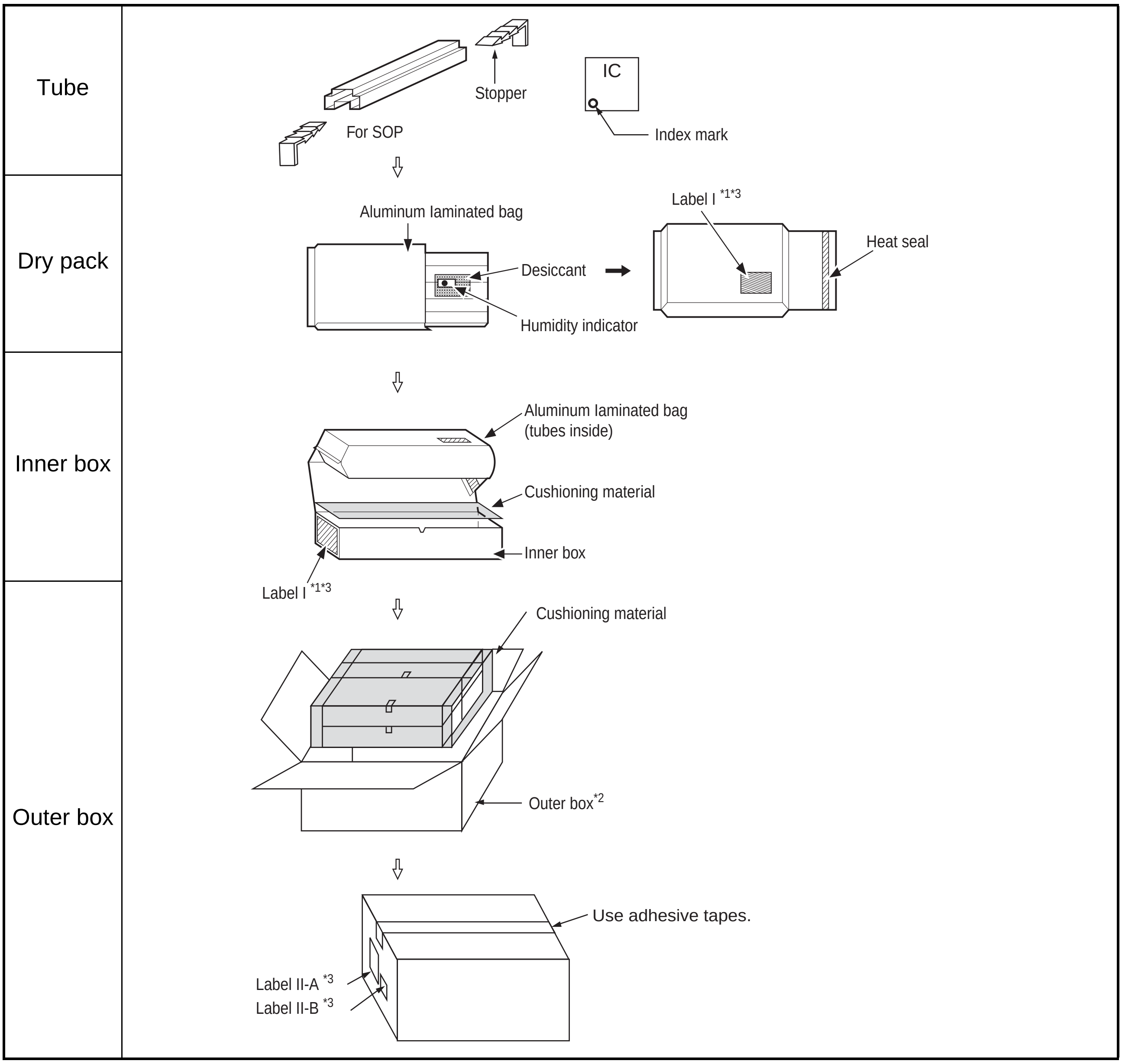


Tube cross-sections and Maximum quantity

Package form	Package code	Maximum quantity		
		pcs/ tube	pcs/inner box	pcs/outer box
SOP, 8, plastic (2)  F08008-SET1-PET:FJ99L-0022-E0008-1-K-3 t = 0.5 Transparent polyethylene terephthalate	FPT-8P-M02	95	7600	30400

(Dimensions in mm)

1.2 Tube Dry pack packing specifications



*1: For a product of witch part number is suffixed with “E1”, a “ G Pb ” marks is display to the moisture barrier bag and the inner boxes.

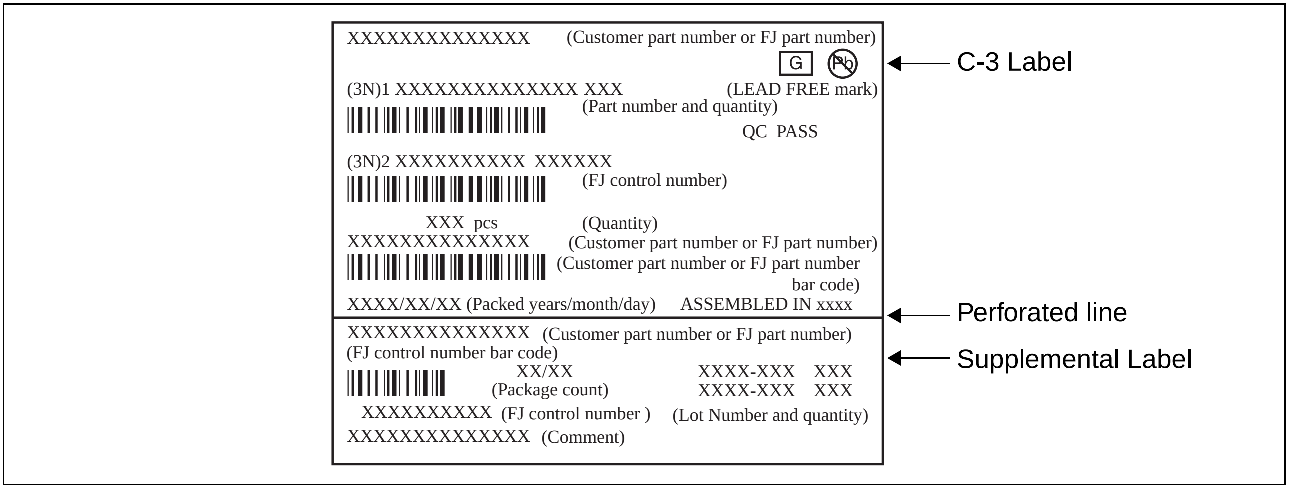
*2: The space in the outer box will be filled with empty inner boxes, or cushions, etc.

*3: Please refer to an attached sheet about the indication label.

Note: The packing specifications may not be applied when the product is delivered via a distributor.

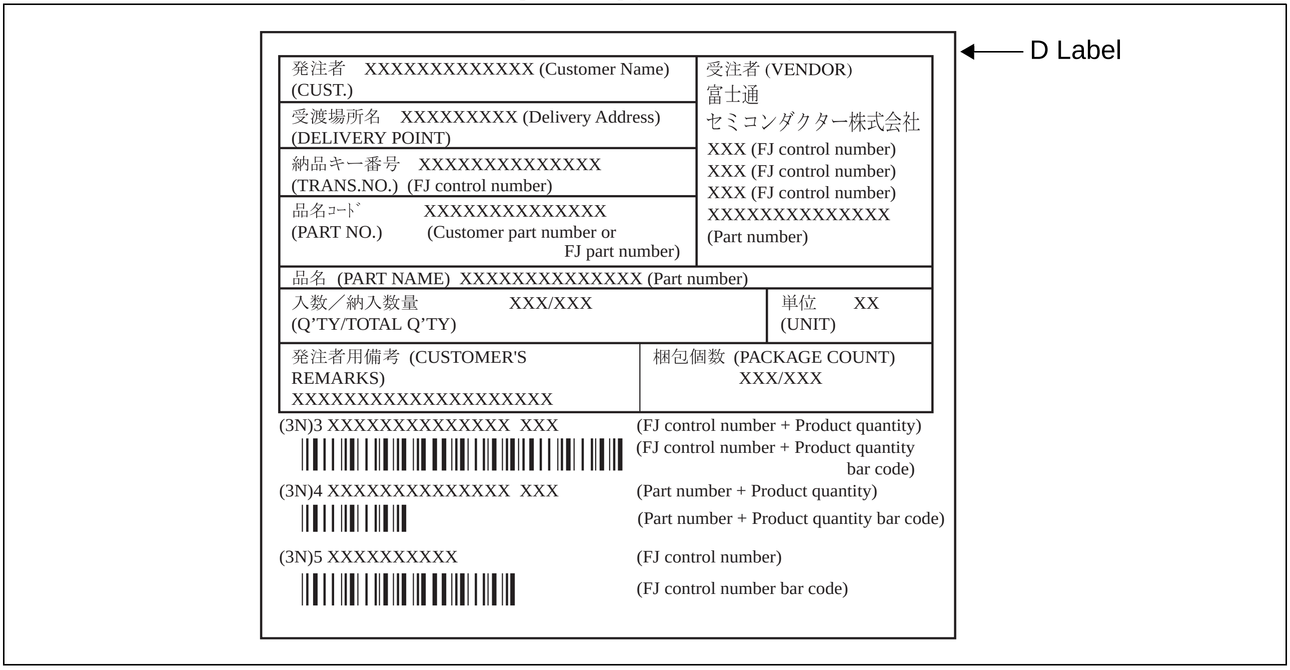
1.3 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



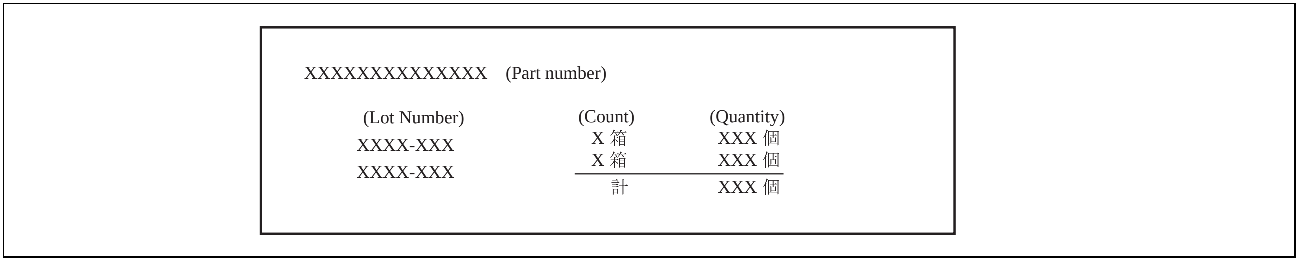
XXXXXXXXXXXXXX (Customer part number or FJ part number)
G (LEAD FREE mark)
(3N)1 XXXXXXXXXXXXXX XXX (Part number and quantity)
QC PASS
(3N)2 XXXXXXXXXX XXXXXX (FJ control number)
XXX pcs (Quantity)
XXXXXXXXXXXXXX (Customer part number or FJ part number)
(Customer part number or FJ part number bar code)
XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx
XXXXXXXXXXXXXX (Customer part number or FJ part number)
(FJ control number bar code)
XX/XX (Package count)
XXXX-XXX XXX
XXXX-XXX XXX
(Lot Number and quantity)
XXXXXXXXXX (FJ control number)
XXXXXXXXXXXXXX (Comment)

Label II-A: Label on Outer box [D Label] (100mm × 100mm)



発注者 XXXXXXXXXXXXX (Customer Name)
(CUST.)
受渡場所名 XXXXXXXXX (Delivery Address)
(DELIVERY POINT)
納品キー番号 XXXXXXXXXXXXXX
(TRANS.NO.) (FJ control number)
品名ｺｰﾄﾞ XXXXXXXXXXXXXX
(PART NO.) (Customer part number or FJ part number)
受注者 (VENDOR)
富士通
セミコンダクター株式会社
XXX (FJ control number)
XXX (FJ control number)
XXX (FJ control number)
XXXXXXXXXXXXXX
(Part number)
品名 (PART NAME) XXXXXXXXXXXXXX (Part number)
入数／納入数量 XXX/XXX
(Q'TY/TOTAL Q'TY)
単位 XX
(UNIT)
発注者用備考 (CUSTOMER'S REMARKS)
XXXXXXXXXXXXXXXXXXXXX
梱包個数 (PACKAGE COUNT)
XXX/XXX
(3N)3 XXXXXXXXXXXXXX XXX (FJ control number + Product quantity)
(FJ control number + Product quantity bar code)
(3N)4 XXXXXXXXXXXXXX XXX (Part number + Product quantity)
(Part number + Product quantity bar code)
(3N)5 XXXXXXXXXX (FJ control number)
(FJ control number bar code)

Label II-B: Outer boxes product indicate



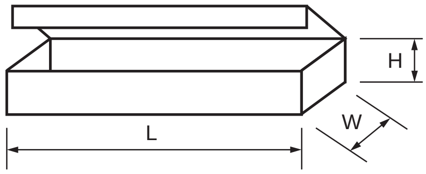
XXXXXXXXXXXXXX (Part number)

(Lot Number)	(Count)	(Quantity)
XXXX-XXX	X 箱	XXX 個
XXXX-XXX	X 箱	XXX 個
	計	XXX 個

Note: Depending on shipment state, “Label II-A” and “Label II-B” on the external boxes might not be printed.

1.4 Dimensions for Containers

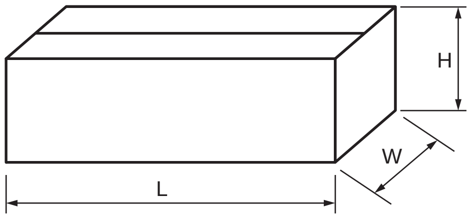
(1) Dimensions for inner box



L	W	H
540	125	75

(Dimensions in mm)

(2) Dimensions for outer box



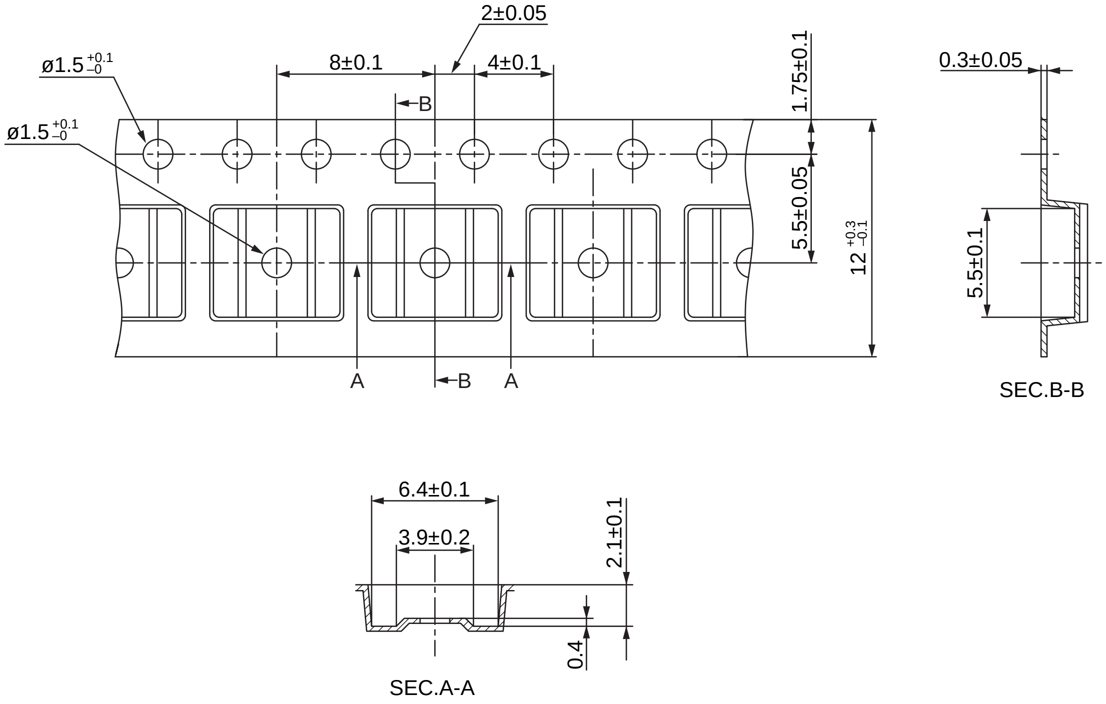
L	W	H
565	270	180

(Dimensions in mm)

2. Emboss Tape

2.1 Tape Dimensions

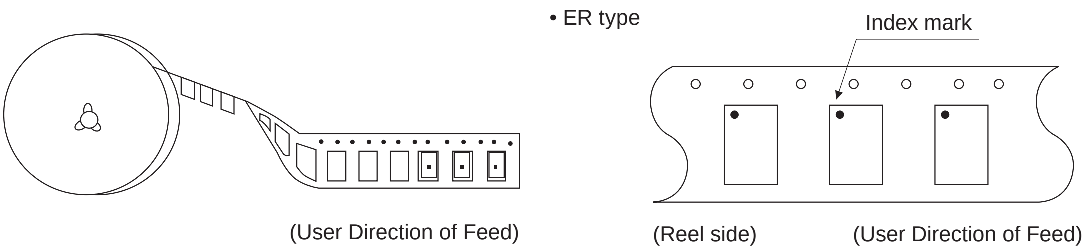
PKG code	Reel No	Maximum storage capacity		
		pcs/reel	pcs/inner box	pcs/outer box
FPT-8P-M02	3	1500	1500	10500



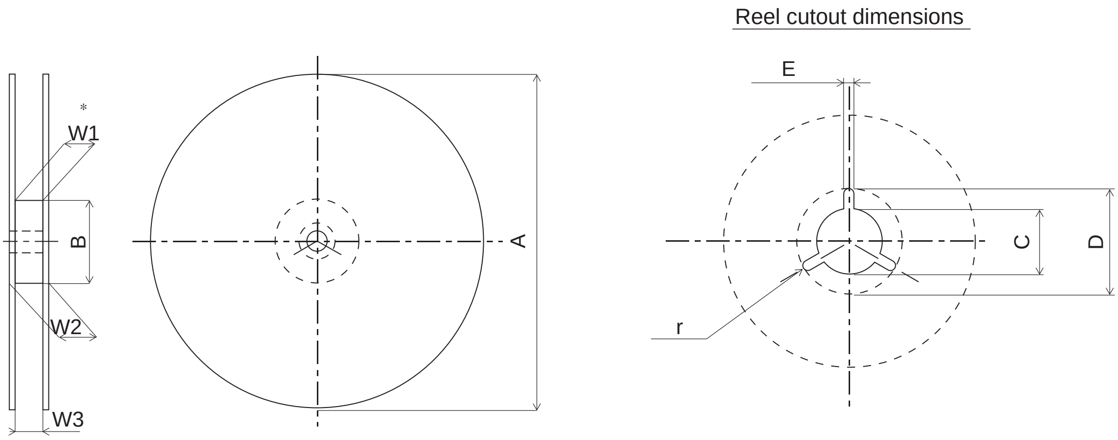
(Dimensions in mm)

Material : Conductive polystyrene
Heat proof temperature : No heat resistance.
Package should not be baked
by using tape and reel.

2.2 IC orientation



2.3 Reel dimensions

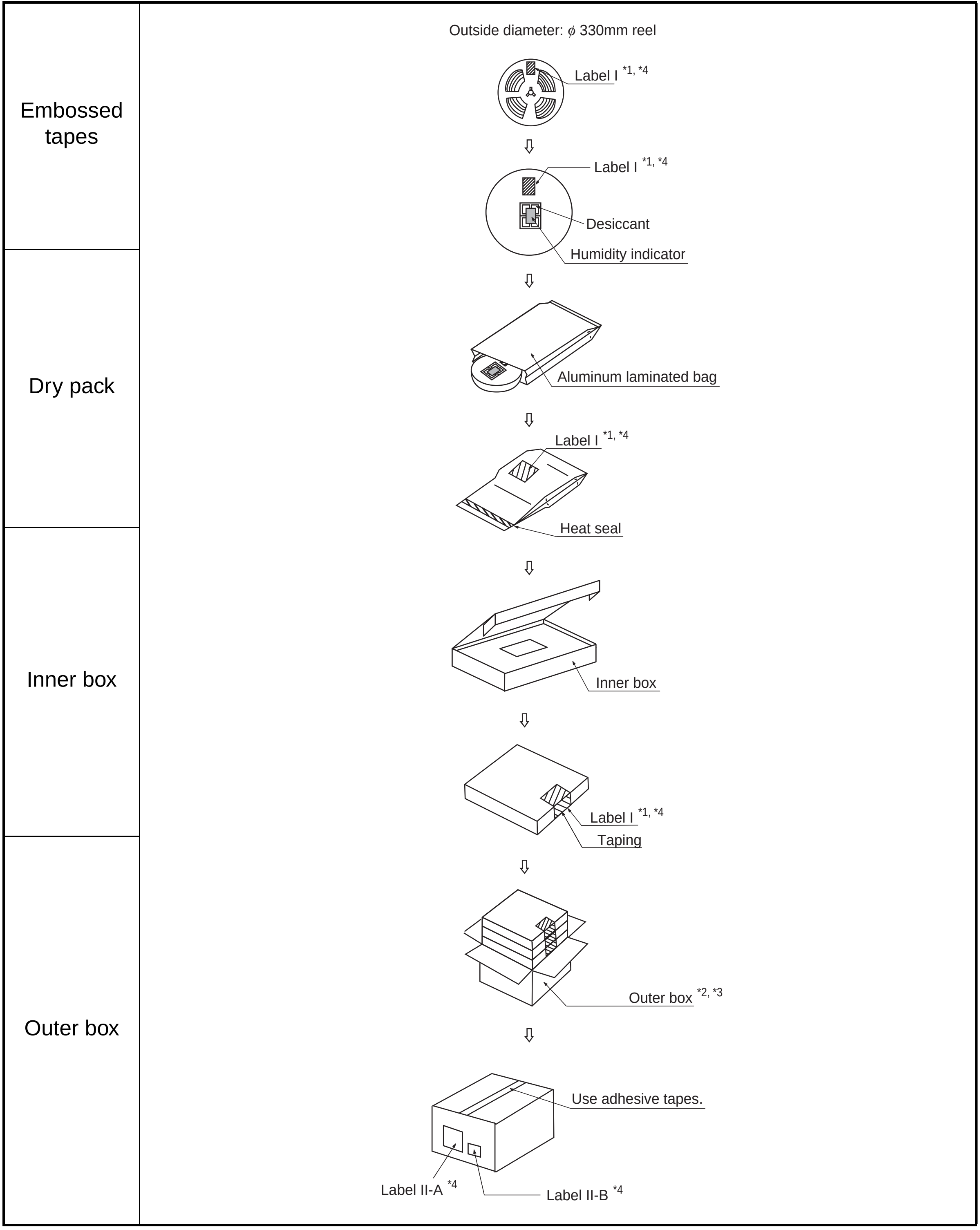


*: Hub unit width dimensions

Dimensions in mm

Reel No	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Tape width / Symbol	8	12		16		24		32		44		56	12	16	24
A	254 ± 2	254 ± 2	330 ± 2	254 ± 2	330 ± 2	254 ± 2	330 ± 2	330 ± 2							
B	100^{+2}_{-0}							100^{+2}_{-0}	150^{+2}_{-0}	100^{+2}_{-0}	150^{+2}_{-0}	100^{+2}_{-0}	100 ± 2		
C	13 ± 0.2												$13^{+0.5}_{-0.2}$		
D	21 ± 0.8												$20.5^{+1}_{-0.2}$		
E	2 ± 0.5														
W1	8.4^{+2}_{-0}	12.4^{+2}_{-0}		16.4^{+2}_{-0}		24.4^{+2}_{-0}		32.4^{+2}_{-0}		44.4^{+2}_{-0}		56.4^{+2}_{-0}	12.4^{+1}_{-0}	16.4^{+1}_{-0}	$24.4^{+0.1}_{-0}$
W2	less than 14.4	less than 18.4		less than 22.4		less than 30.4		less than 38.4		less than 50.4		less than 62.4	less than 18.4	less than 22.4	less than 30.4
W3	7.9 ~ 10.9	11.9 ~ 15.4		15.9 ~ 19.4		23.9 ~ 27.4		31.9 ~ 35.4		43.9 ~ 47.4		55.9 ~ 59.4	12.4 ~ 14.4	16.4 ~ 18.4	24.4 ~ 26.4
r	1.0														

2.4 Taping (ϕ330mm Reel) Dry Pack Packing Specifications



*1: For a product of witch part number is suffixed with “E1”, a “ G Pb ” marks is display to the moisture barrier bag and the inner boxes.

*2: The size of the outer box may be changed depending on the quantity of inner boxes.

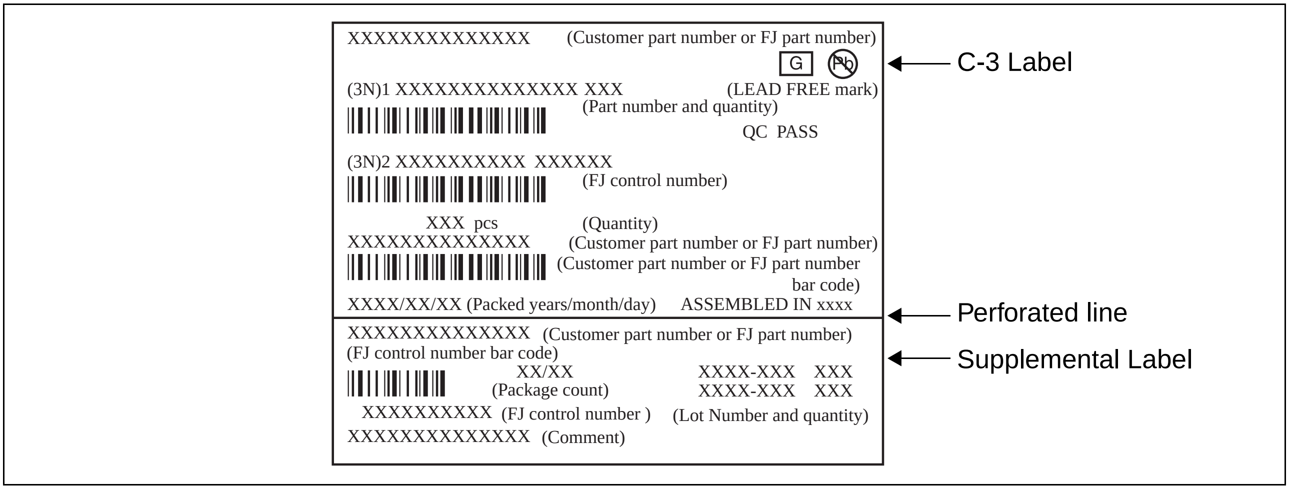
*3: The space in the outer box will be filled with empty inner boxes, or cushions, etc.

*4: Please refer to an attached sheet about the indication label.

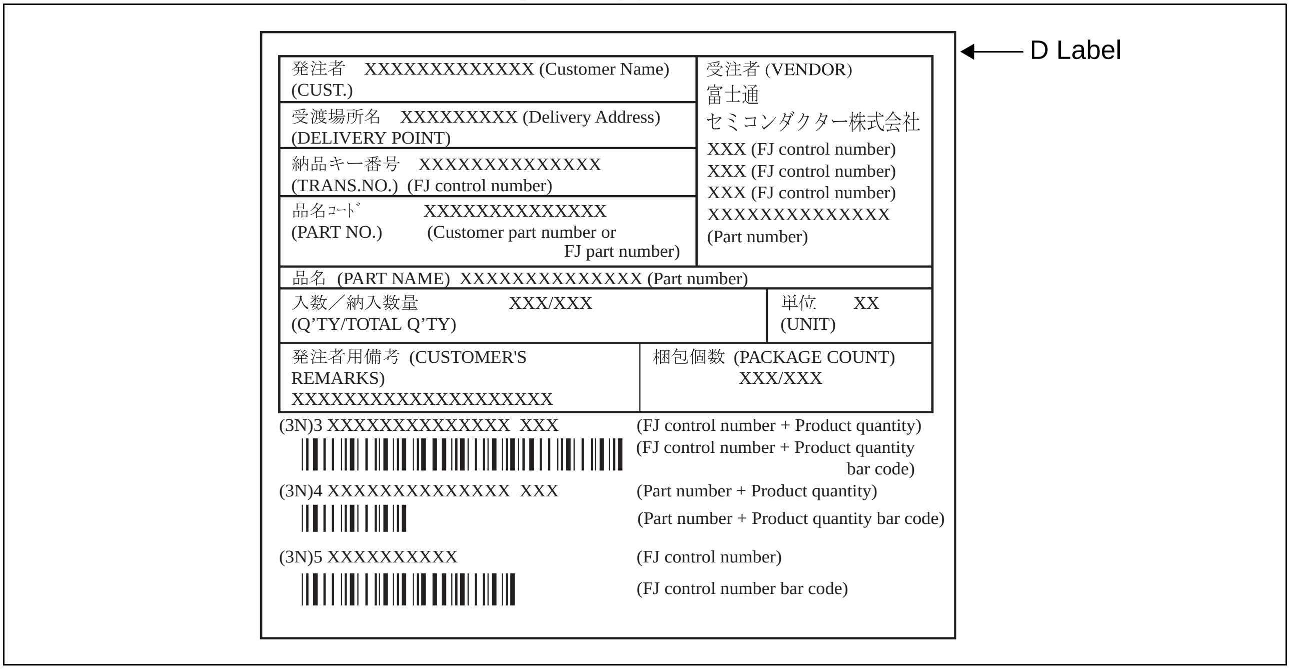
Note: The packing specifications may not be applied when the product is delivered via a distributor.

2.5 Product label indicators

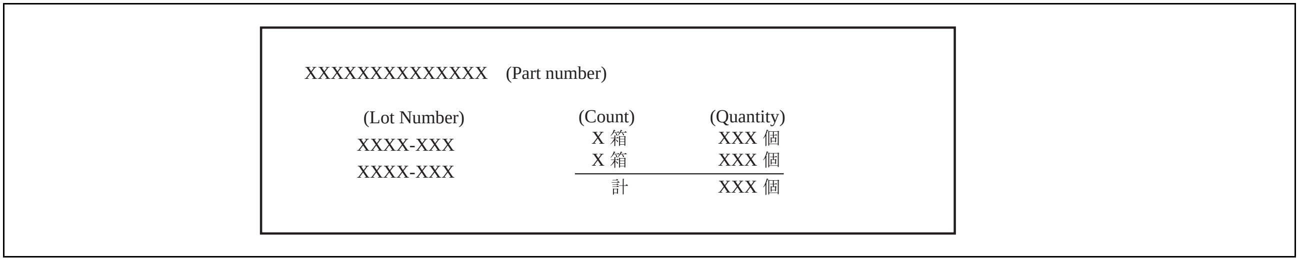
Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]


XXXXXXXXXXXXXX (Customer part number or FJ part number)
G Pb
(3N)1 XXXXXXXXXXXXXX XXX (LEAD FREE mark)
(Part number and quantity)
QC PASS
(3N)2 XXXXXXXXXX XXXXXX
(FJ control number)
XXX pcs (Quantity)
XXXXXXXXXXXXXX (Customer part number or FJ part number)
(Customer part number or FJ part number bar code)
XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx
XXXXXXXXXXXXXX (Customer part number or FJ part number)
(FJ control number bar code)
XX/XX (Package count)
XXXX-XXX XXX
XXXX-XXX XXX
XXXXXXXXXX (FJ control number) (Lot Number and quantity)
XXXXXXXXXXXXXX (Comment)

Label II-A: Label on Outer box [D Label] (100mm × 100mm)


発注者 XXXXXXXXXXXXX (Customer Name)
(CUST.)
受渡場所名 XXXXXXXXX (Delivery Address)
(DELIVERY POINT)
納品キー番号 XXXXXXXXXXXXXX
(TRANS.NO.) (FJ control number)
品名ｺｰﾄﾞ XXXXXXXXXXXXXX
(PART NO.) (Customer part number or FJ part number)
受注者 (VENDOR)
富士通
セミコンダクター株式会社
XXX (FJ control number)
XXX (FJ control number)
XXX (FJ control number)
XXXXXXXXXXXXXX
(Part number)
品名 (PART NAME) XXXXXXXXXXXXXX (Part number)
入数／納入数量 XXX/XXX
(Q'TY/TOTAL Q'TY)
単位 XX
(UNIT)
発注者用備考 (CUSTOMER'S REMARKS)
XXXXXXXXXXXXXXXXXXXX
梱包個数 (PACKAGE COUNT)
XXX/XXX
(3N)3 XXXXXXXXXXXXXX XXX (FJ control number + Product quantity)
(FJ control number + Product quantity bar code)
(3N)4 XXXXXXXXXXXXXX XXX (Part number + Product quantity)
(Part number + Product quantity bar code)
(3N)5 XXXXXXXXXX (FJ control number)
(FJ control number bar code)

Label II-B: Outer boxes product indicate

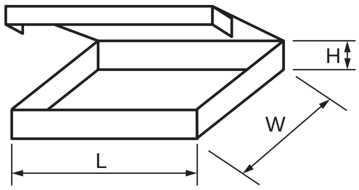

XXXXXXXXXXXXXX (Part number)

(Lot Number)	(Count)	(Quantity)
XXXX-XXX	X 箱	XXX 個
XXXX-XXX	X 箱	XXX 個
	計	XXX 個

Note: Depending on shipment state, “Label II-A” and “Label II-B” on the external boxes might not be printed.

2.6 Dimensions for Containers

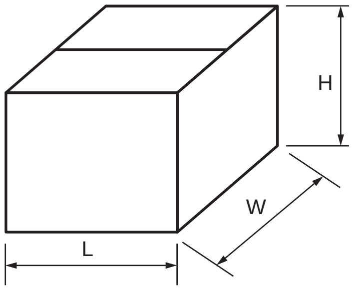
(1) Dimensions for inner box



Tape width	L	W	H
12, 16	365	345	40
24, 32			50
44			65
56			75

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
415	400	315

(Dimensions in mm)

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
16	■ POWER ON/OFF SEQUENCE	Defined values of tpu and tr at operation voltage. Min Max Unit Condition tpu 85 — ns V_{DD} = 5.0 V ± 0.5 V Operation 0.5 — ms V_{DD} = 3.3 V ± 0.3 V Operation tr 0.5 50 ms V_{DD} = 5.0 V ± 0.5 V Operation 0.005 50 ms V_{DD} = 3.3 V ± 0.3 V Operation
17	■ NOTE ON USE	Revised the following description: “Data written before performing IR reflow is not guaranteed after IR reflow.” → “We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.”
18	■ REFLOW CONDITIONS AND FLOOR LIFE	Revised to following description. [JEDEC MSL] : Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020D)
	■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES	Changed the title and revised the description which refers to a website.
19	■ ORDERING INFORMATION	Changed the Minimum shipping quantity. 1 → —* Added the following note below table. *: Please contact our sales office about minimum shipping quantity.
23	1.2 Tube Dry pack packing specifications	Revised the figure of Dry pack.

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