Absolute Maximum Ratings

IN, GATE, GATEP .....-0.3V to +80V
SHDN, CLEAR .....-0.3V to (V_{IN} + 0.3V)
POK, OUTFB.....-0.3V to +80V
GATE to OUTFB.....-0.3V to +12V
GATEP to IN.....-12V to +0.3V
OVSET, UVSET, POKSET .....-0.3V to +12V
Current Sink/Source (All Pins) 50mA
All Other Pins to GND .....-0.3V to (V_{IN} + 0.3V)

(All pins referenced to GND.)

Continuous Power Dissipation (T_A = +70°C)
6-Pin TDFN (derate 23.8mW/°C above +70°C) 1904.8mW
8-Pin TDFN (derate 24.4mW/°C above +70°C) 1951.2mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

6 TDFN-EP

PACKAGE CODE	T633+2
Outline Number	21-0137
Land Pattern Number	90-0058
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	55°C/W
Junction to Case (θ_{JC})	9°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	42°C/W
Junction to Case (θ_{JC})	9

8 TDFN-EP

PACKAGE CODE	T833+2
Outline Number	21-0137
Land Pattern Number	90-0059
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	54°C/W
Junction to Case (θ_{JC})	8°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	8°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

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Electrical Characteristics

(V_{IN} = 14V, C_{GATE} = 6nF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}			5.5		72.0	V
Input Supply Current	I_{IN}	No load	$\overline{SHDN}$ = high		100	150	µA
			$\overline{SHDN}$ = low (MAX6497/MAX6498/MAX6499)		15	24	
			$\overline{SHDN}$ = low (MAX6495/MAX6496)		24	32	
IN Undervoltage Lockout		V_{IN} rising, enables GATE		4.75	5	5.25	V
IN Undervoltage Lockout Hysteresis		V_{IN} falling, disables GATE			155		mV
OVSET Threshold Voltage (MAX6495/MAX6496)	V_{TH+}	OVSET rising		1.22	1.24	1.26	V
	V_{TH-}	OVSET falling			1.18		
OVSET Threshold Hysteresis (MAX6495/MAX6496)	V_{HYST}	OVSET falling			5		%
OVSET Threshold Voltage (MAX6497/MAX6498)	V_{TH+}	OVSET rising		0.494	0.505	0.518	V
	V_{TH-}	OVSET falling			0.13		
OVSET Threshold Voltage (MAX6499)	V_{TH+}	OVSET rising		1.22	1.24	1.26	V
	V_{TH-}	OVSET falling			1.18		
UVSET Threshold Voltage (MAX6499)	V_{TH+}	UVSET rising		1.22	1.24	1.26	V
	V_{TH-}	UVSET falling			1.18		
OVSET/UVSET Threshold Hysteresis (MAX6499)	V_{HYST}	OVSET falling			5		%
POKSET Threshold Voltage (MAX6497/MAX6498)	$V_{POKSET+}$	POKSET rising		1.22	1.24	1.26	V
	$V_{POKSET-}$	POKSET falling			1.18		
POKSET Threshold Hysteresis (MAX6497/MAX6498)	V_{HYST}	POKSET falling			5		%
OVSET, UVSET, POKSET Input Current	I_{SET}			-50		+50	nA
Startup Response Time	t_{START}	$\overline{SHDN}$ rising (Note 2)			100		µs
GATE Rise Time		GATE rising from GND to V_{OUTFB} + 8V, OUTFB = GND			1		ms
OVSET to GATE Propagation Delay	t_{OV}	SET rising from V_{TH} - 100mV to V_{TH} + 100mV				0.6	µs
UVSET to GATE, POKSET to POK Propagation Delay		POKSET, UVSET falling from V_{TH} + 100mV to V_{TH} - 100mV			20		µs
GATE Output High Voltage	V_{OH}	V_{OUTFB} = V_{IN} = 5.5V, R_{GATE} to IN = 1MΩ		V_{IN} + 3.4	V_{IN} + 3.8	V_{IN} + 4.2	V
		V_{OUTFB} = V_{IN}, V_{IN} ≥ 14V, R_{GATE} to IN = 1MΩ		V_{IN} + 8	V_{IN} + 10	V_{IN} + 11	
GATE Output Low Voltage	V_{OL}	GATE sinking 15mA, OUTFB = GND				1	V
		V_{IN} = 5.5V, GATE sinking 1mA, OUTFB = GND				0.9	
GATE Charge-Pump Current	I_{GATE}	GATE = GND			100		µA
GATE to OUTFB Clamp Voltage	V_{CLMP}			12		18	V

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Electrical Characteristics (continued)

(V_{IN} = 14V, C_{GATE} = 6nF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN to GATEP Output Low Voltage		I_{GATEP_SINK} = 75µA, I_{GATEP_SOURCE} = 1µA	7.5		11.7	V
IN to GATEP Clamp Voltage		V_{IN} = 24V, I_{GATEP_SOURCE} = 10µA	12		18	V
$\overline{SHDN}$, $\overline{CLEAR}$ Logic-High Input Voltage	V_{IH}		1.4			V
$\overline{SHDN}$, $\overline{CLEAR}$ Logic-Low Input Voltage	V_{IL}				0.4	V
$\overline{SHDN}$ Input Pulse Width			7			µs
$\overline{CLEAR}$ Input Pulse Width				0.5		µs
$\overline{SHDN}$, $\overline{CLEAR}$ Input Pulldown Current		$\overline{SHDN}$ is Internally pulled down to GND	0.6	1.0	1.4	µA
Thermal Shutdown		(Note 3)		+160		°C
Thermal-Shutdown Hysteresis				20		°C
POKSET to POK Delay (MAX6497/MAX6498)				35		µs
POK Output Low Voltage (MAX6497/MAX6498)	V_{OL}	V_{IN} ≥ 14V, POKSET = GND, I_{SINK} = 3.2mA			0.4	V
		V_{IN} ≥ 2.8V, POKSET = GND, I_{SINK} = 100µA			0.4	
POK Leakage Current (MAX6497/MAX6498)		V_{POKSET} = 14V			100	nA

Note 1: Specifications to T_A = -40°C are guaranteed by design and not production tested.

Note 2: The MAX6495–MAX6499 power up with the external MOSFET in off mode (V_{GATE} = GND). The external MOSFET turns on t_{START} after all input conditions are valid.

Note 3: For accurate overtemperature-shutdown performance, place the device in close thermal contact with the external MOSFET.

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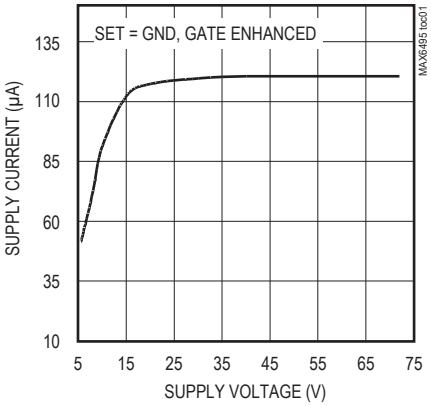
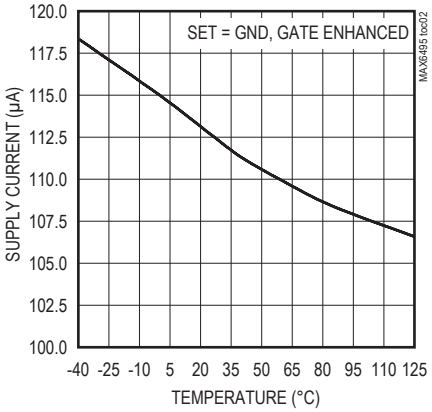
Typical Operating Characteristics

(V_{IN} = +12V, T_A = +25°C, unless otherwise noted.)

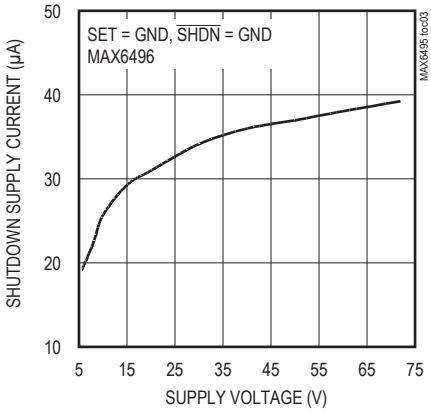
SUPPLY CURRENT vs. SUPPLY VOLTAGE



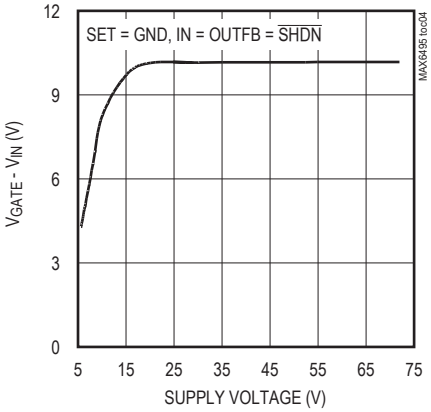
SUPPLY CURRENT vs. TEMPERATURE



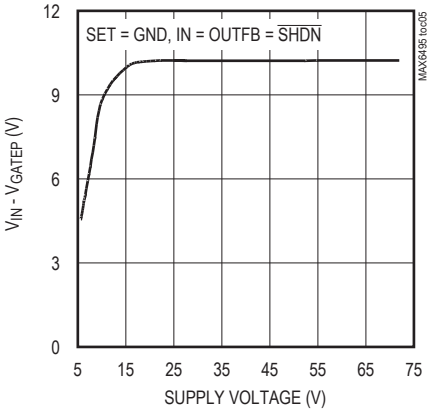
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



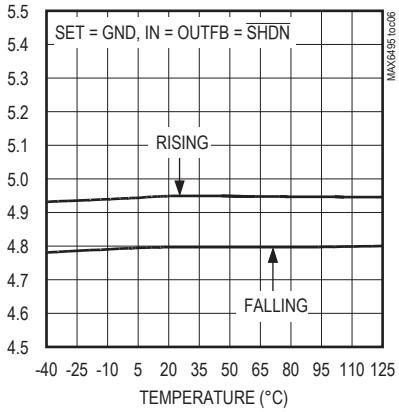
GATE VOLTAGE vs. SUPPLY VOLTAGE



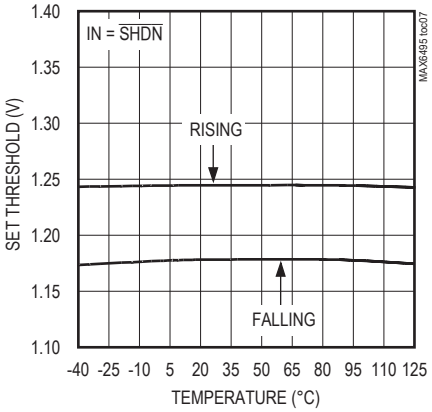
GATEP VOLTAGE vs. SUPPLY VOLTAGE



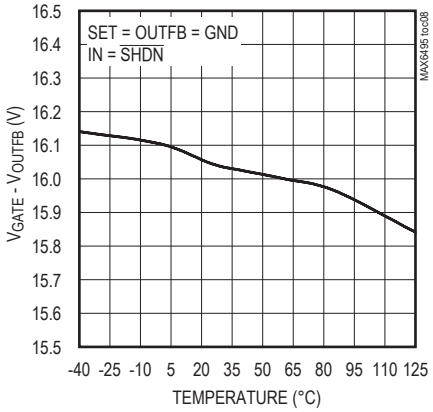
UVLO THRESHOLD vs. TEMPERATURE



SET THRESHOLD vs. TEMPERATURE



GATE TO OUTFB CLAMP VOLTAGE vs. TEMPERATURE



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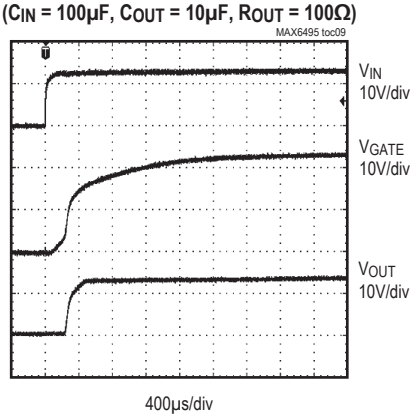
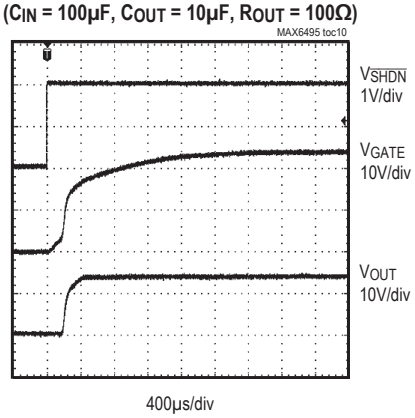
Typical Operating Characteristics (continued)

(V_{IN} = +12V, T_A = +25°C, unless otherwise noted.)

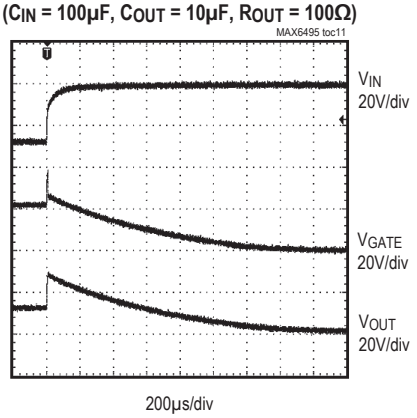
STARTUP WAVEFORM
(C_{IN} = 100µF, C_{OUT} = 10µF, R_{OUT} = 100Ω)



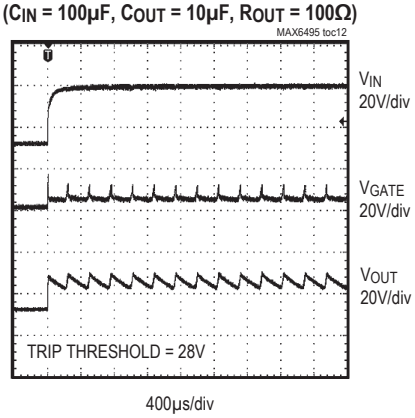
STARTUP FROM SHUTDOWN
(C_{IN} = 100µF, C_{OUT} = 10µF, R_{OUT} = 100Ω)



OVERVOLTAGE SWITCH FAULT
(C_{IN} = 100µF, C_{OUT} = 10µF, R_{OUT} = 100Ω)



OVERVOLTAGE LIMITER
(C_{IN} = 100µF, C_{OUT} = 10µF, R_{OUT} = 100Ω)



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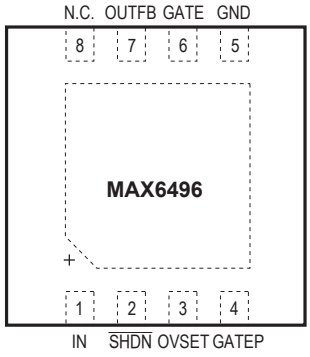
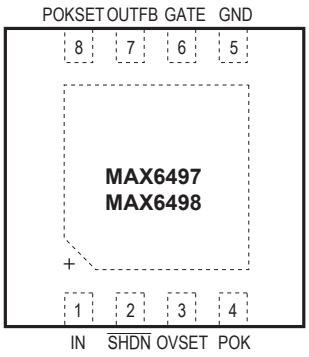
Pin Configurations

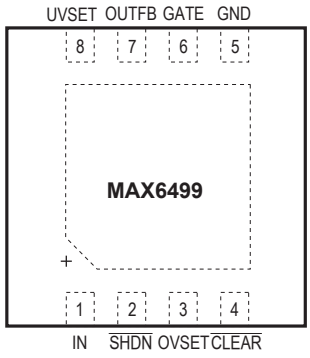
TOP VIEW



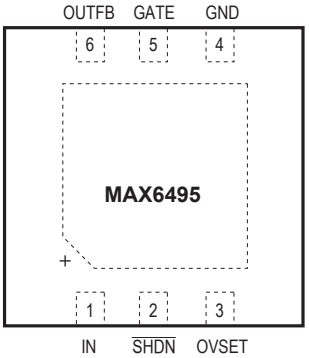
3mm x 3mm TDFN



3mm x 3mm TDFN



3mm x 3mm TDFN



3mm x 3mm TDFN

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Pin Descriptions

PIN				NAME	FUNCTION
MAX6495	MAX6496	MAX6497/ MAX6498	MAX6499		
1	1	1	1	IN	Positive Supply Voltage. Connect IN to the positive side of the input voltage. Bypass IN with a 10µF capacitor to GND.
2	2	2	2	$\overline{SHDN}$	Shutdown Input. Drive $\overline{SHDN}$ low to force GATE low and turn off the external nMOSFET. Drive $\overline{SHDN}$ low and then high to reset the overvoltage-condition latch. $\overline{SHDN}$ is internally pulled to GND with 1µA of current. Connect $\overline{SHDN}$ to IN for normal operation.
3	3	3	3	OVSET	Overvoltage-Threshold Adjustment Input. Connect OVSET to an external resistive voltage-divider network to adjust the desired overvoltage-disable or overvoltage-limit threshold. Connect the resistor network to the input side (drain) of the nMOSFET for overvoltage switch turn-off applications or to the output side (source) of the nMOSFET for overvoltage-limiting applications (MAX6495/MAX6496/MAX6499).
4	5	5	5	GND	Ground
5	6	6	6	GATE	Gate-Driver Output. Connect GATE to the gate of the external n-channel MOSFET switch. GATE is the output of a charge pump with a 100µA pullup current to 10V (typ) above IN during normal operation. GATE is quickly clamped to OUTFB during an overvoltage condition. GATE pulls low when $\overline{SHDN}$ is low.
6	7	7	7	OUTFB	Output-Voltage-Sense Input. Connect OUTFB to the source of the external nMOSFET switch.
—	4	—	—	GATEP	p-Channel Gate-Driver Output. Connect GATEP to the gate of an external pMOSFET to provide low-drop reverse-voltage protection. GATEP is biased to ensure that the pMOSFET is on during normal operating modes, the gate-to-source is not overstressed during load-dump/overvoltage conditions, and the pMOSFET is off during reverse-battery conditions.
—	8	—	—	N.C.	No Connection. Not internally connected.
—	—	4	—	POK	Power-OK Output. POK is an open-drain output. POK remains low while POKSET is below the internal POKSET threshold. POK goes high impedance when POKSET goes above the internal POKSET threshold. Connect POK to an external pullup resistor.
—	—	8	—	POKSET	Power-OK Threshold-Adjustment Input. POK remains low while POKSET is below the internal POKSET threshold (1.18V). POK goes high impedance when POKSET goes above the internal POKSET threshold (1.24V). Connect a resistive divider from OUTFB to POKSET to adjust the desired undervoltage threshold.
—	—	—	4	$\overline{CLEAR}$	Latch Clear Input. Connect $\overline{CLEAR}$ to a logic-high to latch the device off after an overvoltage condition. With OVSET below V_{TH}, pulse $\overline{CLEAR}$ low (5µs typ) to reset the output latch. Connect $\overline{CLEAR}$ to GND to make the latch transparent.
—	—	—	8	UVSET	Undervoltage-Threshold Adjustment Input. Connect UVSET to an external resistive voltage-divider network to adjust the desired undervoltage threshold.
—	—	—	—	EP	Exposed Pad. EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal-resistance path from the IC junction to the PC board. Do not use as the primary electrical connection to GND.

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Detailed Description

Overvoltage Monitoring

When operating in overvoltage mode, the MAX6495–MAX6499 feedback path (Figure 1) consists of IN, OVSET's internal comparator, the internal gate charge pump, and the external nMOSFET, resulting in a switch-on/off function. When the programmed overvoltage threshold is tripped, the internal fast comparator turns off the external MOSFET, clamping GATE to OUTFB within 0.5µs and disconnecting the power source from the load. When IN decreases below the adjusted overvoltage threshold, the MAX6495–MAX6499 slowly enhance GATE above OUTFB, reconnecting the load to the power source.

Overvoltage Limiter (MAX6495/MAX6496/MAX6499)

When operating in overvoltage-limiter mode, the MAX6495/MAX6496/MAX6499 feedback path (Figure 2) consists of OUTFB, OVSET's internal comparator, the internal gate charge pump, and the external n-channel MOSFET, resulting in the external MOSFET operating as a voltage regulator.

During normal operation, GATE is enhanced 10V above OUTFB. The external MOSFET source voltage is monitored through a resistive divider between OUTFB and OVSET. When OUTFB rises above the adjusted overvoltage threshold, an internal comparator sinks the charge-pump current, discharging the external GATE, regulating OUTFB at the OVSET overvoltage threshold. OUTFB remains active during the overvoltage transients and the MOSFET continues to conduct during the overvoltage event, operating in switched-linear mode.

As the transient begins decreasing, OUTFB fall time will depend on the MOSFET's GATE charge, the internal charge-pump current, the output load, and the tank capacitor at OUTFB.

For fast-rising transients and very large-sized MOSFETs, add an additional bypass capacitor from GATE to GND to reduce the effect of the fast-rising voltages at IN. The external capacitor acts as a voltage-divider working against the MOSFET's drain-to-gate capacitance. For a 6000pF gate-to-source capacitance, a 0.1µF capacitor at GATE will reduce the impact of the fast-rising V_{IN} input.

Caution must be exercised when operating the MAX6495/MAX6496/MAX6499 in voltage-limiting mode for long durations. If the V_{IN} is a DC voltage greater than the MOSFET's maximum gate voltage, the MOSFET dissipates power continuously. To prevent damage to the external MOSFET, proper heatsinking should be implemented.

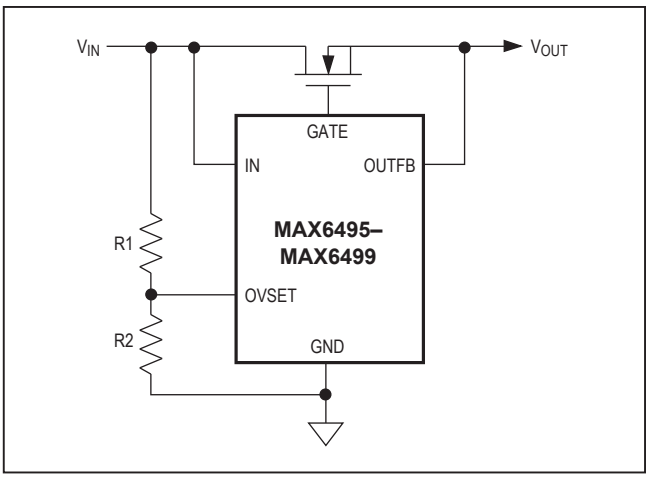

Figure 1. Overvoltage Threshold (MAX6495–MAX6499)

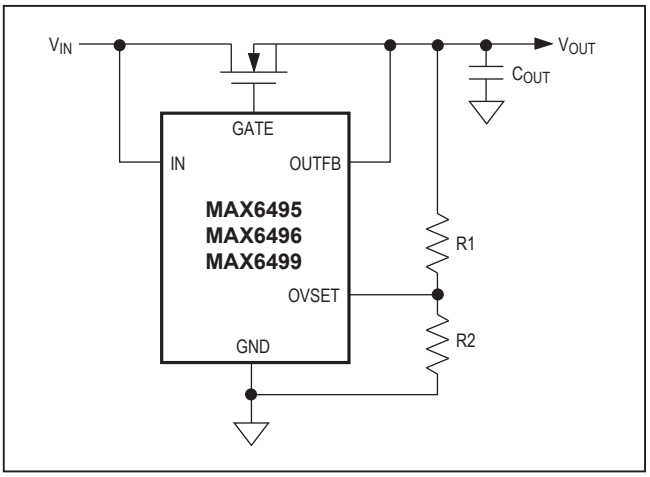

Figure 2. Overvoltage-Limiter Protection Switch Configuration

GATE Voltage

The MAX6495–MAX6499 use a high-efficiency charge pump to generate the GATE voltage. Upon V_{IN} exceeding the 5V (typ) UVLO threshold, GATE enhances 10V above V_{IN} (for $V_{IN} \geq 14V$) with a 100µA pullup current. An overvoltage condition occurs when the voltage at OVSET goes above its V_{TH+} threshold. When the threshold is crossed, GATE falls to OUTFB within 0.5µs with a 100mA pulldown current. The MAX6495–MAX6499 include an internal clamp to OUTFB that ensures GATE is limited to 18V (max) above OUTFB to prevent gate-to-source damage of the external MOSFET.

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The gate cycles during overvoltage-limit and overvoltage-switch modes are quite similar but have distinct characteristics. In overvoltage-switch mode, GATE is enhanced to (V_{IN} + 10V) while the monitored V_{IN} voltage remains below the overvoltage fault threshold (OVSET < V_{TH+}). When an overvoltage fault occurs (OVSET ≥ V_{TH+}), GATE is pulled one diode drop below OUTFB, turning off the external MOSFET and disconnecting the load from the input. GATE remains low (MOSFET off) as long as the V_{IN} voltage is above the overvoltage fault threshold. As V_{IN} falls back below the overvoltage fault threshold, GATE is again enhanced to (V_{IN} + 10V).

In overvoltage-limit mode, GATE is enhanced to (V_{IN} +10V) while the monitored OUTFB voltage remains below the overvoltage fault threshold (OVSET < V_{TH+}). When an overvoltage fault occurs (OVSET ≥ V_{TH+}), GATE is pulled one diode drop below OUTFB until OUTFB drops 5% below the overvoltage fault threshold (MAX6495/MAX6496/MAX6499). GATE is then turned back on until OUTFB reaches the overvoltage fault threshold and GATE is again turned off. GATE cycles in a saw-tooth waveform until OUTFB remains below the overvoltage fault threshold and GATE remains constantly on (V_{IN} +10V). The overvoltage limiter's sawtooth GATE output operates the MOSFET in a switched-linear mode while the input voltage remains above the overvoltage fault threshold. The sawtooth frequency depends on the load capacitance, load current, and MOSFET turn-on time (GATE charge current and GATE capacitance).

GATE goes high when the following startup conditions are met: V_{IN} is above the UVLO threshold, $\overline{SHDN}$ is high, an overvoltage fault is not present, and the device is not in thermal shutdown.

Undervoltage Monitoring (MAX6499)

The MAX6499 includes undervoltage and overvoltage comparators for window detection (see Figure 3 and Figure 12). GATE is enhanced and the nMOSFET is on when the monitored voltage is within the selected "window." When the monitored voltage falls below the lower limit ($V_{TRIPLOW}$) or exceeds the upper limit ($V_{TRIPHIGH}$) of the window, GATE falls to OUTFB turning off the MOSFET. The application in Figure 3 shows the MAX6499 enabling the DC-DC converter when the monitored voltage is in the selected window.

The resistor values R1, R2, and R3 can be calculated as follows:

$$V_{TRIPLOW} = (V_{TH-})\left(\frac{R_{TOTAL}}{R2 + R3}\right)$$

$$V_{TRIPHIGH} = (V_{TH+})\left(\frac{R_{TOTAL}}{R3}\right)$$

where R_{TOTAL} = R1 + R2 + R3.

Use the following steps to determine the values for R1, R2, and R3:

1) Choose a value for R_{TOTAL}, the sum of R1, R2, and R3. Because the MAX6499 has very high input impedance, R_{TOTAL} can be up to 5MΩ.
2) Calculate R3 based on R_{TOTAL} and the desired upper trip point:

$$R3 = \frac{V_{TH+} \times R_{TOTAL}}{V_{TRIPHIGH}}$$

3) Calculate R2 based on R_{TOTAL}, R3, and the desired lower trip point:

$$R2 = \left[\frac{(V_{TH-}) \times R_{TOTAL}}{V_{TRIPLOW}}\right] - R3$$

4) Calculate R1 based on R_{TOTAL}, R2, and R3:

$$R1 = R_{TOTAL} - R2 - R3$$

To improve ESD protection, keep R3 ≥ 1kΩ.

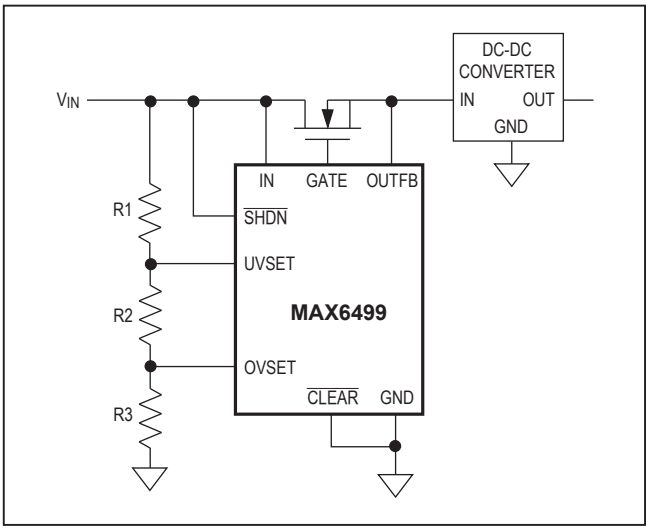

Figure 3. MAX6499 Window-Detector Circuit

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Power-OK Output (MAX6497/MAX6498)

POK is an open-drain output that remains low when the voltage at POKSET is below the internal POKSET threshold (1.18V). POK goes high impedance when POKSET goes above the internal POKSET threshold (1.24V). Connect a resistive divider from OUTFB to GND, and the divider center node to POKSET, to adjust the desired undervoltage threshold. Use a resistor in the 100kΩ range from POKSET to GND to minimize current consumption.

Overvoltage Latch Function

The MAX6497/MAX6499 offers a latch function that prevents the external MOSFET from turning on until the latch is cleared. For the MAX6497, the latch can be cleared by cycling the power on the input IN to a voltage below the undervoltage lockout or by pulling the shutdown input low and then back to a logic-high state. The MAX6499 offers a $\overline{CLEAR}$ input that latches the nMOSFET off when $\overline{CLEAR}$ is high. The latch is removed when the $\overline{CLEAR}$ input is pulsed low. Connect $\overline{CLEAR}$ low to make the latch transparent.

Overvoltage Retry Function

The MAX6498 offers an automatic retry function that tries to enhance the external nMOSFET after the overvoltage condition is removed. When the monitored input voltage detects an overvoltage condition (V_{SET} > V_{TH+}), the nMOSFET is turned off. The MOSFET stays off until the voltage at VSET falls below its V_{TH-} (typically 0.13V), at which point the output tries to turn on again.

Applications Information

Load Dump

Most automotive applications run off a multicell “12V” lead-acid battery with a nominal voltage that swings between 9V and 16V (depending on load current, charging status, temperature, battery age, etc.). The battery voltage is distributed throughout the automobile and is locally regulated down to voltages required by the different system modules. Load dump occurs when the alternator is charging the battery and the battery becomes disconnected. The alternator voltage regulator is temporarily driven out of control. Power from the alternator flows into the distributed power system and elevates the voltage seen at each module. The voltage spikes have rise times typically greater than 5ms and decays within several hundred milliseconds but can extend out to 1s or more depending on the characteristics of the charging system. These transients are capable of destroying sensitive electronic equipment on the first “fault event.”

Setting Overvoltage Thresholds

OVSET provides an accurate means to set the overvoltage level for the devices. Use a resistive divider to set the desired overvoltage condition (see Figure 2). OVSET has a rising 1.24V threshold with a 5% falling hysteresis (MAX6495/MAX6496/MAX6499) and a rising 0.505V threshold with a falling 0.15V threshold (MAX6497/MAX6498).

Begin by selecting the total end-to-end resistance, R_{TOTAL} = R1 + R2. Choose R_{TOTAL} to yield a total current equivalent to a minimum 100 x I_{SET} (OVSET’s input bias current) at the desired overvoltage threshold.

For example:

With an overvoltage threshold (V_{OV}) set to 20V for the MAX6495/MAX6496/MAX6499, R_{TOTAL} < 20V/(100 x I_{SET}), where I_{SET} is OVSET’s 50nA (max) input bias current.

$$R_{TOTAL} < 4M\Omega$$

Use the following formula to calculate R2:

$$R2 = V_{TH+} \times \frac{R_{TOTAL}}{V_{OV}}$$

where V_{TH+} is the 1.24V OVSET rising threshold and V_{OV} is the desired overvoltage threshold.

R2 = 248kΩ. Use a 249kΩ standard resistor.

R_{TOTAL} = R2 + R1, where R1 = 3.751MΩ. Use a 3.74MΩ standard resistor.

A lower value for total resistance dissipates more power but provides slightly better accuracy. To improve ESD protection, keep R2 ≥ 1kΩ.

Reverse-Battery Protection

The MAX6496 is an overvoltage-protection circuit that is capable of driving a pMOSFET to prevent reverse-battery conditions. This MOSFET eliminates the need for external diodes, thus minimizing the input voltage drop (see Figure 8).

Inrush/Slew-Rate Control

Inrush current control can be implemented by placing a capacitor from GATE to GND to slowly ramp up the GATE, thus limiting the inrush current and controlling GATE’s slew rate during initial turn-on. The inrush current can be approximated using the following equation:

$$I_{INRUSH} = \frac{C_{OUT}}{C_{GATE}} \times I_{GATE} + I_{LOAD}$$

where I_{GATE} is GATE’s 100µA sourcing current, I_{LOAD} is the load current at startup, and C_{OUT} is the output capacitor.

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MOSFET Selection

Select external MOSFETs according to the application current level. The MOSFET's on-resistance ($R_{DS(ON)}$) should be chosen low enough to have a minimum voltage drop at full load to limit the MOSFET power dissipation. Determine the device power rating to accommodate an overvoltage fault when operating the MAX6495/MAX6496/MAX6499 in overvoltage-limit mode.

During normal operation, the external MOSFET dissipates little power. The power dissipated in the MOSFET during normal operation is:

$$P = I_{LOAD}^2 \times R_{DS(ON)}$$

where P is the power dissipated in the MOSFET, I_{LOAD} is the output load current, and $R_{DS(ON)}$ is the drain-to-source resistance of the MOSFET.

Most power dissipation in the MOSFET occurs during a prolonged overvoltage event when operating the MAX6495/MAX6496/MAX6499 in voltage-limiter mode. The power dissipated across the MOSFET is as follows (see the *Thermal Shutdown in Overvoltage-Limiter Mode* section):

$$P = V_{DS} \times I_{LOAD}$$

where V_{DS} is the voltage across the MOSFET's drain and source.

Thermal Shutdown

The devices' thermal-shutdown feature turns off GATE if it exceeds the maximum allowable thermal dissipation. Thermal shutdown also monitors the PC board temperature of the external nMOSFET when the devices sit on the same thermal island. Good thermal contact between the MAX6495–MAX6499 and the external nMOSFET is essential for the thermal-shutdown feature to operate effectively. Place the nMOSFET as close to possible to OUTFB.

When the junction temperature exceeds T_J = +160°C, the thermal sensor signals the shutdown logic, turning off the GATE output and allowing the device to cool. The thermal sensor turns the GATE on again after the IC's junction temperature cools by 20°C. Thermal-overload protection is designed to protect the MAX6495–MAX6499 and the external MOSFET in the event of current-limit fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Peak Power-Dissipation Limit

The devices activate an internal 100mA pulldown on GATE when $\overline{SHDN}$ goes low, OVSET exceeds its threshold or UVSET falls below its threshold. Once the voltage on GATE falls below the OUTFB voltage, current begins to flow from OUTFB to the 100mA pulldown through the internal clamp diode, discharging the output capacitors.

Depending on the output capacitance and the initial voltage, a significant amount of energy may be dissipated by the internal 100mA pulldown. To prevent damage to the device ensure that for a given overvoltage threshold, the output capacitance does not exceed the limit provided in Figure 4. This output capacitance represents the sum of all capacitors connected to OUTFB, including reservoir capacitors and DC-DC input filter capacitors.

Thermal Shutdown in Overvoltage-Limiter Mode

When operating the MAX6495/MAX6496/MAX6499 in overvoltage-limit mode for a prolonged period of time, a thermal shutdown is possible. The thermal shutdown is dependent on a number of different factors:

- The device's ambient temperature
- The output capacitor (C_{OUT})
- The output load current (I_{OUT})
- The overvoltage threshold limit (V_{OV})
- The overvoltage waveform period (t_{OV})
- The power dissipated across the package (P_{DISS})

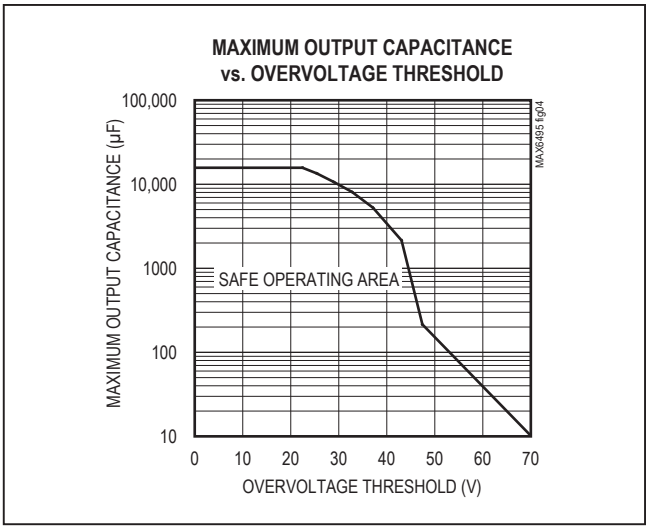

Figure 4. Safe Operating Area for 100mA Pulldown

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During an initial overvoltage occurrence, the discharge time (Δt_1) of C_{OUT}, caused by I_{OUT} and I_{GATEPD}. The discharge time is approximately:

$$\Delta t_1 = C_{OUT} \frac{V_{OV} \times 0.05}{(I_{OUT} + I_{GATEPD})}$$

where V_{OV} is the overvoltage threshold, I_{OUT} is the load current, and I_{GATEPD} is the GATE's 100mA pulldown current.

Upon OUT falling below the threshold point, the MAX6495/MAX6496/MAX6499s' charge-pump current must recover and begins recharging the external GATE voltage. The time needed to recharge GATE from $-V_D$ to the MOSFET's gate threshold voltage is:

$$\Delta t_2 = C_{ISS} \frac{V_{GS(TH)} + V_D}{I_{GATE}}$$

where C_{ISS} is the MOSFET's input capacitance, $V_{GS(TH)}$ is the MOSFET's gate threshold voltage, V_D is the internal clamp (from OUTFB to GATE) diode's forward voltage (1.5V, typ) and I_{GATE} is the charge-pump current (100µA typ).

During Δt_2, C_{OUT} loses charge through the output load. The voltage across C_{OUT} (ΔV_2) decreases until the MOSFET reaches its $V_{GS(TH)}$ threshold and can be approximated using the following formula:

$$\Delta V_2 = I_{OUT} \frac{\Delta t_2}{C_{OUT}}$$

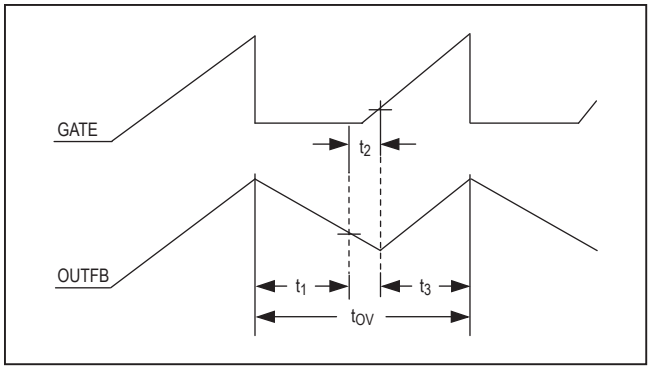

Figure 5. MAX6495/MAX6496/MAX6499 Timing

Once the MOSFET $V_{GS(TH)}$ is obtained, the slope of the output-voltage rise is determined by the MOSFET Q_g charge through the internal charge pump with respect to the drain potential. The new rise time needed to reach a new overvoltage event can be calculated using the following formula:

$$\Delta t_3 \cong \frac{Q_{GD}}{V_{GS}} \frac{\Delta V_{OUT}}{I_{GATE}}$$

where Q_{GD} is the gate-to-drain charge.

The total period of the overvoltage waveform can be summed up as follows:

$$\Delta t_{OV} = \Delta t_1 + \Delta t_2 + \Delta t_3$$

The MAX6495/MAX6496/MAX6499 dissipate the most power during an overvoltage event when I_{OUT} = 0. The maximum power dissipation can be approximated using the following equation:

$$P_{DISS} = V_{OV} \times 0.975 \times I_{GATEPD} \times \frac{\Delta t_1}{\Delta t_{OV}}$$

The die-temperature increase is related to θ_{JC} (8.3°C/W and 8.5°C/W for the MAX6495/MAX6496/MAX6499, respectively) of the package when mounted correctly with a strong thermal contact to the circuit board. The MAX6495/MAX6496/MAX6499 thermal shutdown is governed by the equation:

$$T_J = T_A + P_{DISS} (\theta_{JC} + \theta_{CA}) < +170°C$$

Based on these calculations, the parameters of the MOSFET, the overvoltage threshold, the output load current, and the output capacitors are external variables affecting the junction temperature. If these parameters are fixed, the junction temperature can also be affected by increasing Δt_3, which is the time the switch is on. By increasing the capacitance at the GATE pin, Δt_3 increases as it increases the amount of time required to charge up this additional capacitance (75µA gate current). As a result, Δt_{OV} increases, thereby reducing the power dissipated (P_{DISS}).

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Typical Application Circuits

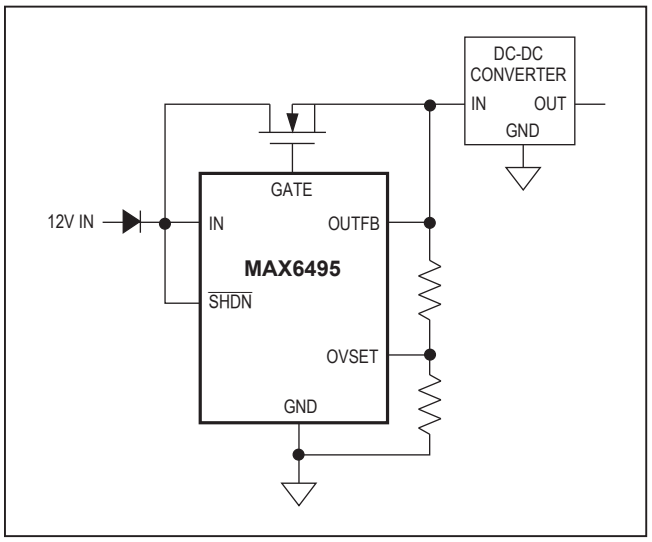

Figure 6. Overvoltage Limiter (MAX6495)

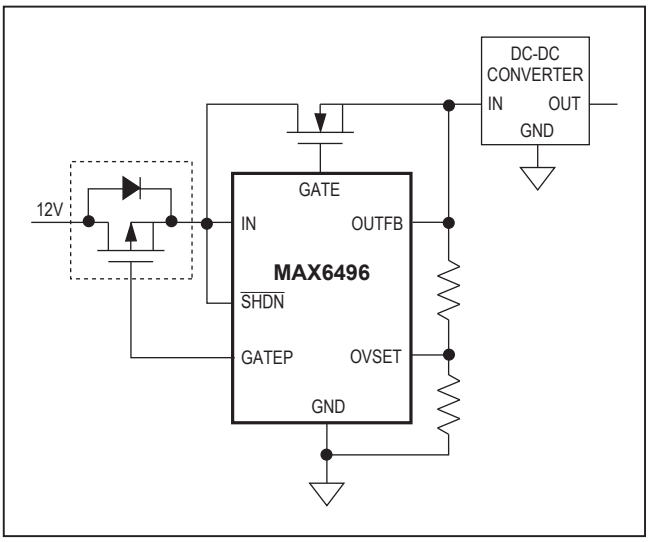

Figure 7. Overvoltage Limiter with Low-Voltage-Drop Reverse-Protection Circuit (MAX6496)

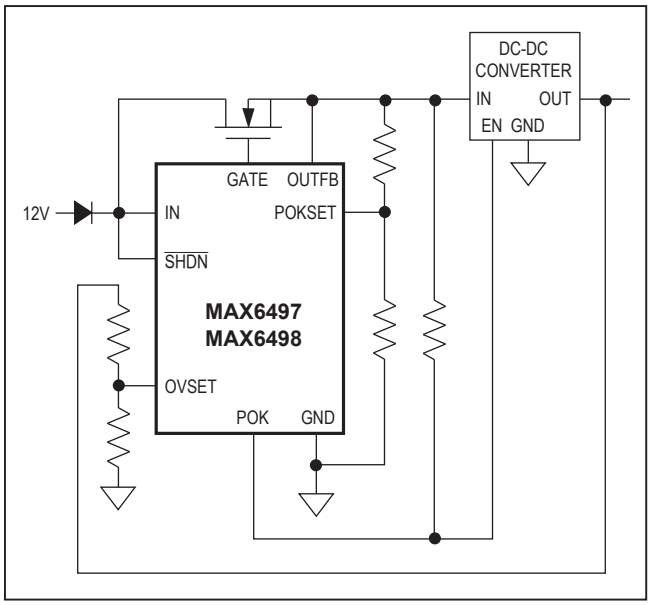

Figure 8. Overvoltage Protection to a DC-DC Converter (MAX6497/MAX6498)

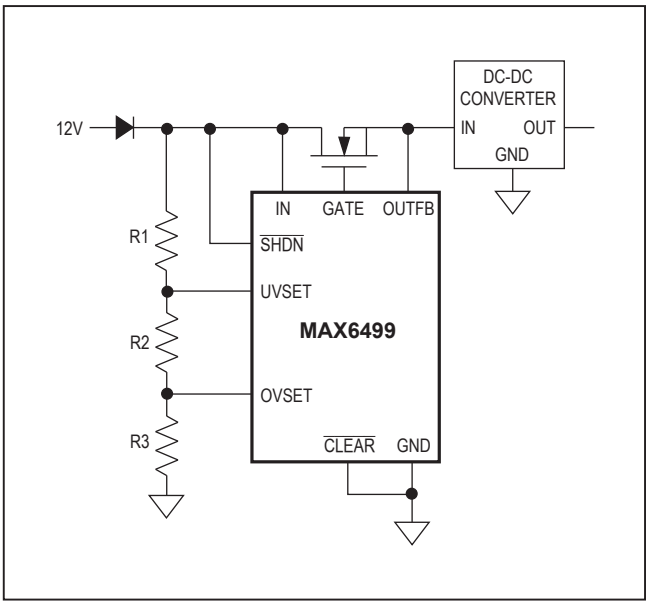

Figure 9. Overvoltage and Undervoltage Window Detector (MAX6499)

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Functional Diagrams

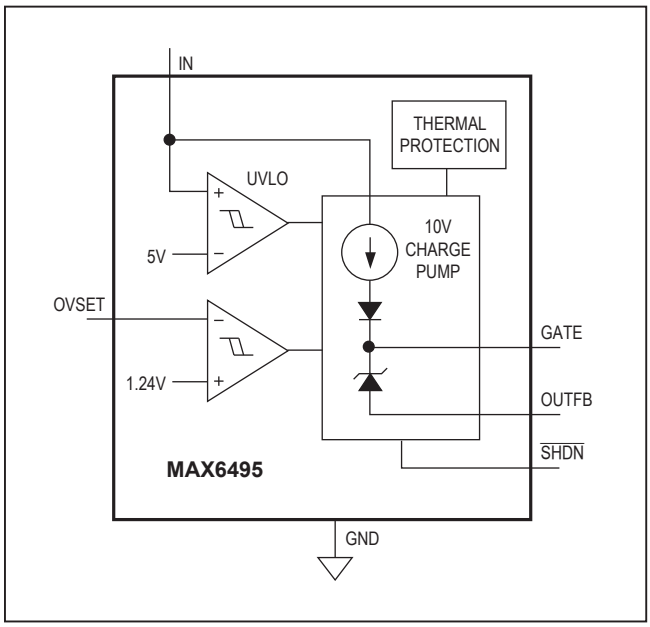

Figure 10. Functional Diagram (MAX6495)

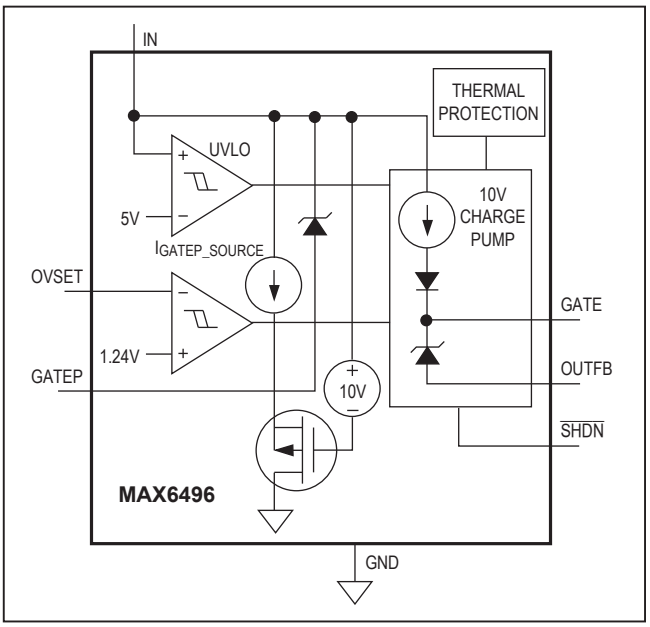

Figure 11. Functional Diagram (MAX6496)

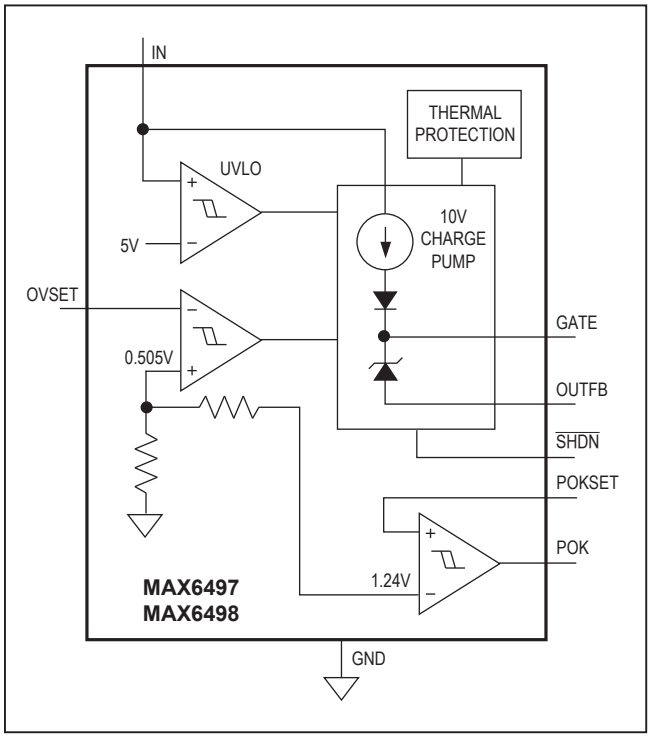

Figure 12. Functional Diagram (MAX6497/MAX6498)

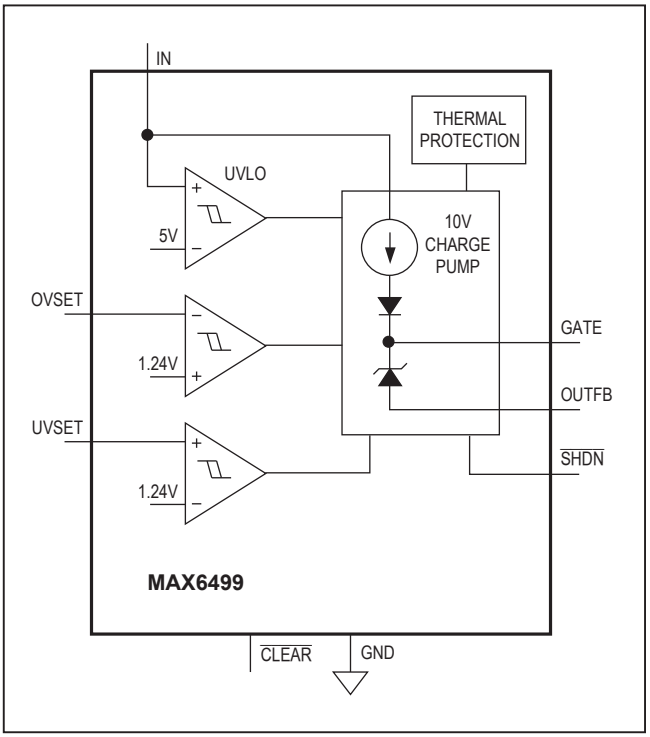

Figure 13. Functional Diagram (MAX6499)

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Selector Guide

PART	Function	p-CHANNEL DRIVER	POK FUNCTION	UNDERVOLTAGE	LATCH/ AUTORETRY	PACKAGE CODE
MAX6495	OV Switch/Limiter	—	—	—	—	T633-2
MAX6496	OV Switch/Limiter	Yes	—	—	—	T833-2
MAX6497	OV Switch	—	Yes	—	Latch	T833-2
MAX6498	OV Switch	—	Yes	—	Autoretry	T833-2
MAX6499	OV/UV Switch/Limiter	—	—	Yes	Latch	T833-2

Ordering Information

PART	PIN-PACKAGE	TOP MARK
MAX6495ATT+T	6 TDFN-EP*	AJM
MAX6495ATT/V+T	6 TDFN-EP*	AUG
MAX6496ATA+T	8 TDFN-EP*	AOF
MAX6496ATA/V+T	8 TDFN-EP*	AOF
MAX6497ATA+T	8 TDFN-EP*	AOC
MAX6498ATA+T	8 TDFN-EP*	AOD
MAX6499ATA+T	8 TDFN-EP*	AOE
MAX6499ATA/V+T	8 TDFN-EP*	BQE

Note: *All devices are specified over the -40°C to +125°C operating temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

/V denotes an automotive qualified part.

Chip Information

PROCESS: BiCMOS

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/05	Initial release	—
1	12/05	Corrected text and formula in the *Detailed Description*.	10, 11
2	1/07	Updated text in the *Applications Information*.	9
3	12/08	Updated package codes in the *Selector Guide*.	1, 13
4	1/09	Added automotive qualified part for MAX6495.	1, 14
5	3/09	Updated *Electrical Characteristics*, added *Peak Power Dissipation Limit* section and new Figure 4. Renumbered subsequent figures throughout data sheet.	3, 9, 10–15
6	7/09	Corrected the MAX6495ATT/V+T top mark in the *Ordering Information* table from AJM to AUG.	2
7	8/09	Updated *Undervoltage Monitoring (MAX6499)* and *Setting Overvoltage Thresholds* sections.	8, 9
8	1/11	Added soldering temperature in the *Absolute Maximum Ratings* section and corrected equation.	2, 11
9	2/12	Added automotive package for MAX6499.	15
10	6/12	Added automotive package for MAX6496.	15
11	4/15	Updated *Benefits and Features* section.	1
12	12/15	Corrected error in data sheet that repeated MAX6496 and excluded MAX6495	1–15
13	6/17	Update pin descriptions and POKSET divider wording	7, 10
14	7/17	Added AEC-Q100 Qualified statement to *Benefits and Features* section	1
15	2/18	Added *Package Information* section	2
16	4/18	Updated the *Benefits and Features* section.	1
17	4/19	Update *Absolute Maximum Ratings* and land pattern for 8TDFN package in the *Package Information* section	2
18	2/21	Updated Ordering Information table	16

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